



# BUK9Y40-55B

N-channel TrenchMOS logic level FET

Rev. 03 — 22 February 2008

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using Nexperia High-Performance Automotive (HPA) TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features

- 175 °C rated
- Q101 compliant
- Logic level compatible
- Very low on-state resistance

### 1.3 Applications

- 12 V and 24 V loads
- General purpose power switching
- Automotive systems
- Motors, lamps and solenoids

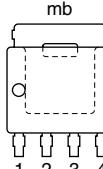
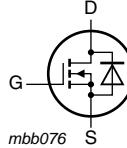
### 1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_D$	drain current	$V_{GS} = 5 \text{ V}$ ; $T_{mb} = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 1</a> and <a href="#">4</a>	-	-	26	A
$P_{tot}$	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 2</a>	-	-	59	W
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}$ ; $I_D = 15 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 12</a> and <a href="#">13</a>	-	34	40	$\text{m}\Omega$
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 26 \text{ A}$ ; $V_{sup} \leq 55 \text{ V}$ ; $R_{GS} = 50 \Omega$ ; $V_{GS} = 5 \text{ V}$ ; $T_{j(init)} = 25 \text{ }^\circ\text{C}$ ; unclamped	-	-	36	$\text{mJ}$

## 2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain	 SOT669 (LFPAK)	

## 3. Ordering information

Table 3. Ordering information

Type number	Package			Version
	Name	Description		
BUK9Y40-55B	LFPAK	plastic single-ended surface-mounted package (LFPAK); 4 leads		SOT669

## 4. Limiting values

Table 4. Limiting values

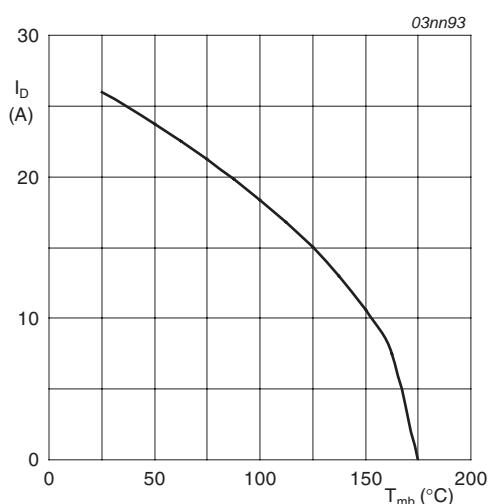
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25^\circ\text{C}$ ; $T_j \leq 175^\circ\text{C}$	-	55	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
$V_{GS}$	gate-source voltage		-15	15	V
$I_D$	drain current	$T_{mb} = 100^\circ\text{C}$ ; $V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 1</a>	-	18	A
		$T_{mb} = 25^\circ\text{C}$ ; $V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 1</a> and <a href="#">4</a>	-	26	A
$I_{DM}$	peak drain current	$T_{mb} = 25^\circ\text{C}$ ; $t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; see <a href="#">Figure 4</a>	-	106	A
$P_{tot}$	total power dissipation	$T_{mb} = 25^\circ\text{C}$ ; see <a href="#">Figure 2</a>	-	59	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 26\text{ A}$ ; $V_{sup} \leq 55\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 5\text{ V}$ ; $T_{j(init)} = 25^\circ\text{C}$ ; unclamped	-	36	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see <a href="#">Figure 3</a>	<a href="#">[1]</a> <a href="#">[2]</a> <a href="#">[3]</a>	-	J
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25^\circ\text{C}$	-	26	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25^\circ\text{C}$	-	106	A

[1] Single-pulse avalanche rating limited by maximum junction temperature of  $175^\circ\text{C}$ .

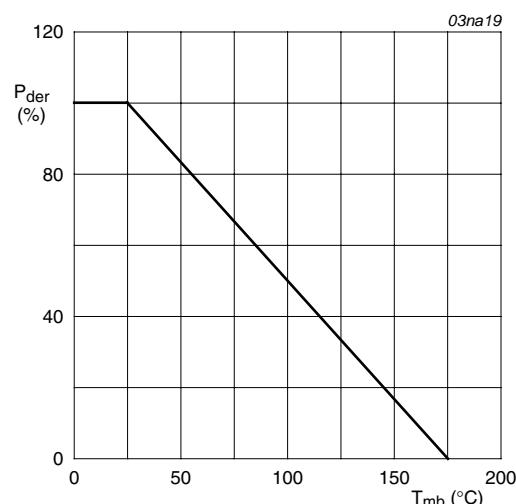
[2] Repetitive avalanche rating limited by average junction temperature of  $170^\circ\text{C}$ .

[3] Refer to application note AN10273 for further information.



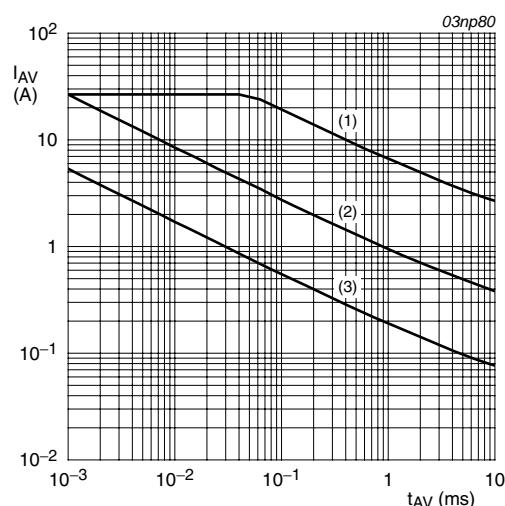
$V_{GS} \geq 5 \text{ V}$

**Fig 1. Continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot}(25\text{ °C})} \times 100 \text{ %}$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**

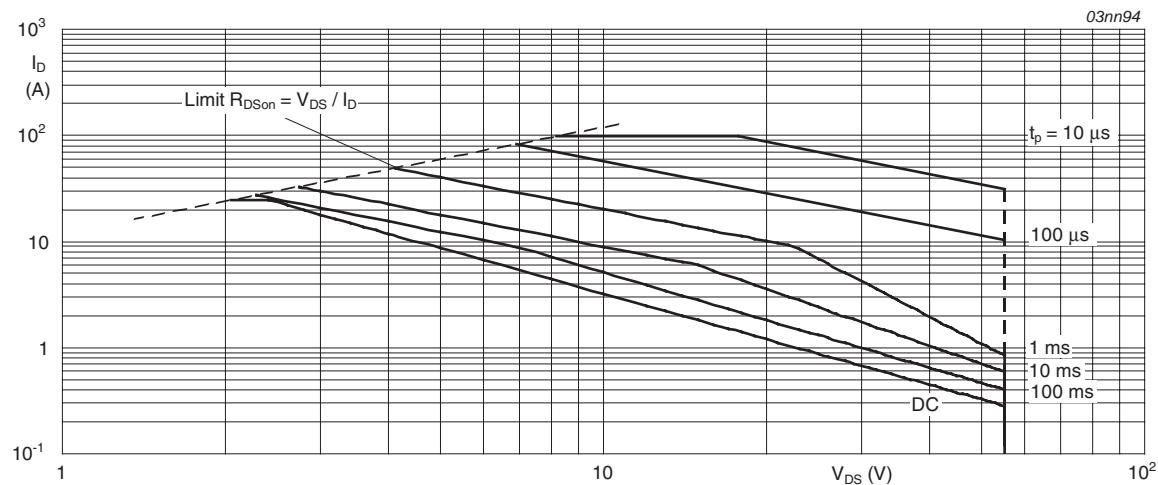


(1) Single-pulse;  $T_j = 25 \text{ °C}$ .

(2) Single-pulse;  $T_j = 150 \text{ °C}$ .

(3) Repetitive.

**Fig 3. Single-shot and repetitive avalanche rating; avalanche current as a function of avalanche period**



$T_{mb} = 25^\circ\text{C}$ ;  $I_{DM}$  is single pulse

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	2.5	K/W

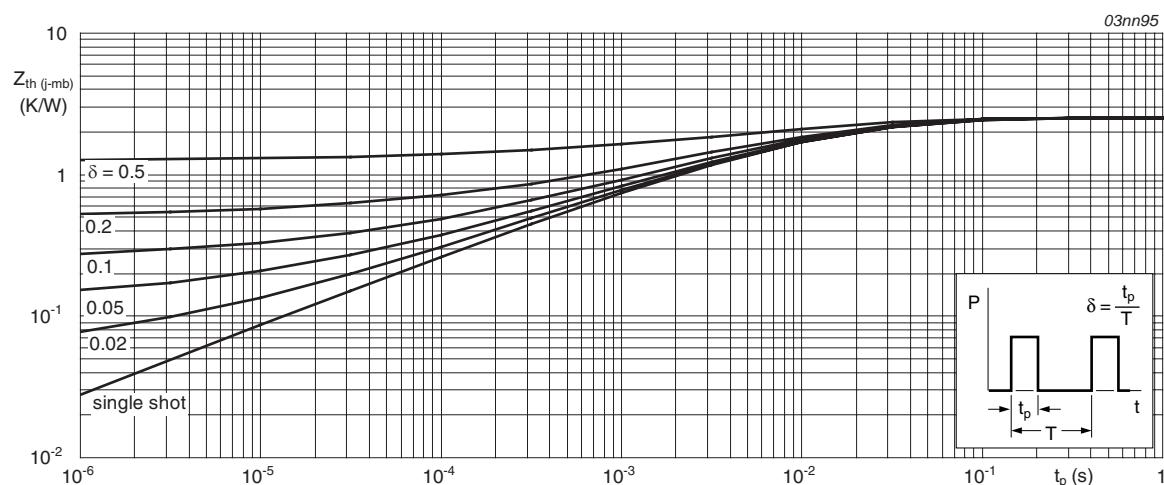
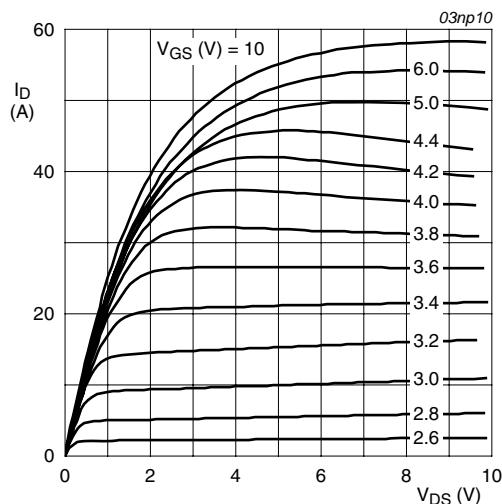


Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration

## 6. Characteristics

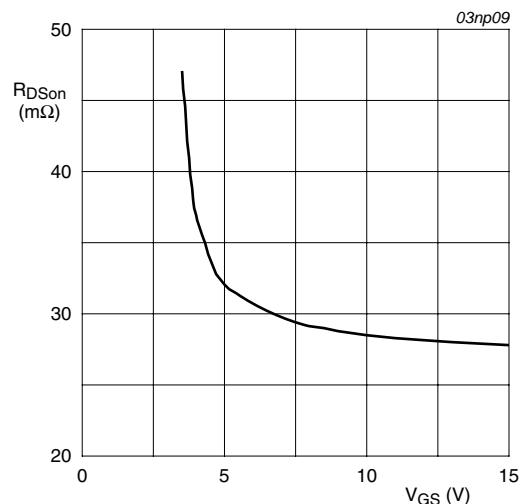
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 0.25 mA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	55	-	-	V
		I <sub>D</sub> = 0.25 mA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C	50	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 175 °C; see <a href="#">Figure 11</a>	0.5	-	-	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C; see <a href="#">Figure 11</a>	1.1	1.5	2	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = -55 °C; see <a href="#">Figure 11</a>	-	-	2.3	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 55 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.02	1	μA
		V <sub>DS</sub> = 55 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C	-	-	500	μA
I <sub>GSS</sub>	gate leakage current	V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 15 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		V <sub>DS</sub> = 0 V; V <sub>GS</sub> = -15 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 15 A; T <sub>j</sub> = 175 °C; see <a href="#">Figure 12</a> and <a href="#">13</a>	-	-	84	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 15 A; T <sub>j</sub> = 25 °C	-	32	36	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 15 A; T <sub>j</sub> = 25 °C	-	-	45	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 15 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 12</a> and <a href="#">13</a>	-	34	40	mΩ
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 20 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 16</a>	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 30 V; T <sub>j</sub> = 25 °C	-	45	-	ns
Q <sub>r</sub>	recovered charge	-	25	-	-	nC
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 15 A; V <sub>DS</sub> = 44 V; V <sub>GS</sub> = 5 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 14</a>	-	11	-	nC
Q <sub>GS</sub>	gate-source charge	-	2	-	-	nC
Q <sub>GD</sub>	gate-drain charge	-	5	-	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; T <sub>j</sub> = 25 °C; see <a href="#">Figure 15</a>	-	765	1020	pF
C <sub>oss</sub>	output capacitance	-	123	148	-	pF
C <sub>rss</sub>	reverse transfer capacitance	-	71	97	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 30 V; R <sub>L</sub> = 2.2 Ω; V <sub>GS</sub> = 5 V; R <sub>G(ext)</sub> = 10 Ω; T <sub>j</sub> = 25 °C	-	17	-	ns
t <sub>r</sub>	rise time	-	93	-	-	ns
t <sub>d(off)</sub>	turn-off delay time	-	35	-	-	ns
t <sub>f</sub>	fall time	-	72	-	-	ns



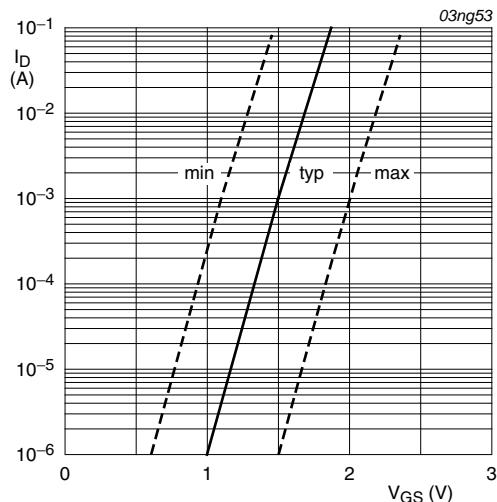
$T_j = 25^\circ\text{C}; t_p = 300\ \mu\text{s}$

**Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



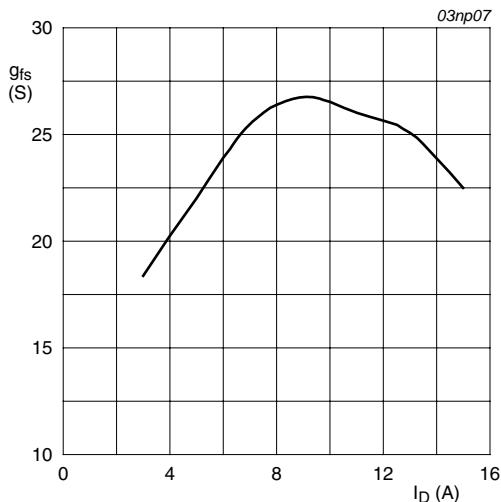
$T_j = 25^\circ\text{C}; I_D = 15\ \text{A}$

**Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**



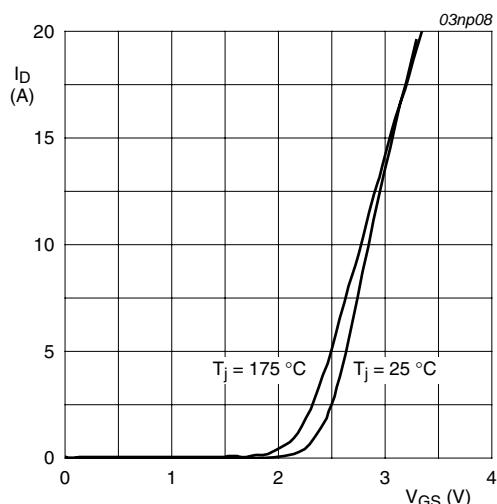
$T_j = 25^\circ\text{C}; V_{DS} = V_{GS}$

**Fig 8. Sub-threshold drain current as a function of gate-source voltage**



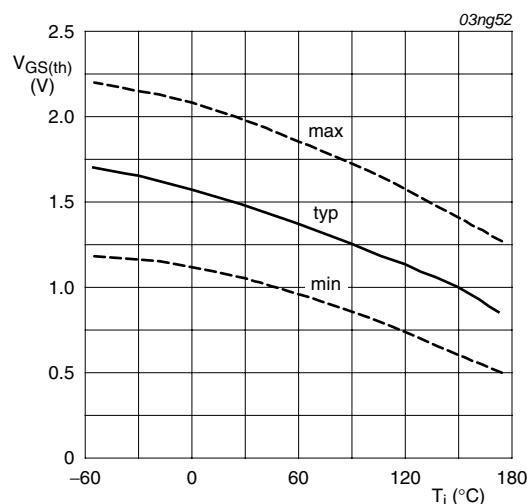
$T_j = 25^\circ\text{C}; V_{DS} = 25\ \text{V}$

**Fig 9. Forward transconductance as a function of drain current; typical values**



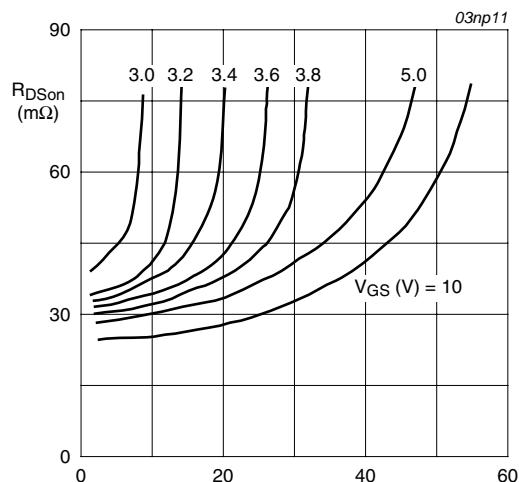
$V_{DS} = 25 \text{ V}$

**Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



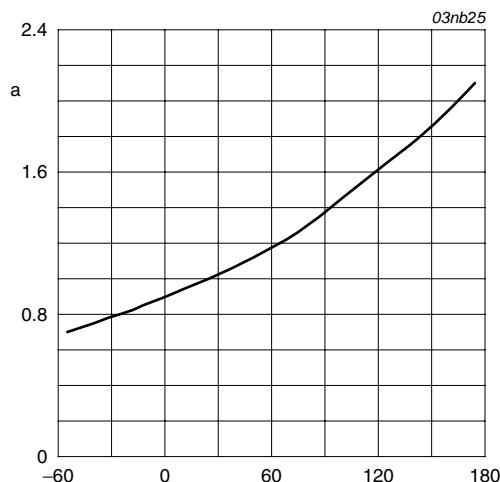
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig 11. Gate-source threshold voltage as a function of junction temperature**



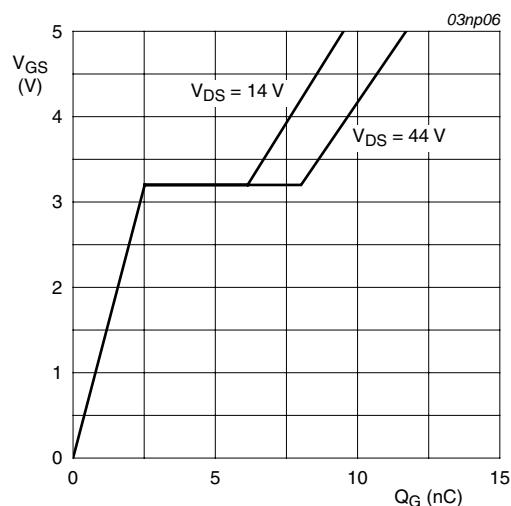
$T_j = 25 \text{ °C}$

**Fig 12. Drain-source on-state resistance as a function of drain current; typical values**

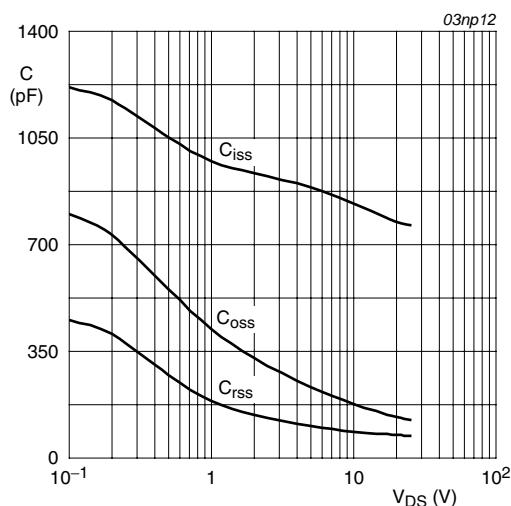


$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

**Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature**



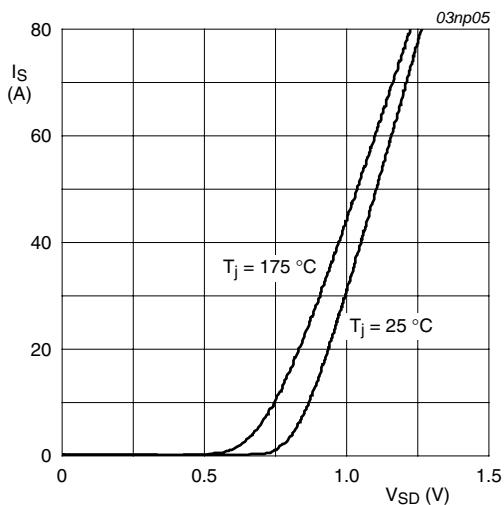
$T_j = 25\text{ }^\circ\text{C}$ ;  $I_D = 15\text{ A}$



$V_{GS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

**Fig 14. Gate-source voltage as a function of gate charge; typical values**

**Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



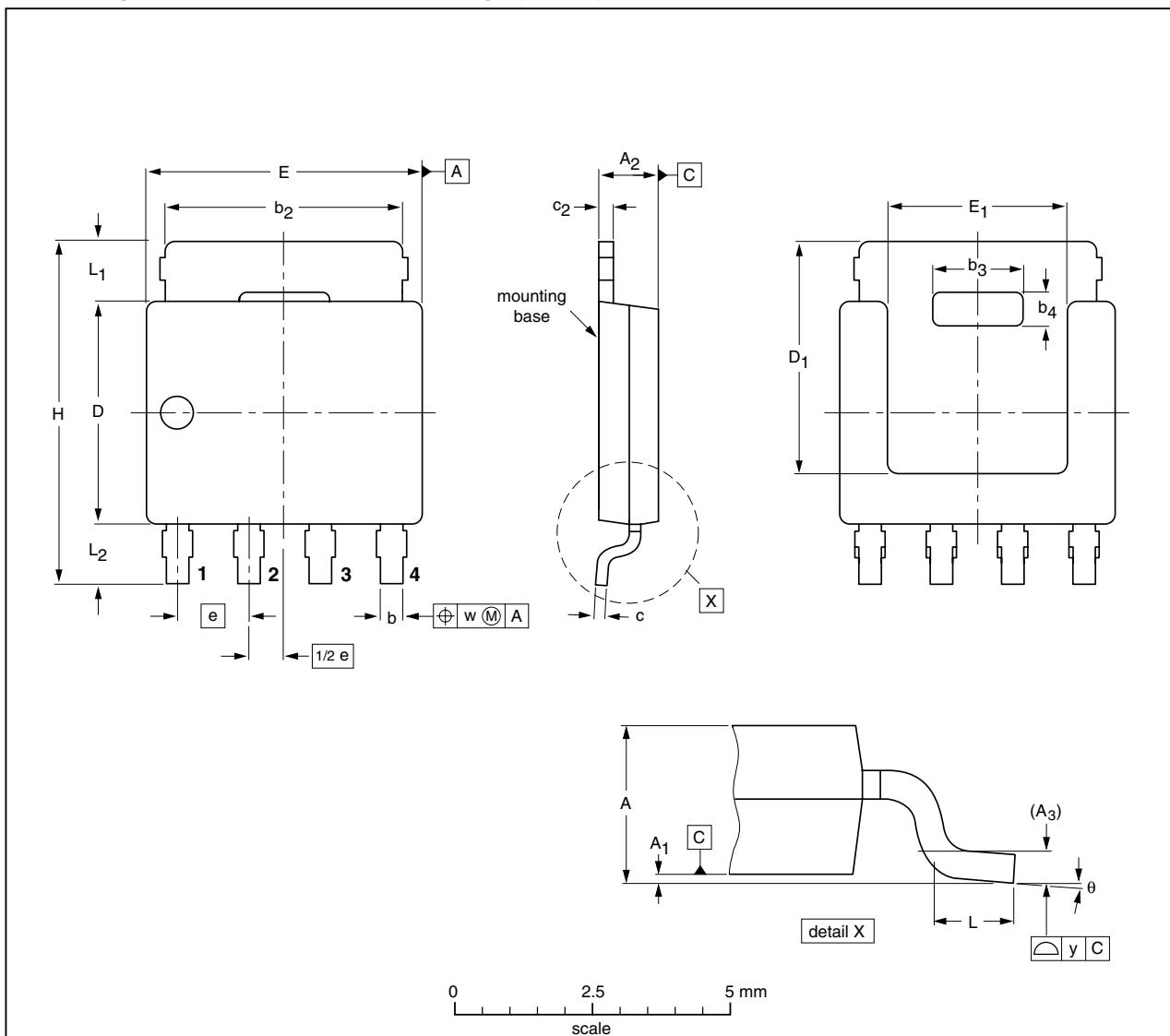
$V_{GS} = 0\text{ V}$

**Fig 16. Source current as a function of source-drain voltage; typical values**

## 7. Package outline

Plastic single-ended surface-mounted package (LFPAK); 4 leads

SOT669



### DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>	c	c <sub>2</sub>	D <sup>(1)</sup>	D <sub>1(1)</sub> <sup>(1)</sup> max	E <sup>(1)</sup>	E <sub>1(1)</sub> <sup>(1)</sup>	e	H	L	L <sub>1</sub>	L <sub>2</sub>	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25 0.35	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20 3.80	5.0 4.8	3.3 3.1	1.27 1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25 0.1	0.1 0.0	8° 0°

### Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA				
SOT669		MO-235					-04-10-13 06-03-16

Fig 17. Package outline SOT669 (LFPAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9Y40-55B_3	20080222	Product data sheet	-	BUK9Y40-55B_2
Modifications:				<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li></ul>
BUK9Y40-55B_2	20060411	Product data sheet	-	BUK9Y40_55B-01
BUK9Y40_55B-01	20040528	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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