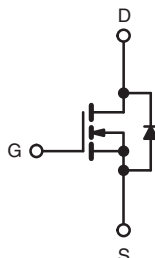
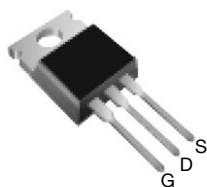


D Series Power MOSFET

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	550	
$R_{DS(on)}$ max. at 25 °C (Ω)	$V_{GS} = 10$ V	0.4
Q_g max. (nC)	58	
Q_{gs} (nC)	8	
Q_{gd} (nC)	14	
Configuration	Single	

TO-220AB


N-Channel MOSFET

FEATURES

- Optimal Design
 - Low Area specific On-Resistance
 - Low Input Capacitance (C_{iss})
 - Reduced Capacitive Switching Losses
 - High Body Diode Ruggedness
 - Avalanche Energy Rated (U_{IS})
- Optimal Efficiency and Operation
 - Low Cost
 - Simple Gate Drive Circuitry
 - Low Figure-Of-Merit (FOM): $R_{on} \times Q_g$
 - Fast Switching
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Note

* Lead (Pb)-containing terminations are not RoHS-compliant. Exemptions may apply.

APPLICATIONS

- Consumer Electronics
 - Displays (LCD or Plasma TV)
- Server and Telecom Power Supplies
 - SMPS
- Industrial
 - Welding, Induction Heating, Motor Drives
- Battery Chargers



RoHS*
COMPLIANT
HALOGEN
FREE
Available

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	SiHP14N50D-E3
Lead (Pb)-free and Halogen-free	SiHP14N50D-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 30	
Gate-Source Voltage AC ($f > 1$ Hz)		30	
Continuous Drain Current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current ^a	I_{DM}	38	W/°C
Linear Derating Factor		1.6	
Single Pulse Avalanche Energy ^b	E_{AS}	56	mJ
Maximum Power Dissipation	P_D	208	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	°C
Drain-Source Voltage Slope	dV/dt	24	V/ns
Reverse Diode dV/dt ^d		0.4	
Soldering Recommendations (Peak Temperature)	for 10 s	300°	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 2.3$ mH, $R_g = 25$ Ω , $I_{AS} = 7$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, starting $T_J = 25$ °C.

**THERMAL RESISTANCE RATINGS**

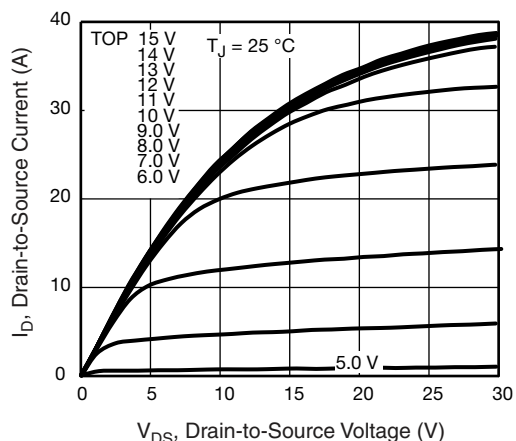
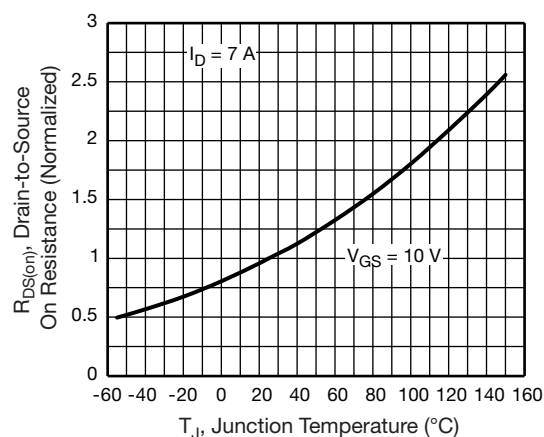
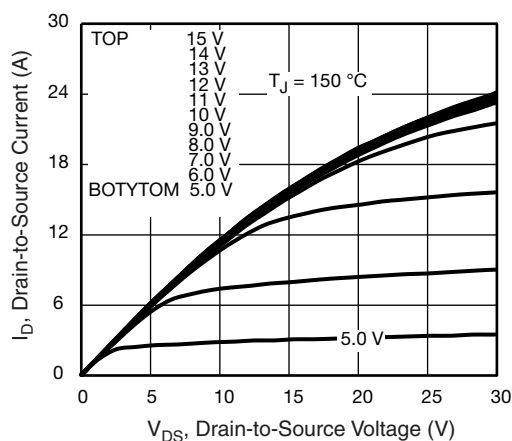
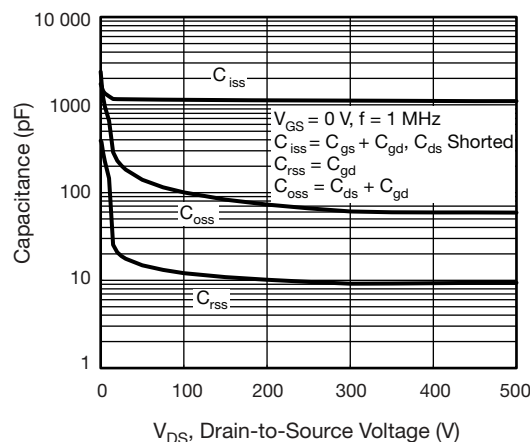
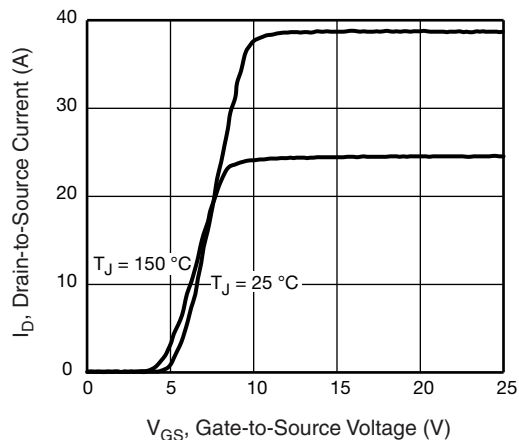
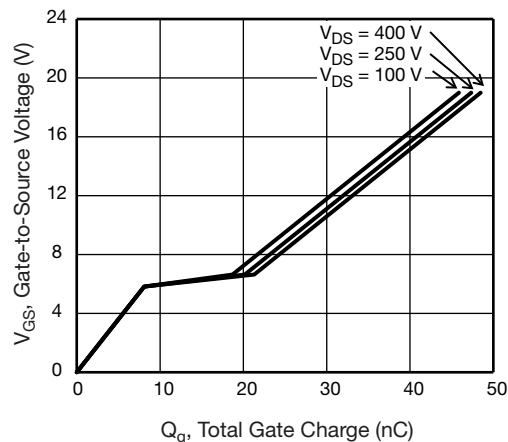
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.6	

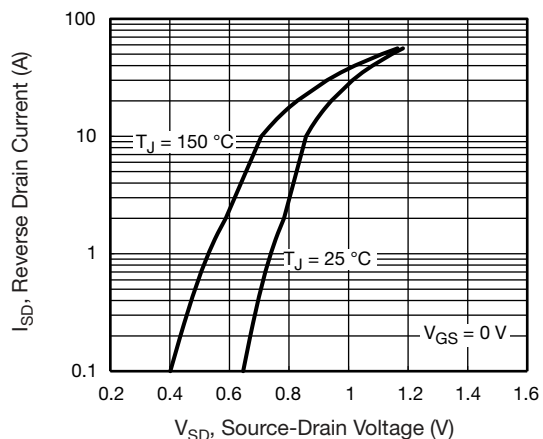
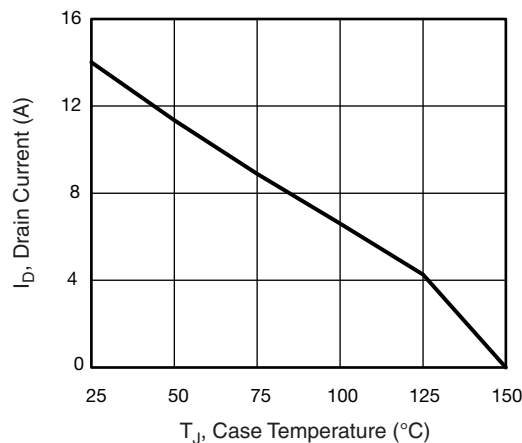
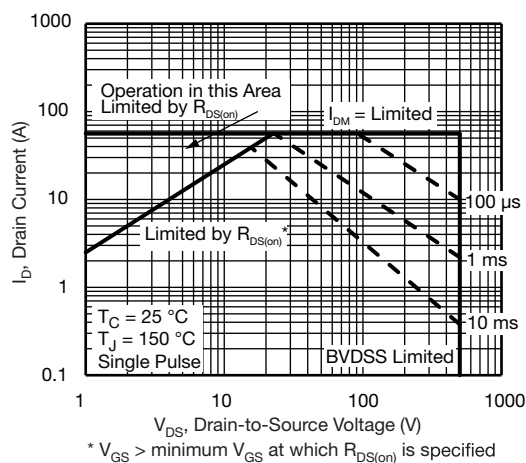
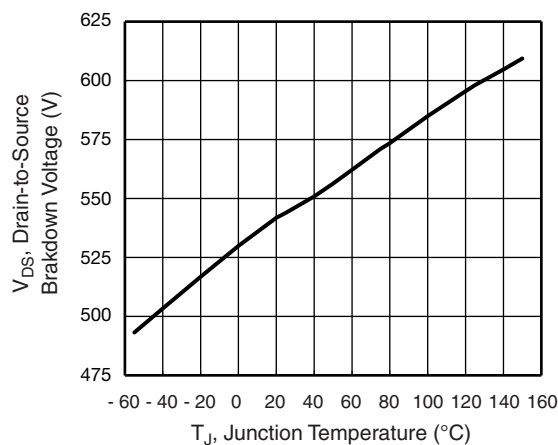
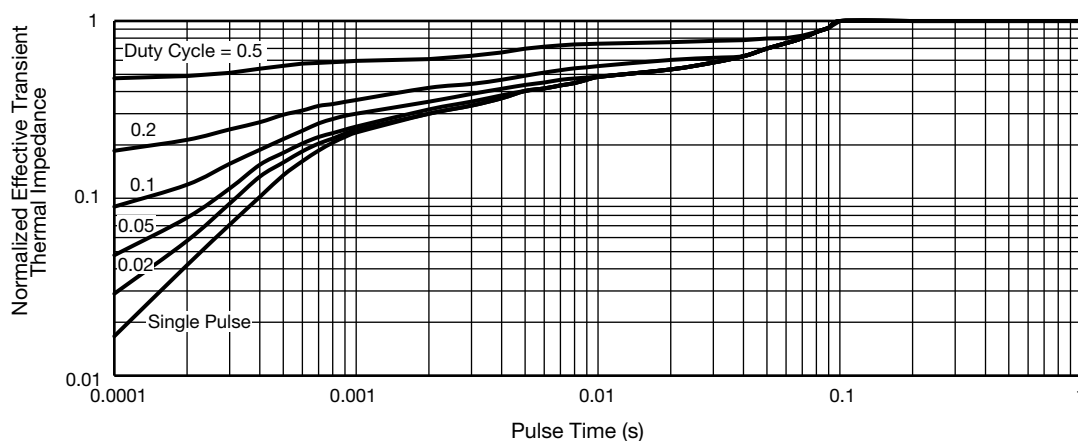
SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

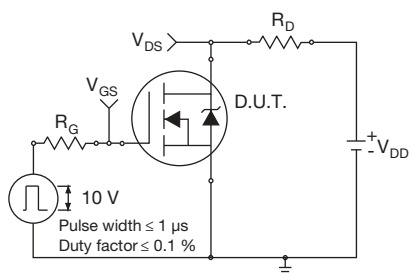
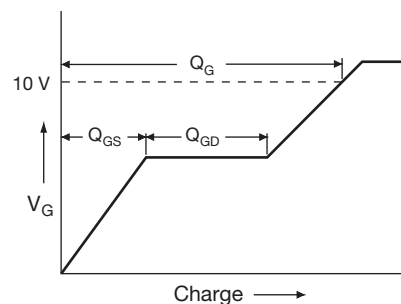
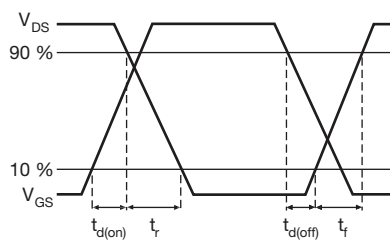
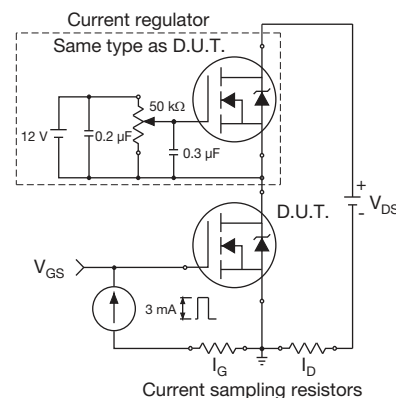
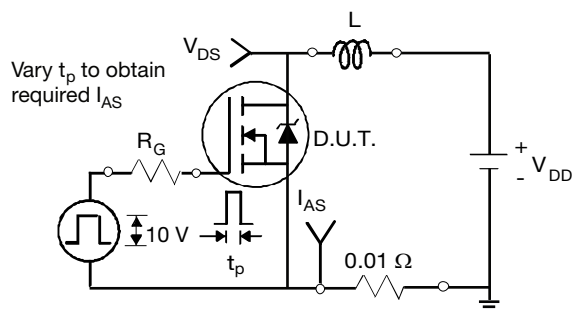
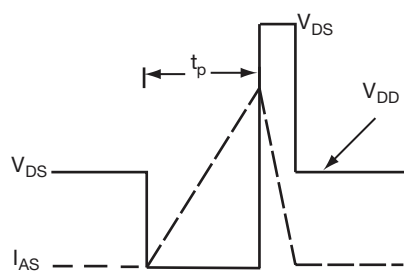
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C , $I_D = 250\text{ }\mu\text{A}$	-	0.58	-	V/°C
Gate Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 400\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ °C}$	-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 7\text{ A}$	-	0.320	0.40	Ω
Forward Transconductance ^a	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 7\text{ A}$	-	5.2	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$	-	1144	-	pF
Output Capacitance	C_{oss}		-	100	-	
Reverse Transfer Capacitance	C_{rss}		-	12	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ V to } 480\text{ V}$	-	87	-	
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$		-	125	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$, $I_D = 7\text{ A}$, $V_{DS} = 400\text{ V}$	-	29	58	nC
Gate-Source Charge	Q_{gs}		-	8	-	
Gate-Drain Charge	Q_{gd}		-	14	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400\text{ V}$, $I_D = 7\text{ A}$, $V_{GS} = 10\text{ V}$, $R_g = 9.1\text{ }\Omega$	-	16	32	ns
Rise Time	t_r		-	27	54	
Turn-Off Delay Time	$t_{d(off)}$		-	29	58	
Fall Time	t_f		-	26	52	
Gate Input Resistance	R_g	$f = 1\text{ MHz}$, open drain	-	1.7	-	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	14	A
Pulsed Diode Forward Current	I_{SM}		-	-	56	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ °C}$, $I_S = 7\text{ A}$, $V_{GS} = 0\text{ V}$	-	-	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ °C}$, $I_F = I_S = 7\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $V_R = 20\text{ V}$	-	319	-	ns
Reverse Recovery Charge	Q_{rr}		-	3.0	-	μC
Reverse Recovery Current	I_{RRM}		-	18	-	A

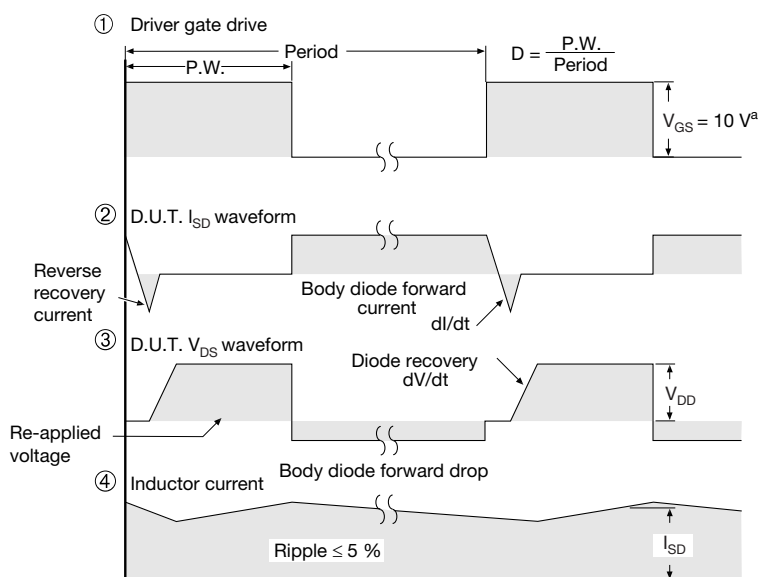
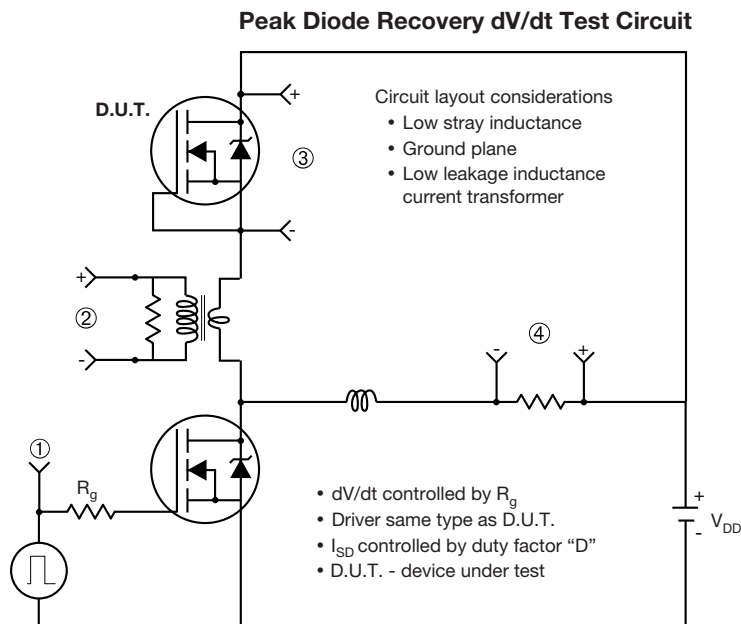
Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage


Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Maximum Safe Operating Area

Fig. 10 - Temperature vs. Drain-to-Source Voltage

Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case


Fig. 12 - Switching Time Test Circuit

Fig. 16 - Basic Gate Charge Waveform

Fig. 13 - Switching Time Waveforms

Fig. 17 - Gate Charge Test Circuit

Fig. 14 - Unclamped Inductive Test Circuit

Fig. 15 - Unclamped Inductive Waveforms

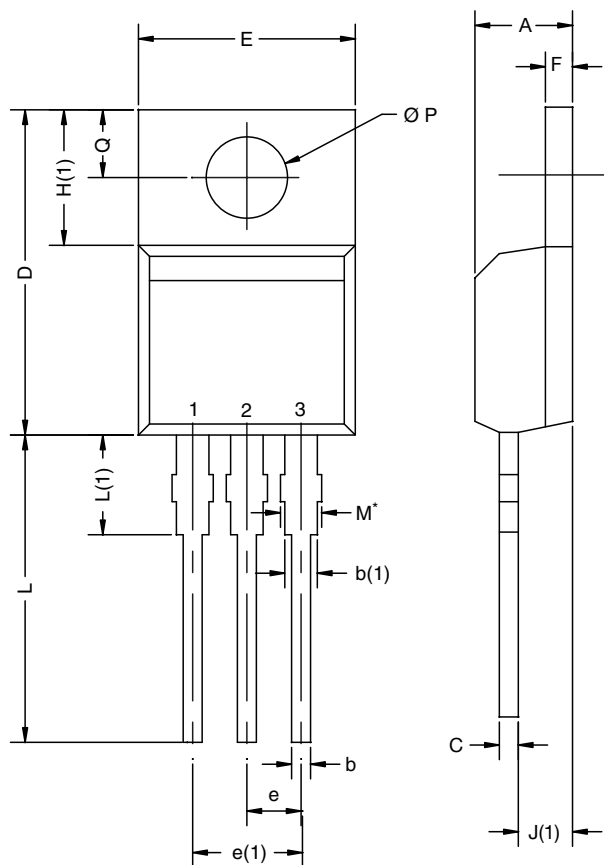

Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 18 - For N-Channel

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TO-220AB

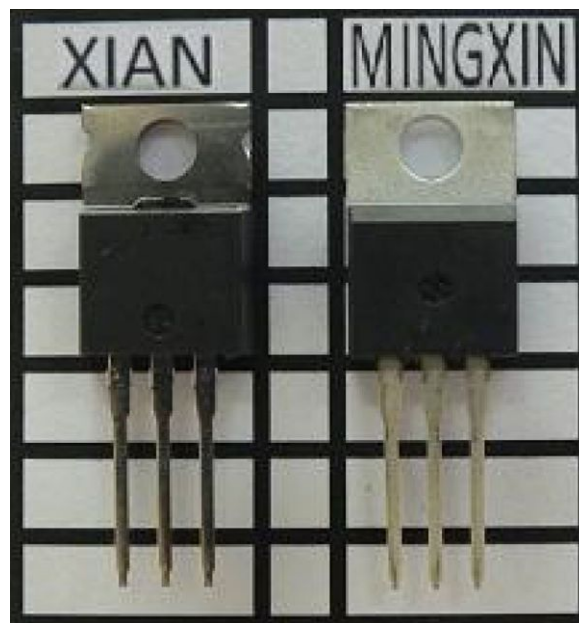


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
$\varnothing P$	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: X12-0208-Rev. N, 08-Oct-12
DWG: 5471

Notes

- * M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM
- Xi'an and Mingxin actual photo





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