

# HEF4520B

## Dual binary counter

Rev. 7 — 30 March 2016

Product data sheet

### 1. General description

The HEF4520B is a dual 4-bit internally synchronous binary counter. The counter has an active HIGH clock input (nCP0) and an active LOW clock input ( $\overline{\text{nCP1}}$ ), buffered outputs from all four bit positions (nQ0 to nQ3) and an active HIGH overriding asynchronous master reset input (nMR).

The counter advances on either the LOW-to-HIGH transition of the nCP0 input if  $\overline{\text{nCP1}}$  is HIGH or the HIGH-to-LOW transition of the  $\overline{\text{nCP1}}$  input if nCP0 is LOW. Either nCP0 or  $\overline{\text{nCP1}}$  may be used as the clock input to the counter while the other clock input may be used as a clock enable input. Schmitt trigger action makes the clock input highly tolerant of slower clock rise and fall times. A HIGH on nMR resets the counter (nQ0 to nQ3 = LOW) independent of nCP0 and  $\overline{\text{nCP1}}$ .

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

### 2. Features and benefits

- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

### 3. Ordering information

**Table 1. Ordering information**

All types operate from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

Type number	Package		Version
	Name	Description	
HEF4520BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1



4. Functional diagram

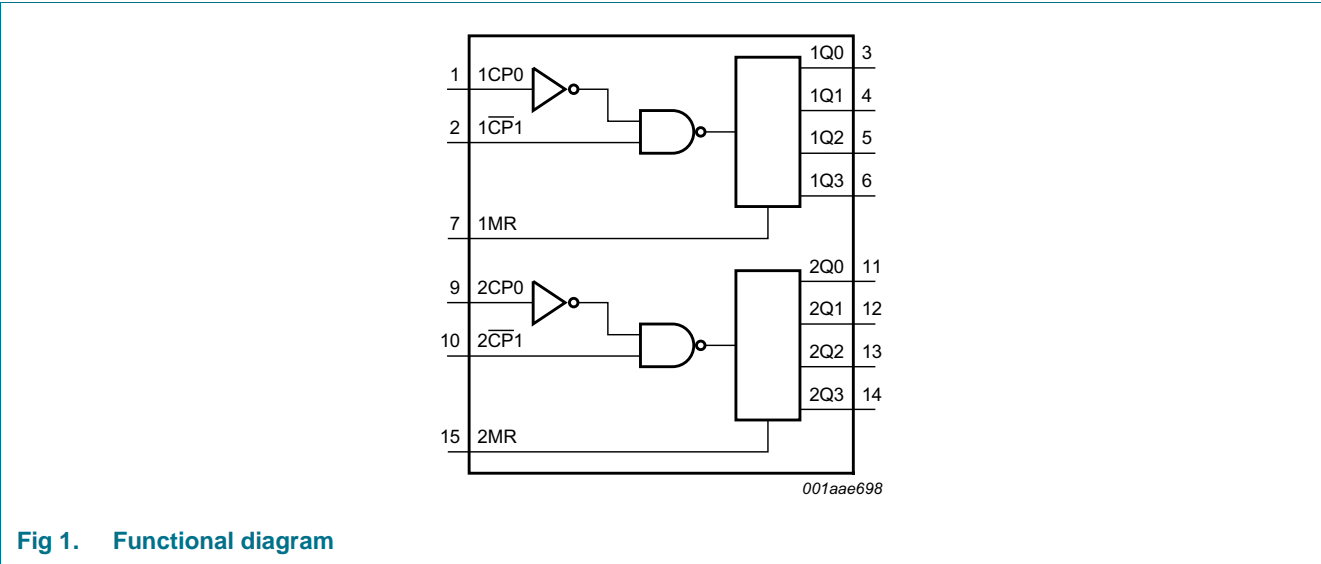


Fig 1. Functional diagram

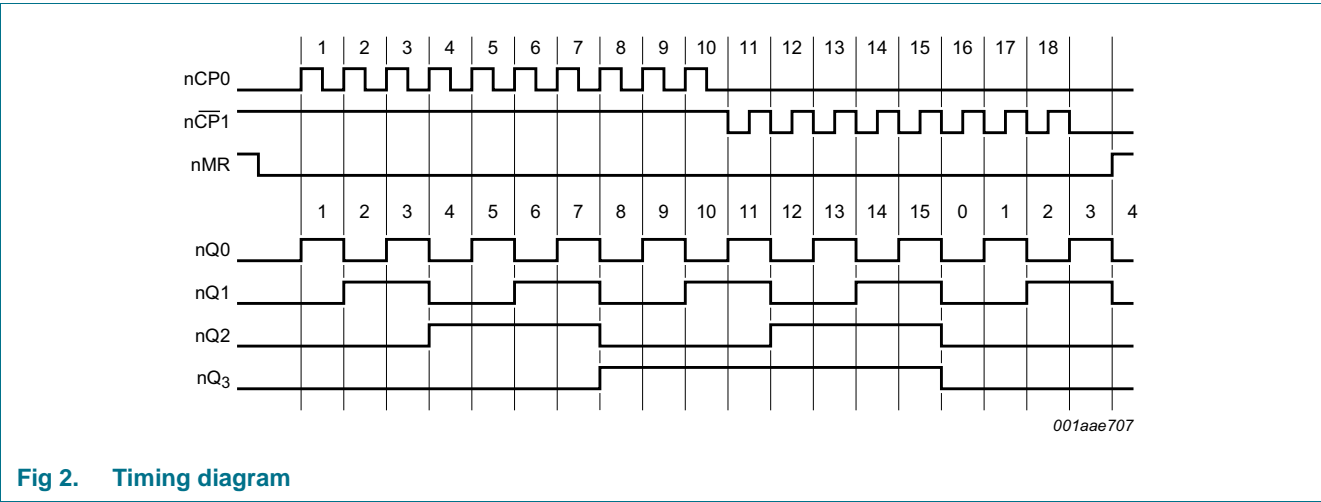


Fig 2. Timing diagram

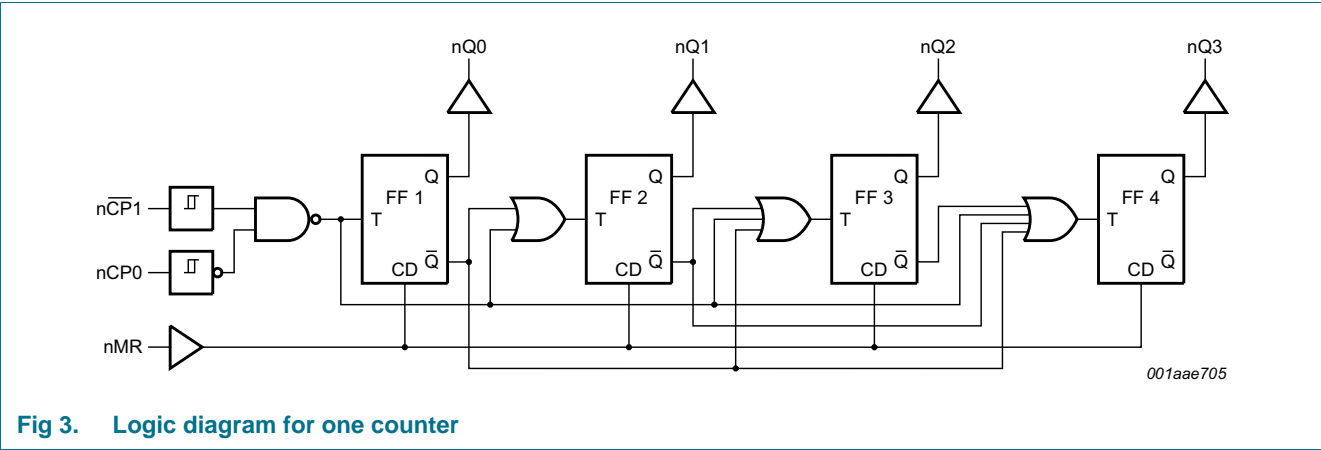


Fig 3. Logic diagram for one counter

5. Pinning information

5.1 Pinning

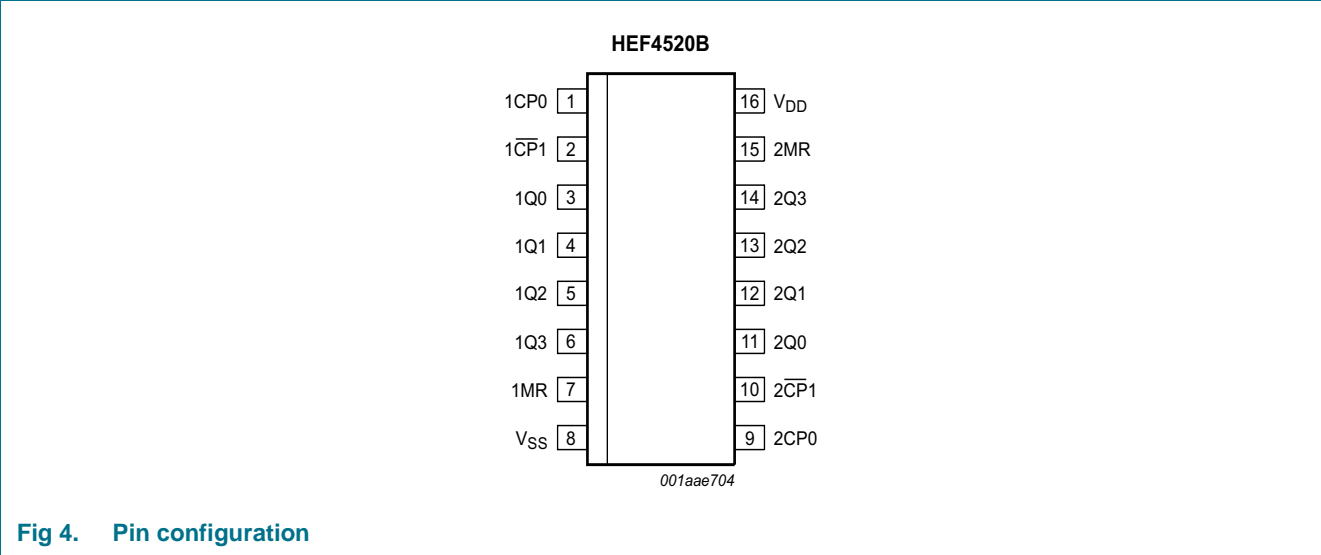


Fig 4. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1CP0, 2CP0	1, 9	clock input (LOW-to-HIGH triggered)
1CP1, 2CP1	2, 10	clock input (HIGH-to-LOW triggered)
1Q0 to 1Q3	3, 4, 5, 6	output
1MR, 2MR	7, 15	master reset input
V <sub>SS</sub>	8	ground supply voltage
2Q0 to 2Q3	11, 12, 13, 14	output
V <sub>DD</sub>	16	supply voltage

6. Functional description

Table 3. Function table<sup>[1]</sup>

nCP0	nCP1	nMR	Mode
↑	H	L	counter advances
L	↓	L	counter advances
↓	X	L	no change
X	↑	L	no change
↑	L	L	no change
H	↓	L	no change
X	X	H	nQ0 to nQ3 = LOW

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition; ↓ = negative-going transition.

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA
$I_{I/O}$	input/output current		-	$\pm 10$	mA
$I_{DD}$	supply current		-	50	mA
$T_{stg}$	storage temperature	per output	-65	+150	°C
$T_{amb}$	ambient temperature		-40	+85	°C
$P_{tot}$	total power dissipation	SO16 package <a href="#">[1]</a>	-	500	mW
$P$	power dissipation		-	100	mW

[1] For SO16 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

## 9. Static characteristics

**Table 6. Static characteristics**

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ °C}$		$T_{amb} = 25\text{ °C}$		$T_{amb} = 85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$ ; $V_I = V_{SS}$ or $V_{DD}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$ ; $V_I = V_{SS}$ or $V_{DD}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
$I_I$	input leakage current	$V_{DD} = 15\text{ V}$	15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	$I_O = 0\text{ A}$ ; $V_I = V_{SS}$ or $V_{DD}$	5 V	-	20	-	20	-	150	$\mu\text{A}$
			10 V	-	40	-	40	-	300	$\mu\text{A}$
			15 V	-	80	-	80	-	600	$\mu\text{A}$
$C_I$	input capacitance		-	-	-	-	7.5	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; for test circuit see [Figure 6](#); unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula	Min	Typ	Max	Unit
$t_{PHL}$	HIGH to LOW propagation delay	nCP0, nCP1 $\rightarrow$ nQn; see <a href="#">Figure 5</a>	5 V <a href="#">[1]</a>	$83\text{ ns} + (0.55\text{ ns/pF})C_L$	-	110	220	ns
			10 V	$39\text{ ns} + (0.23\text{ ns/pF})C_L$	-	50	100	ns
			15 V	$32\text{ ns} + (0.16\text{ ns/pF})C_L$	-	40	80	ns
		nMR $\rightarrow$ nQn; see <a href="#">Figure 5</a>	5 V	$48\text{ ns} + (0.55\text{ ns/pF})C_L$	-	75	150	ns
			10 V	$24\text{ ns} + (0.23\text{ ns/pF})C_L$	-	35	70	ns
			15 V	$17\text{ ns} + (0.16\text{ ns/pF})C_L$	-	25	50	ns

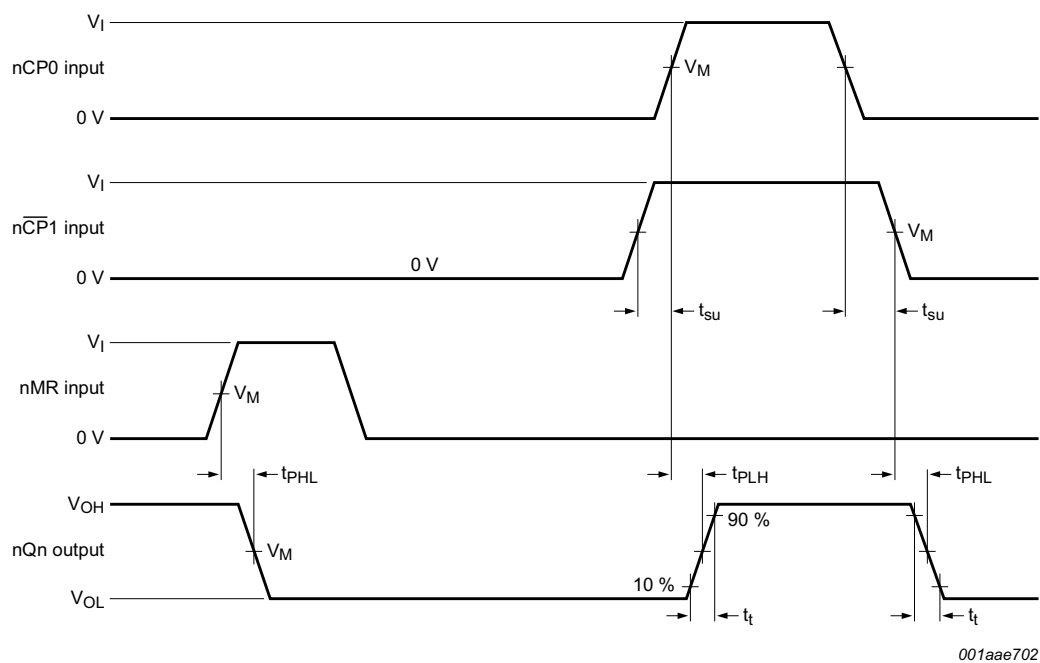
**Table 7. Dynamic characteristics ...continued** $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; for test circuit see [Figure 6](#); unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula	Min	Typ	Max	Unit
$t_{PLH}$	LOW to HIGH propagation delay	nCP0, $\overline{nCP1} \rightarrow nQn$ ; see <a href="#">Figure 5</a>	5 V [1]	$83\text{ ns} + (0.55\text{ ns/pF})C_L$	-	110	220	ns
			10 V	$39\text{ ns} + (0.23\text{ ns/pF})C_L$	-	50	100	ns
			15 V	$32\text{ ns} + (0.16\text{ ns/pF})C_L$	-	40	80	ns
$t_t$	transition time	nQn; see <a href="#">Figure 5</a>	5 V [1]	$10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
$t_W$	pulse width	nCP0 input LOW; minimum width; see <a href="#">Figure 5</a>	5 V		60	30	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		$\overline{nCP1}$ input HIGH; minimum width; see <a href="#">Figure 5</a>	5 V		60	30	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		nMR input HIGH; minimum width; see <a href="#">Figure 5</a>	5 V		30	15	-	ns
			10 V		20	10	-	ns
			15 V		16	8	-	ns
$t_{su}$	set-up time	nCP0 $\rightarrow \overline{nCP1}$ ; see <a href="#">Figure 5</a>	5 V		50	25	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		$\overline{nCP1} \rightarrow nCP0$ ; see <a href="#">Figure 5</a>	5 V		50	25	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
$t_{rec}$	recovery time	see <a href="#">Figure 5</a>	5 V		50	25	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
$f_{max}$	maximum frequency	nCP0, $\overline{nCP1}$ ; see <a href="#">Figure 5</a>	5 V		8	16	-	MHz
			10 V		15	30	-	MHz
			15 V		20	40	-	MHz

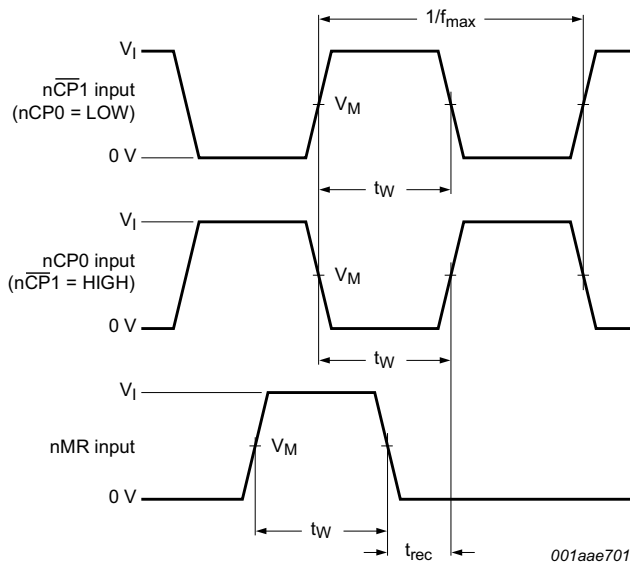
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ( $C_L$  in pF).**Table 8. Dynamic power dissipation  $P_D$**  $P_D$  can be calculated from the formulas shown.  $V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu\text{W}$ )	Where:
$P_D$	dynamic power dissipation	5 V	$P_D = 850 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz, $f_o$ = output frequency in MHz, $C_L$ = output load capacitance in pF, $V_{DD}$ = supply voltage in V, $\Sigma(f_o \times C_L)$ = sum of the outputs.
		10 V	$P_D = 3800 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 10200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

11. Waveforms



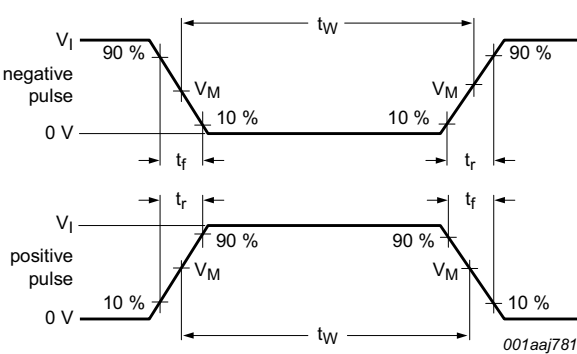
a. nCP0 and nCP1 set-up times, propagation delays and output transition times



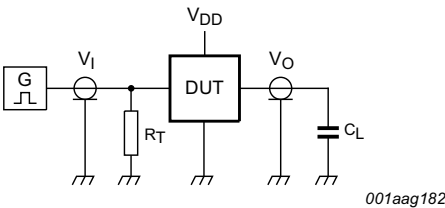
b. nMR recovery time, minimum nCP0, nCP1, and nMR pulse widths and maximum frequency

Measurement points are given in [Table 9](#).  
The logic levels  $V_{OH}$  and  $V_{OL}$  are typical output voltage levels that occur with the output load.

Fig 5. Waveforms showing measurements for switching times



a. Input waveforms



b. Test circuit

Test data is given in [Table 9](#).

Definitions for test circuit:

DUT = Device Under Test;

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

Fig 6. Test circuit for measuring switching times

Table 9. Measurement points and test data

Supply voltage	Input			Load
$V_{DD}$	$V_I$	$V_M$	$t_r, t_f$	$C_L$
5 V to 15 V	$V_{DD}$	$0.5V_I$	$\leq 20$ ns	50 pF



12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

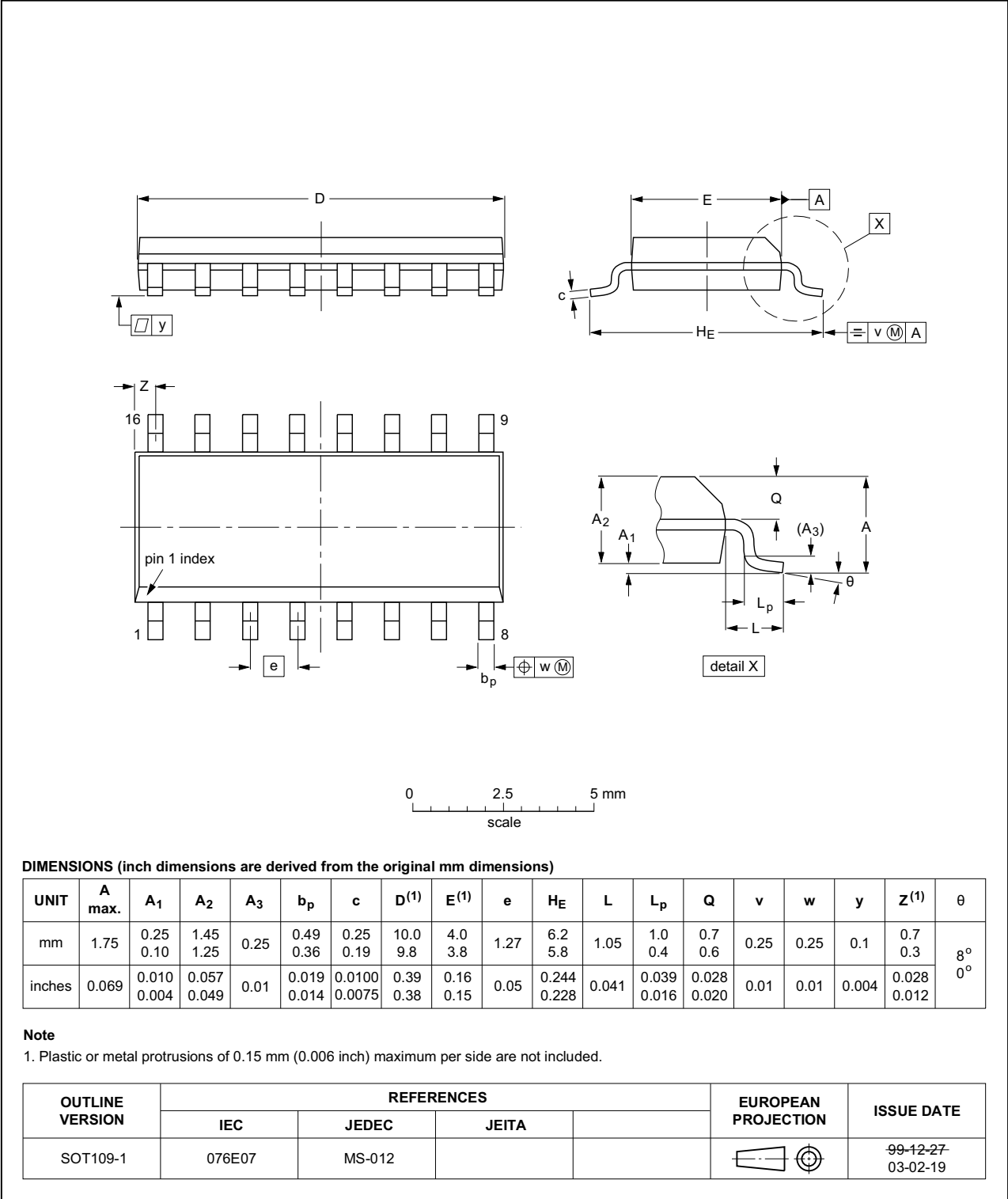


Fig 7. Package outline SOT109-1 (SO16)

## 13. Revision history

**Table 10. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4520B v.7	20160330	Product data sheet	-	HEF4520B v.6
Modifications:	<ul style="list-style-type: none"><li>Type number HEF4520BP (SOT38-4) removed.</li></ul>			
HEF4520B v.6	20111118	Product data sheet	-	HEF4520B v.5
Modifications:	<ul style="list-style-type: none"><li>Section Applications removed</li><li><a href="#">Table 6</a>: <math>I_{OH}</math> minimum values changed to maximum</li></ul>			
HEF4520B v.5	20091210	Product data sheet	-	HEF4520B v.4
HEF4520B v.4	20090828	Product data sheet	-	HEF4520B_CNV v.3
HEF4520B_CNV v.3	19950101	Product specification	-	HEF4520B_CNV v.2
HEF4520B_CNV v.2	19950101	Product specification	-	-

## 14. Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 30 March 2016

Document identifier: HEF4520B