AT24CS64

I²C-Compatible (2-wire) Serial EEPROM with a Unique, Factory Programmed 128-bit Serial Number

64-Kbit (8,192 x 8)

DATASHEET

Standard Features

- Low-voltage Operation
  - V_{CC} = 1.7V to 5.5V
- Internally Organized as 8,192 x 8 (64-Kbit)
- I²C-compatible (2-Wire) Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 400kHz (1.7V) and 1MHz (2.5V, 5.0V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 32-byte Page Write Mode
  - Partial Page Writes Allowed
- Self-timed Write Cycle (5ms Maximum)
- High-reliability
  - Endurance: 1,000,000 Write Cycles
  - Data Retention: 100 Years
- Green Package Options (Pb/Halide-free/RoHS-compliant)
  - 8-lead JEDEC SOIC, 8-lead TSSOP, and 8-pad UDFN
- Die Sale Options: Wafer Form and Tape and Reel Available

Enhanced Features in the CS Serial EEPROM Series

- All Standard Features Supported
- 128-bit Unique Factory-programmed Serial Number
  - Permanently Locked, Read-only Value
  - Stored in a Separate Memory Area
  - Guaranteed Unique Across Entire CS Series of Serial EEPROMs

1. Description

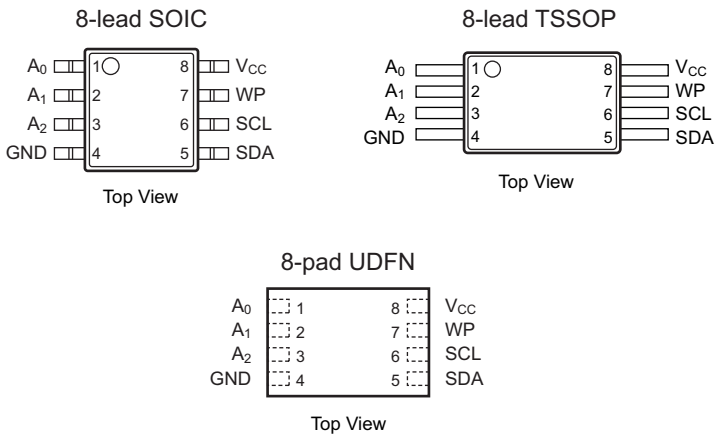
The Atmel® AT24CS64 provides 65,536 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 8,192 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT24CS64 is available in space-saving, 8-lead JEDEC SOIC, 8-lead TSSOP, and 8-pad UDFN packages and is accessed via a 2-wire serial interface. Full operation is guaranteed from 1.7V to 5.5V V_{CC}.

The AT24CS64 provides the additional feature of a factory programmed, guaranteed unique 128-bit serial number, while maintaining all of the traditional features available in the 64-Kbit Serial EEPROM. The time consuming step of performing and ensuring true serialization of product on a manufacturing line can be removed from the production flow by employing the CS Series Serial EEPROM. The 128-bit serial number is programmed and permanently locked from future writing during the Atmel production process. Further, this 128-bit location does not consume any of the user read/write area of the 64-Kbit Serial EEPROM. The uniqueness of the serial number is guaranteed across the entire CS Series of Serial EEPROMs, regardless of the size of the memory array or the type of interface protocol. This means that as an application's needs for memory size or interface protocol evolve in future generations, any previously deployed serial number from any Atmel CS Series Serial EEPROM part will remain valid.

2. Pin Descriptions and Pinout

Figure 2-1. Pin Configuration

Pin Name	Function
$A_0 – A_2$	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
GND	Ground
V_{CC}	Power Supply



Note: Drawings are not to scale.

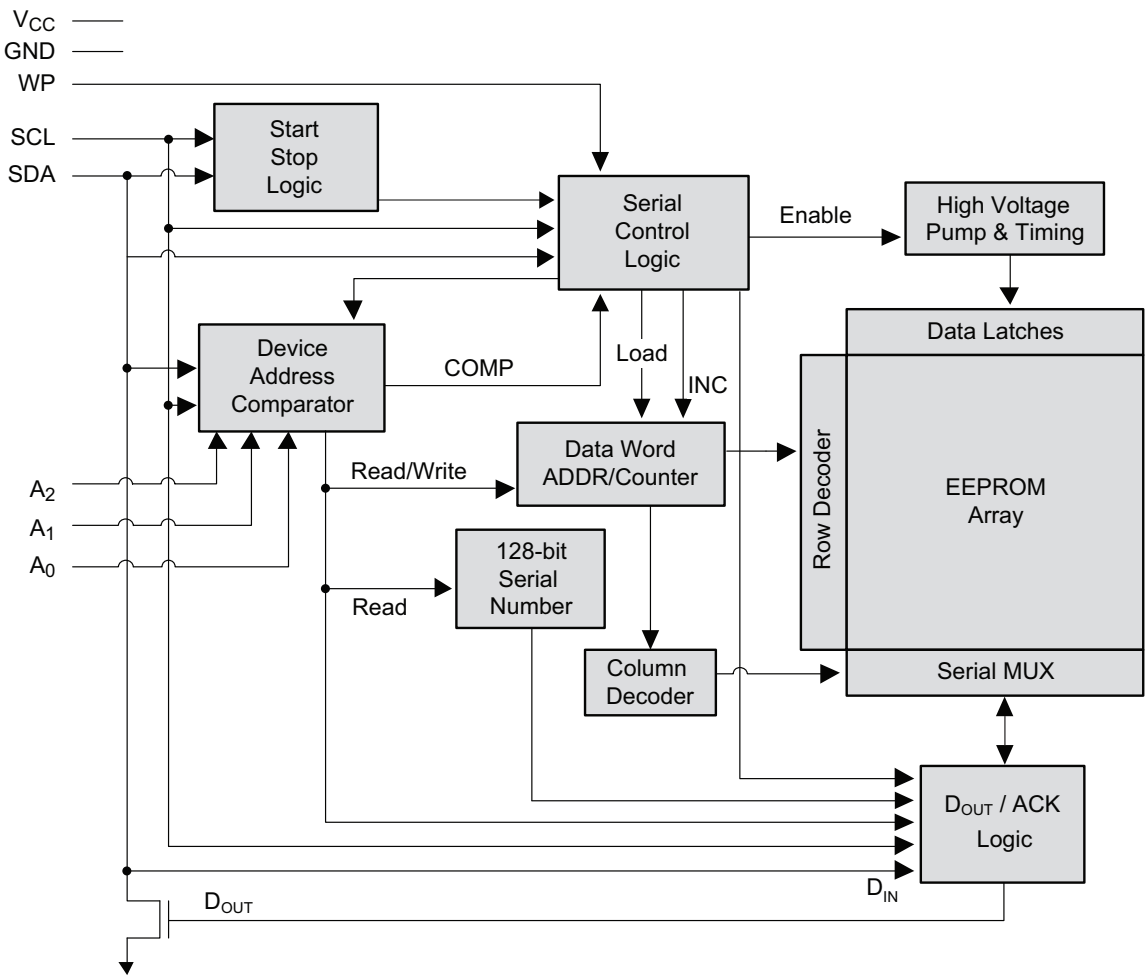
3. Absolute Maximum Ratings

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin With Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4. Block Diagram

Figure 4-1. Block Diagram



5. Pin Description

Serial Clock (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

Device/Page Addresses (A_2, A_1, A_0): The A_2, A_1, and A_0 pins are device address inputs that are hard wired for the AT24CS64. As many as eight 64-Kbit devices may be addressed on a single bus system. For more detail, see Section 8., “Device Addressing” on page 10.

Write Protect (WP): AT24CS64 has a Write Protect (WP) pin that provides hardware data protection. When the Write Protect pin is connected to ground (GND), normal read/write operations to the full array are possible. When the Write Protect pin is connected to V_{CC}, all write operations to the memory are inhibited but read operations are still possible. This operation is summarized in Table 5-1 below.

Table 5-1. Write Protect

WP Pin Status	Part of the Array Protected
At V_{CC}	Full Array
At GND	Normal Read/Write Operations

6. Memory Organization

AT24CS64, 64K Serial EEPROM: Internally organized with 256 pages of 32 bytes each, the 64K requires a 13-bit data word address for random word addressing.

6.1 Pin Capacitance

Table 6-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0MHz, V_{CC} = 5.5V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

6.2 DC Characteristics

Table 6-2. DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = 1.7V to 5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		1.7		5.5	V
I_{CC1}	Supply Current V_{CC} = 5.0V	Read at 400kHz		0.4	1.0	mA
I_{CC2}	Supply Current V_{CC} = 5.0V	Write at 400kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 1.7V	V_{IN} = V_{CC} or V_{SS}			1.0	µA
I_{SB2}	Standby Current V_{CC} = 5.5V	V_{IN} = V_{CC} or V_{SS}			6.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level[1]		–0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low Level V_{CC} = 1.7V	I_{OL} = 0.15mA			0.2	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1mA			0.4	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

6.3 AC Characteristics

Table 6-3. AC Characteristics

Applicable over recommended operating range from T_{AI} = -40°C to +85°C, V_{CC} = 1.7V to 5.5V, CL = 1TTL Gate and 100pF (unless otherwise noted).

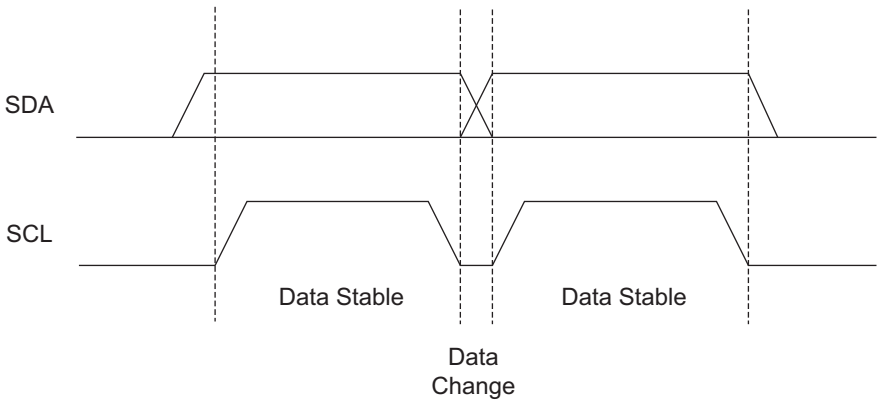
Symbol	Parameter	1.7V		2.5V, 5.0V		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.2		0.4		µs
t_{HIGH}	Clock Pulse Width High	0.6		0.4		µs
t_I	Noise Suppression Time		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	0.05	0.55	µs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3		0.5		µs
$t_{HD.STA}$	Start Hold Time	0.6		0.25		µs
$t_{SU.STA}$	Start Setup Time	0.6		0.25		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Setup Time	100		100		ns
t_R	Inputs Rise Time(1)		0.3		0.3	µs
t_F	Inputs Fall Time(1)		300		100	ns
$t_{SU.STO}$	Stop Setup Time	0.6		0.25		µs
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance(1)	3.3V, +25°C, Page Mode	1,000,000				Write Cycles

Note: 1. This parameter is ensured by characterization only.

7. Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined in Figure 7-2.

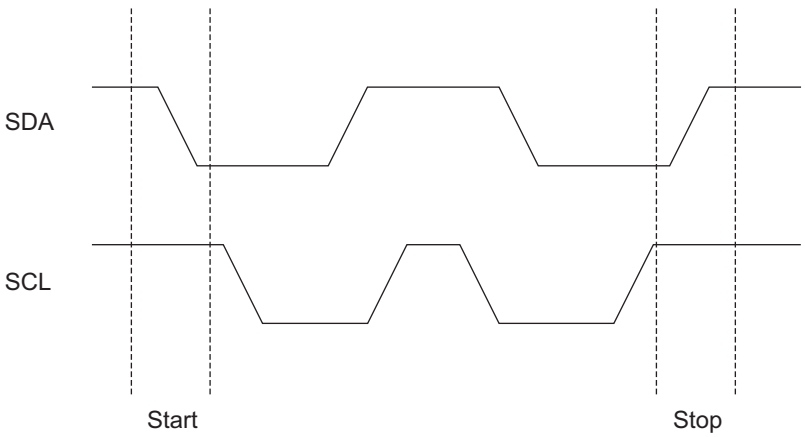
Figure 7-1. Data Validity



Start Condition: A high-to-low transition of SDA with SCL high is a Start condition which must precede any other command.

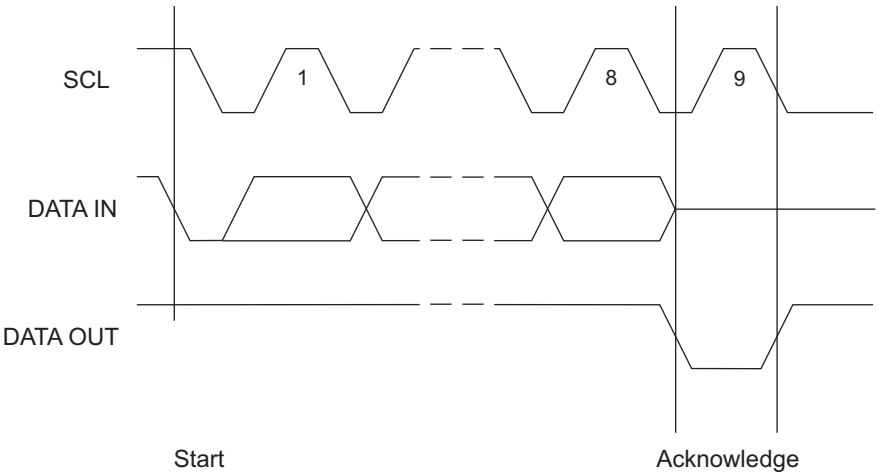
Stop Condition: A low-to-high transition of SDA with SCL high is a Stop condition. After a read sequence, the Stop command will place the EEPROM in a standby power mode.

Figure 7-2. Start and Stop Definition



Acknowledge: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Figure 7-3. Output Acknowledge



Standby Mode: The AT24CS64 features a low-power standby mode which is enabled upon power-up as well as after the receipt of the Stop condition and the completion of any internal operations.

2-wire Software Reset: After an interruption in protocol, power loss, or system reset, any 2-wire part can be reset by following these steps:

1. Create a Start condition (if possible).
2. Clock nine cycles.
3. Create another Start condition followed by Stop condition.

The device should be ready for the next communication after above steps have been completed. In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device.

Figure 7-4. Software Reset

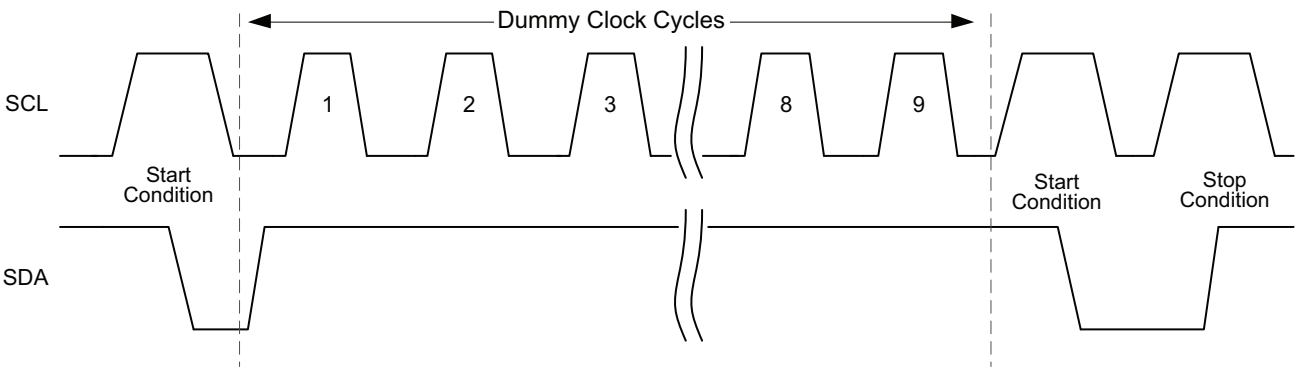


Figure 7-5. Bus Timing
SCL: Serial Clock, SDA: Serial Data I/O

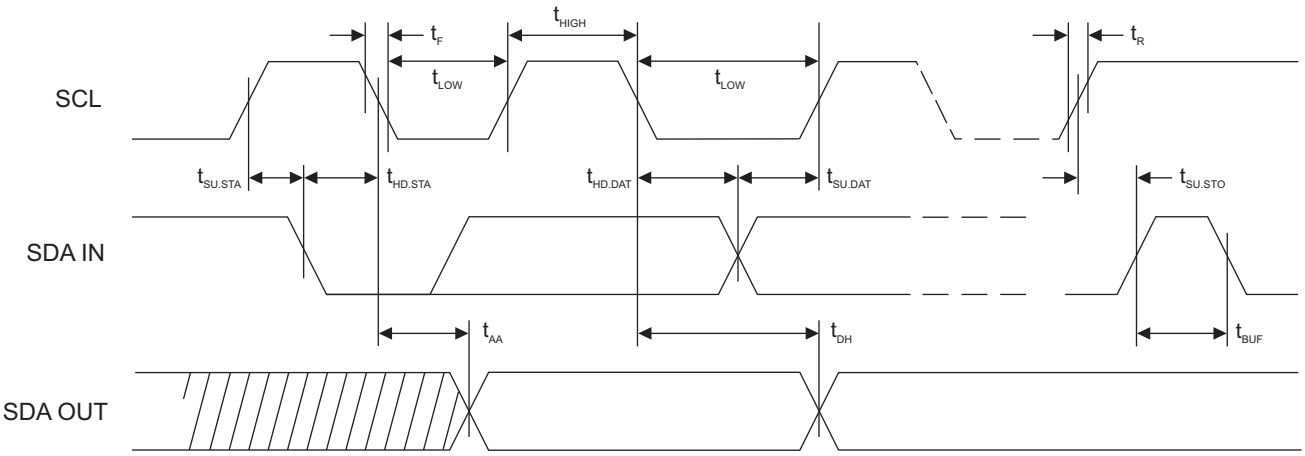
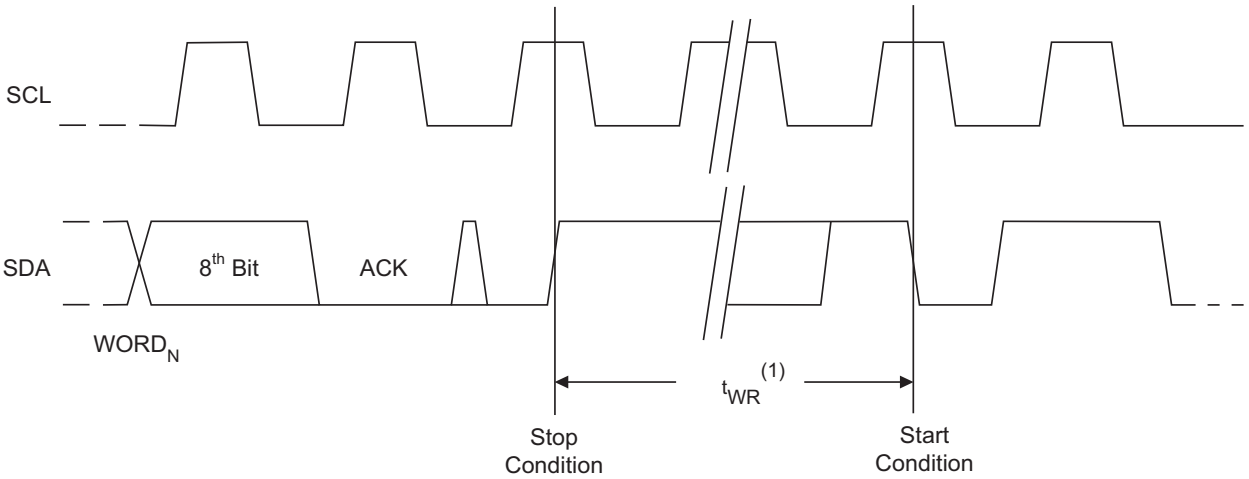


Figure 7-6. Write Cycle Timing
SCL: Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid Stop condition of a write sequence to the end of the internal clear/write cycle.

8. Device Addressing

Standard EEPROM Access: The 64K EEPROM device requires an 8-bit device address word following a Start condition to enable the chip for a read or write operation.

The device address word consists of a mandatory '1010' (Ah) sequence for the first four most significant bits as shown in Figure 8-1. This is common to all Serial EEPROM devices.

The next three bits are the A2, A1, and A0 device address bits for the 64K EEPROM. These three bits must compare to their corresponding hard-wired input pins A_2, A_1, and A_0 in order for the part to acknowledge.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a valid compare of the device address with hard-wired input pins A_2, A_1, and A_0, the EEPROM will output a zero. If a compare is not successfully made, the chip will return to a standby state.

Serial Number Access: The AT24CS64 utilizes a separate memory block containing a factory programmed 128-bit serial number. Access to this memory location is obtained by beginning the device address word with a '1011' (Bh) sequence.

The behavior of the next three bits (A2, A1, and A0) remain the same as during a standard EEPROM addressing sequence. These three bits must compare to their corresponding hard-wired input pins A_2, A_1, and A_0 in order for the part to acknowledge.

The eighth bit of the device address needs be set to a one to read the Serial Number. A zero in this bit position, other than during a dummy write sequence to set the address pointer, will result in a unknown data read from the part. Writing or altering the 128-bit serial number is not possible.

Further specific protocol is needed to read the serial number from of the device. See Section 10., “Read Operations” on page 12 for more details on accessing the special feature.

Table 8-1. Device Address

Access Area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEPROM	1	0	1	0	A_2	A_1	A_0	R/$\overline{W}$
Serial Number	1	0	1	1	A_2	A_1	A_0	1
	MSB							LSB

Table 8-2. First Word Address

Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEPROM	X	X	X	A12	A11	A10	A9	A8
Serial Number	X	X	X	X	1	0	X	X
	MSB							LSB

Note: X = Don't care bit.

Table 8-3. Second Word Address

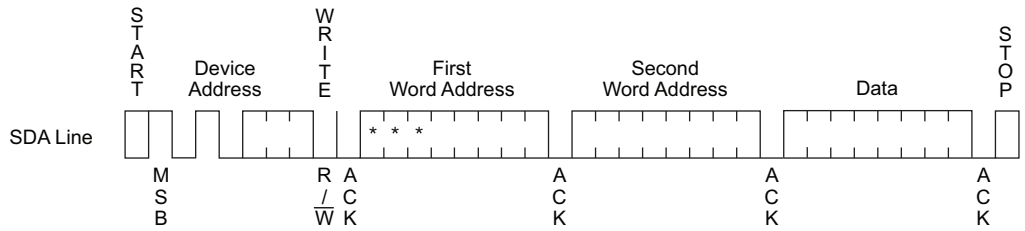
Access Area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEPROM	A7	A6	A5	A4	A3	A2	A1	A0
Serial Number	X	X	X	A4	A3	A2	A1	A0
	MSB							LSB

Note: X = Don't care bit.

9. Write Operations

Byte Write: A Byte Write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a Stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory (see Figure 7-6). All inputs are disabled during this write cycle and the EEPROM will not respond until the Write is complete (see Figure 9-1).

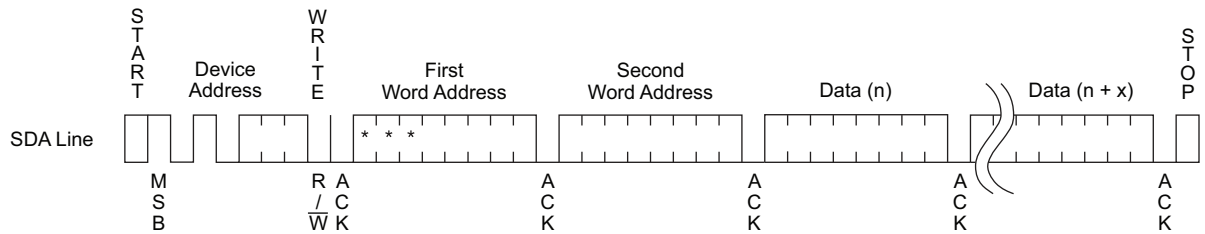
Figure 9-1. Byte Write



Note: * = Don't care bit.

Page Write: The 64K EEPROM is capable of a 32-byte Page Write. A Page Write is initiated in the same way as a Byte Write, but the microcontroller does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 additional data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the Page Write sequence with a Stop condition.

Figure 9-2. Page Write



Note: * = Don't care bit.

The data word address lower five bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the internally generated word address reaches the page boundary, the subsequent byte loaded will be placed at the beginning of the same page. If more than eight data words are transmitted to the EEPROM, the data word address will roll-over and previously loaded data will be overwritten.

Acknowledge Polling: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a Start condition followed by the device address word. The Read/Write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the next read or write sequence to begin.

10. Read Operations

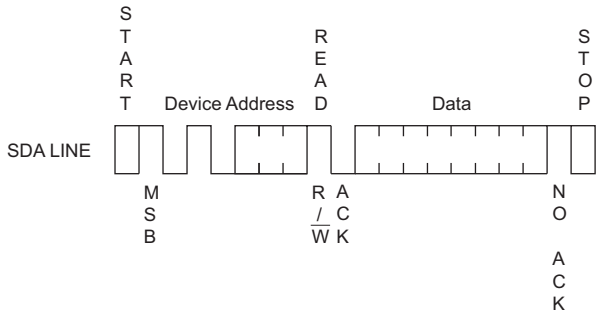
Read operations are initiated in the same way as Write operations with the exception that the Read/Write select bit in the device address word is set to one. There are four read operations:

- Current Address Read
- Random Address Read
- Sequential Read
- Serial Number Read

Current Address Read: The internal data word address counter maintains the last address accessed during the last Read or Write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

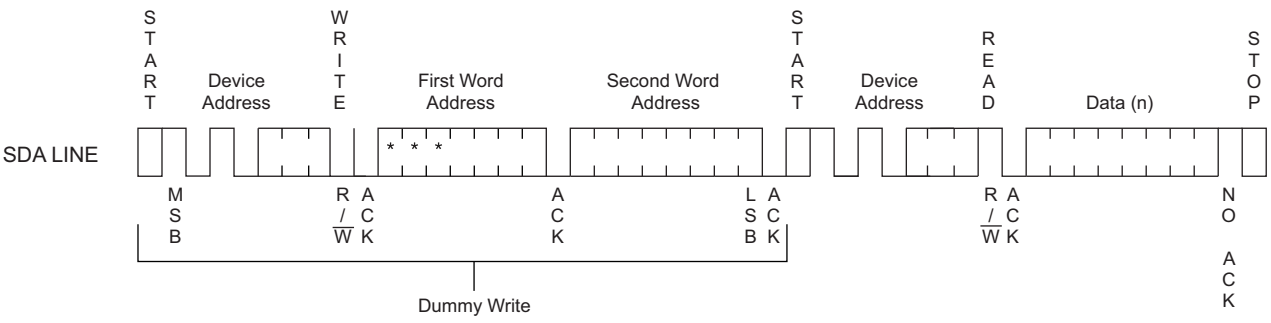
Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with a zero but does generate a following Stop condition.

Figure 10-1. Current Address Read



Random Read: A Random Read requires a dummy byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another Start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following Stop condition.

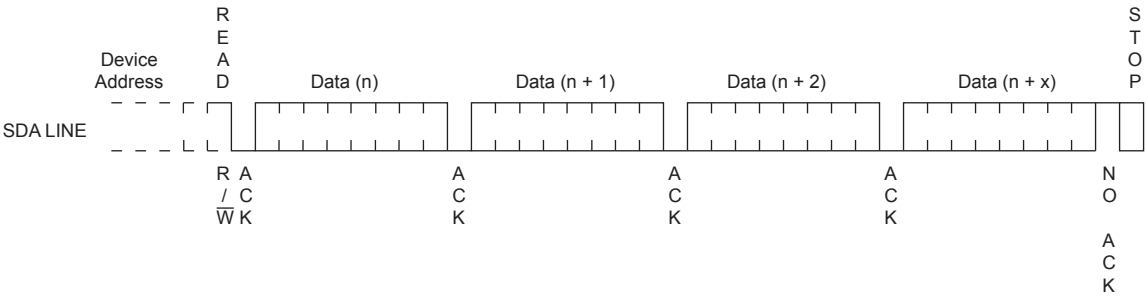
Figure 10-2. Random Read



Note: * = Don't care bit.

Sequential Read: Sequential Reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a zero but does generate a following Stop condition.

Figure 10-3. Sequential Read



Serial Number Read: Reading the serial number is similar to the sequential read sequence but requires use of the device address seen in Table 8-1 on page 10, a dummy write, and the use of a specific word address.

Note: The entire 128-bit value must be read from the starting address of the serial number block to guarantee a unique number.

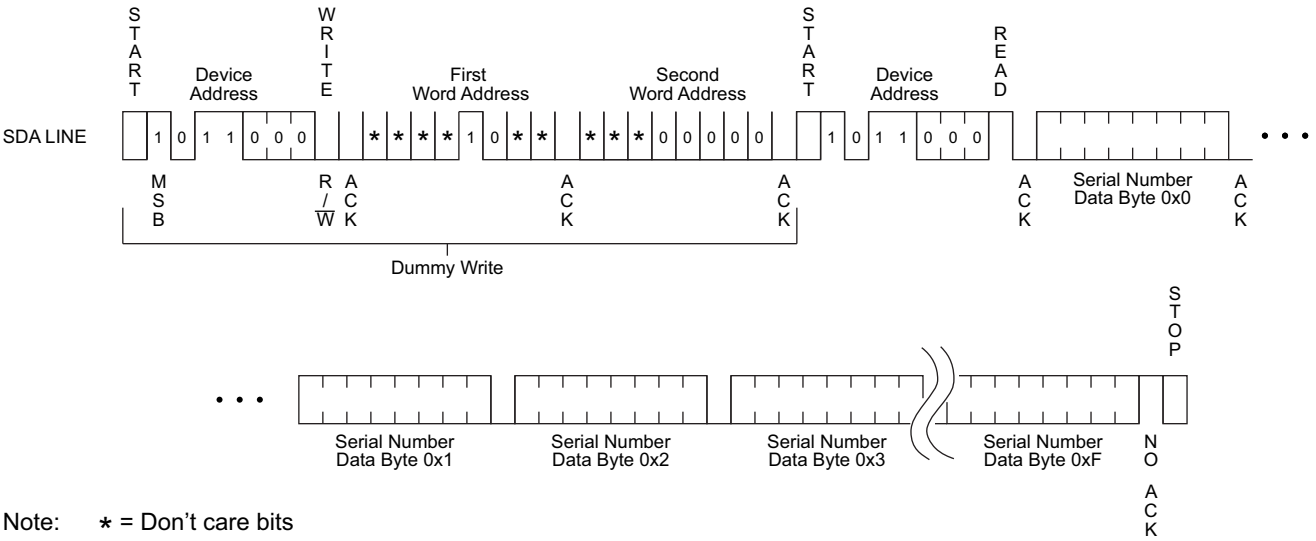
Since the address pointer of the device is shared between the regular EEPROM array and the serial number block, a dummy write sequence, as part of a Random Read or Sequential Read protocol, should be performed to ensure the address pointer is set to zero. A Current Address Read of the serial number block is supported but if the previous operation was to the EEPROM array, the address pointer will retain the last location accessed, incremented by one. Reading the serial number from a location other than the first address of the block will not result in a unique serial number.

Additionally, the word address contains a `'10'` sequence in bit A11 and A10 of the word address, regardless of the intended address as depicted in Table 8-2 on page 10. If a word address other than `'10'` is used, then the device will output undefined data.

Example: If the application desires to read the first byte of the serial number, the word address input would need to be 0800h.

When the end of the 128-bit serial number is reached (16 bytes of data), continued reading of the extended memory region will result in an additional 16 bytes of 00h data. Upon reaching the end of the 32-byte extended memory region, the data word address will roll-over back to the beginning of the 128-bit serial number. The Serial Number Read operation is terminated when the microcontroller does not respond with a zero (ACK) and instead issues a Stop condition (see Figure 10-4 on page 14).

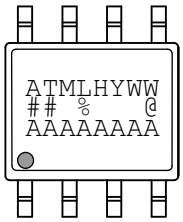
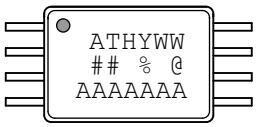
Figure 10-4. Serial Number Read



Note: * = Don't care bits

11. Part Markings

AT24CS64: Package Marking Information

8-lead SOIC	8-lead TSSOP	8-lead UDFN
		2.0 x 3.0 mm Body 

Note 1: ● *designates pin 1*

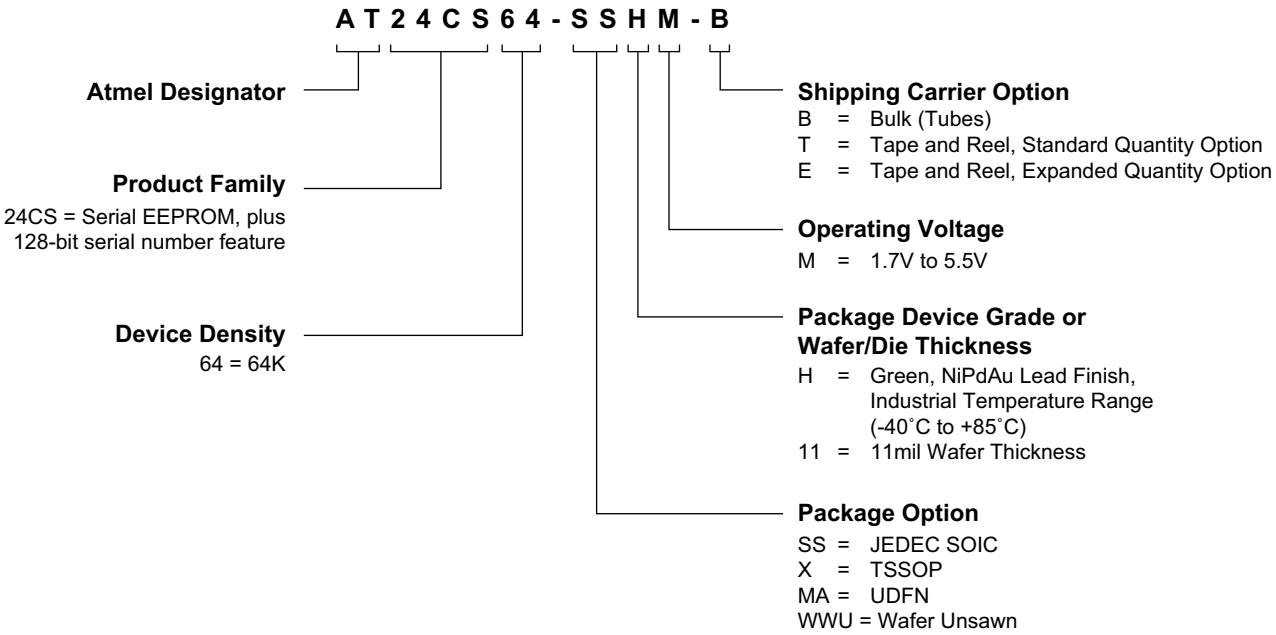
Note 2: Package drawings are not to scale

Catalog Number Truncation			
AT24CS64		Truncation Code ##: NC	
Date Codes			**Voltages**
Y = Year	M = Month	WW = Work Week of Assembly	Minimum Voltage = %
3: 2013 7: 2017 4: 2014 8: 2018 5: 2015 9: 2019 6: 2016 0: 2020	A: January B: February ... L: December	02: Week 2 04: Week 4 ... 52: Week 52	M: 1.7V min
Country of Assembly	**Lot Number**		**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number		H: Industrial/NiPdAu
Trace Code			**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

8/9/13

Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	TITLE	DRAWING NO.	REV.
	24CS64SM, AT24CS64 Package Marking Information	24CS64SM	A

12. Ordering Code Detail



13. Ordering Information

Additional package types that are not listed may be available. Please contact Atmel for more details.

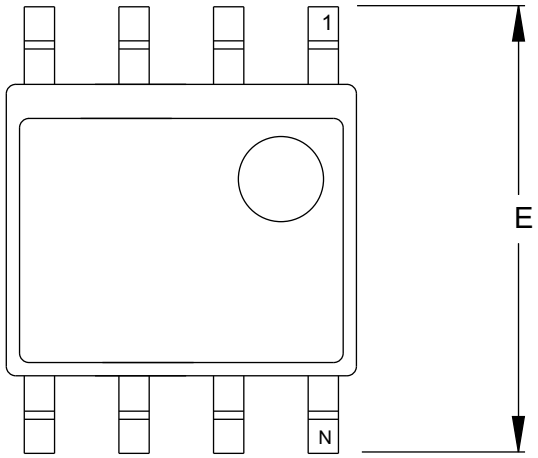
Atmel Ordering Code[1]	Lead Finish	Package	Delivery Information		Operation Range
			Form	Quantity	
AT24CS64-SSHM-B	NiPdAu (Lead-free/Halogen-free)	8S1	Bulk (Tubes)	100 per Tube	Industrial Temperature (-40°C to 85°C)
AT24CS64-SSHM-T			Tape and Reel	4,000 per Reel	
AT24CS64-XHM-B		8X	Bulk (Tubes)	100 per Tube	
AT24CS64-XHM-T			Tape and Reel	5,000 per Reel	
AT24CS64-MAHM-T		8MA2	Tape and Reel	5,000 per Reel	
AT24CS64-MAHM-E			Tape and Reel	15,000 per Reel	
AT24CS64-WWU11M[2]	N/A	Wafer Sale	Note 2		

Notes:
1. Consistent with the general semiconductor market trend, Atmel will supply devices with either gold or copper bond wires to increase manufacturing flexibility and to ensure a long-term continuity of supply. There is no difference in product quality, reliability, or performance between the two variations.
2. For Wafer sales, please contact Atmel Sales.

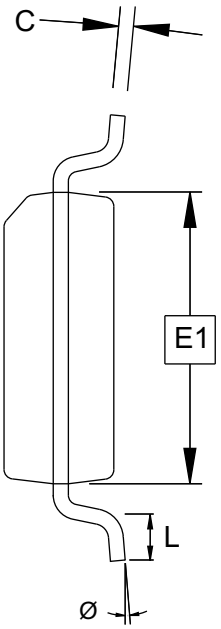
Package Type	
8S1	8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead, 4.4mm body, Plastic Thin Shrink Small Outline Package (TSSOP)
8MA2	8-pad, 2.0mm x 3.0mm body, 0.5mm pitch, Dual No Lead (UDFN)

14. Packaging Information

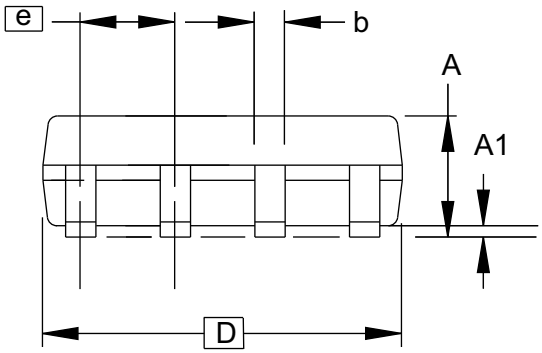
14.1 8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

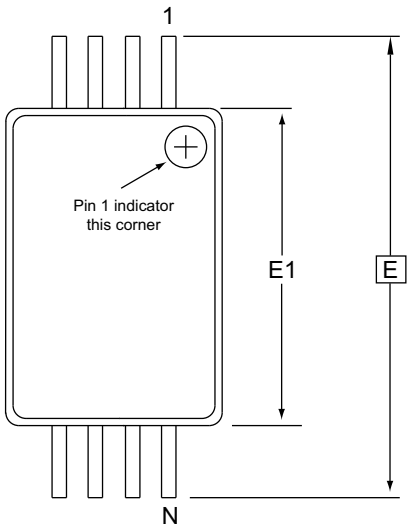
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

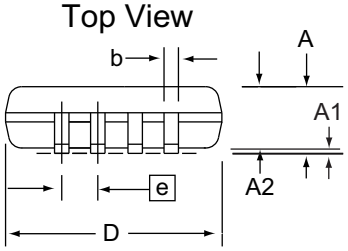
6/22/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**GPC** SWB	**DRAWING NO.** 8S1	**REV.** G

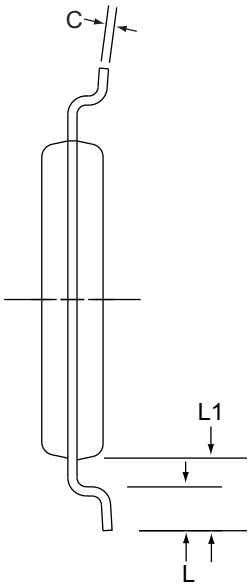
14.2 8X — 8-lead TSSOP



Top View



Side View



End View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

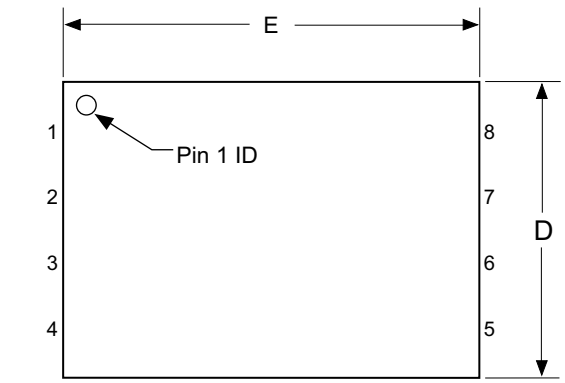
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	0.25	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

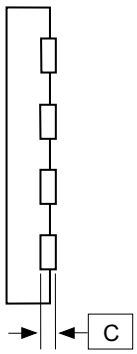
2/27/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	GPC TNR	DRAWING NO. 8X	REV. E

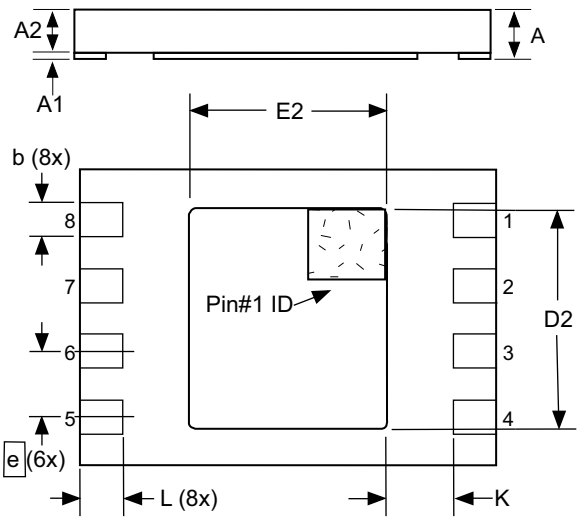
14.3 8MA2 — 8-pad UDFN



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Notes:
1. This drawing is for general information only. Refer to Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. The Pin #1 ID is a laser-marked feature on Top View.
3. Dimensions b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
4. The Pin #1 ID on the Bottom View is an orientation feature on the thermal pad.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.50	0.55	0.60	
A1	0.0	0.02	0.05	
A2	-	-	0.55	
D	1.90	2.00	2.10	
D2	1.40	1.50	1.60	
E	2.90	3.00	3.10	
E2	1.20	1.30	1.40	
b	0.18	0.25	0.30	3
C	1.52 REF			
L	0.30	0.35	0.40	
e	0.50 BSC			
K	0.20	-	-	

11/26/14

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8MA2, 8-pad 2 x 3 x 0.6mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No-Lead Package (UDFN)	**GPC** YNZ	**DRAWING NO.** 8MA2	**REV.** G

15. Revision History

Doc. Rev.	Date	Comments
8870D	01/2015	Add the UDFN Expanded Quantity Option an update the ordering information section.
8870C	08/2014	Add bulk SOIC and TSSOP ordering codes. Update ordering code table, 8X and 8MA2 package drawings, and update the disclaimer page.
8870B	05/2014	Update 8MA2 and 8X package drawings, disclaimer page, and datasheet status from preliminary to complete.
8870A	08/2013	Initial document release.

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