



# PSMN6R1-30YLD

N-channel 30 V, 6.1 mΩ logic level MOSFET in LFPAK56 using NextPowerS3 Technology

19 September 2014

Product data sheet

## 1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LFPAK56 package. NextPowerS3 portfolio utilising Nexperia's unique "SchottkyPlus" technology delivers high efficiency, low spiking performance usually associated with MOSFETs with an integrated Schottky or Schottky-like diode but without problematic high leakage current. NextPowerS3 is particularly suited to high efficiency applications at high switching frequencies.

## 2. Features and benefits

- Ultra low  $Q_G$ ,  $Q_{GD}$  and  $Q_{OSS}$  for high system efficiency, especially at higher switching frequencies
- Superfast switching with soft-recovery; s-factor  $> 1$
- Low spiking and ringing for low EMI designs
- Unique "SchottkyPlus" technology; Schottky-like performance with  $< 1 \mu\text{A}$  leakage at 25 °C
- Optimised for 4.5 V gate drive
- Low parasitic inductance and resistance
- High reliability clip bonded and solder die attach Power SO8 package; no glue, no wire bonds, qualified to 175 °C
- Wave solderable; exposed leads for optimal visual solder inspection

## 3. Applications

- On-board DC-to-DC solutions for server and telecommunications
- Secondary-side synchronous rectification in telecommunication applications
- Voltage regulator modules (VRM)
- Point-of-Load (POL) modules
- Power delivery for V-core, ASIC, DDR, GPU, VGA and system components
- Brushed and brushless motor control

## 4. Quick reference data

Table 1. Quick reference data

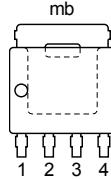
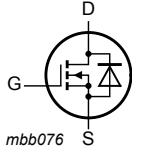
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25 \text{ }^\circ\text{C} \leq T_j \leq 175 \text{ }^\circ\text{C}$	-	-	30	V
$I_D$	drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; $V_{GS} = 10 \text{ V}$ ; <a href="#">Fig. 2</a>	-	-	66	A
$P_{tot}$	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 1</a>	-	-	47	W

**nexperia**

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T <sub>j</sub>	junction temperature			-55	-	175	°C
<b>Static characteristics</b>							
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 15 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>		-	6.5	8.35	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 15 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>		-	5.05	6	mΩ
<b>Dynamic characteristics</b>							
Q <sub>GD</sub>	gate-drain charge	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 15 A; V <sub>DS</sub> = 15 V; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>		-	2.1	3.15	nC
Q <sub>G(tot)</sub>	total gate charge	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 15 A; V <sub>DS</sub> = 15 V; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>		-	6.8	10.2	nC
<b>Source-drain diode</b>							
S	softness factor	I <sub>S</sub> = 15 A; V <sub>GS</sub> = 0 V; dI <sub>S</sub> /dt = -100 A/μs; V <sub>DS</sub> = 15 V; <a href="#">Fig. 16</a>		-	1.3	-	

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain	 LFPAK56; Power-SO8 (SOT669)	

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN6R1-30YLD	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN6R1-30YLD	6D130L

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$25^{\circ}\text{C} \leq T_j \leq 175^{\circ}\text{C}$		-	30	V
$V_{DGR}$	drain-gate voltage	$25^{\circ}\text{C} \leq T_j \leq 175^{\circ}\text{C}; R_{GS} = 20\text{ k}\Omega$		-	30	V
$V_{GS}$	gate-source voltage			-20	20	V
$P_{\text{tot}}$	total power dissipation	$T_{mb} = 25^{\circ}\text{C}$ ; <a href="#">Fig. 1</a>		-	47	W
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25^{\circ}\text{C}$ ; <a href="#">Fig. 2</a>		-	66	A
		$V_{GS} = 10\text{ V}; T_{mb} = 100^{\circ}\text{C}$ ; <a href="#">Fig. 2</a>		-	46	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25^{\circ}\text{C}$ ; <a href="#">Fig. 3</a>		-	263	A
$T_{\text{stg}}$	storage temperature			-55	175	$^{\circ}\text{C}$
$T_j$	junction temperature			-55	175	$^{\circ}\text{C}$
$T_{\text{sld(M)}}$	peak soldering temperature			-	260	$^{\circ}\text{C}$
$V_{\text{ESD}}$	electrostatic discharge voltage	HBM		250	-	V
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25^{\circ}\text{C}$		-	39	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25^{\circ}\text{C}$		-	250	A
<b>Avalanche ruggedness</b>						
$E_{\text{DS(AL)S}}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25^{\circ}\text{C}; I_D = 15\text{ A}; V_{\text{sup}} \leq 30\text{ V}; R_{GS} = 50\text{ }\Omega$ ; unclamped; $t_p = 145\text{ }\mu\text{s}$	[1]	-	42	mJ

[1] Protected by 100% test

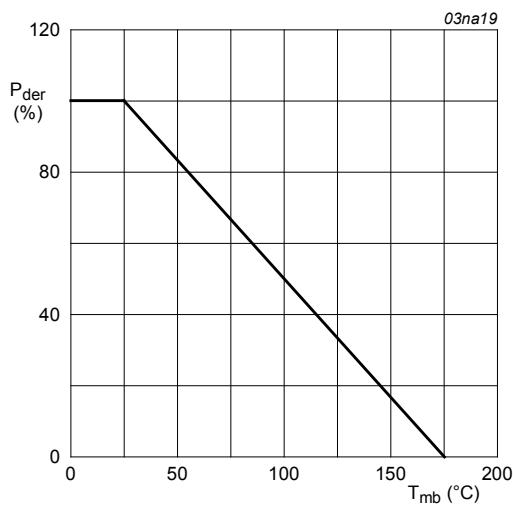


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot}(25^{\circ}\text{C})} \times 100 \%$$

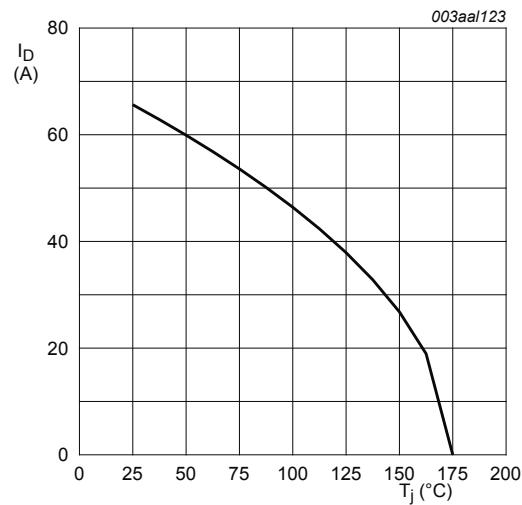


Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10 \text{ V}$$

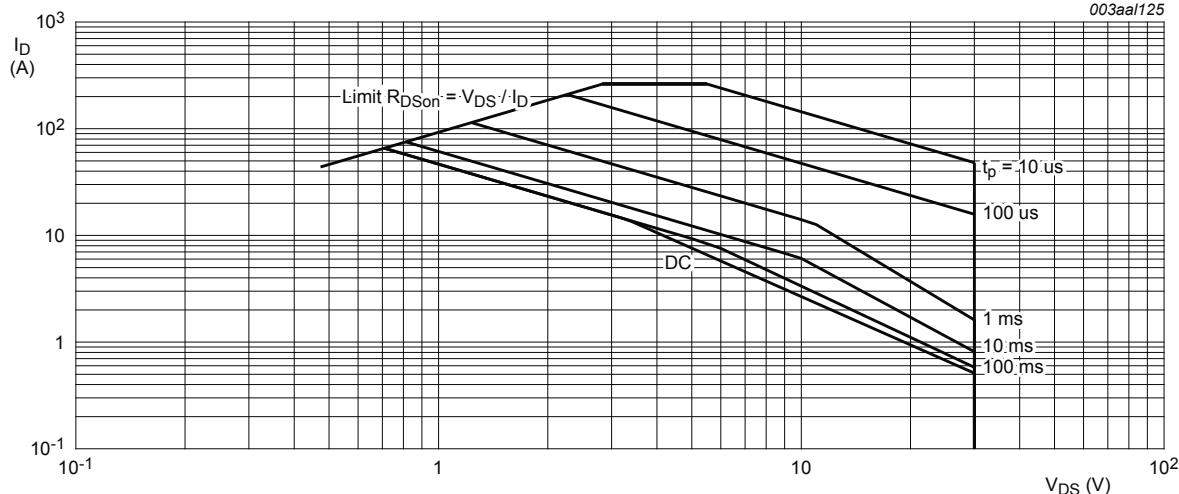


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$$T_{mb} = 25^{\circ}\text{C}; I_{DM} \text{ is a single pulse}$$

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	3	3.22	K/W

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	<a href="#">Fig. 5</a>		-	50	-	K/W
		<a href="#">Fig. 6</a>		-	125	-	K/W

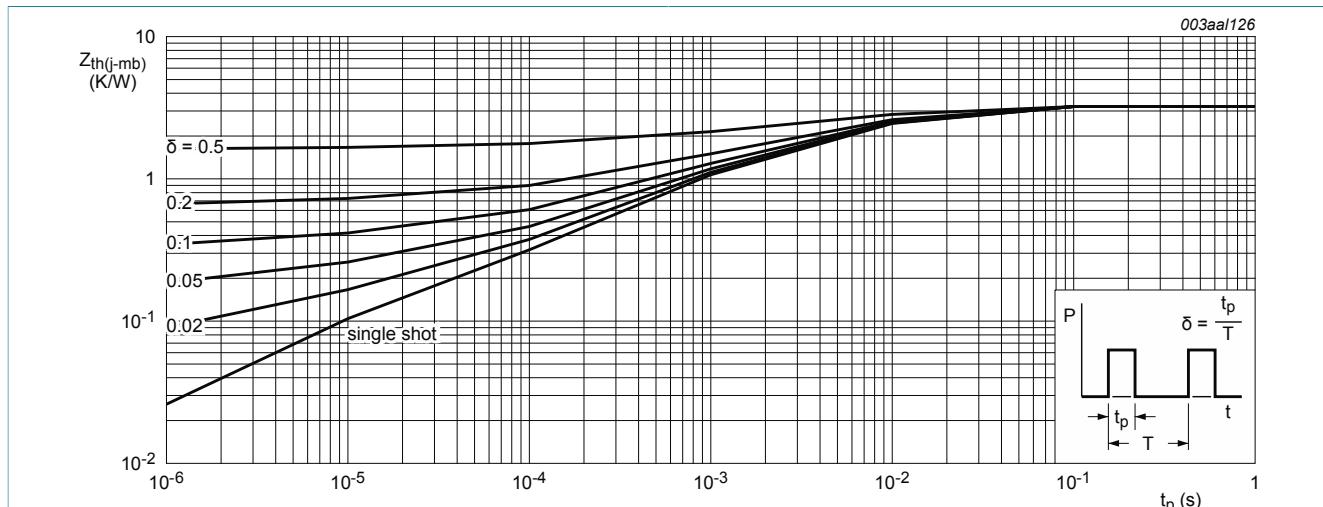


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

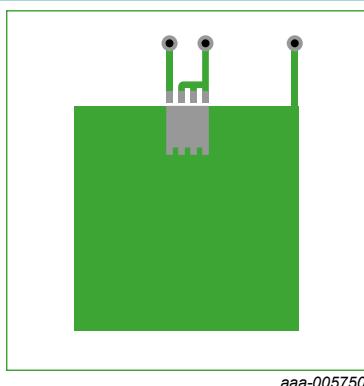


Fig. 5. PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper

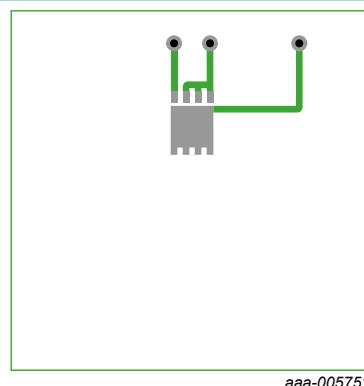


Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Static characteristics</b>							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$		30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55^\circ C$		27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25^\circ C$		1.2	1.68	2.2	V

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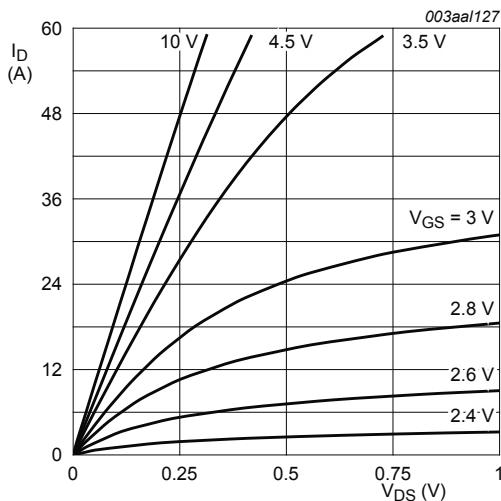
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25^\circ C \leq T_j \leq 150^\circ C$		-	-3.9	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 24 V; V_{GS} = 0 V; T_j = 25^\circ C$		-	-	1	μA
		$V_{DS} = 24 V; V_{GS} = 0 V; T_j = 150^\circ C$		-	-	100	μA
$I_{GSS}$	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5 V; I_D = 15 A; T_j = 25^\circ C$ <a href="#">Fig. 10</a>		-	6.5	8.35	mΩ
		$V_{GS} = 4.5 V; I_D = 15 A; T_j = 150^\circ C$ <a href="#">Fig. 11</a> ; <a href="#">Fig. 10</a>		-	-	13.8	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 25^\circ C$ <a href="#">Fig. 10</a>		-	5.05	6	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 150^\circ C$ <a href="#">Fig. 11</a> ; <a href="#">Fig. 10</a>		-	-	9.9	mΩ
$R_G$	gate resistance	$f = 1 MHz$		-	0.44	0.88	Ω

## Dynamic characteristics

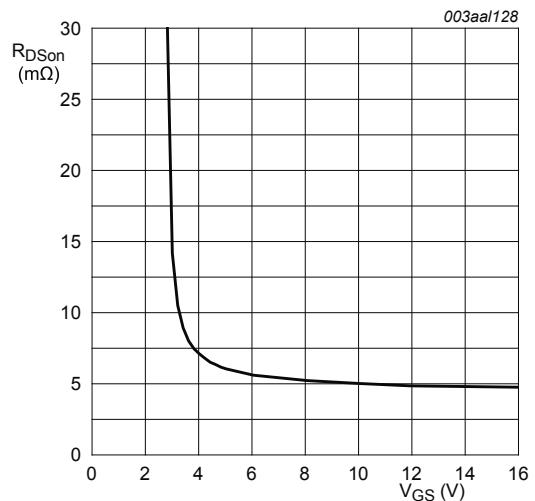
$Q_{G(tot)}$	total gate charge	$I_D = 15 A; V_{DS} = 15 V; V_{GS} = 10 V$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>		-	14.2	21.3	nC
		$I_D = 15 A; V_{DS} = 15 V; V_{GS} = 4.5 V$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>		-	6.8	10.2	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$		-	13.3	-	nC
$Q_{GS}$	gate-source charge	$I_D = 15 A; V_{DS} = 15 V; V_{GS} = 4.5 V$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>		-	2.2	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	1.3	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	0.9	-	nC
$Q_{GD}$	gate-drain charge			-	2.1	3.15	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 15 A; V_{DS} = 15 V$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>		-	2.7	-	V
$C_{iss}$	input capacitance	$V_{DS} = 15 V; V_{GS} = 0 V; f = 1 MHz$ $T_j = 25^\circ C$ ; <a href="#">Fig. 14</a>		-	817	1225	pF
$C_{oss}$	output capacitance			-	605	908	pF
$C_{rss}$	reverse transfer capacitance			-	62	93	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 V; R_L = 1 \Omega; V_{GS} = 4.5 V$ $R_{G(ext)} = 5 \Omega$		-	7.5	-	ns
$t_r$	rise time			-	11	-	ns
$t_{d(off)}$	turn-off delay time			-	9.8	-	ns
$t_f$	fall time			-	7.2	-	ns

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$Q_{oss}$	output charge	$V_{GS} = 0 \text{ V}$ ; $V_{DS} = 15 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ\text{C}$		-	11.8	-	nC
<b>Source-drain diode</b>							
$V_{SD}$	source-drain voltage	$I_S = 10 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 15</a>		-	0.78	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 15 \text{ A}$ ; $dI_S/dt = -100 \text{ A}/\mu\text{s}$ ; $V_{GS} = 0 \text{ V}$ ; $V_{DS} = 15 \text{ V}$ ; <a href="#">Fig. 16</a>		-	23.8	47.6	ns
$Q_r$	recovered charge		[1]	-	12.6	25.2	nC
$t_a$	reverse recovery rise time			-	10.3	-	ns
$t_b$	reverse recovery fall time			-	13.5	-	ns
S	softness factor			-	1.3	-	

[1] includes capacitive recovery



**Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values**



**Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25 \text{ }^\circ\text{C}$ ;  $I_D = 15 \text{ A}$

## N-channel 30 V, 6.1 mΩ logic level MOSFET in LFPAK56 using NextPowerS3 Technology

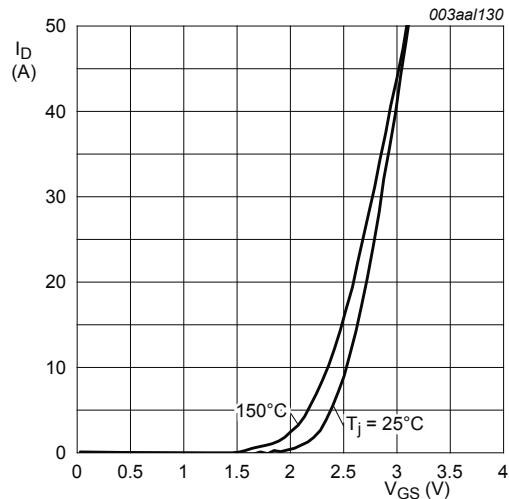


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 12\text{V}$

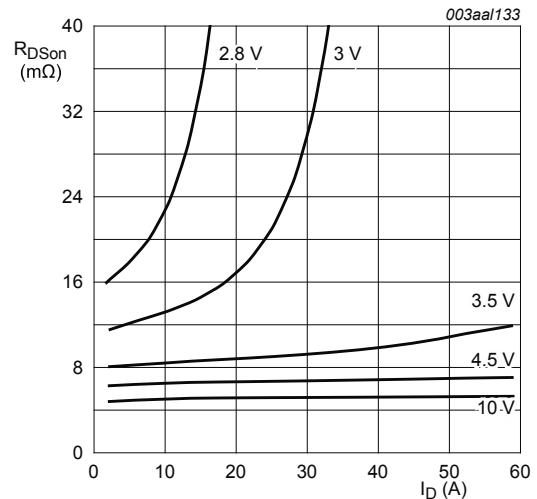


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ\text{C}$

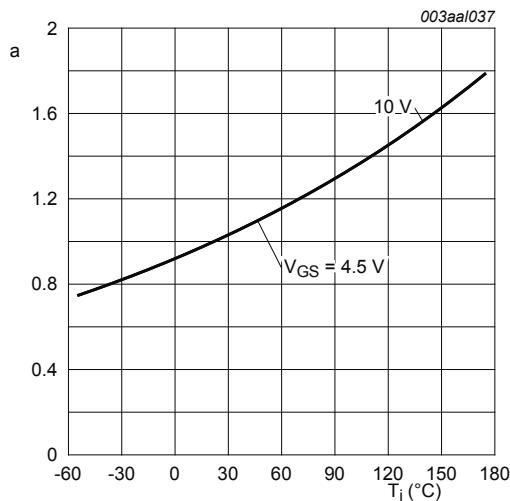


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

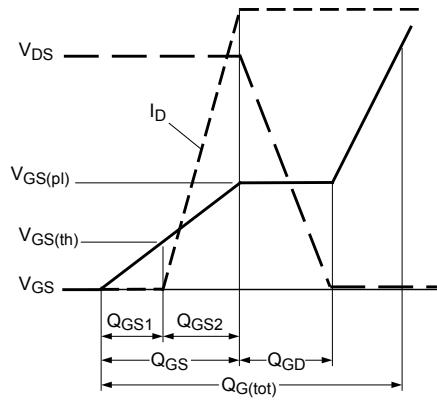


Fig. 12. Gate charge waveform definitions

## N-channel 30 V, 6.1 mΩ logic level MOSFET in LFPAK56 using NextPowerS3 Technology

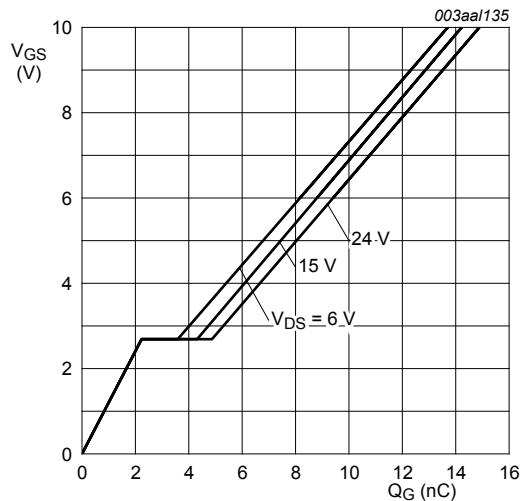


Fig. 13. Gate-source voltage as a function of gate charge; typical values

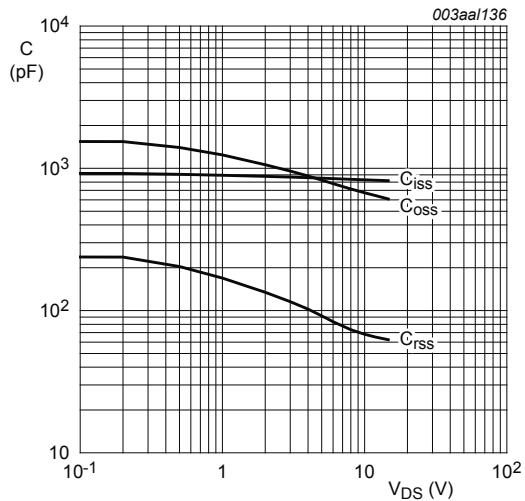
 $T_j = 25^\circ C$ ;  $I_D = 15A$ 

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

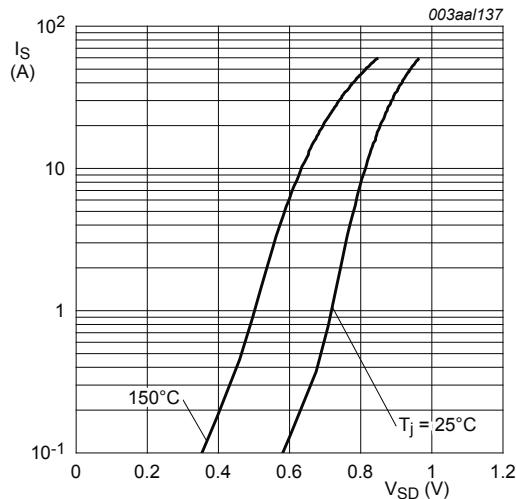
 $V_{GS} = 0V$ ;  $f = 1MHz$ 

Fig. 15. Source current as a function of source-drain voltage; typical values

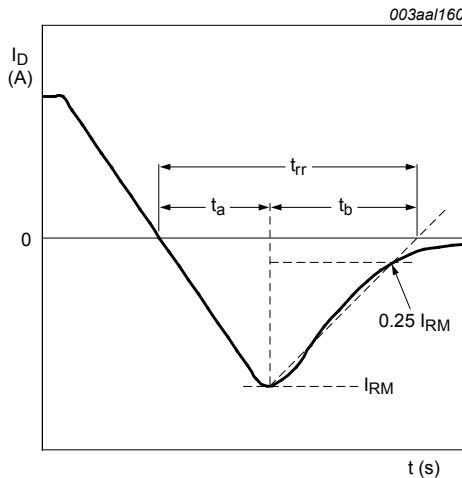
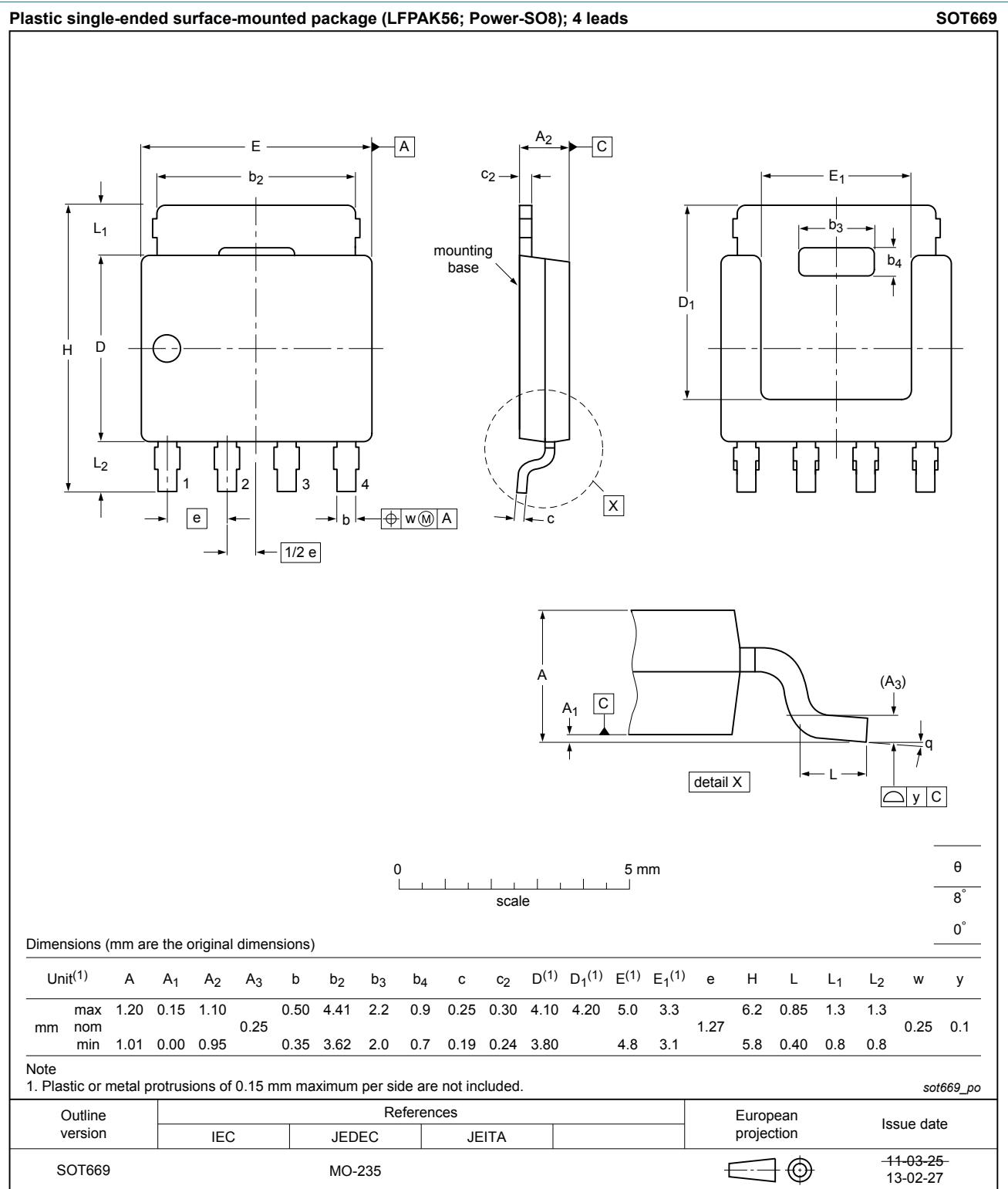


Fig. 16. Reverse recovery timing definition

## 11. Package outline



## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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