NTTFS6H850NL

Power MOSFET

80 V, 8.6 mΩ, 64 A, Single N−Channel

Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- These Devices are Pb−Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	80	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3, 4)	Steady State	T_C = 25°C	I_D	64	A
		T_C = 100°C		45	
Power Dissipation $R_{\theta JC}$ (Notes 1, 2, 3)		T_C = 25°C	P_D	73	W
		T_C = 100°C		37	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3, 4)	Steady State	T_A = 25°C	I_D	14.8	A
		T_A = 100°C		10.4	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)		T_A = 25°C	P_D	3.9	W
		T_A = 100°C		1.9	
Pulsed Drain Current	T_C = 25°C, t_p = 10 µs		I_{DM}	308	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	61	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 3.4 A)			E_{AS}	208	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Note 3)	$R_{\theta JC}$	2.0	°C/W
Junction−to−Ambient − Steady State (Note 3)	$R_{\theta JA}$	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51−12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

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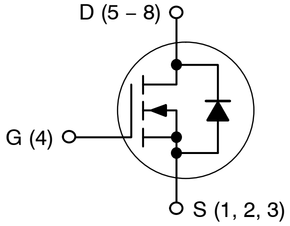
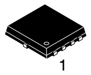
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
80 V	8.6 mΩ @ 10 V	64 A
	11 mΩ @ 4.5 V	

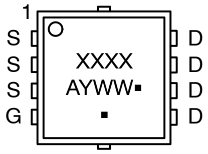
N−Channel





WDFN8
(µ8FL)
CASE 511AB

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		80			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				44.2		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 80 V	T_J = 25°C			10	μA
			T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 5)							
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A			7.1	8.6	mΩ
		V_{GS} = 4.5 V, I_D = 10 A			8.9	11	
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 70 μA		1.2	1.6	2.0	V
Gate Threshold Voltage Temperature Coefficient	$V_{GS(TH)}/T_J$				−5.2		mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 8 V, I_D = 10 A			64.1		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz V_{DS} = 40 V			1450		pF
Reverse Transfer Capacitance	C_{rss}				10		pF
Output Capacitance	C_{oss}				182		pF
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 40 V, I_D = 10 A			26		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 40 V, I_D = 10 A			13		
Gate−to−Source Charge	Q_{GS}				4.0		
Gate−to−Drain Charge	Q_{GD}				4.2		
SWITCHING CHARACTERISTICS (Note 6)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 4.5 V, V_{DS} = 64 V, I_D = 10 A, R_G = 2.5 mΩ			9		ns
Turn−Off Delay Time	$t_{d(off)}$				21		
Rise Time	t_r				26		
Fall Time	t_f				5		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 10 A	T_J = 25°C		0.8	1.2	V
			T_J = 125°C		0.7		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI/dt = 100 A/μs, I_S = 10 A			37		ns
Charge Time	t_a				22		
Discharge Time	t_b				15		
Reverse Recovery Charge	Q_{RR}				40		nC

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

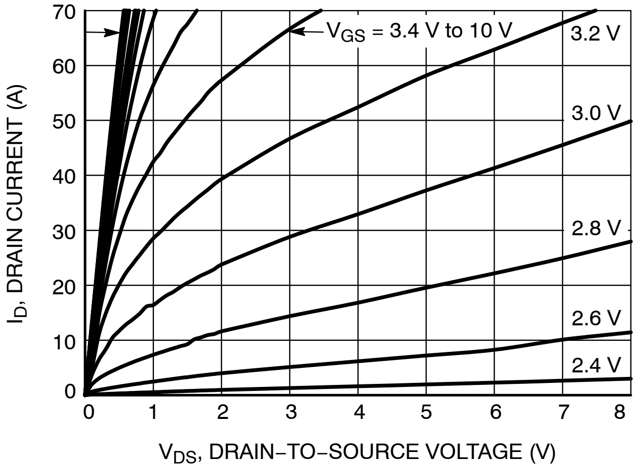


Figure 1. On−Region Characteristics

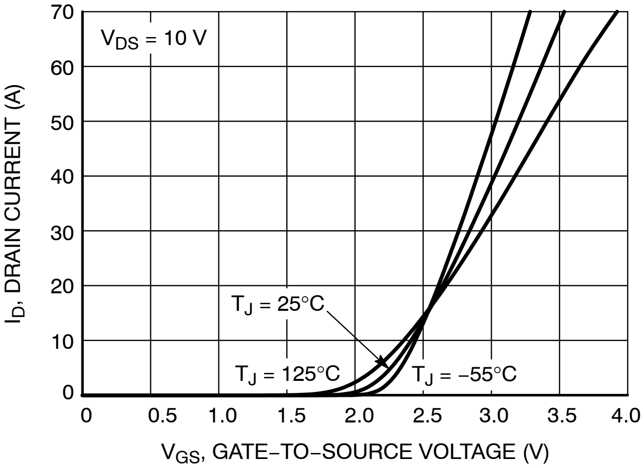


Figure 2. Transfer Characteristics

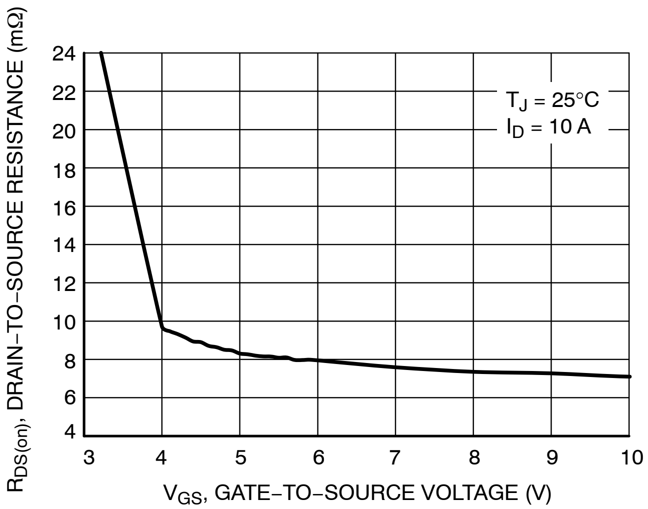


Figure 3. On−Resistance vs. Gate−to−Source Voltage

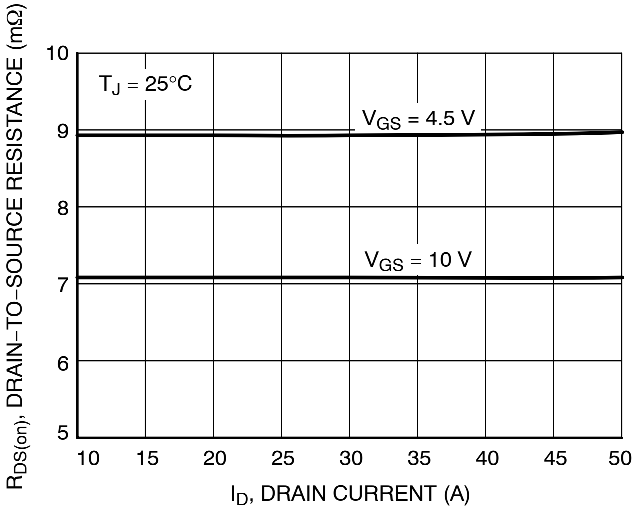


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

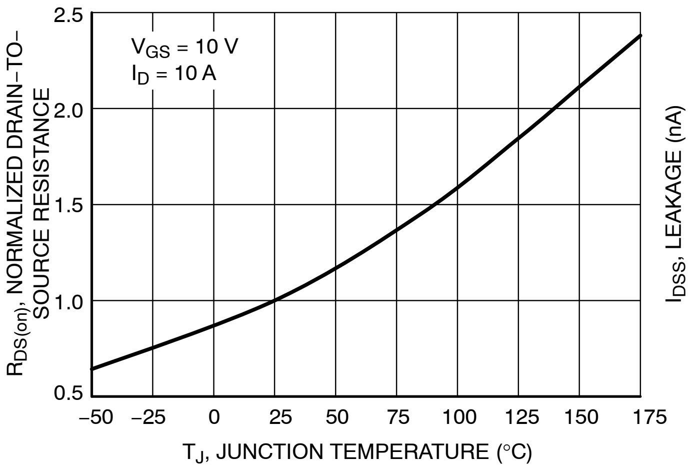


Figure 5. On−Resistance Variation with Temperature

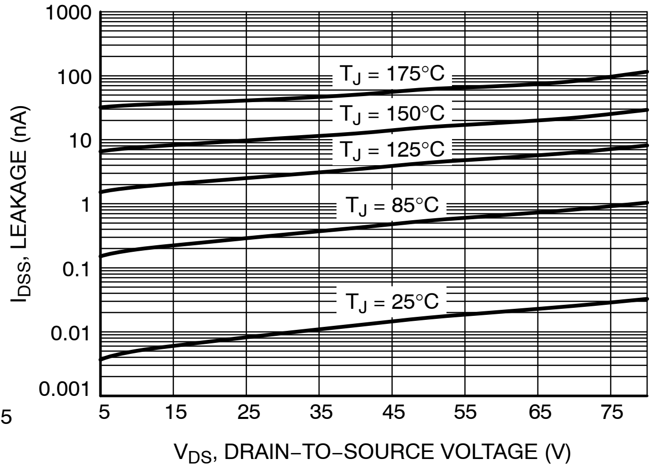


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

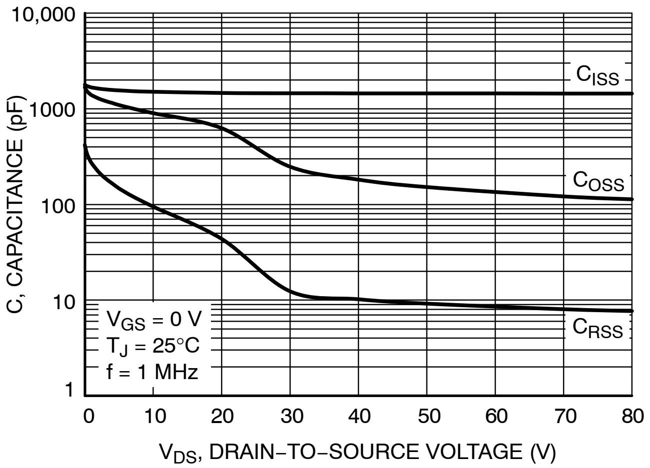


Figure 7. Capacitance Variation

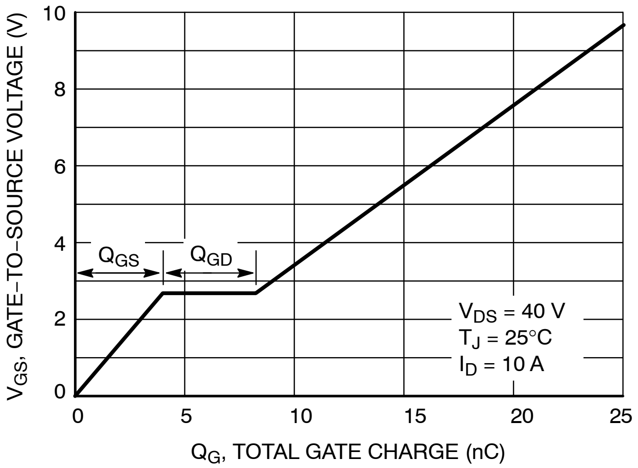


Figure 8. Gate−to−Source vs. Total Charge

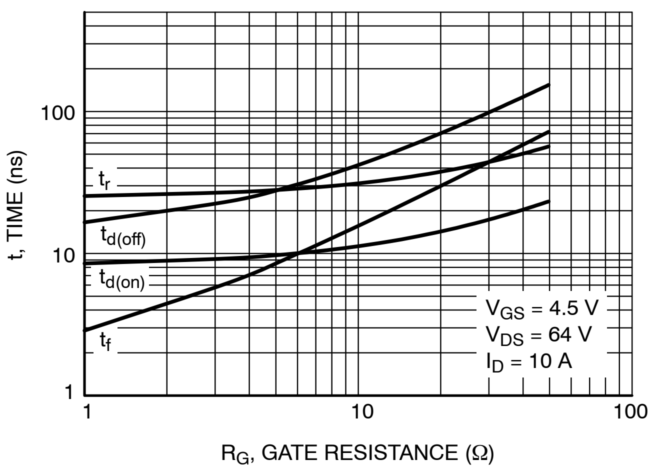


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

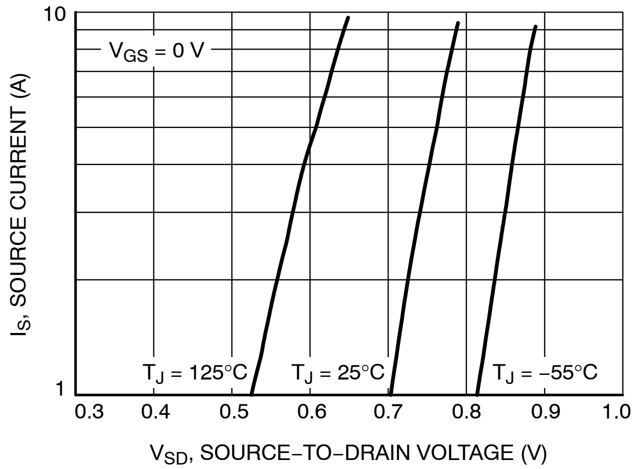


Figure 10. Diode Forward Voltage vs. Current

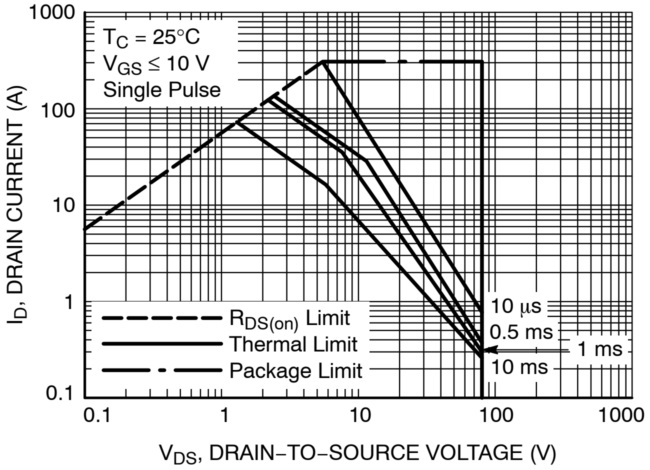


Figure 11. Maximum Rated Forward Biased Safe Operating Area

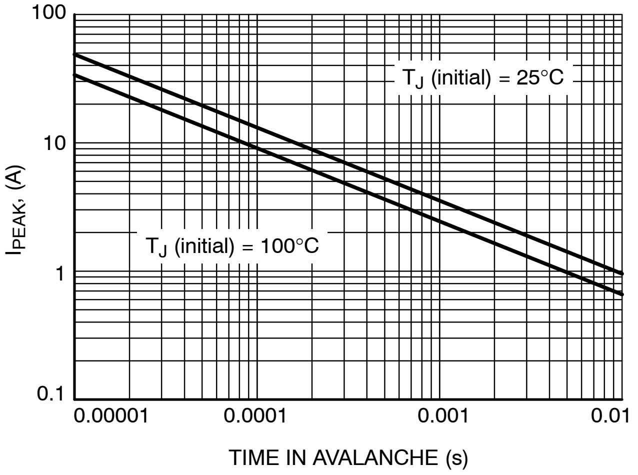


Figure 12. Maximum Drain Curent vs. Time in Avalanche

TYPICAL CHARACTERISTICS

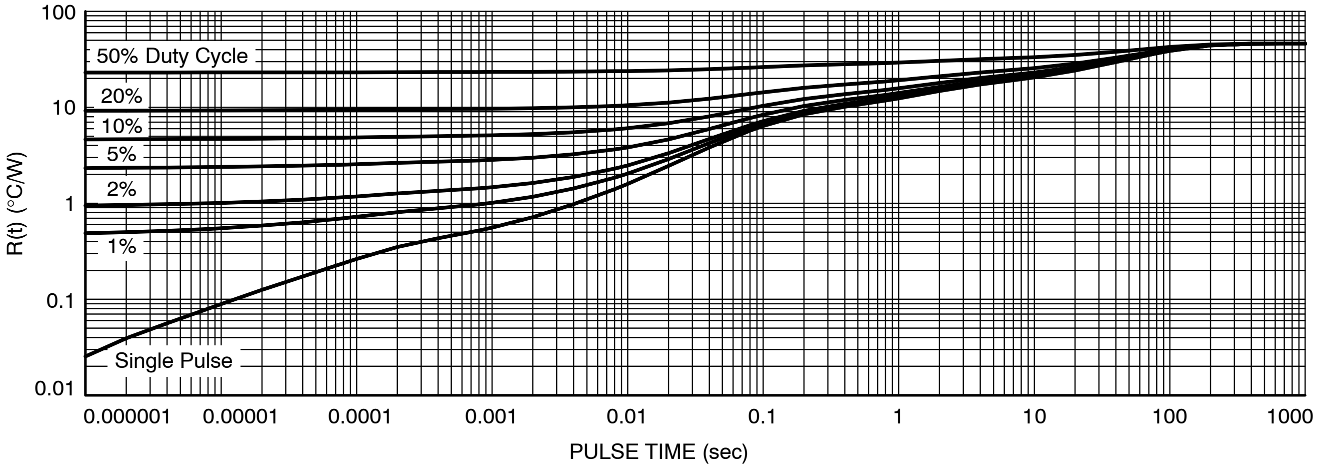


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

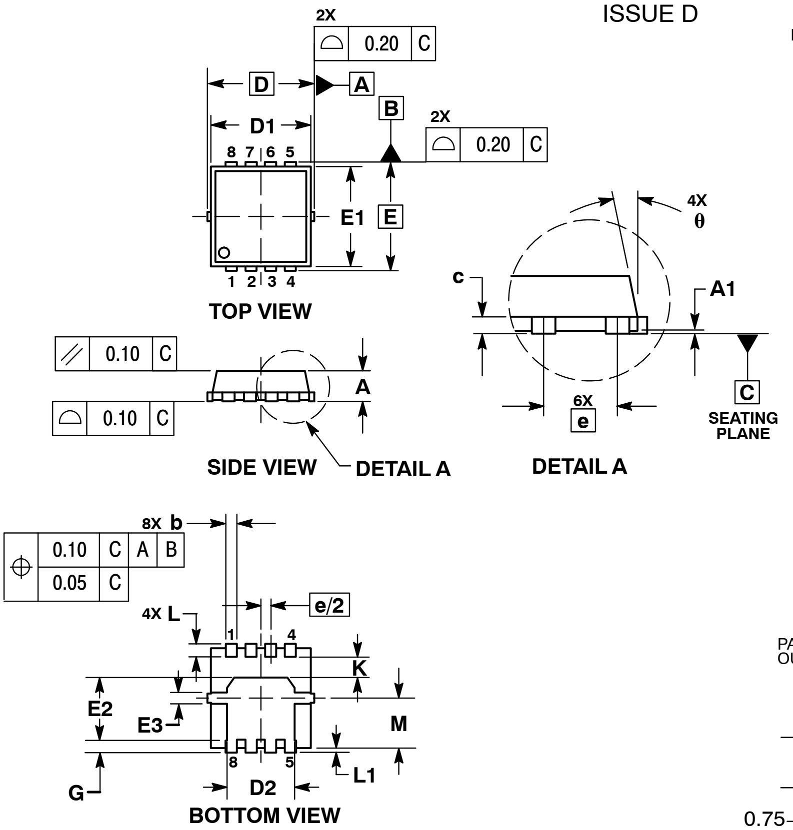
Device	Marking	Package	Shipping†
NTTFS6H850NLTAG	850L	WDFN8 (Pb−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

WDFN8 3.3x3.3, 0.65P

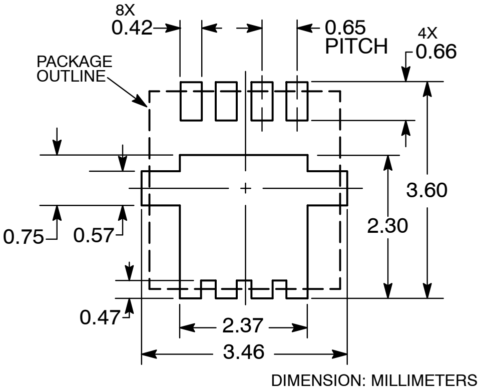
CASE 511AB
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °	---	12 °	0 °	---	12 °

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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