



16-Mbit (2M words × 8 bit) Static RAM with Error-Correcting Code (ECC)

Features

- High speed□ t_{AA} = 10 ns
- Embedded error-correcting code (ECC) for single-bit error correction
- Low active and standby currents
 □ I_{CC} = 90 mA typical at 100 MHz
 □ I_{SB2} = 20 mA typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- ERR pin to indicate 1-bit error detection and correction
- Available in Pb-free 54-pin TSOP II, and 48-ball VFBGA packages

Functional Description

The CY7C1069G and CY7C1069GE are dual chip enable high-performance CMOS fast static RAM devices with embedded ECC. The CY7C1069G device is available in standard pin configurations. The CY7C1069GE device includes a single bit error indication pin (ERR) that signals the host

processor in the case of an ECC error-detection and correction event.

To write to the device, take Chip Enables ($\overline{\text{CE}}_1$ LOW and CE₂ HIGH) and Write Enable ($\overline{\text{WE}}$) input LOW. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₂₀).

To read from the device, take <u>Chip Enables</u> (\overline{CE}_1 LOW and \overline{CE}_2 HIGH) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins. See Truth Table – CY7C1069G/CY7C1069GE on page 14 for a complete description of Read and Write modes. The input and output pins (I/O₀ through I/O₇) are placed in a high impedance state when the device is <u>de</u>selected (\overline{CE}_1 HIGH or \overline{CE}_2 LOW), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE}_1 LOW, \overline{CE}_2 HIGH, and \overline{WE} LOW).

On CY7C1069GE devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = High) ^[1].

All I/Os (I/O₀ through I/O₇) are placed in a high impedance state when the device is deselected ($\overline{\text{CE}}_1$ HIGH or $\overline{\text{CE}}_2$ LOW), and control signals are de-asserted ($\overline{\text{CE}}_1$ / $\overline{\text{CE}}_2$, $\overline{\text{OE}}$, WE). CY7C1069G and CY7C1069GE devices are available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout, and in a 48-ball VFBGA package.

For a complete list of related documentation, here.

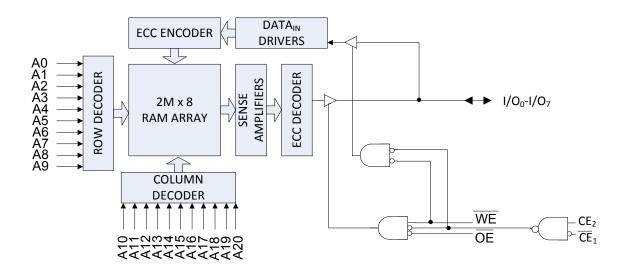
Note

Revised December 5, 2017

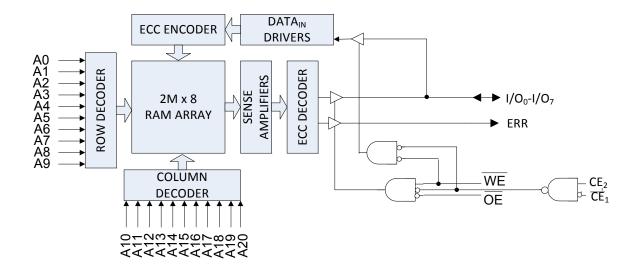
^{1.} Automatic write back on error detection feature is not supported in this device.



Logic Block Diagram - CY7C1069G



Logic Block Diagram - CY7C1069GE





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Pin Configurations

Figure 1. 54-pin TSOP II pinout (Top View) - CY7C1069G [2]

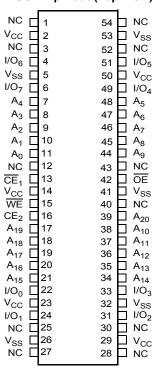
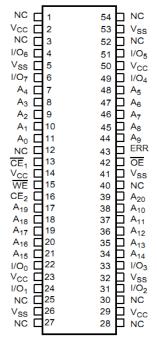


Figure 2. 54-pin TSOP II pinout (Top View) – CY7C1069GE [2, 3]



Note

- 2. NC pins are not connected on the die.
- 3. ERR is an Output pin. If not used, this pin should be left floating.



Pin Configurations (continued)

Figure 3. 48-ball VFBGA pinout (Top View) – CY7C1069G [4]

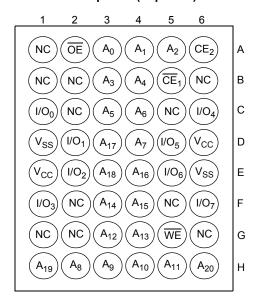
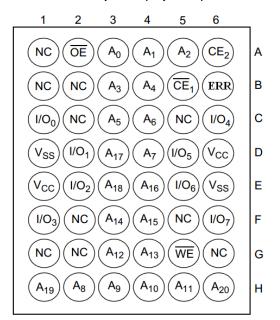


Figure 4. 48-ball VFBGA pinout (Top View) – CY7C1069GE [4, 5]



Note

- 4. NC pins are not connected on the die.5. ERR is an Output pin. If not used, this pin should be left floating.



Product Portfolio

					Power Dissipation				
Product	Features and Options (see the Pin	Pango	V Bango (V)	Speed			Standby, Icpa (mA)		
Product	Configurations section)	Range	V _{CC} Range (V)	(ns)					
					Typ ^[6]	Max	Typ ^[6]	Max	
CY7C1069G18	Dual-chip enable	Industrial	1.65 V-2.2 V	15	70	80	20	30	
CY7C1069G30			2.2 V-3.6 V	10	90	110			
CY7C1069G			4.5 V–5.5 V	10	90	110			
CY7C1069GE18	Dual-chip enable and ERR		1.65 V-2.2 V	15	70	80			
CY7C1069GE30	output		2.2 V-3.6 V	10	90	110			
CY7C1069GE			4.5 V–5.5 V	10	90	110			

^{6.} Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.



Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested. Storage temperature-65 °C to +150 °C Ambient temperature with power applied -55 °C to +125 °C Supply voltage on V_{CC} relative to GND-0.5 V to +6.0 V DC voltage applied to outputs in High Z State $^{[7]}$ –0.5 V to V $_{\rm CC}$ + 0.5 V

DC input voltage [7]	.–0.5 V to V _{CC} + 0.5 V
Current into outputs (LOW)	20 mA
Static Discharge Voltage (MIL-STD-883, Method 3015)	>2001 V
Latch up current	> 140 mA

Operating Range

Grade	Ambient Temperature	V _{CC}
Industrial	–40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the Operating Range of -40 °C to 85 °C

Doromotor	Description		Test Canditions	10	Unit		
Parameter	Desc	ription	Test Conditions	Min	Typ ^[8]	Max	Unit
V _{OH}	Output HIGH	1.65 V to 2.2 V	V _{CC} = Min, I _{OH} = -0.1 mA	1.4	_	_	V
	voltage	2.2 V to 2.7 V	V _{CC} = Min, I _{OH} = -1.0 mA	2.0	-	-	
		2.7 V to 3.0 V	V _{CC} = Min, I _{OH} = -4.0 mA	2.2	-	-	
		3.0 V to 3.6 V	V _{CC} = Min, I _{OH} = -4.0 mA	2.4	_	_	
		4.5 V to 5.5 V	V _{CC} = Min, I _{OH} = -4.0 mA	2.4	_	_	
		4.5 V to 5.5 V	V _{CC} = Min, I _{OH} = -0.1 mA	V _{CC} – 0.4 ^[9]	_	_	
V _{OL}	Output LOW	1.65 V to 2.2 V	V _{CC} = Min, I _{OL} = 0.1 mA	_	_	0.2	V
	voltage	2.2 V to 2.7 V	V _{CC} = Min, I _{OL} = 2 mA	_	_	0.4	
		2.7 V to 3.6 V	V _{CC} = Min, I _{OL} = 8 mA	_	_	0.4	
		4.5 V to 5.5 V	V _{CC} = Min, I _{OL} = 8 mA	_	_	0.4	
V _{IH}	Input HIGH voltage	1.65 V to 2.2 V	-	1.4	_	V _{CC} + 0.2	V
		2.2 V to 2.7 V	-	2.0	_	V _{CC} + 0.3	
		2.7 V to 3.6 V	_	2.0	_	V _{CC} + 0.3	
		4.5 V to 5.5 V	-	2.0	_	V _{CC} + 0.5	
V _{IL}	Input LOW	1.65 V to 2.2 V	-	-0.2	_	0.4	V
	voltage [7]	2.2 V to 2.7 V	_	-0.3	-	0.6	
		2.7 V to 3.6 V	-	-0.3	_	0.8	
		4.5 V to 5.5 V	_	-0.5	-	0.8	
I _{IX}	Input leakage c	urrent	$GND \le V_{IN} \le V_{CC}$	-1.0	-	+1.0	μΑ
I _{OZ}	Output leakage current		$GND \le V_{OUT} \le V_{CC}$, Output disabled	-1.0	_	+1.0	μА
I _{CC}	Operating supp	ly current	V _{CC} = Max, I _{OUT} = 0 mA, f = 100 MHz CMOS levels	_	90.0	110.0	mA
			CMOS levels f = 66.7 MHz	_	70.0	80.0	
I _{SB1}	Automatic CE power down current – TTL inputs		$\begin{aligned} &\text{Max V}_{\text{CC}}, \overline{\text{CE}} \geq \text{V}_{\text{IH}}^{[10]}, \\ &\text{V}_{\text{IN}} \geq \text{V}_{\text{IH}} \text{ or V}_{\text{IN}} \leq \text{V}_{\text{IL}}, \text{ f = f}_{\text{MAX}} \end{aligned}$	_	-	40.0	mA
I _{SB2}	Automatic CE p current – CMOS	oower down S inputs	$\begin{aligned} &\text{Max V}_{\text{CC}}, \overline{\text{CE}} \geq \text{V}_{\text{CC}} - 0.2 \text{ V}^{[10]}, \\ &\text{V}_{\text{IN}} \geq \text{V}_{\text{CC}} - 0.2 \text{ V or V}_{\text{IN}} \leq 0.2 \text{ V, f} = 0 \end{aligned}$	-	20.0 [8]	30.0	mA

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^{7.} V_{IL(min)} = -2.0 V and V_{IH(max)} = V_{CC} + 2 V for pulse durations of less than 20 ns.

8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

9. This parameter is guaranteed by design and is not tested.

10. <u>For</u> all dual chip enable devices, CE is the logical combination of CE and C



Capacitance

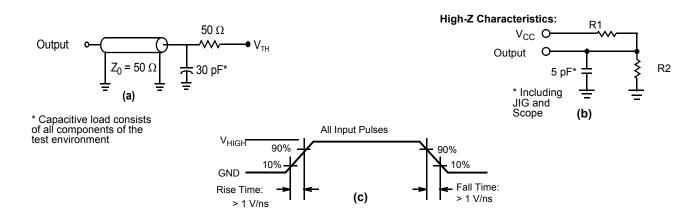
Parameter [11]	Description	iption Test Conditions		48-ball VFBGA	Unit
C _{IN}	Input capacitance	$T_A = 25 ^{\circ}\text{C}, f = 1 \text{MHz}, V_{CC} = V_{CC(typ)}$	10	10	pF
C _{OUT}	I/O capacitance		10	10	pF

Thermal Resistance

Parameter [11]	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	Unit
Θ_{JA}		Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	93.63	31.50	°C/W
$\Theta_{\sf JC}$	Thermal resistance (junction to case)		21.58	15.75	°C/W

AC Test Loads and Waveforms

Figure 5. AC Test Loads and Waveforms [12]



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V_{TH}	0.9	1.5	1.5	V
V _{HIGH}	1.8	3	3	V

^{11.} Tested initially and after any design or process changes that may affect these parameters.

^{12.} Full device AC operation assumes a 100- μ s ramp time from 0 to V_{CC} (min) and 100- μ s wait time after V_{CC} stabilization.



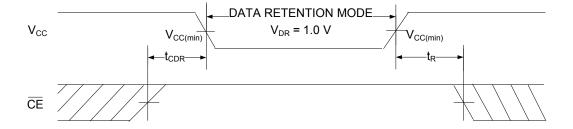
Data Retention Characteristics

Over the Operating Range of -40 °C to 85 °C

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V _{CC} for data retention	-	1.0	-	V
I _{CCDR}	Data retention current	$V_{CC} = V_{DR}, \overline{CE} \ge V_{CC} - 0.2 \text{ V}^{[13]}, \ V_{IN} \ge V_{CC} - 0.2 \text{ V or } V_{IN} \le 0.2 \text{ V}$	_	30.0	mA
t _{CDR} ^[14]	Chip deselect to data retention time	-	0	-	ns
t _R ^[14, 15]	Operation recovery time	V _{CC} ≥ 2.2 V	10.0	ı	ns
		V _{CC} < 2.2 V	15.0	-	ns

Data Retention Waveform

Figure 6. Data Retention Waveform [13]



^{13.} For all dual chip enable devices, CE is the logical combination of CE₁ and CE₂. When CE₁ is LOW and CE₂ is HIGH, CE is LOW; when CE₁ is HIGH or CE₂ is LOW, CE is HIGH.

 ^{14.} This parameter is guaranteed by design and is not tested.
 15. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min.)} ≥ 100 μs or stable at V_{CC(min.)} ≥ 100 μs.



AC Switching Characteristics

Over the Operating Range of -40 °C to 85 °C

Parameter [16]	Description	10	ns	15 ns		
Parameter	Description	Min		Min	Max	Unit
Read Cycle				1		
t _{POWER}	V _{CC} stable to first access ^[17, 18]	100.0	_	100.0	_	μS
t _{RC}	Read cycle time	10.0	_	15.0	_	ns
t _{AA}	Address to data / ERR valid	_	10.0	_	15.0	ns
t _{OHA}	Data / ERR hold from address change	3.0	_	3.0	-	ns
t _{ACE}	CE LOW to data / ERR valid [19]	_	10.0	_	15.0	ns
t _{DOE}	OE LOW to data / ERR valid	_	5.0	_	8.0	ns
t _{LZOE}	OE LOW to low Z [20, 21, 22]	0	_	1.0	_	ns
t _{HZOE}	OE HIGH to high Z [20, 21, 22]	_	5.0	_	8.0	ns
t _{LZCE}	CE LOW to low Z [19, 20, 21, 22]	3.0	_	3.0	_	ns
t _{HZCE}	CE HIGH to high Z [19, 20, 21, 22]	_	5.0	_	8.0	ns
t _{PU}	CE LOW to power-up [18, 19]	0	_	0	_	ns
t _{PD}	CE HIGH to power-down [18, 19]	-	10.0	_	15.0	ns
Write Cycle [2	3, 24]					
t _{WC}	Write cycle time	10.0	_	15.0	_	ns
t _{SCE}	CE LOW to write end [19]	7.0	_	12.0	_	ns
t _{AW}	Address setup to write end	7.0	_	12.0	-	ns
t _{HA}	Address hold from write end	0	_	0	-	ns
t _{SA}	Address setup to write start	0	_	0	-	ns
t _{PWE}	WE pulse width	7.0	_	12.0	-	ns
t _{SD}	Data setup to write end	5.0	-	8.0	_	ns
t _{HD}	Data hold from write end	0	_	0	-	ns
t _{LZWE}	WE HIGH to low Z [20, 21, 22]	3.0	_	3.0	_	ns
t _{HZWE}	WE LOW to high Z [20, 21, 22]	_	5.0	_	8.0	ns

- 16. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for V_{CC} ≥ 3 V) and V_{CC}/2 (for V_{CC} < 3 V), and input pulse levels of 0 to 3 V (for V_{CC} ≥ 3 V) and 0 to V_{CC} (for V_{CC} < 3V). Test conditions for the read cycle use output loading shown in part (a) of Figure 5 on page 8, unless specified otherwise.
- $17.\,t_{POWER}\,\text{gives minimum amount of time that the power supply is at stable}\,\,V_{CC}\,\,\text{until first memory access is performed}.$
- 18. These parameters are guaranteed by design and are not tested.
- 19. For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
- 20. t_{HZOE}, t_{HZOE}, t_{HZOE}, t_{LZOE}, t_{LZOE}, are specified with a load capacitance of 5 pF as in (b) of Figure 5 on page 8. Transition is measured ±200 mV from steady state voltage.
- 21. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZOE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
- 22. Tested initially and after any design or process changes that may affect these parameters.
- 23. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{\parallel}$, $\overline{CE} = V_{\parallel}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 24. The minimum write pulse width for write cycle No.2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) should be sum of t_{HZWE} and t_{SD} .



Switching Waveforms

Figure 7. Read Cycle No. 1 of CY7C1069G (Address Transition Controlled) $^{[25,\,26]}$

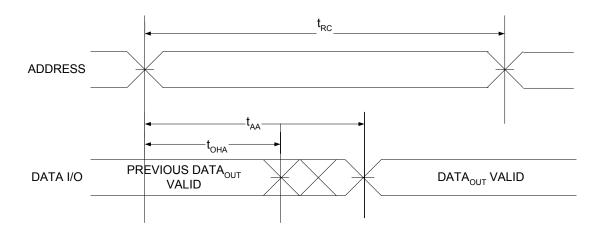
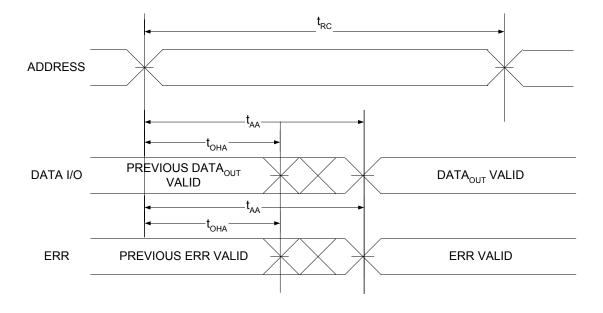


Figure 8. Read Cycle No. 2 of CY7C1069GE (Address Transition Controlled) $^{[25,\ 26]}$

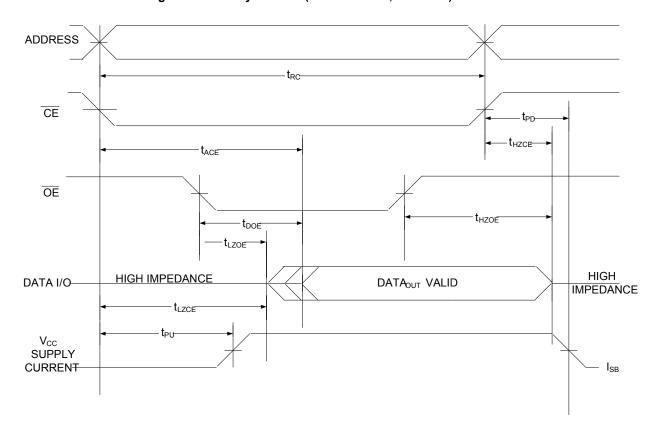


^{25.} The device is continuously selected, \overline{OE} = V_{IL} , \overline{CE} = V_{IL} . 26. \overline{WE} is HIGH for read cycle.



Switching Waveforms (continued)

Figure 9. Read Cycle No. 3 (OE Controlled, WE HIGH) [27, 28, 29]



^{27.} $\underline{\text{For}}$ all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$. When $\overline{\text{CE}}_1$ is LOW and $\overline{\text{CE}}_2$ is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or $\overline{\text{CE}}_2$ is LOW, $\overline{\text{CE}}$ is HIGH.

^{28.} $\overline{\text{WE}}$ is HIGH for read cycle.

^{29.} Address valid prior to or coincident with $\overline{\text{CE}}$ LOW transition.



Switching Waveforms (continued)

Figure 10. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) $^{[30,\ 31,\ 32]}$

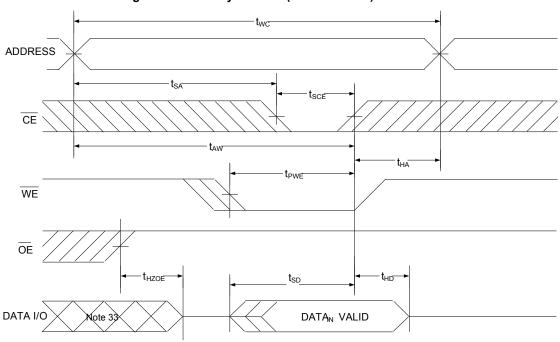
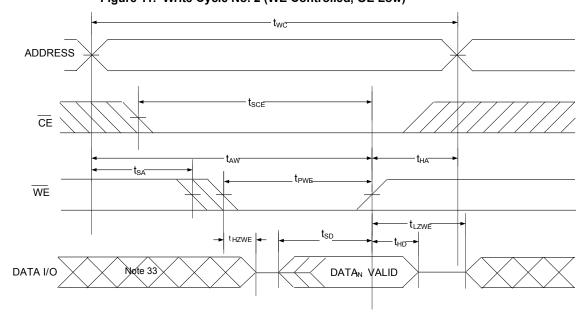


Figure 11. Write Cycle No. 2 (WE Controlled, $\overline{\text{OE}}$ Low) $^{[30,\ 31,\ 32,\ 34]}$



- 30. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$. When $\overline{\text{CE}}_1$ is LOW and $\overline{\text{CE}}_2$ is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or $\overline{\text{CE}}_2$ is LOW, $\overline{\text{CE}}$ is HIGH.
- 31. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{\parallel}$, $\overline{CE} = V_{\parallel}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 32. Data I/O is in high impedance state if $\overline{\text{CE}} = \text{V}_{\text{IH}}$, or $\overline{\text{OE}} = \text{V}_{\text{IH}}$. 33. During this time I/O are in output put state. Do not apply input signals.
- 34. The minimum write cycle width should be sum of t_{HZWE} and t_{SD} ,



Truth Table - CY7C1069G/CY7C1069GE

CE ₁	CE ₂	OE	WE	I/O ₀ -I/O ₇	Mode	Power
Н	X ^[35]	X ^[35]	X ^[35]	High Z	Power-down	Standby (I _{SB})
X ^[35]	L	X ^[35]	X ^[35]	High Z	Power-down	Standby (I _{SB})
L	Н	L	Н	Data out	Read all bits	Active (I _{CC})
L	Н	X ^[35]	L	Data in	Write all bits	Active (I _{CC})
L	Н	Н	Н	High Z	Selected, outputs disabled	Active (I _{CC})

ERR Output - CY7C1069GE

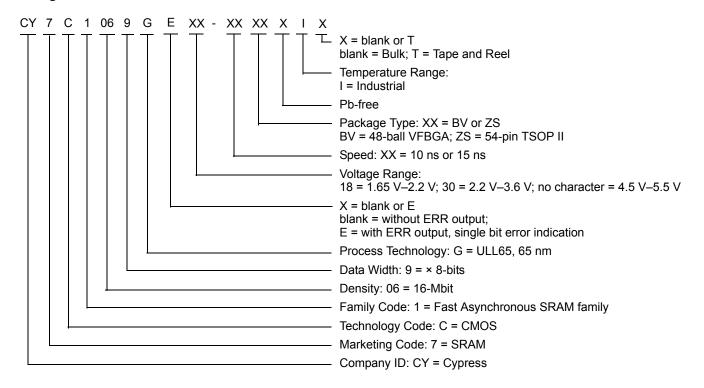
Output [36]	Mode	
0	Read Operation, no single bit error in the stored data.	
1	1 Read Operation, single bit error detected and corrected.	
High Z Device deselected or Outputs disabled or Write Operation		



Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (All Pb-free)	ERR Pin / Ball	Operating Range
10	2.2 V-3.6 V	CY7C1069G30-10BVXI	51-85150	48-ball VFBGA	No	Industrial
		CY7C1069G30-10BVXIT	51-85150	48-ball VFBGA, Tape and Reel	No	
	CY7C1069G30-10ZSXI	51-85160	54-pin TSOP II	No		
		CY7C1069G30-10ZSXIT	51-85160	54-pin TSOP II, Tape and Reel	No	
		CY7C1069GE30-10ZSXI	51-85160	54-pin TSOP II	Yes	
		CY7C1069GE30-10ZSXIT	51-85160	54-pin TSOP II, Tape and Reel	Yes	
	4.5 V–5.5 V	CY7C1069G-10BVXI	51-85150	48-ball VFBGA	No	
		CY7C1069G-10BVXIT	51-85150	48-ball VFBGA, Tape and Reel	No	
		CY7C1069G-10ZSXI	51-85160	54-pin TSOP II	No	
		CY7C1069G-10ZSXIT	51-85160	54-pin TSOP II, Tape and Reel	No	

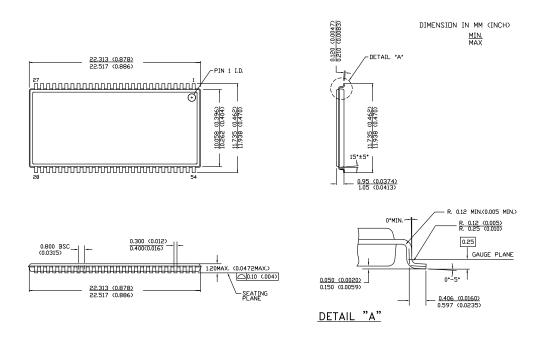
Ordering Code Definitions





Package Diagrams

Figure 12. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline, 51-85160

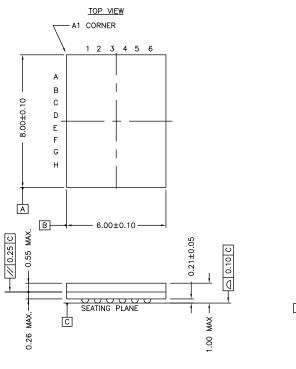


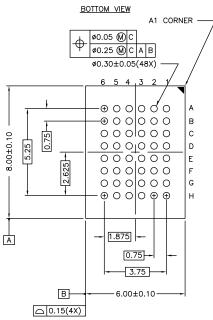
51-85160 *E



Package Diagrams (continued)

Figure 13. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150





NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)
posted on the Cypress web.

51-85150 *H



Acronyms

Acronym	Description		
CE	Chip Enable		
CMOS	Complementary Metal Oxide Semiconductor		
I/O	Input/Output		
ŌĒ	Output Enable		
SRAM	Static Random Access Memory		
TSOP	Thin Small Outline Package		
TTL	Transistor-Transistor Logic		
VFBGA	Very Fine-Pitch Ball Grid Array		
WE	Write Enable		

Document Conventions

Units of Measure

Symbol	Unit of Measure			
°C	degree Celsius			
MHz	megahertz			
μΑ	microampere			
μS	microsecond			
mA	milliampere			
mm	millimeter			
ns	nanosecond			
Ω	ohm			
%	percent			
pF	picofarad			
V	volt			
W	watt			



Document History Page

	Document Title: CY7C1069G/CY7C1069GE, 16-Mbit (2M words × 8 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-81539						
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change			
*H	4800609	NILE	07/31/2015	Changed status from Preliminary to Final.			
*1	5436514	NILE	09/14/2016	Updated Maximum Ratings: Updated Note 7 (Replaced "2 ns" with "20 ns"). Updated DC Electrical Characteristics: Removed Operating Range "2.7 V to 3.6 V" and all values corresponding to V _{OH} parameter. Included Operating Ranges "2.7 V to 3.0 V" and "3.0 V to 3.6 V" and all values corresponding to V _{OH} parameter. Changed minimum value of V _{IH} parameter from 2.2 V to 2 V corresponding to Operating Range "4.5 V to 5.5 V". Updated Ordering Information: Updated part numbers. Updated to new template.			
*J	5984763	AESATMP9	12/05/2017	Updated logo and copyright.			



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