VNQ500

Quad channel high-side driver

Features

Max supply voltage	V_{CC}	41V
Operating voltage range	V_{CC}	5.5 to 36V
Max on-state resistance	R_{ON}	500mΩ
Current limitation (typ)	I_{LIM}	0.4A
Off-state supply current	I_S	25 µA

- CMOS compatible I/O's
- Chip Enable
- Junction over temperature protection and diagnostic
- Current limitation
- Shorted load protection
- Undervoltage shutdown
- Protection against loss of ground
- Very low standby current
- In compliance with the 2002/95/EC european directive

PowerSSO-12

Description

The VNQ500 is a monolithic device designed in STMicroelectronics VIPower M0-3 technology, intended for driving any kind of load with one side connected to ground.

Active current limitation, combined with latched thermal shutdown, protect the device against overload.

In the case of over temperature of one channel the relative I/O pin is pulled down.

The device automatically turns off in the case of ground pin disconnection.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-12	VNQ500PEP-E	VNQ500PEPTR-E

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1 Block diagram and pin description

Figure 1. Block diagram

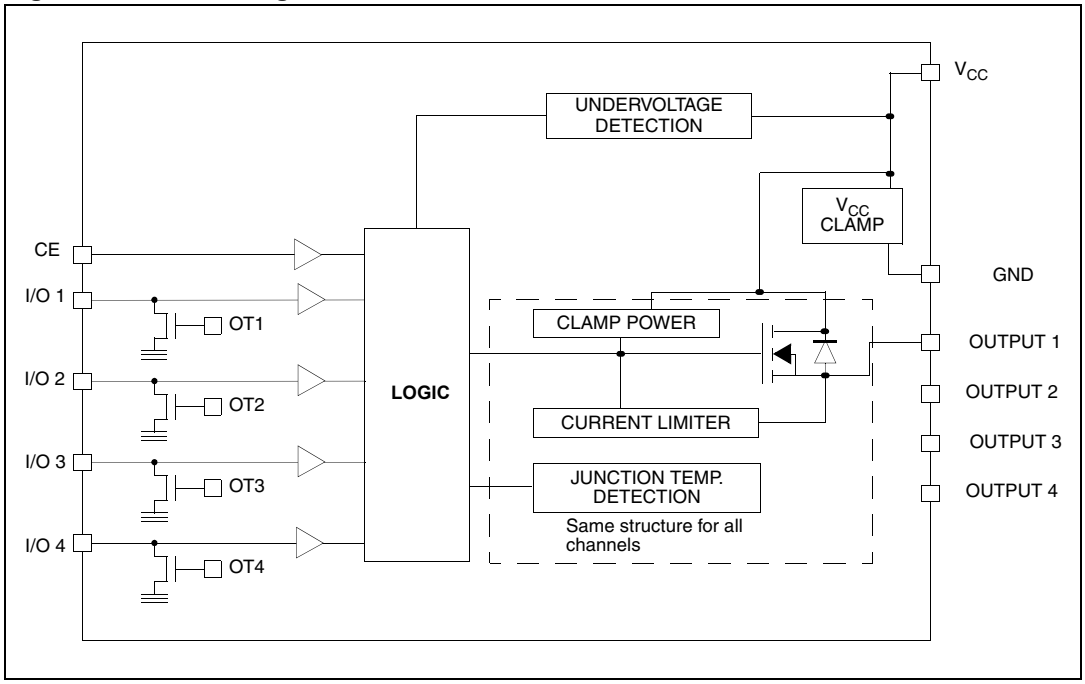
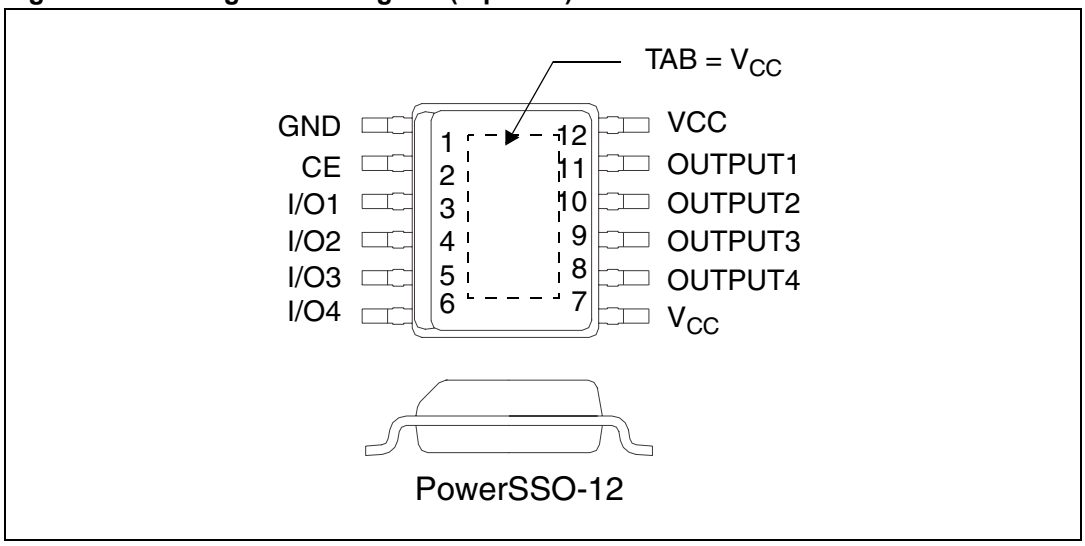


Table 2. Pin definitions and functions

Pin No	Symbol	Function
TAB	V_{CC}	Positive power supply voltage
7,12	V_{CC}	Positive power supply voltage
1	GND	Logic ground
2	CE	Chip Enable
3	I/O 1	Input/output of channel 1
4	I/O 2	Input/output of channel 2
5	I/O 3	Input/output of channel 3
6	I/O 4	Input/output of channel 4
8	OUTPUT 4	High-side output of channel 4
9	OUTPUT 3	High-side output of channel 3
10	OUTPUT 2	High-side output of channel 2
11	OUTPUT 1	High-side output of channel 1

Figure 2. Configuration diagram (top view)



2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse supply voltage	-0.3	V
$- I_{GND}$	DC ground pin reverse current	- 250	mA
I_{OUT}	DC output current	Internally limited	A
$- I_{OUT}$	Reverse DC output current	-1	A
I_{IN}	DC Input current	+/- 10	mA
V_{ESD}	Electrostatic discharge (R = 1.5KΩ; C = 100pF) - I/On - OUTn and V_{CC}	 4000 5000	 V V
P_{tot}	Power dissipation at T_c = 25°C	7.3	W
T_j	Junction operating temperature	Internally limited	°C
T_{stg}	Storage temperature	- 55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value		Unit
$R_{thj\text{-}case}$	PowerSSO-12 thermal resistance junction-case	17		°C/W
$R_{thj\text{-}amb}$	PowerSSO-12 thermal resistance junction-ambient	61(1)	50(2)	°C/W

1. When mounted on a standard single-sided FR-4 board with 0.5 cm^2 of Cu (at least 35mm thick) connected to all V_{CC} pins.
2. When mounted on a standard single-sided FR-4 board with 8 cm^2 of Cu (at least 35mm thick) connected to all V_{CC} pins.

2.3 Electrical characteristics

Values specified in this section are for 8V<V_{CC}<36V; -40°C< T_j <150°C, unless otherwise stated.

Figure 3. Current and voltage conventions

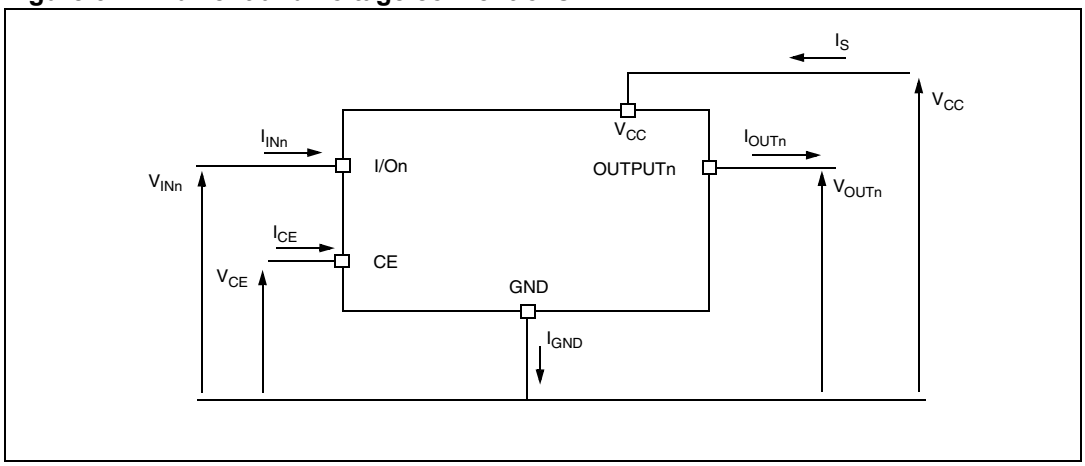


Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}(1)	Operating supply voltage		5.5	13	36	V
V_{USD}(1)	Undervoltage shutdown		3	4	5.5	V
V_{OV}(1)	Overvoltage shutdown		36			V
R_{ON}	On-state resistance	I_{OUTn} = 0.25A; T_j = 25°C I_{OUTn} = 0.25A			500 1000	mΩ mΩ
I_S	Supply current	Off-state; V_{CC} = 13V; V_{CE} = $V_{I/On}$ = 0V; V_{CE} = $V_{I/On}$ = 0V; V_{CC} = 13V; T_{case} = 25°C On-state (all channels ON); V_{CC} = 13V			25 20 8	µA µA mA
I_{LGND}(1)	Output current at turn-off	V_{CC} = V_{CE} = $V_{I/On}$ = V_{GND} = 13V; V_{OUTn} = 0V			1	mA
$I_{L(off1)}$(1)	Off-state output current	$V_{I/On}$ = V_{OUTn} = 0V	0		50	µA
$I_{L(off3)}$(1)	Off-state output current	$V_{I/On}$ = V_{OUTn} =0 V, V_{CC} = 13V; T_J = 125°C			5	µA
$I_{L(off4)}$(1)	Off-state output current	$V_{I/On}$ = V_{OUTn} = 0V, V_{CC} = 13V; T_J = 25°C			3	µA

1. Per channel.

Table 6. Switching (V_{CC} =13V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{on}	Turn-on time	R_L= 52Ω from 80% V_{OUT}(1)		50		µs
t_{off}	Turn-off time	R_L= 52Ω to 10% V_{OUT} (1)		75		µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L= 52Ω from V_{OUT} = 1.3V to V_{OUT} = 10.4V (1)		0.3		V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L= 52Ω from V_{OUT} = 11.7V to V_{OUT} = 1.3V (1)		0.3		V/µs

1. See *Figure 4: Switching time waveforms: turn-on and turn-off*.

Table 7. Input and CE pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{INL}	I/O low level				1.25	V
I_{INL}	Low level I/O current	V_{IN} = 1.25V	1			µA
V_{INH}	I/O high level		3.25			V
I_{INH}	High level I/O current	V_{IN} = 3.25V			10	µA
$V_{I(hyst)}$	I/O hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN} = 1mA I_{IN} = - 1mA	6	6.8 - 0.7	8	V V

Table 8. Protections and diagnostics(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	I/O low level default detection	I_{IN} = 1mA, latched thermal shutdown			0.5	V
T_{TSD}	Junction shutdown temperature		150	175	200	°C
I_{lim}	DC short circuit current	V_{CC} = 13V; R_{LOAD} = 10mΩ	0.4	0.6	0.9	A
V_{demag}	Turn-off output clamp voltage	I_{OUT} = 0.25 A; L = 50mH	V_{CC} - 41	V_{CC} - 48	V_{CC} - 55	V
t_{reset}	Thermal latch reset time	T_j < T_{TSD} (see third figure in *Figure 6: Waveforms*)			10	µs

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Figure 4. Switching time waveforms: turn-on and turn-off

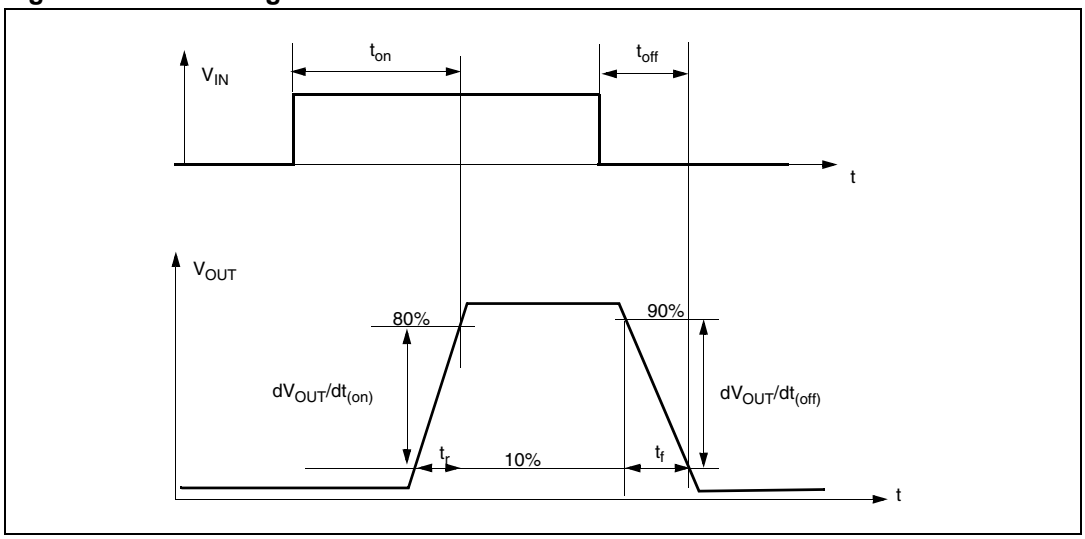
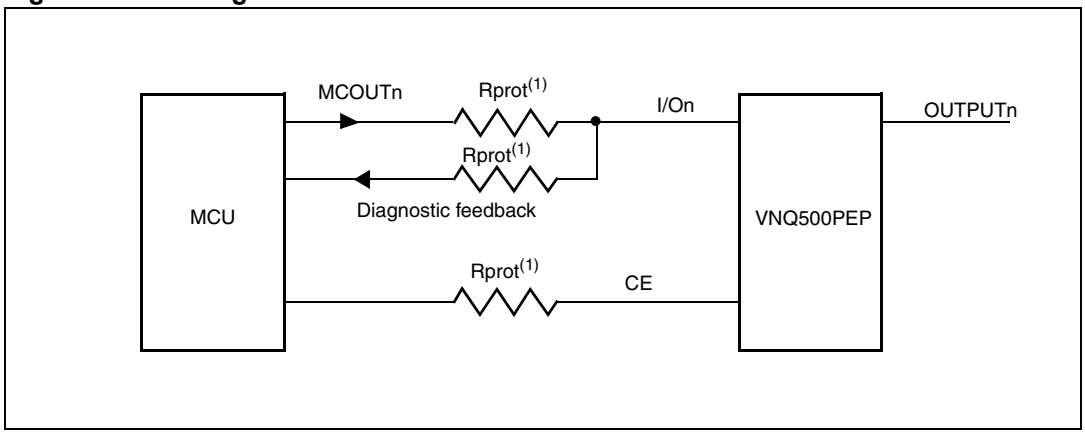


Figure 5. Driving circuit



1. See *Figure 19: Application schematic*.

Table 9. Truth table

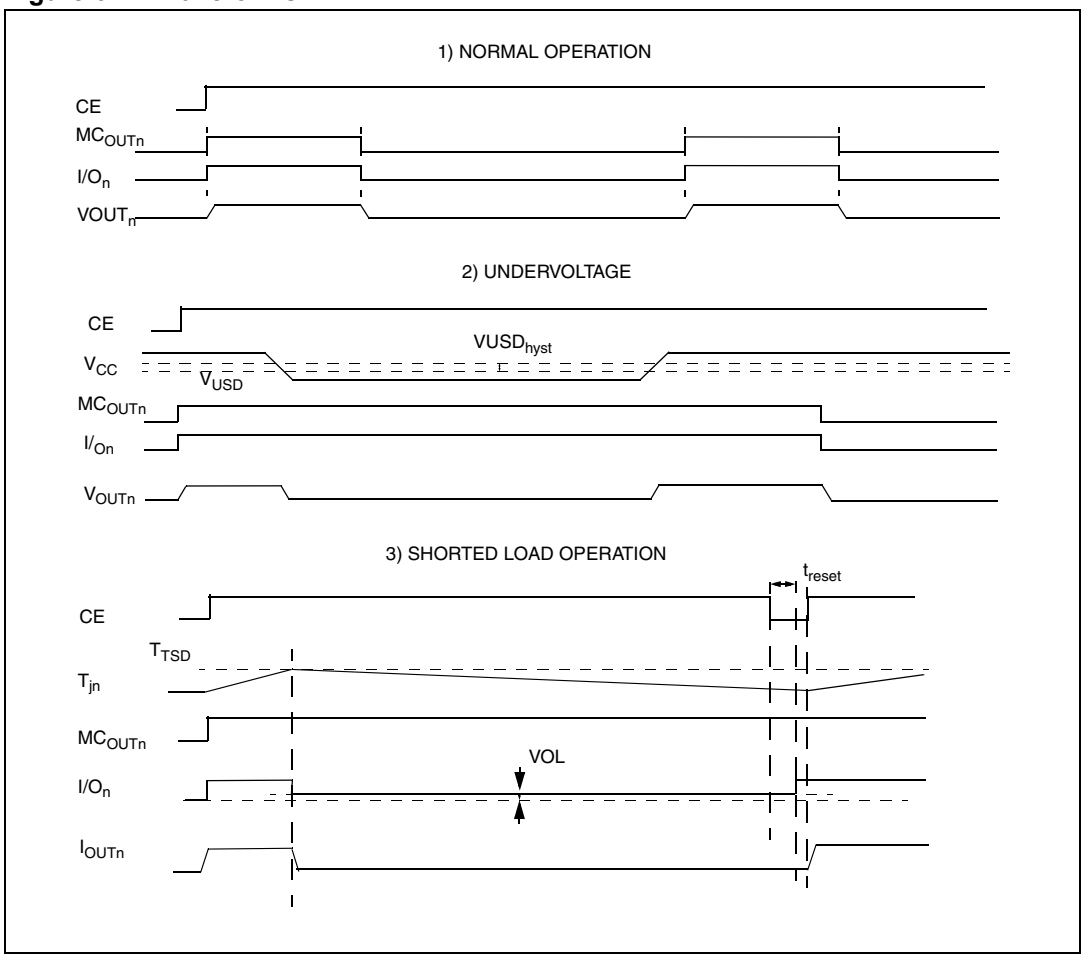
Conditions	MCOUTn	CE	I/On	Output_n
Normal operation	L H	H H	L H	L H
Current limitation	L H	H H	L H	L H
Over temperature	L H	H H	L L (latched)	L L
Undervoltage	L H	H H	L H	L L
Standby	X	L	X	L

Table 10. Electrical transient requirements on V_{CC} pin

ISO T/R 7637/1 Test pulse	Test level				
	I	II	III	IV	Delays and impedance
1	- 25V(1)	- 50V(1)	- 75V(1)	- 100V(1)	2ms, 10Ω
2	+ 25V(1)	+ 50V(1)	+ 75V(1)	+ 100V(1)	0.2ms, 10Ω
3a	- 25V(1)	- 50V(1)	- 100V(1)	- 150V(1)	0.1µs, 50Ω
3b	+ 25V(1)	+ 50V(1)	+ 75V(1)	+ 100V(1)	0.1µs, 50Ω
4	- 4V(1)	- 5V(1)	- 6V(1)	- 7V(1)	100ms, 0.01Ω
5	+ 26.5V(1)	+ 46.5V(2)	+ 66.5V(2)	+ 86.5V(2)	400ms, 2Ω

1. All functions of the device are performed as designed after exposure to disturbance.
2. One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off-state output current

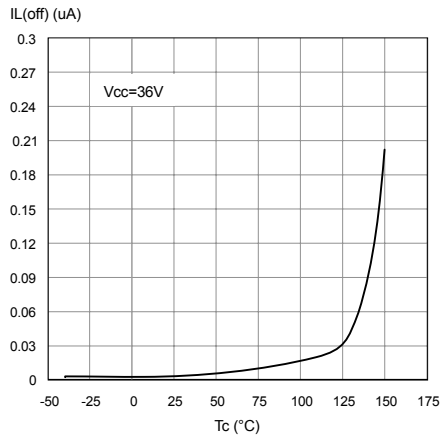


Figure 8. High level input current

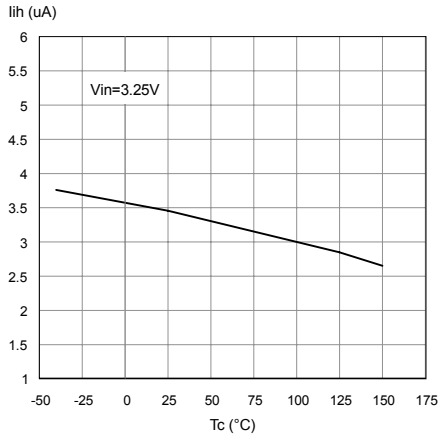


Figure 9. Input clamp voltage

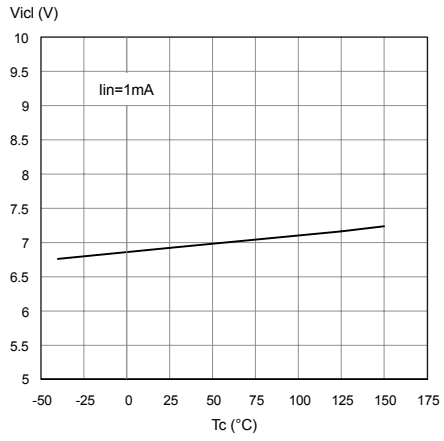


Figure 10. Turn-off voltage slope

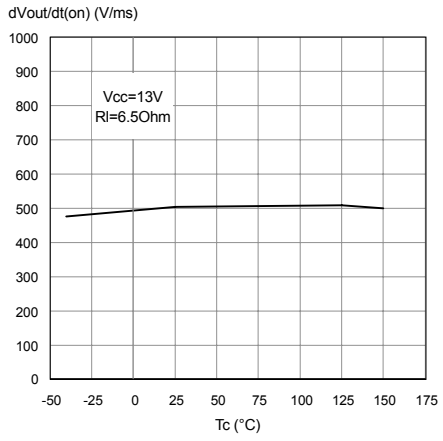


Figure 11. Overvoltage shutdown

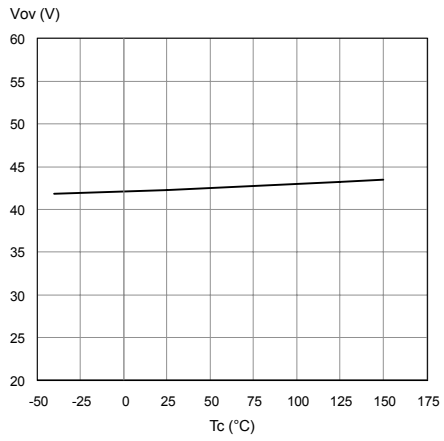


Figure 12. Turn-off voltage slope

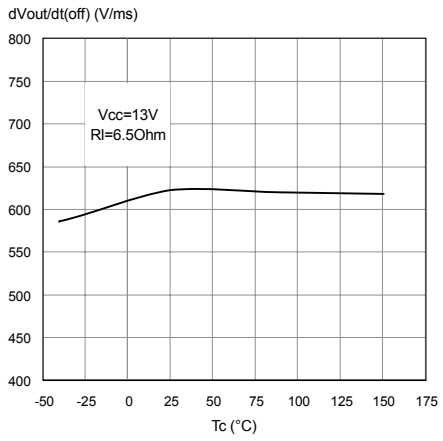


Figure 13. I_{LIM} vs T_{case}

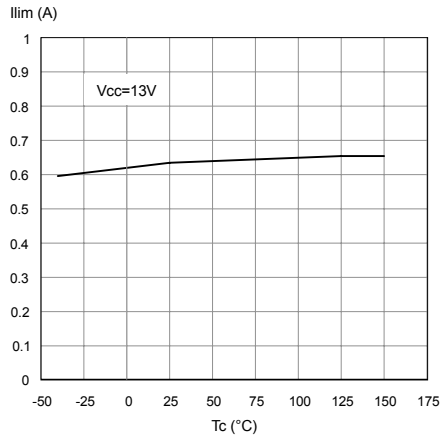


Figure 14. On-state resistance vs V_{CC}

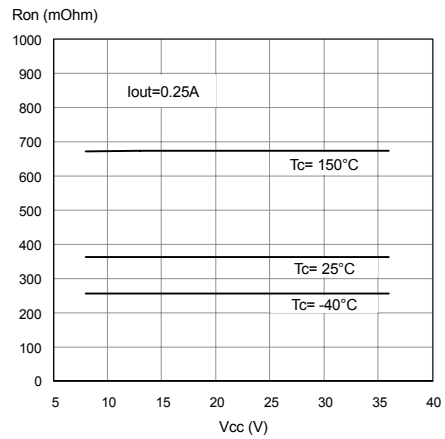


Figure 15. Input high level

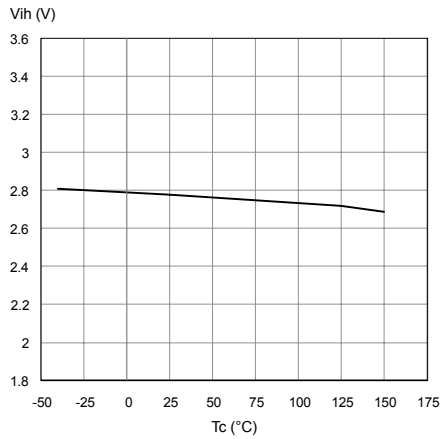


Figure 16. Input hysteresis voltage

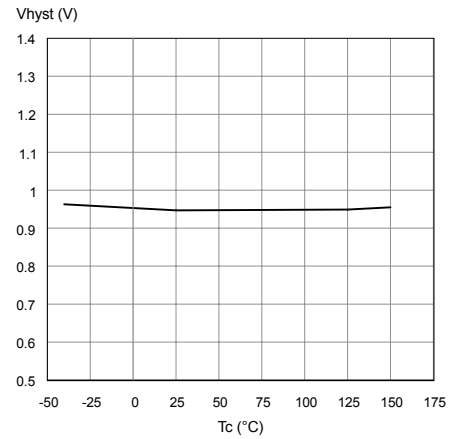


Figure 17. On-state resistance vs Tcase

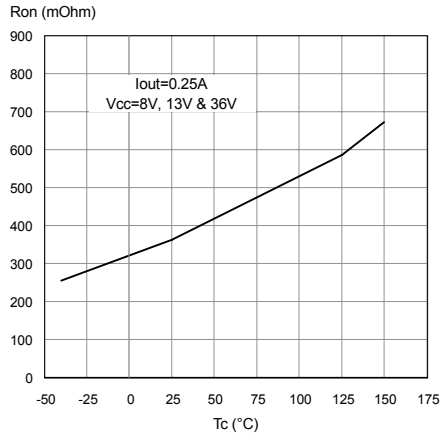
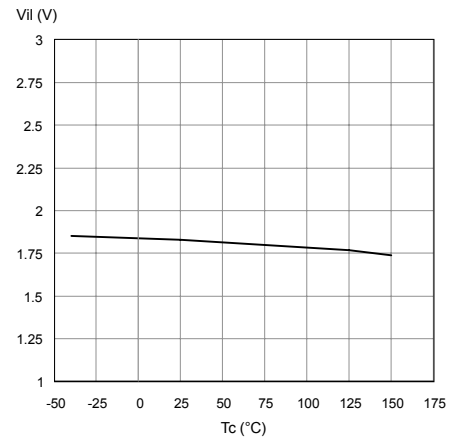
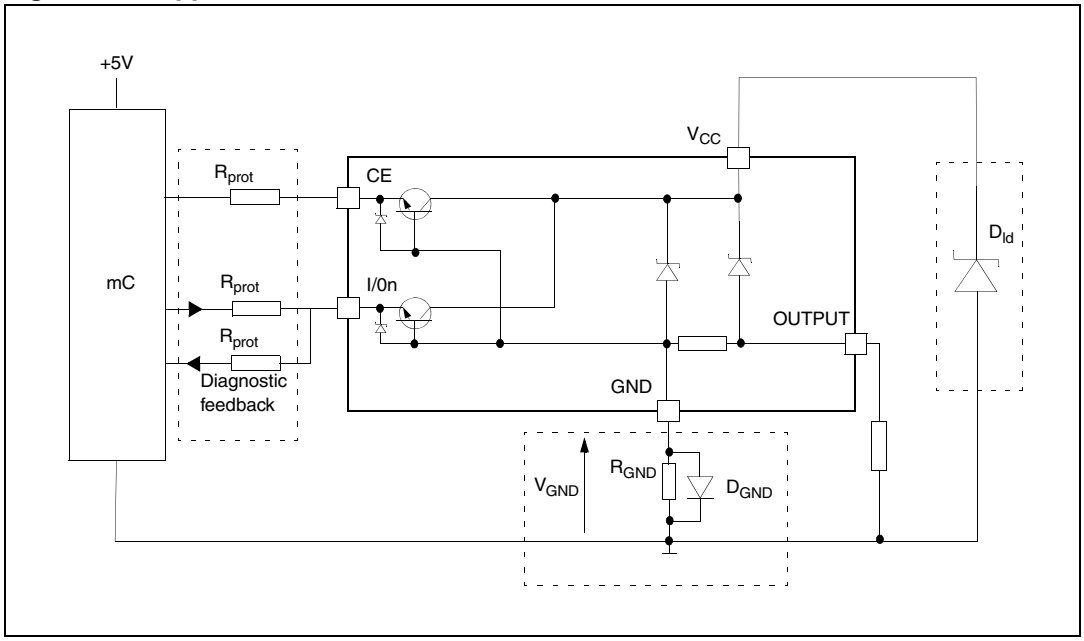


Figure 18. Input low level



3 Application information

Figure 19. Application schematic



3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

3.1.1 Solution 1: a resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following show how to dimension the R_{GND} resistor:

1. $R_{GND} \leq 600mV / (I_{S(on)max})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC}<0$ during reverse battery situations) is:

$$P_D= (-V_{CC})^2/R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that, if the microprocessor ground is not shared by the device ground, then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high-side drivers sharing the same R_{GND}.

If the calculated power dissipation requires the use of a large resistor, or several devices have to share the same resistor, then ST suggests using solution 2 below.

3.1.2 Solution 2: a diode (D_{GND}) in the ground line

Note that a resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift (≈600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} maximum DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than those shown in the ISO T/R 7637/1 table.

3.3 MCU I/O protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/O pins from latching up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os:

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$$

Example

For the following conditions:

V_{CCpeak}= - 100V

$I_{latchup} \geq$ 20mA

$V_{OH\mu C} \geq$ 4.5V

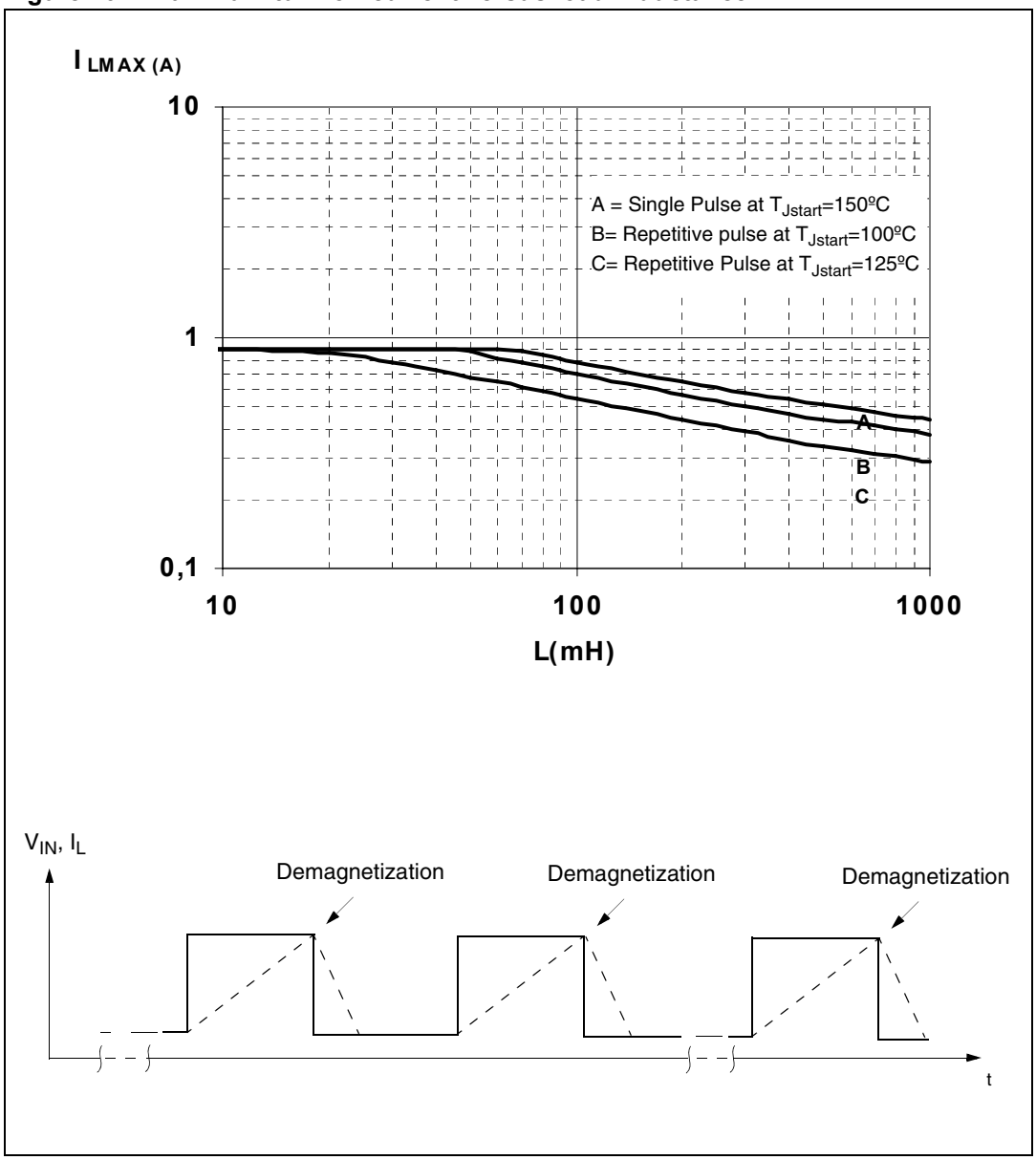
5kΩ ≤ R_{prot} ≤ 180kΩ.

Recommended values are:

R_{prot} =10kΩ

3.4 Maximum demagnetization energy (V_{CC} = 13.5V)

Figure 20. Maximum turn-off current versus load inductance



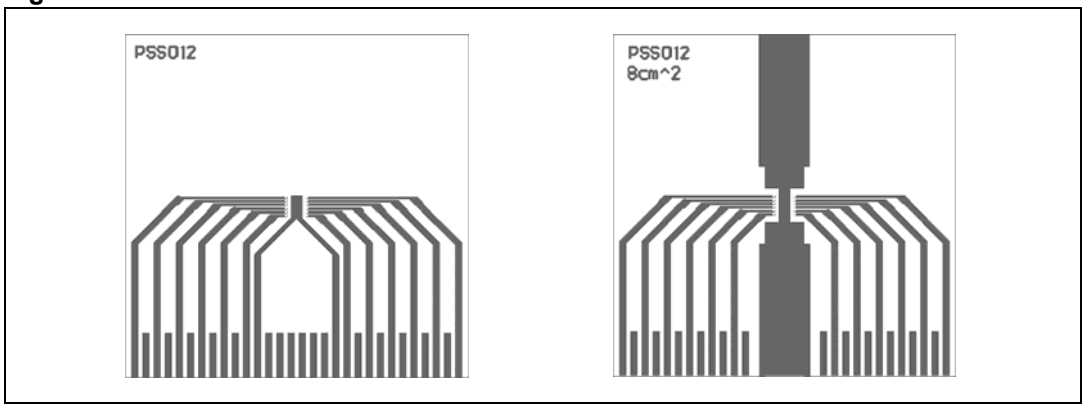
Note: Values are generated with R_L=0 Ω.

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

4 Package and thermal data

4.1 PowerSSO-12 thermal data

Figure 21. PowerSSO-12 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 78mm x 78mm, PCB thickness=2mm,Cu thickness=35µm, Copper areas: from minimum pad lay-out to 16 cm^2).

Figure 22. $R_{thj\text{-}amb}$ Vs PCB copper area in open box free air condition

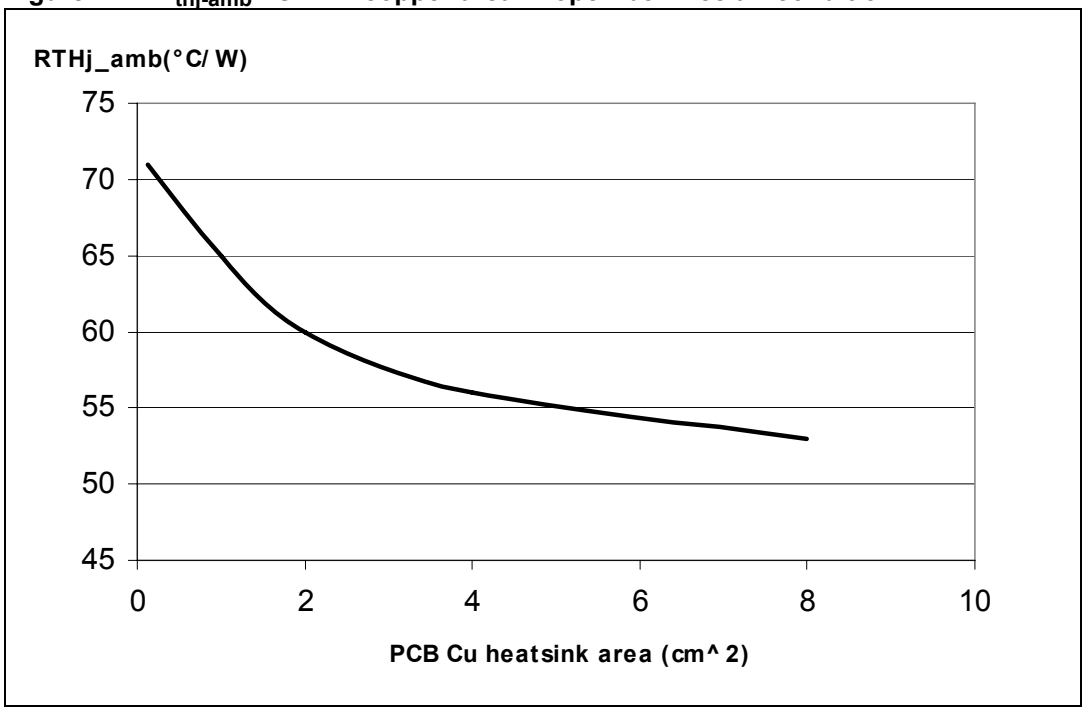
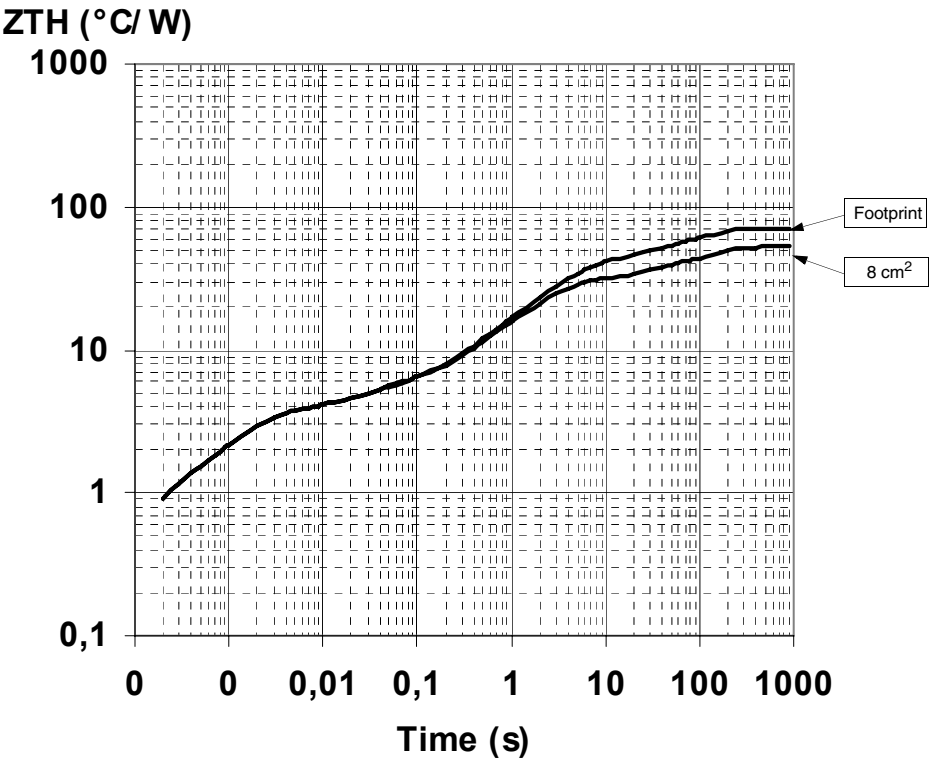


Figure 23. Thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Figure 24. Thermal fitting model of a quad channel HSD in PowerSSO-12

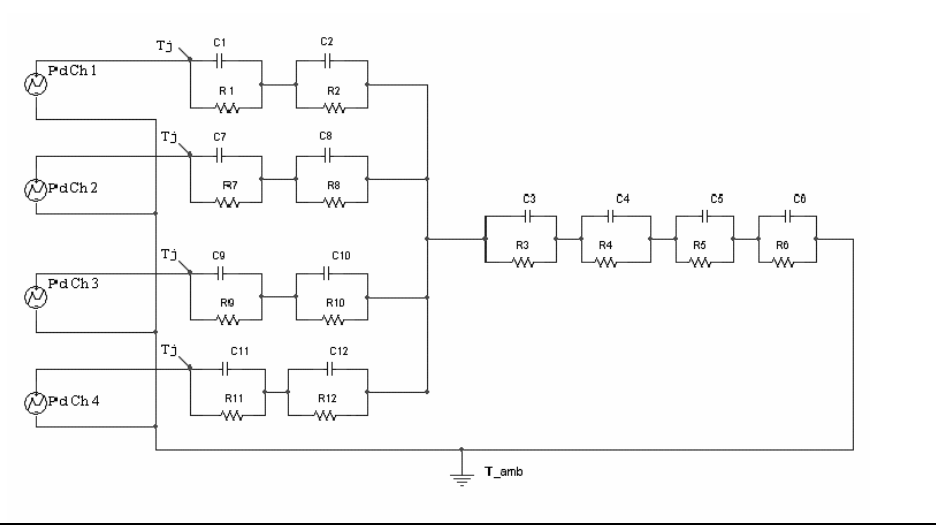


Table 11. Thermal parameter

Area/island (cm^2)	Footprint	8
R1=R7=R9=R11 (°C/W)	0.8	
R2=R8=R10=R12 (°C/W)	2.6	
R3 (°C/W)	1.5	
R4 (°C/W)	8	
R5 (°C/W)	28	18
R6 (°C/W)	30	22
C1=C7=C9=C11 (W.s/°C)	0.00006	
C2=C8=C10=C12 (W.s/°C)	0.0005	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.1	
C5 (W.s/°C)	0.15	0.17
C6 (W.s/°C)	3	5

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

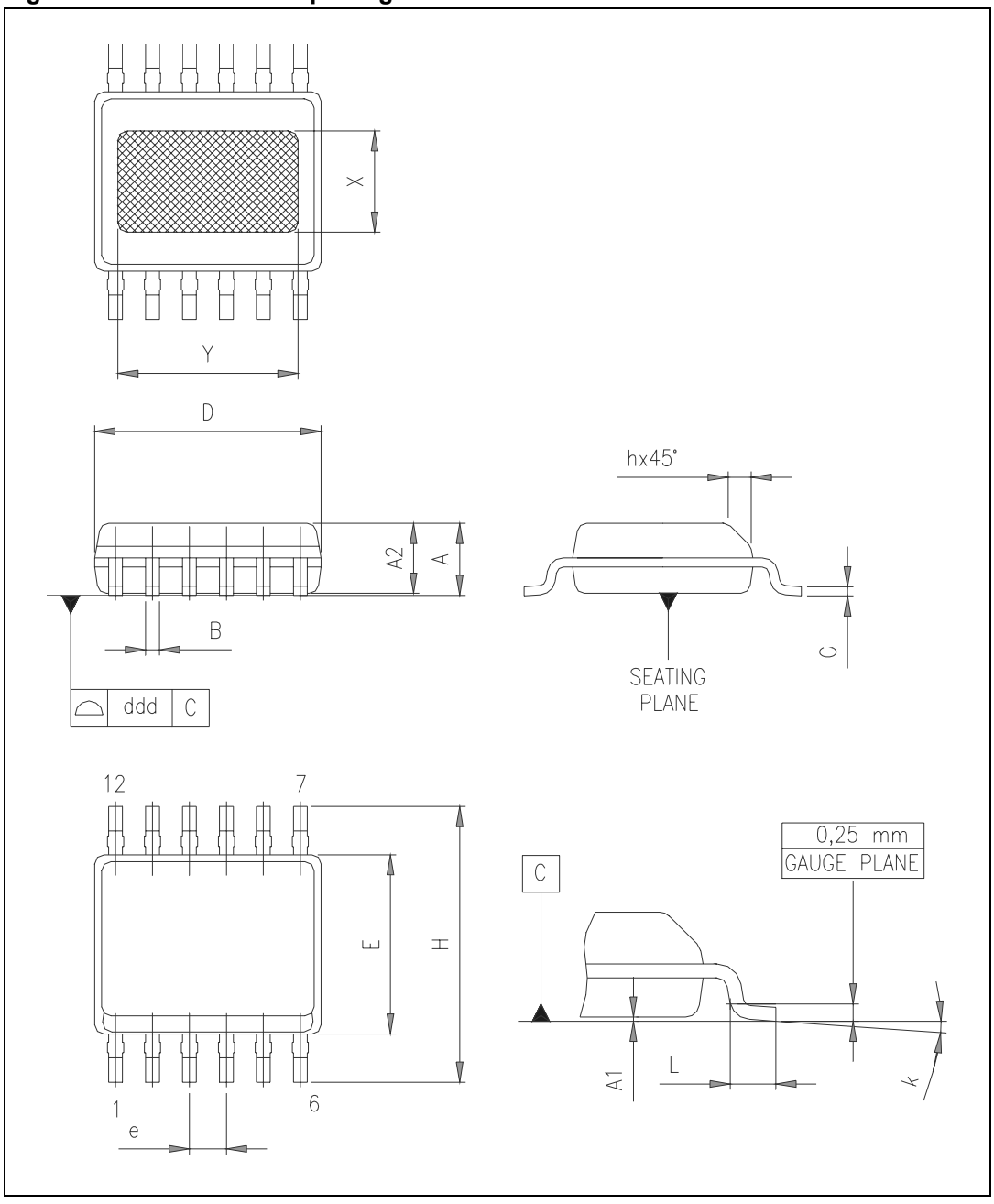
ECOPACK® is an ST trademark.

5.2 PowerSSO-12 mechanical data

Table 12. PowerSSO-12 mechanical data

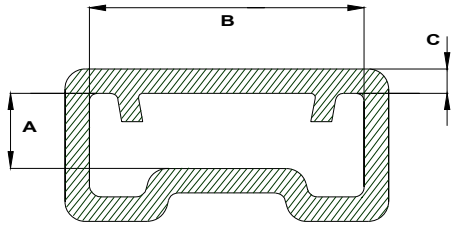
Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0º		8º
X	1.900		2.500
Y	3.600		4.200
ddd			0.100

Figure 25. PowerSSO-12 package dimensions



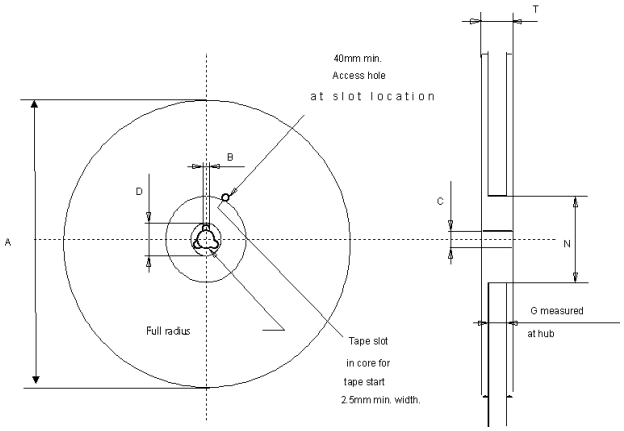
5.3 PowerSS0-12 packing information

Figure 26. PowerSSO-12 tube shipment (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	1.85
B	6.75
C (± 0.1)	0.6

Figure 27. PowerSSO-12 tape and reel shipment (suffix "TR")



Reel dimensions

Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

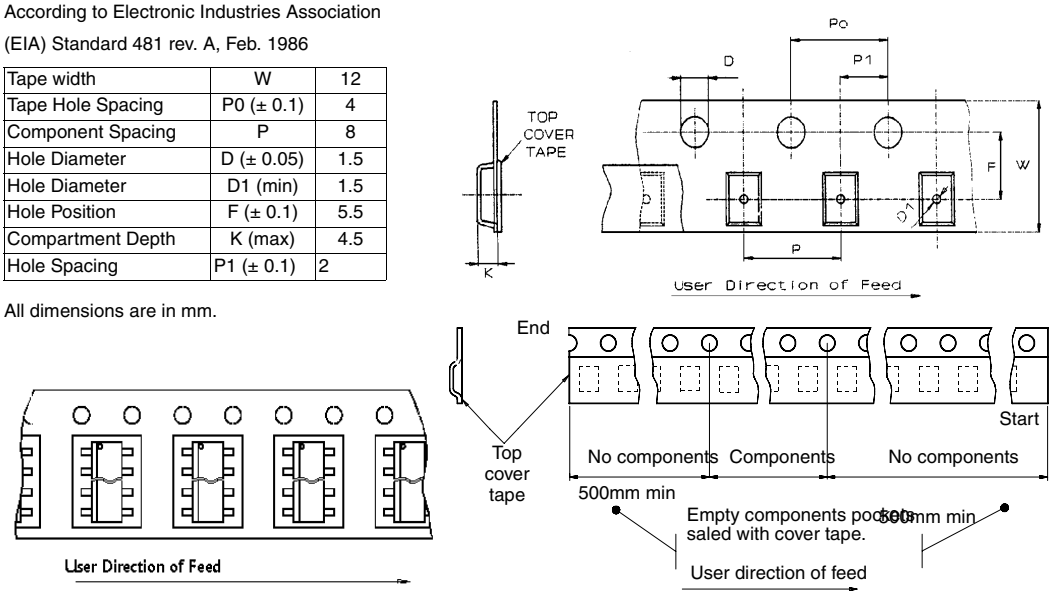
Tape dimensions

According to Electronic Industries Association

(EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	12
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D (± 0.05)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.1)	5.5
Compartment Depth	K (max)	4.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.



6 Revision history

Table 13. Document revision history

Date	Revision	Changes
24-Jan-2006	1	Initial release.
09-Dec-2008	2	Document restructured and reformatted. Updated *Table 3: Absolute maximum ratings* - corrected P_{tot} value. Updated *Table 4: Thermal data*. Updated *Figure 6: Waveforms* - corrected MC_{OUTn} signal. Updated *Table 10: Electrical transient requirements on VCC pin*. Corrected *Figure 22: Rthj-amb Vs PCB copper area in open box free air condition*. Added *ECOPACK® packages* information.
14-Jul-2009	3	Replaced the obsolete root part number VNQ500PEP-E with the new root part number VNQ500.

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