Digital Power Factor Correction Controller with Accurate AC Power Metering

Data Sheet

ADP1047/ADP1048

FEATURES

- Flexible digital power factor correction (PFC) controller
- Single phase operation (ADP1047); interleaved and bridgeless operation (ADP1048)
- True rms ac power metering
- Enhanced dynamic response
- Optimized light load efficiency performance
  - Output voltage adjustment
  - Frequency reduction
- Inrush current control
- Switching frequency spread spectrum for improved EMI
- External frequency synchronization
- PMBus compliant
  - Programmable ac line fault detection and protection
  - Programmable output fault detection and protection
- Extensive fault protection for high reliability systems
- Frequency range from 30 kHz to 400 kHz
- 8 kB EEPROM
- Programming via easy-to-use graphical user interface (GUI)

APPLICATIONS

- AC/DC power supplies for applications
  - Computing server and storage
  - Network and communication infrastructure
  - Industrial and medical

GENERAL DESCRIPTION

The ADP1047/ADP1048 are digital power factor correction (PFC) controllers that provide accurate input power metering capability and inrush current control for ac/dc systems. The ADP1047 is designed for single phase PFC applications; the ADP1048 is designed especially for interleaved and bridgeless PFC applications.

The digital PFC function is based on a conventional boost PFC with multiplication of the output voltage feedback combined with the input current and voltage to provide optimum harmonic correction and power factor for ac/dc systems. All signals are converted into the digital domain to provide maximum flexibility; all key parameters can be reported and adjusted via the PMBus™ interface. The ADP1047/ADP1048 allow users to optimize system performance, maximize efficiency across the load range, and reduce design time to market.

The ADP1047/ADP1048 provide accurate rms measurement of input voltage, current, and power. This information can be reported to the microcontroller of the power supply via the PMBus interface.

TYPICAL APPLICATIONS CIRCUIT

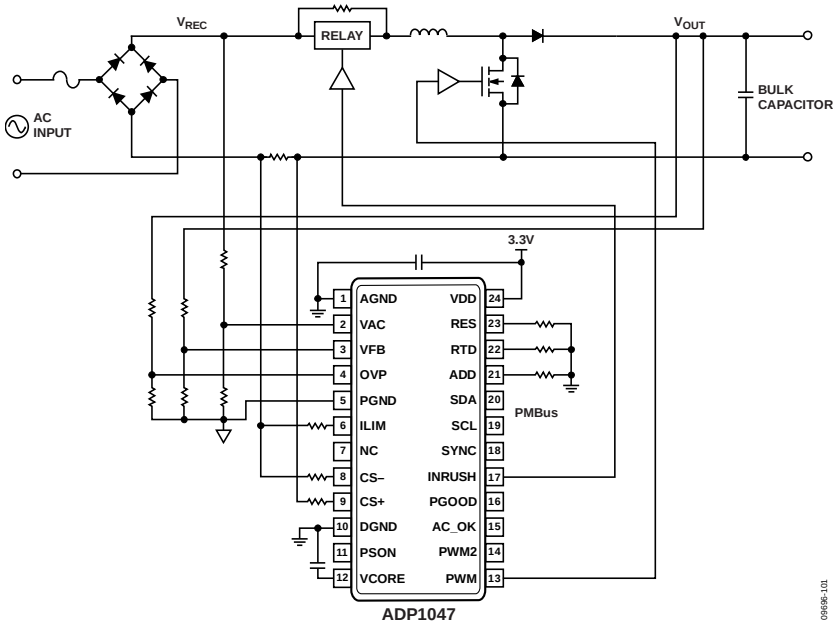

Figure 1.

Rev. 0

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REVISION HISTORY

9/11—Revision 0: Initial Version

The combination of a flexible, digitally controlled PFC engine and accurate input power metering facilitates the adoption of intelligent power management systems that are capable of making decisions to improve end-user system efficiency. The device supports additional efficiency improvements through programmable frequency reduction at light load and the capability to reduce the output voltage at light load.

The ADP1047/ADP1048 provide enhanced integrated features and functions; the inrush current and soft start control functions provide significant component count reduction with easy design optimization.

The devices are designed for high reliability, redundant power supply applications and have extensive and robust protection circuitry: independent overvoltage protection (OVP) and overcurrent protection (OCP), ground continuity monitoring, and ac sensing. Internal overtemperature protection (OTP) is provided whereby the external temperature can be recorded via an external sensing device.

The internal 8 kB EEPROM stores all programmed values and allows standalone control without a microcontroller. All parametric reporting and adjustments can be programmed via an easy-to-use GUI. No complex programming is required.

The ADP1047/ADP1048 operate from a single 3.3 V supply. The devices are available in a 24-lead QSOP package that is specified over an ambient temperature range of −40°C to +85°C.

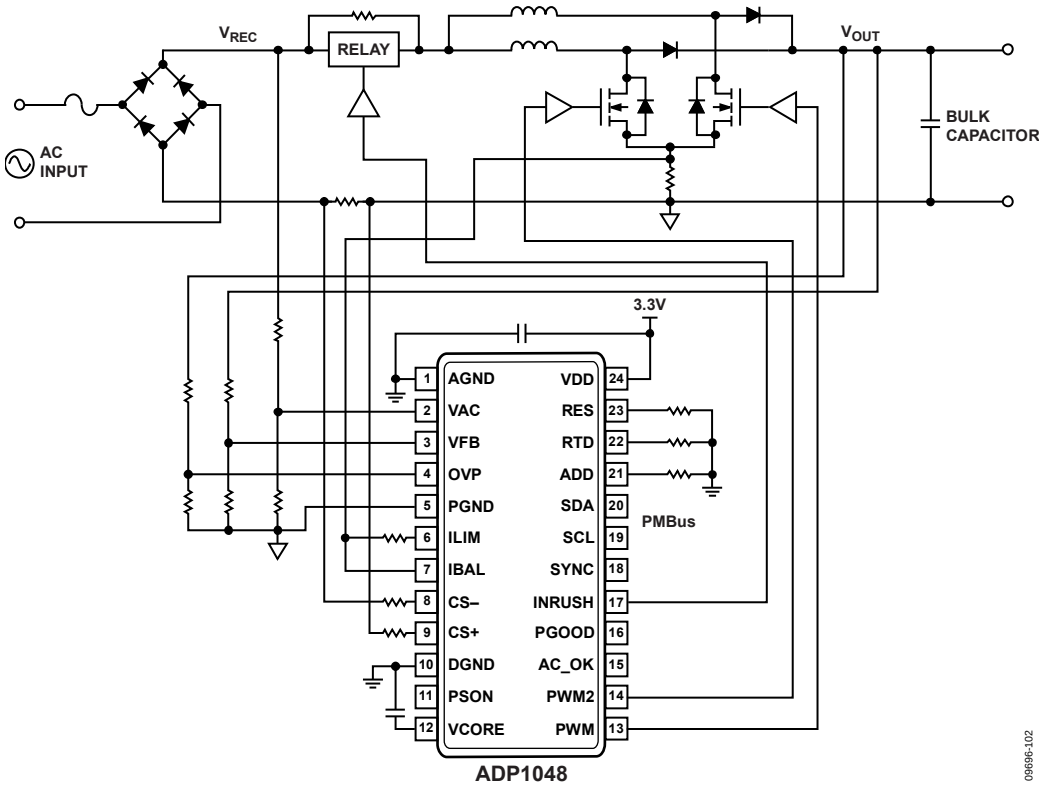


Figure 2. Typical Interleaved Application, ADP1048

SPECIFICATIONS

VDD = 3.3 V, T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Operating Supply Voltage	VDD		3.0	3.3	3.6	V
Supply Current	I_{DD}	Normal operation (PSON high) and no load on PWM output		17	40	mA
Supply Current for Programming	I_{DD_PK}	During EEPROM programming (50 ms)		I_{DD} + 8		mA
Shutdown Current	I_{DD_SD}			100		µA
POWER-ON RESET						
Power-On Reset		VDD rising	1.8		3	V
Undervoltage Lockout	UVLO	VDD falling	2.75	2.85	2.95	V
Overvoltage Lockout	OVLO		3.7	3.9	4.1	V
VCORE PIN						
Output Voltage Range		Temperature = 25°C	2.26	2.45	2.65	V
PWM OUTPUTS		PWM, PWM2 pins				
Output Low Voltage	V_{PWMOL}	Sink current = 10 mA			0.4	V
Output High Voltage	V_{PWMOH}	Source current = 10 mA	VDD − 0.4			V
Rise Time		C_{LOAD} = 50 pF		4		ns
Fall Time		C_{LOAD} = 50 pF		4		ns
VAC ADC						
Input Voltage Range			0		1.6	V
Leakage Current					5	µA
Equivalent Resolution				11		Bits
Voltage Sense Measurement Accuracy		From 2.5% to 97.5% of input voltage range				
		VDD = 3.3 V	−1.3		+1.3	% FSR
		VDD varies from 3.0 V to 3.6 V	−1.99		+1.99	% FSR
VFB ADC						
Input Voltage Range			0		1.6	V
Equivalent Resolution				11		Bits
Voltage Sense Measurement Accuracy		From 2.5% to 97.5% of input voltage range				
		VDD = 3.3 V	−1.2		+1.2	% FSR
		VDD varies from 3.0 V to 3.6 V	−1.72		+1.72	% FSR
CURRENT SENSE ADC						
High Input Voltage Range			0		750	mV
Low Input Voltage Range			0		500	mV
Equivalent Resolution				11		Bits
Current Sense Measurement Accuracy		From 0% to 97.5% of input voltage range				
		VDD = 3.3 V	−1.7		+1.7	% FSR
		VDD varies from 3.0 V to 3.6 V	−2.06		+2.06	% FSR
Current Source		10 kΩ level shifting resistor, $V_{CS+} - V_{CS-}$ = 0 V				
High Input				74		µA
Low Input				84		µA
Current Source Resolution				±0.03		%
RTD PIN						
Input Voltage Range			0		0.8	V
Current Source Accuracy			9	10	11	µA
Equivalent Resolution				14		Bits

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Voltage Sense Measurement Accuracy		From 2.5% to 97.5% of input voltage range				
		VDD = 3.3 V	−1.52		+1.52	% FSR
		VDD varies from 3.0 V to 3.6 V	−1.97		+1.97	% FSR
IBAL PIN (ADP1048 ONLY)		Interleaved operation mode				
Input Voltage Range			0		0.8	V
Equivalent Resolution				11		Bits
Channel Mismatch		DC input and acquiring time window on each channel is 526 µs	−5		+5	% FSR
POWER METER						
Measurement Accuracy		From 2.5% to 97.5% of input voltage range				
		VDD = 3.3 V	−2.3		+2.3	% FSR
		VDD varies from 3.0 V to 3.6 V	−2.75		+2.75	% FSR
SWITCHING FREQUENCY						
Frequency Range		Programmable	30		400	kHz
Accuracy			−3.85		+3.85	%
OSCILLATOR, CLOCK, AND PLL						
Oscillator Frequency			1.516	1.56	1.62	MHz
Digital Clock Frequency				200		MHz
PLL Frequency				200		MHz
RES PIN						
Temperature Stability			−120	0	+120	ppm/°C
PGOOD, AC_OK PINS						
Output Low Voltage					0.8	V
Output High Voltage			2.0			V
FAST OVERCURRENT PROTECTION						
Fast OCP Threshold						
Positive Signal			1455	1500	1550	mV
Negative Signal			452	500	523	mV
Current Source Accuracy				±4.4		%
Current Source Resolution				±3.2		%
Propagation Delay		From threshold trip to PWM disabled			140	ns
RMS OVERCURRENT PROTECTION						
RMS Accuracy		VDD = 3.3 V	−1.7		+1.7	%
Propagation Delay		AC line frequency = 50 Hz		12		ms
FAST OVERVOLTAGE PROTECTION						
Fast OVP Threshold		Fully programmable from 1 V to 1.5 V				
Rising		Register 0xFE2F, Bits[6:0]	1		1.5	V
Falling		Register 0xFE30, Bits[6:0]	1		1.5	V
OVP Threshold Minimum Step				3.9		mV
Accuracy			−4		+4	LSB
Propagation Delay (Latency)		Does not include blanking/debounce			120	ns
Blanking Time		Blanking after threshold reprogramming		10		µs
ACCURATE OVERVOLTAGE PROTECTION						
Accuracy		VDD = 3.3 V	−1.2		+1.2	%
Propagation Delay		AC line frequency = 50 Hz		12		ms
OPEN-LOOP PROTECTION						
VFB Error Threshold	ΔVFB		±33	±111	±242	mV
Propagation Delay				200		ns
Debounce Time				10		µs
Common-Mode Input Range			−0.2		+1.6	V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SDA, SCL PINS		VDD = 3.3 V				
Input Low Voltage					0.8	V
Input High Voltage			2.2			V
Output Low Voltage					0.4	V
Pull-Up Current			100		350	µA
Leakage Current			−5		+5	µA
SERIAL BUS TIMING						
Clock Frequency			10	100	400	kHz
Glitch Immunity	t_{SW}				50	ns
Bus Free Time	t_{BUF}		1.3			µs
Start Condition Hold Time	$t_{HD;STA}$		0.6			µs
Start Condition Setup Time	$t_{SU;STA}$		0.6			µs
Stop Condition Setup Time	$t_{SU;STO}$		0.6			µs
Data Hold Time	$t_{HD;DAT}$		300			ns
Data Setup Time	$t_{SU;DAT}$		100			ns
SCL Low Timeout	$t_{TIMEOUT}$		25		35	ms
SCL Low Time	t_{LOW}		1.3			µs
SCL High Time	t_{HIGH}		0.6			µs
Clock Low Extend Time	$t_{LOW;SEXT}$				25	ms
SCL, SDA Rise Time	t_R		20		300	ns
SCL, SDA Fall Time	t_F		20		300	ns
EEPROM RELIABILITY						
Endurance			10,000			Cycles
Data Retention		Temperature = 85°C	20			Years

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (Continuous), VDD	3.8 V
Digital Core Supply Voltage, VCORE	2.7 V
Digital Pins	−0.3 V to VDD + 0.3 V
Analog Pins	−0.3 V to VDD + 0.3 V
AGND to DGND	−0.3 V to +0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS-Compliant Assemblies (20 sec to 40 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
24-Lead QSOP (RQ-24)	44.4	6.4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

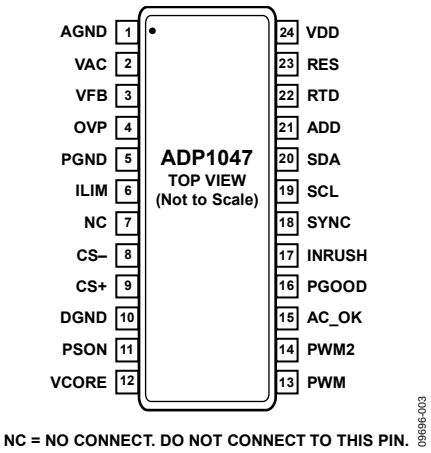


Figure 3. ADP1047 Pin Configuration

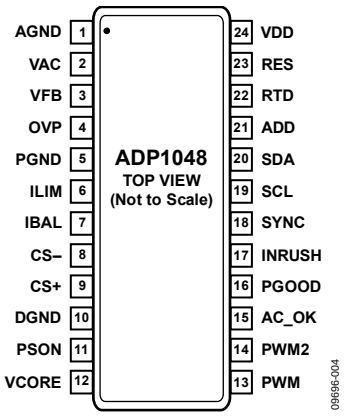


Figure 4. ADP1048 Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	AGND	Analog Ground. AGND should be connected directly to DGND.
2	VAC	Input Line Voltage Sense. The VAC signal is referred to PGND.
3	VFB	Feedback Voltage Sense. The VFB signal is referred to PGND. VFB is the feedback signal for PFC power circuit regulation. It is used as the analog voltage input to the VFB ADC.
4	OVP	Overvoltage Protection. The OVP signal is referred to PGND. This signal is used for redundant overvoltage protection.
5	PGND	Power Ground. PGND is the connection for the ground line of the power rail. There should be a low impedance path between PGND and AGND.
6	ILIM	Fast Current Limiting. This pin is referred to PGND.
7	NC/IBAL	ADP1047: No Connect. Do not connect to this pin. ADP1048: Current Balancing Input for Interleaved Operation. The IBAL input is referred to PGND.
8	CS–	Differential Current Sense Negative Input. The CS– signal is used for current measurement, monitoring, and protection. A 0.1%, 10 kΩ resistor must be used to connect to this circuit.
9	CS+	Differential Current Sense Positive Input. The CS+ signal is used for current measurement, monitoring, and protection. A 0.1%, 10 kΩ resistor must be used to connect to this circuit.
10	DGND	Digital Ground. DGND should be connected directly to AGND.
11	PSON	Power Supply Enable Signal. The PSON signal is used to enable/disable the PFC controller. The PSON signal is referred to DGND.
12	VCORE	Output of 2.5 V Regulator. Connect a 100 nF capacitor from VCORE to DGND.
13	PWM	PWM Output for PFC Regulation. The PWM signal is referred to AGND.
14	PWM2	Auxiliary PWM Output (ADP1047) or Interleaved PWM Output (ADP1048). The PWM2 signal is referred to AGND.
15	AC_OK	Open-Drain Output. User-configurable signal from a combination of flags. The AC_OK signal is referred to AGND.
16	PGOOD	Open-Drain Output. User-configurable signal from a combination of flags. The PGOOD signal is referred to AGND.
17	INRUSH	Inrush Current Control Signal to an External Inrush Driver. This open-drain output is referred to AGND.
18	SYNC	Allows parallel PFC controllers to synchronize to reduce interference. This pin is referred to DGND.
19	SCL	I^2C Serial Clock Input. The SCL signal is referred to DGND.
20	SDA	I^2C Serial Data Input and Output (Open-Drain). The SDA signal is referred to DGND.
21	ADD	Address Select Input. Connect a resistor from ADD to AGND (see the PMBus Address section).
22	RTD	Thermistor Input. A thermistor is placed from RTD to AGND. The RTD signal is referred to AGND.
23	RES	Internal Voltage Reference. Connect a 0.1%, 50 kΩ resistor from RES to AGND.
24	VDD	Positive Supply Input. The range is from 3.0 V to 3.6 V. The VDD signal is referred to AGND.

FUNCTIONAL BLOCK DIAGRAMS

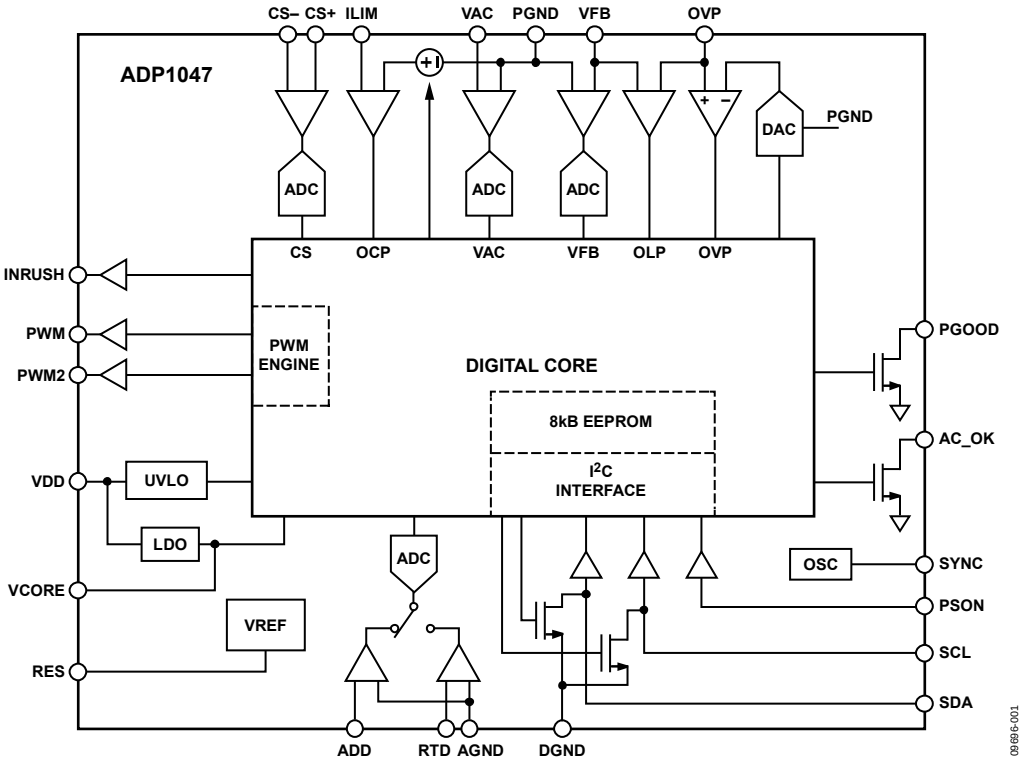


Figure 5. ADP1047 Functional Block Diagram

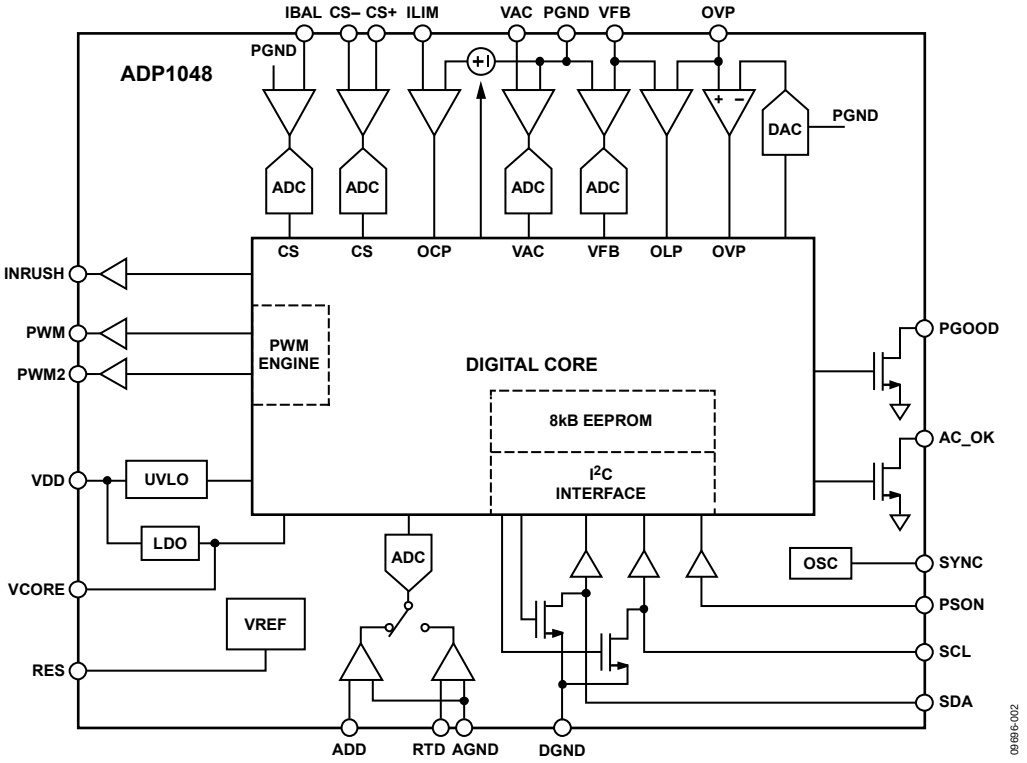


Figure 6. ADP1048 Functional Block Diagram

CONTROLLER ARCHITECTURE

The ADP1047/ADP1048 integrate the following functions:

- Power factor correction control loop (see the Power Factor Correction Control Loop section)
- Advanced input power metering (see the Advanced Input Power Metering section)
- PMBus digital communication (see the PMBus Digital Communication section)

This section describes the internal architecture of the chip.

CURRENT SENSE

Current sensing is used for the control, protection, and monitoring of the PFC stage. For normal operation, the power factor correction control loop requires inductor current information. The typical implementation uses a sense resistor on the input bus. A combination of two current transformers in series with the power switch and the boost diode can be used to reconstruct the inductor current and minimize losses in the resistive shunt, but, in general, a good quality shunt resistor provides much better accuracy in measuring input current and input power.

The inputs to the current sense ADC are differential. A pair of matched current sources is provided to level shift the negative signal across the current sense element in the input range of the current sense ADC (see Figure 7).

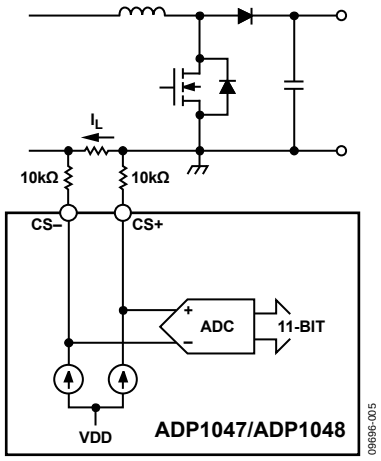


Figure 7. Current Sense Configuration

The current sense can be calibrated digitally to remove any errors due to external components (see the Current Sense Gain and Offset Trim section). This calibration can be performed in the production environment; the settings are saved in the EEPROM of the ADP1047/ADP1048.

The output of the Σ-Δ ADC is used for the following purposes:

- The output is decimated at the switching frequency for the control loop. The effective number of bits (ENOB) is >7 when the current loop bandwidth is 10 kHz; the ENOB is >10 when the current loop bandwidth is 1 kHz.
- The 11-bit result is calculated and updated at each half line cycle for high accuracy ac line current and input power monitoring and for overcurrent protection (accurate OCP).

RMS INPUT OVERCURRENT PROTECTION

The ADP1047/ADP1048 provide rms overcurrent protection (OCP). RMS OCP (or accurate OCP) is distinct from the instantaneous pulse-by-pulse fast overcurrent protection and is based on the rms value of the input ac current.

The measured value is compared to the limit set in the IIN_OC_FAULT_LIMIT register (Register 0x5B) at the end of each half cycle of the ac line. If the limit is exceeded, the action programmed in the IIN_OC_FAULT_RESPONSE register (Register 0x5C) is triggered.

In addition, an input current warning limit can be programmed in the IIN_OC_WARN_LIMIT register (Register 0x5D). This warning limit has no action attached to it, but it sets flags in the STATUS_BYTE register (Register 0x78, Bit 0), the STATUS_WORD register (Register 0x79, Bit 13), and the STATUS_INPUT register (Register 0x7C, Bit 1).

FAST OVERCURRENT PROTECTION (ILIM PIN)

A dedicated current limiting pin (ILIM) is provided to protect the part from pulse-by-pulse overcurrent events. When the threshold is crossed, the PWM pulse is terminated. This action is independent of any programming of the fast OCP flag. The next switching cycle resumes normally. Additional actions can be programmed (see Table 5).

The OCP comparator on the ILIM pin can accept positive or negative signals; the pin is referred to PGND (power ground) and has programmable level shifting current sources (see Table 5). These sources can be changed during normal operation to adapt to the level at which the overcurrent protection is triggered.

The OCP comparator also features programmable blanking and debounce times (see Table 5). If OCP is triggered, the PWM signal is terminated and operation resumes at the next switching cycle unless a different action is specified for the fast OCP response in Register 0xFE00.

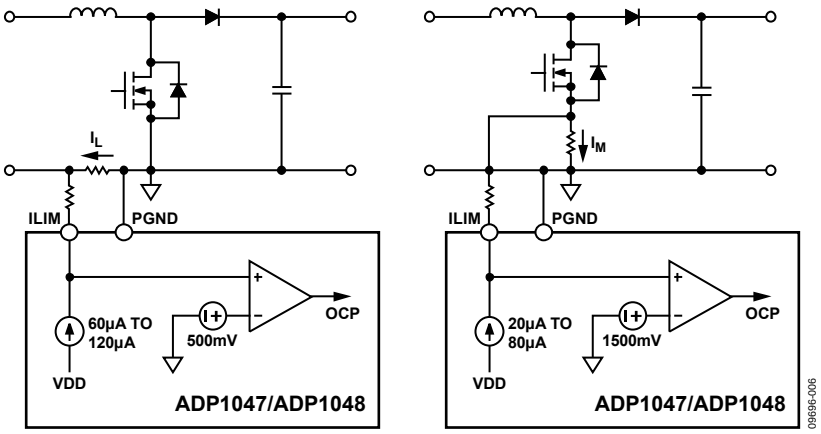


Figure 8. Fast Overcurrent Protection Schemes

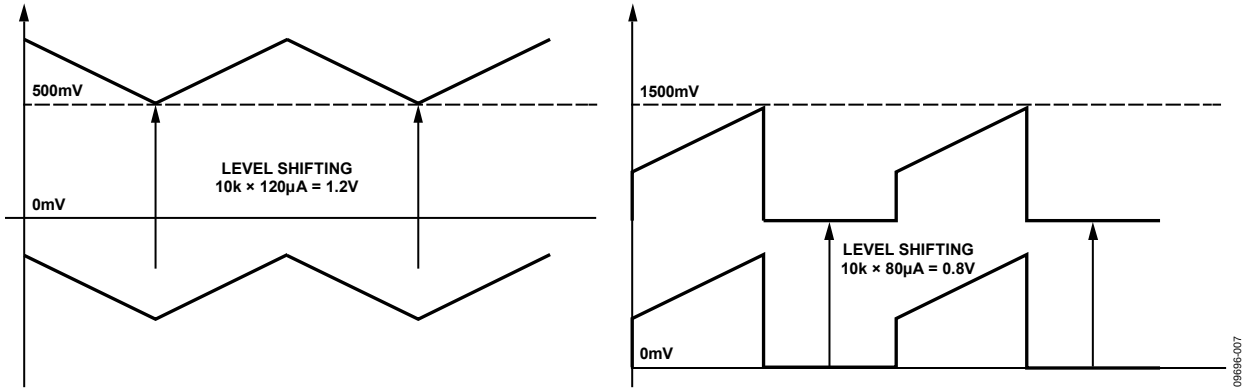


Figure 9. Level Shifting and Threshold for OCP

Table 5. Programmable Options for Fast Overcurrent Protection

Parameter	Values or Options	Comments
Debounce Time	40 ns, 80 ns, 120 ns, 240 ns	Register 0xFE3D, Bits[4:3]
Blanking Time	40 ns, 80 ns, 120 ns, 160 ns, 200 ns, 400 ns, 600 ns, 800 ns	Blanking from the leading edge; Register 0xFE3D, Bits[2:0]
Propagation Delay	140 ns typical	Fixed value; does not include blanking or debounce
Threshold Value and Polarity	500 mV (negative); 1500 mV (positive)	Fixed values
Level Shifting Current Sources	60 µA, 80 µA, 100 µA, 120 µA (negative) 20 µA, 40 µA, 60 µA, 80 µA (positive)	Register 0xFE3E, Bits[7:5]
Actions for Fast OCP	Ignore (still terminates the PWM pulse); allow n switching cycles, then shut down and soft start; allow n switching cycles, then shut down and wait for PSON signal	n = 1, 2, 4, 8; Register 0xFE00, Bits[7:6]

CURRENT BALANCING (IBAL PIN, ADP1048 ONLY)

The ADP1048 has a dedicated circuit to maintain current balance in each interleaved phase when operating in interleaved PFC topology. This ensures that each interleaved phase provides equal power regardless of the tolerance of the inductor and the boost switch driving circuitry.

The input is through the IBAL pin specifically provided for the ADP1048. The current balancing circuit monitors the current flowing in both switches of the interleaved PFC topology and stores this information. It compensates the PWM signals, ensuring equal current flow to balance the current between interleaved phases. Several switching cycles are required for the circuit to operate effectively. The current balance settings are programmed in Register 0xFE43 and Register 0xFE95.

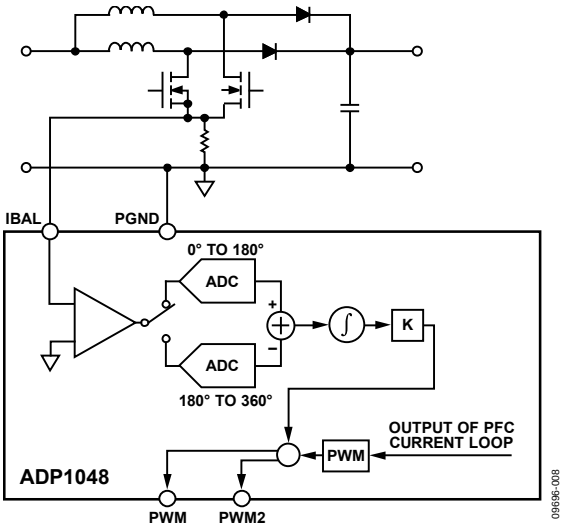


Figure 10. Current Balancing (IBAL) for the ADP1048

VOLTAGE SENSE

Voltage sensing is used for the control, protection, and monitoring of the PFC stage. Input and output voltages are sensed using dedicated ADCs and references (see Figure 11).

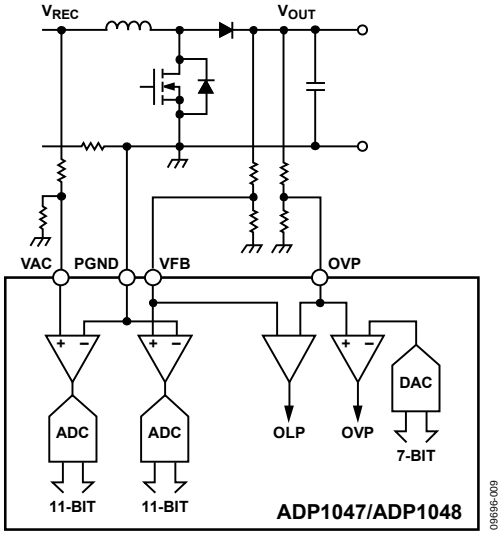


Figure 11. Typical Voltage Sense Configuration

The voltage sense can be calibrated digitally to remove any errors due to external components (see the Output Voltage (VFB) Calibration and Trim section). This calibration can be performed in the production environment; the settings are saved in the EEPROM of the ADP1047/ADP1048.

Input Voltage Sensing (VAC Pin)

The VAC pin is used for the monitoring and protection of the rectified power supply input voltage. The sense point on the power rail requires an external resistor divider to bring the signal within the operating input range of the ADC (0 V to 1.6 V). This scaled-down signal is fed into a high speed Σ-Δ ADC.

The output of the Σ-Δ ADC goes to the digital filter and is used for the following purposes:

- The output is decimated at the switching frequency for the control loop. The effective number of bits (ENOB) is >7 when the current loop bandwidth is 10 kHz; the ENOB is >10 when the current loop bandwidth is 1 kHz.
- The 11-bit result is calculated and updated at each half line cycle for high accuracy input voltage and power monitoring.

Output Voltage Sensing (VFB Pin)

The VFB pin is used for the control, monitoring, and protection of the output voltage. This voltage is the main feedback loop for the power supply control loop. The sense point on the power rail requires an external resistor divider to bring the signal within the operating input range of the ADC (0 V to 1.6 V). This scaled-down signal is fed into a high speed Σ-Δ ADC.

The output of the Σ-Δ ADC goes to the digital filter and is used for the following purposes:

- The 11-bit result is used at each half line cycle for the normal control loop to control the value of the output voltage.
- The 10-bit, 1.5 kHz update rate is used for the fast voltage control loop to control the value of the output voltage during large transients.

To reduce the current distortion from the output voltage feedback, a prefilter is implemented before the voltage loop filter. The prefilter detects the zero-crossing point of the input voltage to identify the half input line cycle. The prefilter then performs an averaging function for the sampled VFB signal during this half line cycle. In this way, the fundamental frequency of the output bulk voltage ripple and its harmonics are significantly attenuated.

OVERVOLTAGE PROTECTION

The ADP1047/ADP1048 have two OVP circuits: an ADC-based comparator and a fast comparator.

Accurate Overvoltage Protection (VFB Pin)

Overvoltage protection (OVP) is implemented using the information available on the output of the VFB ADC. The information from the VFB ADC is averaged over one half the ac line frequency; therefore, the response of this OVP is relatively slow.

The threshold for the accurate OVP is fully programmable using the VOUT_OV_FAULT_LIMIT register (Register 0x40). The programmed value is the dc average voltage.

When the accurate OVP threshold is crossed, the accurate OVP flag is set. The response to this flag can be programmed for one of several actions using the VOUT_OV_FAULT_RESPONSE register (Register 0x41). If the disable PWM option is selected, a voltage hysteresis can be programmed for the accurate OVP threshold using Register 0xFE50.

Fast Overvoltage Protection (OVP Pin)

A fast OVP mode is implemented using a programmable comparator on the OVP pin. Fast OVP is used for overvoltage protection of the bulk capacitors and to provide open-loop protection. The sense point on the power rail requires an external resistor divider to match the divider applied to VFB. This separate divider introduces a level of redundancy in sensing the output voltage to improve system reliability.

If the voltage divider on the VFB pin is damaged or drifts in value, the OVP pin can still detect an overvoltage condition and take the appropriate programmed action.

The fast OVP signal is fed into a comparator with a programmable threshold to set the trip point for overvoltage. The threshold is set using a DAC.

Table 6. Programmable Options for Fast Overvoltage Protection (Fast OVP)

Parameter	Values or Options	Comments
Debounce Time	120 ns, 240 ns, 480 ns, 640 ns	Minimum duration of pulse to be considered; programmable using Register 0xFE31, Bits[1:0]
Blanking Time	10 µs (fixed)	Duration of time while the comparator is blanked and the threshold changes from rising to falling
Propagation Delay	120 ns max (fixed)	Does not include blanking or debounce
Threshold Rising	1 V to 1.5 V	Programmable using Register 0xFE2F, Bits[6:0]
Threshold Falling	1 V to 1.5 V	Programmable using Register 0xFE30, Bits[6:0]
Actions for Fast OVP	Immediate shutdown and wait for PSON; disable PWM until the flag is cleared; shut down and soft start; ignore (do nothing)	Register 0xFE01, Bits[7:6]

Figure 12 shows an example of the output voltage and the OVP thresholds set. The rising and falling thresholds, FAST_OVP_FAULT_RISE and FAST_OVP_FAULT_FALL, respectively, are used for fast OVP protection. FAST_OVP_FAULT_RISE corresponds to OVP_{UP}, which is the trip point for overvoltage protection (see Figure 13). FAST_OVP_FAULT_FALL corresponds to OVP_{DOWN}, which is the reset point for the fast OVP.

When the rising threshold is triggered, the programmed action is applied and the threshold is switched to the programmed falling threshold (if the programmed falling threshold is different from the rising threshold).

A blanking time is applied when the thresholds are switched to avoid spurious signals (see the timing diagram in Figure 13). A programmable debounce time is applied to the OVP signal as well to avoid false triggering.

The rising and falling thresholds are programmable from 1 V to 1.5 V (at the OVP pin) using Register 0xFE2F and Register 0xFE30, respectively.

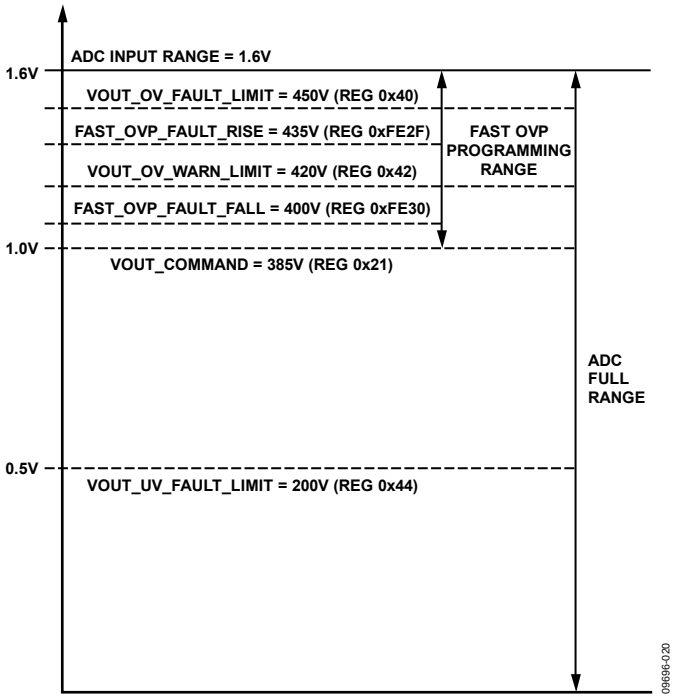


Figure 12. Output Voltage Levels

Open-Loop Protection

Open-loop protection detects differences between the OVP and VFB pins. Identical resistor dividers are applied to these pins; therefore, if a voltage difference is present, it means that one or more resistors in the dividers have the wrong values or are not connected. In this case, it is usually recommended that the user shut down the system to prevent damage.

The open-loop protection detects a difference in voltage in excess of ~100 mV, which equates to approximately 6.6% of the full-scale range.

A debounce time of 10 µs is added to avoid false triggering. If filtering capacitors are applied to the OVP and VFB pins, care must be taken to make sure that the time constant difference does not exceed 10 µs.

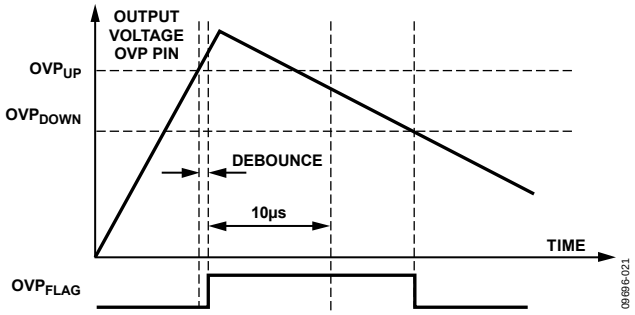


Figure 13. OVP Thresholds and Timing

Table 7. Programmable Options for Open-Loop Protection (OLP)

Parameter	Values or Options	Comments
Debounce Time	10 µs (fixed)	Minimum duration of pulse to be considered
Propagation Delay	200 ns (fixed)	Does not include debounce
Actions for OLP	Immediate shutdown and wait for PSON; disable PWM until the flag is cleared; shut down and soft start; ignore (do nothing)	Register 0xFE02, Bits[7:6]

POWER FACTOR CORRECTION CONTROL LOOP

The ADP1047/ADP1048 implement the average current mode power factor correction control loop using a traditional multiplier approach. The implementation of the loop is digital, and all the signals are converted from analog to digital before they are processed by the control loop. Σ-Δ ADCs are used to achieve high performance, cost-effective implementation. Each ADC has its own dedicated voltage reference.

DIGITAL COMPENSATION FILTERS

The ADP1047/ADP1048 are digital PFC controllers with ac power monitoring. They are implemented in the digital domain using a dedicated state machine, which allows the user to program the loop response specifically, with no need for external loop compensation.

The detailed control loop configuration is illustrated in Figure 14. V_{REF} is the digital reference voltage setting; V_{FB} is the sensed feedback voltage of the output. The difference between V_{REF} and V_{FB} is processed first by the voltage loop filter (H_V). Its output, V_{EA}, is then multiplied by the instantaneous rectified input voltage, V_{AC}, and divided by the square of the rms value of V_{AC}. The result, I_{REF}, is used as the reference signal for the current. The output of the current loop filter (H_I) is the duty cycle command. The mathematical expression is

$$I_{REF} = \frac{V_{EA} \times V_{AC}}{V_{AC\_RMS}^2}$$

Both the voltage loop and current loop digital compensating filters, $H_V(z)$ and $H_I(z)$, are programmable. The filter transfer function in the digital domain is

$$H(z) = k \times b \times \frac{\left(z - \frac{a}{256}\right)}{(z-1)}$$

where:
a is the filter zero.
b is the filter gain.
k is related to the switching frequency.

The frequency gains and zero locations can all be programmed individually to tailor the loop response to the application. It is recommended that the Analog Devices, Inc., GUI software be used to program the filter (see the Software GUI section). The GUI displays the filter response in Bode plot format and can be used to calculate all stability criteria for the power supply.

Optimized Compensation Filters

Instead of a single programmable compensation filter, the ADP1047/ADP1048 offer the following filter presets so that the dynamic response of the control loop can be tailored to optimize different operating conditions.

- Low line current filter
- High line current filter
- Fast voltage compensation filter

The ADP1047/ADP1048 can be configured to switch automatically between the high and low line filters when the rms value of the ac line crosses the programmed threshold between the high and low lines. (The high line threshold is programmed in Register 0xFE35; the low line threshold is programmed in Register 0xFE36.)

The ADP1047/ADP1048 check for the value of the rms input voltage at each half line cycle. When a transition between the high and low line threshold is detected, the part waits for four full line cycles before switching to the correct filter at the zero crossing of the input line cycle. This is done to avoid spurious transitions due to a missing or distorted voltage line cycle.

During soft start, one of four combinations of filters can be used, depending on whether the fast loop mode is enabled and whether the high line or low line is detected for soft start (see Table 8).

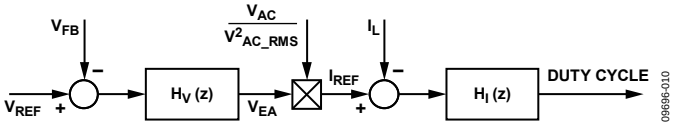


Figure 14. Control Loop Digital Filters

Table 8. Summary of the PFC Digital Compensation Filters for Soft Start

Line Filter	Normal Compensation Filter	Fast Voltage Compensation Filter
High Line	High line current filter, normal voltage filter	High line current filter, fast voltage filter
Low Line	Low line current filter, normal voltage filter	Low line current filter, fast voltage filter

Fast Loop Mode

During transients, a fast loop mode is enabled to allow for faster loop responses. Typical timing can be seen in Figure 15. The fast loop mode has separate settings and can be programmed to respond quickly to load transients. The user can disable the fast loop mode if it is not required by the application.

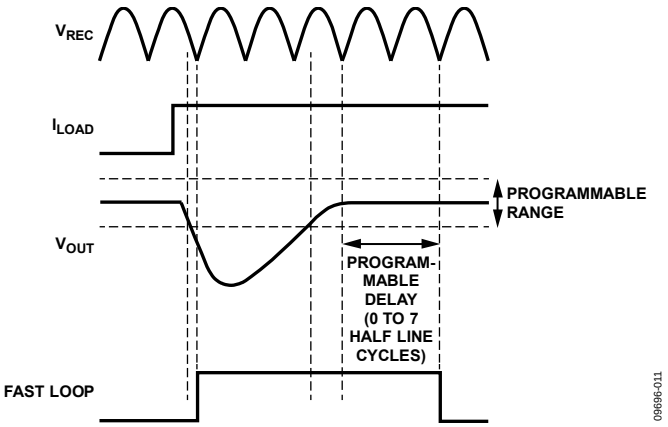


Figure 15. Fast Loop for Transient Response Improvement

When fast loop mode is enabled and the feedback output voltage is out of range from the desired reference value (programmable band of 1.5%, 3%, 6%, or 12%, set in Register 0xFE24), the ADP1047/ADP1048 enter fast loop mode.

To ensure a smooth transition, the ADP1047/ADP1048 switch from the regular filter to the fast loop filter at the zero crossing of the rectified input voltage. When the output voltage returns to regulation within the programmed band, the controller switches back (after a programmable delay of 0 to 7 half line cycles) to the normal loop at the next zero crossing of the rectified input voltage.

If the output voltage does not return to regulation within the programmed band after a fixed time of 630 ms, the control loop automatically switches back to the normal loop.

In the normal compensation loop, the sampling frequency of the output voltage is the same as the ripple oscillation frequency (which is commonly 100 Hz or 120 Hz).

During fast loop operation, the feedback voltage is sampled at 1.5 kHz, and the fast filter is applied to regulate the output voltage. The output voltage is averaged and decimated at 1.5 kHz (see Figure 16).

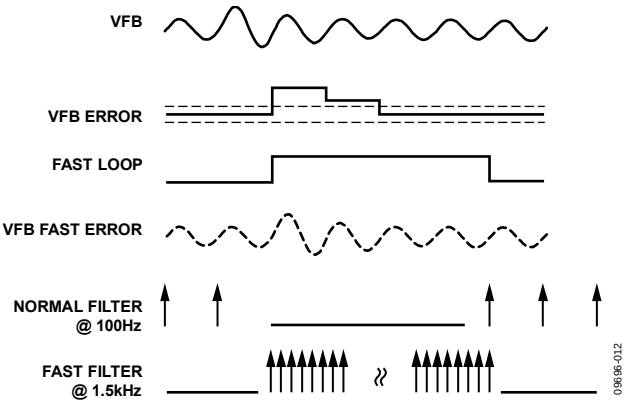


Figure 16. Fast Loop Operation

Based on the requirements of the application, the user can enable or disable the fast loop mode by programming Register 0xFE24. It is recommended that fast loop mode be enabled for the ADP1047/ADP1048 during large load transients. The fast loop mode settings are also used during soft start, even when the fast loop is disabled.

PULSE-WIDTH MODULATION

The ADP1047/ADP1048 can implement either leading edge or trailing edge modulation. Trailing edge modulation is the more popular modulation scheme. Using trailing edge modulation, the rms ripple current in the bulk capacitors can be reduced when used with downstream converter synchronization. It is recommended that the Analog Devices, Inc., GUI software be used to program PWM (see the Software GUI section).

DUTY CYCLE MINIMUM/MAXIMUM LIMITS

The ADP1047/ADP1048 allow the user to program the minimum off time and the minimum on time for the PWM outputs separately, thereby allowing the minimum and maximum duty cycles to be set.

The minimum off time represents the minimum time that the PWM is low during each switching cycle. It can be programmed from 40 ns to 1.2 µs in steps of 80 ns using Register 0xFE15, Bits[3:0]. In this way, the maximum duty cycle can be clamped between 96% and 99.8% at the minimum frequency and between 48.8% and 96.8% at the maximum frequency.

The minimum on time is the smallest PWM pulse that the modulator generates on the PWM output. It can be programmed from 0 ns to 1200 ns in steps of 80 ns using Register 0xFE15, Bits[7:4].

AUXILIARY PWM OUTPUT (ADP1047 ONLY)

For the ADP1047, the PWM2 pin is the output for the auxiliary PWM, which can be independent of the main PWM output. PWM2 can be used as the control signal for auxiliary switching in the zero-voltage transition soft-switched PFC boost circuit.

SWITCHING FREQUENCY PROGRAMMING

The switching frequency of the PWM outputs can be programmed from 30 kHz to 400 kHz using Register 0xFE1B, Bits[5:0] (see Table 9).

Table 9. Switching Frequency Settings from 30 kHz to 400 kHz (Register 0xFE1B, Bits[5:0])

Frequency Setting (Decimal)	Frequency (kHz)	Frequency Setting (Decimal)	Frequency (kHz)	Frequency Setting (Decimal)	Frequency (kHz)	Frequency Setting (Decimal)	Frequency (kHz)
0	30.05	16	107.76	32	204.92	48	277.78
1	32.55	17	111.61	33	208.33	49	284.09
2	35.51	18	115.74	34	211.86	50	290.70
3	39.06	19	120.19	35	215.52	51	297.62
4	43.40	20	125.00	36	219.30	52	304.88
5	48.83	21	130.21	37	223.21	53	312.50
6	52.06	22	135.87	38	227.27	54	320.51
7	55.80	23	142.05	39	231.48	55	328.95
8	60.10	24	148.81	40	235.85	56	337.84
9	65.10	25	156.25	41	240.38	57	347.22
10	71.02	26	164.47	42	245.10	58	357.14
11	78.13	27	173.61	43	250.00	59	367.65
12	86.81	28	183.82	44	255.10	60	378.79
13	97.66	29	195.31	45	260.42	61	390.63
14	100.81	30	198.41	46	265.96	62	403.23
15	104.17	31	201.61	47	271.74	63	403.23

LINE FAULT PROTECTIONS AND SOFT START SEQUENCING

PSON OPERATION

To comply with PMBus standards, the PFC circuit controlled by the ADP1047/ADP1048 can be turned on and off by the hardware PSON pin and/or the software PSON command. The setting of Bit 2 in Register 0x02 determines whether the PSON pin and/or the PSON command is used. If the PSON pin is used, the pin can be configured to be either active high or active low (see Table 18).

AC LINE DETECTION

The ADP1047/ADP1048 are capable of detecting several parameters of the ac line input voltage and taking the appropriate programmed actions when necessary. The detection is a combination of time and voltage measurements and is implemented via the VAC pin, which detects the rectified ac input voltage. This allows early detection of ac line faults and early warning for the host system, thereby increasing reliability.

Five main parameters are related to ac line detection.

- VAC_LINE_PERIOD (Register 0xFE85)
- VAC_THRESHOLD_SET (Register 0xFE25)
- VAC_THRESHOLD_READ (Register 0xFE26)
- MIN_AC_PERIOD_SET (Register 0xFE27)
- MAX_AC_PERIOD_SET (Register 0xFE28)

AC Line Period and Zero Crossing

The input ac line period is measured every half period of the ac line cycle and is reported in the VAC_LINE_PERIOD register (Register 0xFE85).

During the first 40 ms, the ac line period is measured between two consecutive falling crossings of the threshold value, which is set in the VAC_THRESHOLD_SET register (Register 0xFE25, Bits[6:0]). The ac line period is then measured between two consecutive falling crossings and compared to the average value of the input line voltage, which is calculated during each half line period. The VAC average reading can be found in the VAC_THRESHOLD_READ register (Register 0xFE26, Bits[6:0]).

If the measured period is larger than MAX_AC_PERIOD_SET or smaller than MIN_AC_PERIOD_SET, the default, MAX_AC_PERIOD_SET, is used as the value of the period.

As shown in Figure 17, the two consecutive crossing points, B and C, are used to determine the zero-crossing point of the ac line. The middle point between B and C is calculated as the zero-crossing point.

This information is used by the control loop, as well as the power metering block.

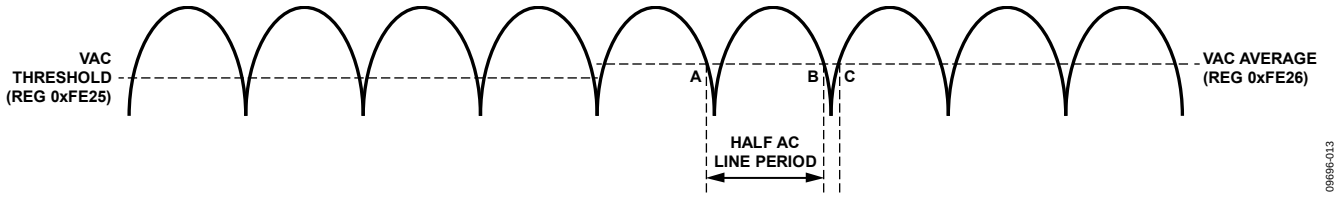


Figure 17. AC Line Period Detection

AC Line Value Detection

To operate, the controller must detect the ac line value. At startup, the controller waits for the PSON signal (hardware PSON, software PSON, or both, depending on how the part is programmed).

When the PSON signal is present, the controller looks for the ac line period and value (see Figure 18).

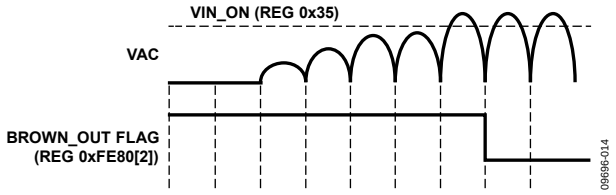


Figure 18. VAC Detection for Startup

The start-up value for the ac line used by the controller to initiate the start-up procedure is stored in the VIN_ON register (Register 0x35). This value is the minimum rms value of the ac line required for the system to start up. The controller measures the value of VAC at every half line cycle and compares it with VIN_ON. If VAC is larger than the value in the VIN_ON register, the soft start procedure is initiated and the BROWN_OUT flag is reset.

AC Line Early Fault Detection

After the VIN_ON limit is crossed and the system starts up, the controller constantly monitors the condition of the ac line (see Figure 19).

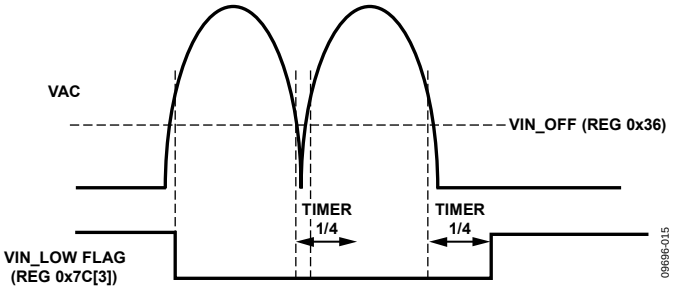


Figure 19. AC Line Early Fault Detection

To provide early detection of ac line faults, the instantaneous value of VAC is compared to the VIN_OFF value in Register 0x36. If VAC remains below the VIN_OFF threshold for a time longer than the programmed period, the VIN_LOW flag is set in Register 0x7C. The programmed period can be either a fraction of the detected ac line period (one-quarter or one-half) or it can be an absolute time (2 ms or 4 ms); the value is set in Register 0xFE2E.

The controller does not take any action, but the VIN_LOW signal can be used to set the AC_OK signal and to trigger immediate actions in the power system.

The VIN_OFF threshold is intended solely to provide early warning of problems on the ac line; it is not used to shut down the power supply. The VIN_UV_FAULT_LIMIT register (Register 0x59) is used for that purpose.

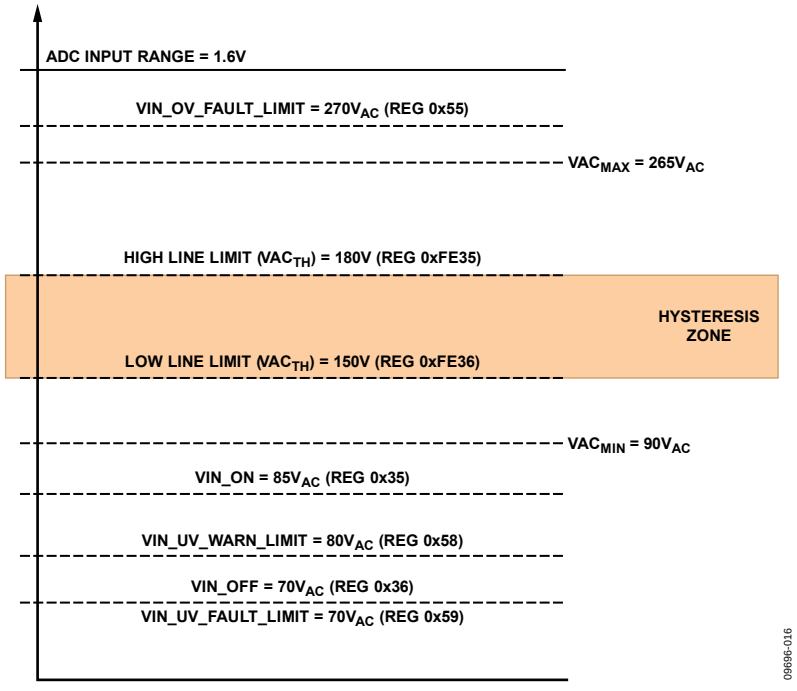


Figure 20. Input Voltage Limits

SOFT START PROCEDURE

The PSON signal is used to enable or disable the PFC stage. After PSON is asserted, the ADP1047/ADP1048 start monitoring VAC and, if the ac line conditions are met, they initiate the soft start procedure, as shown in Figure 21.

Startup is gated by the rms value of the ac line voltage measured on one half period of the ac line frequency. When VAC is above the VIN_ON value, the BROWN_OUT flag is reset and the soft start sequence is initiated. At the same time, the inrush delay time and soft start delay time timers begin. Both of these timers can be programmed to count 0 to 7 line cycles (or 0 to 14 half line cycles in steps of 2).

After the inrush delay time programmed in Register 0xFE2E, Bits[2:0], the INRUSH flag is reset and the inrush signal (Pin 17) is asserted, closing the inrush current relay. (Note that the INRUSH flag is active low.) The inrush signal is set at the zero crossing of the ac voltage, if this crossing is detected. This setting allows zero voltage turn-on if a solid-state switch is used (zero voltage turn-on is not relevant with mechanical relays).

After the soft start delay time (programmed in Register 0xFE2D, Bits[5:3]), the output voltage is ramped up according to the soft start time programmed in Register 0xFE2D, Bits[2:0].

Some of the flags can be blanked during soft start so that the programmed action of the flag does not take place if the flag is set during the soft start period (see Register 0xFE08 and Register 0xFE09).

When output voltage regulation is reached and all flags are OK, the POWER_GOOD# flag is reset and the PGOOD signal (Pin 16) is set to Logic Level 1. (Note that the POWER_GOOD# flag is active low.)

The soft start time can be programmed to one of eight values: 112 ms, 168 ms, 224 ms, 280 ms, 392 ms, 504 ms, 616 ms, or 728 ms (set in Register 0xFE2D, Bits[2:0]).

The soft start delay time (Register 0xFE2D, Bits[5:3]) can be programmed from 0 to 7 full line cycles in increments of 1 (that is, two of the rectified half line cycles).

The inrush delay time (Register 0xFE2E, Bits[2:0]) can be programmed from 0 to 7 full line cycles in increments of 1 (that is, two of the rectified half line cycles).

If no zero crossings are detected, the programmed maximum ac line period, MAX_AC_PERIOD_SET (Register 0xFE28), is used.

LINE FAULT PROTECTIONS

Line faults occur when the ac line is not behaving correctly and include anomalies such as a missing ac line cycle (can be partial), brownout, or high distortion levels. When a line fault occurs, the ADP1047/ADP1048 can be programmed to react according to the situation.

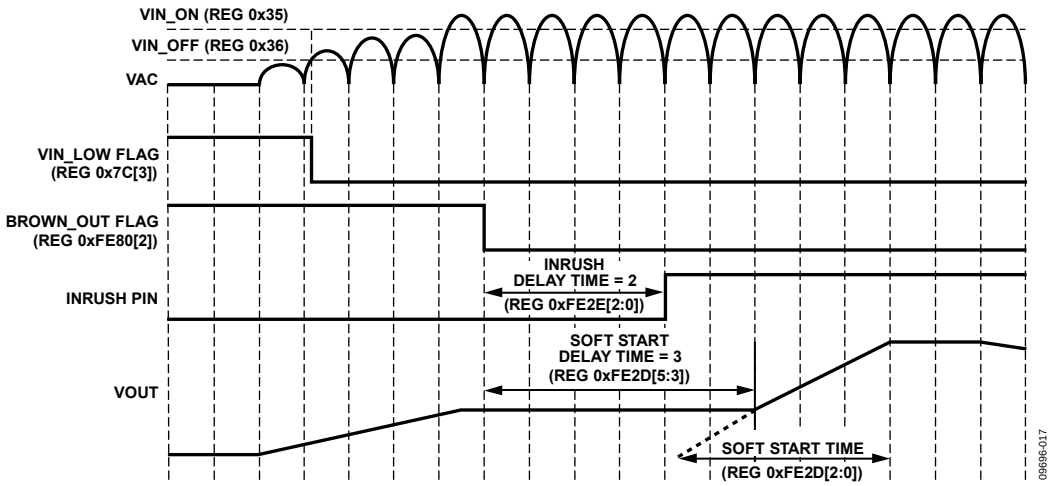


Figure 21. Soft Start and Inrush Current Control Timing

Missing AC Line Cycles

Figure 22 shows examples of the typical missing ac line cycles fault. The VIN_LOW flag is set when the instantaneous voltage is below VIN_OFF for more than a quarter or half line cycle (depending on how it is programmed). This flag can be used as an early warning to the system via the AC_OK pin when more than a half cycle is missing. The BROWN_OUT flag is also set; this flag does not cause a shutdown.

If any other flag that is programmed for shut down is set (in this example, VOUT_UV_FAULT), the power supply shuts down, the INRUSH pin is asserted, and the controller prepares for the next soft start cycle.

If the BROWN_OUT flag is cleared before VOUT drops below the VOUT_UV_FAULT_LIMIT value (Register 0x44), operation resumes in normal mode (or fast loop mode if enabled); otherwise, if VOUT drops below VOUT_UV_FAULT_LIMIT, the INRUSH pin is reset and a new soft start cycle is started.

PSON Delay

The PSON start delay is programmable using Register 0xFE06, Bits[3:2]. Four options are available: 0 ms, 50 ms, 250 ms, and 1000 ms.

Brownout Conditions

Brownout is another typical line fault condition in which the line drops below the minimum specified operating level. This level can be set with VIN_UV_FAULT_LIMIT (Register 0x59).

This flag can be programmed according to the standard PMBus flag response. For example, it can be programmed to shut down and restart after a certain delay.

During brownout, there are other conditions that can occur, such as input overcurrent or output undervoltage. Each of these faults can be programmed to shut down or disable the output, based on the response action.

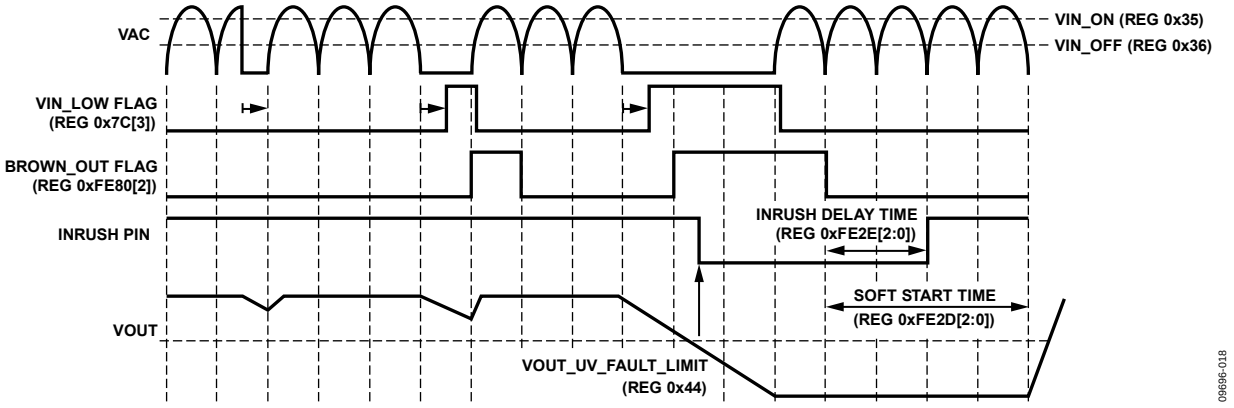


Figure 22. Line Fault (Missing Cycles) Timing Diagram

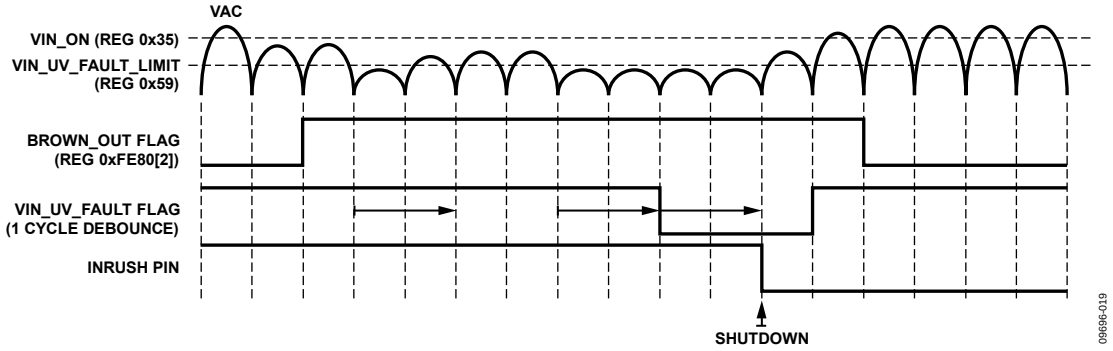


Figure 23. Brownout Timing Diagram (VIN_UV_FAULT_RESPONSE Register Programmed to Shut Down After a One-Cycle Debounce)

ADVANCED INPUT POWER METERING

The ADP1047/ADP1048 monitor and communicate critical information, including input and output voltage, input and output current, temperature, and efficiency. They also monitor and communicate OVP, UVP, OCP, OTP, and open-loop protection functions. An I^2C interface reads all these values and flags and programs their thresholds. The on-chip EEPROM can be used to store all of the settings for the thresholds.

True rms values are calculated at the end of each half ac line cycle by integrating the instantaneous values across each line cycle. These values have a resolution of 11 bits and are used to calculate the average, but are not available to be read through the PMBus interface.

The averaging window is programmable from zero full line cycles to 4096 full line cycles using Register 0xFE3A. At the end of each averaging period, the new value for average power is written to the READ_PIN register (Register 0x97) and is available to be read back through the interface until it is overwritten by the next averaged value at the end of the next averaging period.

For this reason, the polling frequency used to read average power through the PMBus interface must be equal to or higher than the averaging window to maintain data integrity. The averaging window is programmable over a wide range of times to accommodate different situations.

Input voltage, input current, output voltage, and input power are reported in linear format in the following registers:

- Input voltage: READ_VIN (Register 0x88)
- Input current: READ_IIN (Register 0x89)
- Output voltage: READ_VOUT (Register 0x8B)
- Input power: READ_PIN (Register 0x97)

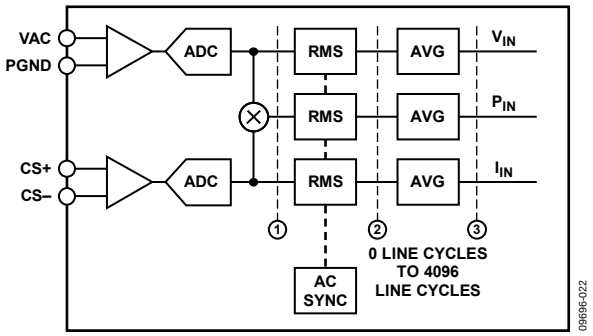


Figure 24. Block Diagram of Power Monitoring

Table 10. Data Format and Range for V_{IN}, I_{IN}, P_{IN}, and V_{OUT}

Metering Data	Mantissa (Bits)	Exponent (N)	Minimum Range	Minimum LSB	Maximum Range	Maximum LSB
V_{IN}	11	−3 to −1	256 V	0.125 V	1024 V	0.5 V
I_{IN}	11	−10 to −5	2 A	0.976 mA	64 A	0.03125 A
P_{IN}	11	−4 to +3	256 W	125 mW	32.8 kW	16 W
V_{OUT}	11	−3 to 0	256 V	0.125 V	2048 V	1 V

POWER SUPPLY SYSTEM AND FAULT MONITORING

The ADP1047/ADP1048 have extensive system and fault monitoring capabilities. The system monitoring functions include voltage, current, power, and temperature readings. The fault conditions include out of limit for current, voltage, power, and temperature. The limits for the fault conditions are programmable. An extensive set of flags is set when certain thresholds or limits are exceeded. These flags are described in Table 11 and Table 12.

FLAG CONVENTIONS

A flag indicates a fault condition; therefore, a flag is set (equal to 1, or high) when the fault or bad condition occurs. Good flags, such as POWER_GOOD# and AC_OK, are active low flags. For example, POWER_GOOD# = 1 indicates a problem.

Note that the signals relative to a flag are active high. For example, if the POWER_GOOD# flag is set to 1, the PGOOD pin is at Logic Level 0 because the POWER_GOOD# flag is inverted at the pin to provide active high signals.

MANUFACTURER-SPECIFIC FLAGS

The manufacturer-specific flags are flags that are not covered by the PMBus specification. Some flags simply indicate a condition (typically, warning flags). The response to some of the flags is individually programmable (typically, fault flags).

There is also a set of latched fault registers. These registers contain the same flags, but the flags remain set to allow users to detect an intermittent fault. Reading a latched register resets the flags in that register. The latched fault registers are Register 0xFE80, Register 0xFE81, and Register 0xFE82.

Table 11. Summary of Manufacturer-Specific Flags

Bit Name	Address	Description (1 = Flag Set)	Action
MAX_MODULATION	0xFE80[7]	The maximum modulation limit is reached.	
MIN_MODULATION	0xFE80[6]	The minimum modulation limit is reached.	
OLP	0xFE80[5]	Signals a difference of more than ~100 mV between the VFB and OVP signals (one of the two voltage dividers is probably disconnected or malfunctioning).	Programmable
FAST_OVP	0xFE80[4]	The threshold set for the comparator on the OVP pin has been crossed.	Programmable
AC_PERIOD	0xFE80[3]	The controller is not able to detect the ac line period; the maximum value of the period is used and this flag is set.	
BROWN_OUT	0xFE80[2]	VAC is lower than the value stored in VIN_ON (Register 0x35).	Can set AC_OK flag
SOFT_START	0xFE80[1]	The system is in soft start sequence; fast loop filter is in use.	
INRUSH	0xFE80[0]	INRUSH control relay is off.	INRUSH pin (can also set AC_OK flag)
EEPROM_UNLOCKED	0xFE81[6]	EEPROM is unlocked and its contents can be written.	
EEPROM_CRC	0xFE81[5]	The downloaded contents of the EEPROM are incorrect.	
I2C_ADDRESS	0xFE81[4]	The resistor on the ADD pin has a value that can cause an error in the address assignment (the address falls too close to the threshold between two addresses).	
LOW_LINE	0xFE81[3]	The input voltage is higher than the high line threshold.	Programmable
FAST_OCP	0xFE81[2]	The threshold set for the comparator on the ILIM pin has been crossed.	Programmable
SYNC_LOCK	0xFE81[1]	External synchronization frequency is locked.	
AC_OK	0xFE81[0]	The output of the AC_OK pin is low. (This flag is a programmable combination of other internal flags and refers to the condition of the input voltage.)	AC_OK pin
LOW_POWER	0xFE82[5]	The input power has dropped below the threshold for low power mode operation.	Programmable
FAST_LOOP	0xFE82[4]	The fast loop compensation filter is in use.	Can set POWER_GOOD# flag
VCORE_OV	0xFE82[3]	An overvoltage condition is present on the VCORE rail.	Programmable
VDD_3.3V_OV	0xFE82[2]	An overvoltage condition is present on the VDD rail.	Programmable
VDD_3.3V_UV	0xFE82[1]	An undervoltage condition is present on the VDD rail.	Shutdown

STANDARD PMBus FLAGS

When the corresponding bit of a standard PMBus flag is set in the STATUS_WORD or STATUS_BYTE register, the programmed action takes place as shown in Figure 25.

Figure 25 shows the bits in the six standard PMBus fault response registers: Register 0x41, Register 0x45, Register 0x50, Register 0x56, Register 0x5A, and Register 0x5C. All six PMBus fault response registers follow the same format. For more information, see the PMBus Fault Flag Response section.

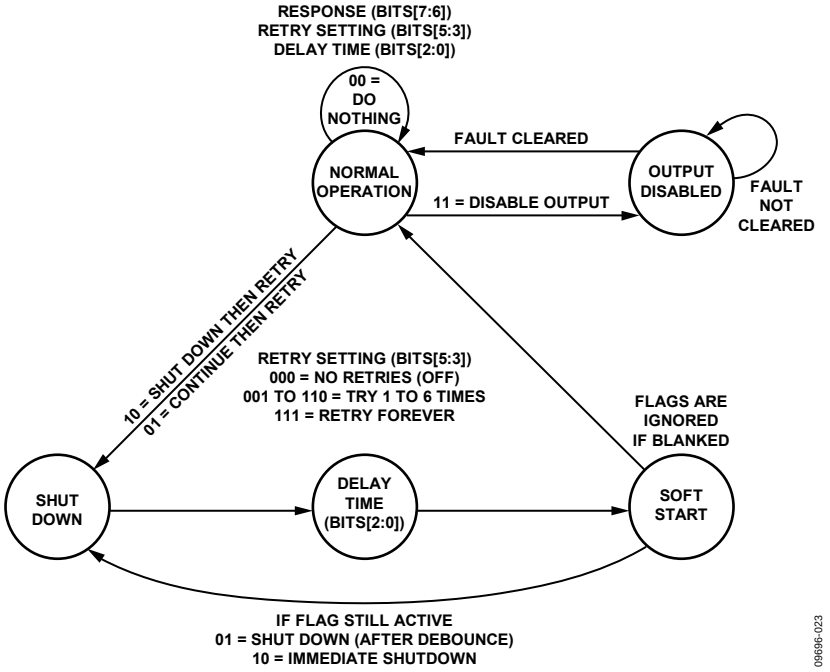


Figure 25. Standard PMBus Fault Response

Table 12. Summary of Standard PMBus Flags Implemented on the ADP1047/ADP1048

Name	Address	Description	Action
STATUS_BYTE (0x78)			
PSON_OFF	0x78[6]	Power supply on signal: this flag indicates that the PSON signal (hardware or software) is inactive.	
VOUT_OV	0x78[5]	General output overvoltage fault. This flag is a combination (OR) of any output overvoltage flag: Register 0x7A[7] and Register 0xFE80[4] (FAST_OVP).	Programmable
VIN_UV	0x78[3]	General input undervoltage fault (same data as in Register 0x7C[4]).	Programmable
TEMPERATURE	0x78[2]	Temperature fault or warning.	Programmable
CML	0x78[1]	Communications, memory, or logic fault.	
NONE_OF_THE_ABOVE	0x78[0]	A fault or warning not listed in Register 0x78[7:1].	
STATUS_WORD (0x79)			
VOUT	0x79[15]	Any fault or warning on the output voltage (overvoltage, undervoltage, fast OVP, or accurate OVP).	
INPUT	0x79[13]	Input voltage, input current, or input power fault or warning (same data as in Register 0x7C, Bits[7:0]).	
MFR	0x79[12]	Manufacturer-specific fault or warning (same data as in Register 0xFE80, Register 0xFE81, and Register 0xFE82).	
POWER_GOOD#	0x79[11]	Power good. This flag is a programmable combination of other internal flags and refers to the condition of the output voltage. This flag sets the PGOOD pin. The POWER_GOOD# flag is an inverted version of the PGOOD pin.	PGOOD pin
UNKNOWN	0x79[8]	A fault or warning not listed in Bits[15:1].	

Name	Address	Description	Action
STATUS_VOUT (0x7A)			
VOUT_OV_FAULT	0x7A[7]	The output voltage is above the VOUT_OV_FAULT_LIMIT.	Programmable
VOUT_OV_WARN	0x7A[6]	The output voltage is above the VOUT_OV_WARN_LIMIT.	
VOUT_UV_WARN	0x7A[5]	The output voltage is below the VOUT_UV_WARN_LIMIT.	
VOUT_UV_FAULT	0x7A[4]	The output voltage is below the VOUT_UV_FAULT_LIMIT.	Programmable
STATUS_INPUT (0x7C)			
VIN_OV_FAULT	0x7C[7]	The input voltage on VAC is larger than the value in VIN_OV_FAULT_LIMIT.	Programmable
VIN_UV_WARN	0x7C[5]	The input voltage on VAC is smaller than the value in VIN_UV_WARN_LIMIT.	
VIN_UV_FAULT	0x7C[4]	The input voltage on VAC is smaller than the value in VIN_UV_FAULT_LIMIT.	Programmable
VIN_LOW	0x7C[3]	VAC is lower than VIN_OFF. This signal shuts down the power supply.	Can set AC_OK flag
IIN_OC_FAULT	0x7C[2]	The input current measured on the CS ADC is larger than the value in IIN_OC_FAULT_LIMIT.	Programmable
IIN_OC_WARN	0x7C[1]	The input current measured on the CS ADC is larger than the value in IIN_OC_WARN_LIMIT.	Can set AC_OK flag
PIN_OP_WARN	0x7C[0]	Input overpower warning.	
STATUS_TEMPERATURE (0x7D)			
OT_FAULT	0x7D[7]	The measured temperature is above the value set in OT_FAULT_LIMIT.	Programmable
OT_WARN	0x7D[6]	The measured temperature is above the value set in OT_WARN_LIMIT.	

PMBus FAULT FLAG RESPONSE

All standard PMBus fault response registers follow the same format. The six standard PMBus fault response registers are

- VOUT_OV_FAULT_RESPONSE (Register 0x41)
- VOUT_UV_FAULT_RESPONSE (Register 0x45)
- OT_FAULT_RESPONSE (Register 0x50)
- VIN_OV_FAULT_RESPONSE (Register 0x56)
- VIN_UV_FAULT_RESPONSE (Register 0x5A)
- IIN_OC_FAULT_RESPONSE (Register 0x5C)

The standard PMBus fault response registers are composed of eight bits: Bits[7:6] define the response type, Bits[5:3] define the retry settings, and Bits[2:0] contain the delay information.

Bits[7:6] define the response type as follows:

- Bits[7:6] = 00 (ignore). When the corresponding fault flag is set, no action is taken and the power supply continues to operate normally.
- Bits[7:6] = 01 or 10 (shutdown and retry). When the corresponding fault flag is set, the system shuts down and then retries for the number of times programmed in Bits[5:3]. The difference between the 01 and 10 options is that when Bits[7:6] = 01, a debounce (programmed in Bits[2:0]) is applied to the flag.
- Bits[7:6] = 11 (disable output). When the corresponding fault flag is set, the system does not enter a shutdown/soft start sequence. Instead, the output is disabled indefinitely until the flag is cleared. Care must be taken when selecting this option because it may cause the system to stall in an endless loop.

Concurrent Faults

When multiple faults occur at the same time, the state machine executes the response that has the highest priority. Flag priority is determined by the response of the faults as determined by Bits[7:6]. The higher the number in these two bits, the higher the priority.

For example, if OVP is programmed to disable the output (Bits[7:6] = 11) and OCP is programmed to shut down and retry after a delay (Bits[7:6] = 01), and both faults occur at the same time, the OVP action is executed first. If the OVP condition is cleared and the OCP flag is still set, the programmed action for OCP is executed.

If two or more faults occur at the same time and all the faults have the same response priority, the fault with the smallest retry setting takes priority. For example, if one fault has a retry setting programmed to 011 and the other has a retry setting of 001, the lower number of retries is executed.

MANUFACTURER-SPECIFIC FLAG RESPONSE

Manufacturer-specific flags follow a different response from the standard PMBus flags because these flags are much faster and, in some cases, operate on a pulse-by-pulse basis.

FAST OCP Flag Response (Register 0xFE00)

The fast OCP flag responds to an overcurrent condition that occurs on the comparator connected to the ILIM pin. This comparator performs a pulse-by-pulse current limiting function (see the Fast Overcurrent Protection (ILIM Pin) section).

Four different actions can be programmed for this flag using Bits[7:6]. Regardless of the programmed flag response, the PWM pulse is always terminated when the threshold programmed for the comparator is crossed.

- 00 (ignore, do nothing). No action is taken. The PWM pulses are still terminated as long as the OCP condition persists.
- 01 (shut down and soft start). The power supply is shut down, and a soft start sequence is initiated after the delay that is programmed in the IIN_OC_FAULT_RESPONSE register (Register 0x5C, Bits[2:0]).
- 10 (shutdown and wait for PSON). After the number of switching cycles programmed in Bits[5:4], the power supply is shut down until the PSON signal is received.
- 11 (disable the PWM until the flag is cleared). After the number of switching cycles programmed in Bits[5:4], the PWM is disabled until the flag is cleared; no soft start is initiated.

FAST OVP Flag Response (Register 0xFE01)

The fast OVP flag responds to an overvoltage condition on the programmable comparator connected to the OVP pin. This comparator constantly monitors the output voltage and its operation (see the Fast Overvoltage Protection (OVP Pin) section).

Four different actions can be programmed for this flag.

- 00 (ignore, do nothing). No action is taken.
- 01 (shut down and soft start). The power supply is shut down, and a soft start sequence is initiated after the delay programmed in the VOUT_OV_FAULT_RESPONSE register (Register 0x41, Bits[2:0]).
- 10 (immediate shutdown and wait for PSON). The power supply is shut down until the PSON signal is received.
- 11 (disable the PWM until the flag is cleared). The PWM is disabled until the flag is cleared; no soft start is done.

OLP Flag Response (Register 0xFE02)

The OLP flag responds to differences between the OVP and VFB pins. Open-loop protection detects a difference in voltage in excess of ~100 mV, which equates to approximately 6.6% of the full-scale range (see the Open-Loop Protection section).

Four different actions can be programmed for this flag.

- 00 (ignore, do nothing). No action is taken.
- 01 (shut down and soft start). The power supply is shut down, and a soft start sequence is initiated after the delay programmed in the VOUT_OV_FAULT_RESPONSE register (Register 0x41, Bits[2:0]).
- 10 (immediate shutdown and wait for PSON). The power supply is shut down until the PSON signal is received.
- 11 (disable the PWM until the flag is cleared). The PWM is disabled until the flag is cleared; no soft start is done.

VDD and VCORE OV Flag Response (Register 0xFE03 and Register 0xFE04)

These two flags respond to an overvoltage condition on the VDD (3.3 V) and VCORE (2.5 V) rails. These rails must be properly decoupled and filtered to guarantee proper operation of the digital controller. The controller can be programmed to ignore the flags or to shut down and restart. A debounce time of 2.56 µs or 660 µs can be set.

The controller can also be instructed to reload the contents of the EEPROM upon restart or to resume operation without reloading the EEPROM contents. Reloading the contents of the EEPROM to RAM prevents device malfunction if the RAM contents have been corrupted during the overvoltage condition.

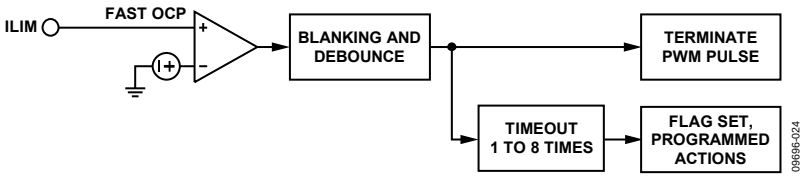


Figure 26. Fast OCP Flag

MONITORING FUNCTIONS

Voltage, current, power, and temperature measurements are taken by the ADP1047/ADP1048. These values are stored in the following registers and can be read through the PMBus interface.

- Input voltage measurement (Register 0x88)
- Output voltage measurement (Register 0x8B)
- Input current measurement (Register 0x89)
- Input power measurement (Register 0x97)
- Temperature measurement (Register 0xFE86)

FIRST ERROR FAULT

The ADP1047/ADP1048 provide a FLAG_FAULT_ID register (Register 0xFE07) that records the first fault that causes a system shutdown. For example, if the overtemperature (OT) fault causes the system to shut down, the OT_FAULT flag (0011) is stored in the FLAG_ FAULT_ID register (Register 0xFE07, Bits[3:0]). In addition, the flag ID of the fault that occurred before the fault that caused the system shutdown is included in Bits[7:4] of Register 0xFE07.

The contents of this register are stored until read by the user. The flag ID is also saved in EEPROM when the shutdown occurs. In this way, it is possible to determine the cause of a shutdown in case of system failure.

OVERTEMPERATURE PROTECTION (OTP)

If the temperature sensed at the RTD pin exceeds the programmable fault threshold, the OTP flag is set, and the power supply can be programmed to shut down. A PTC or NTC thermistor can be used.

To set the fault and warning thresholds for OTP, program Register 0xFE19 and Register 0xFE1A, respectively. To set the temperature hysteresis for the fault and warning thresholds, program Register 0xFE3F. The response to an OTP fault flag is programmable in Register 0x50.

AC_OK AND PGOOD SIGNALS

The ADP1047/ADP1048 have two digital status pins: AC_OK and PGOOD. Both signals represent an OR function for a programmable list of internal flags. Users can blank some of these flags to tailor the AC_OK and PGOOD signals to their needs using Register 0xFE0B and Register 0xFE0A, respectively. When the signals on the AC_OK and PGOOD pins are set, the corresponding internal flag is also set.

The programmable delay block acts like a debounce. That is, the signal must be active for at least the duration of the programmed delay before the flag is set. The debounce times for the AC_OK and PGOOD pins can be programmed separately in Register 0xFE05.

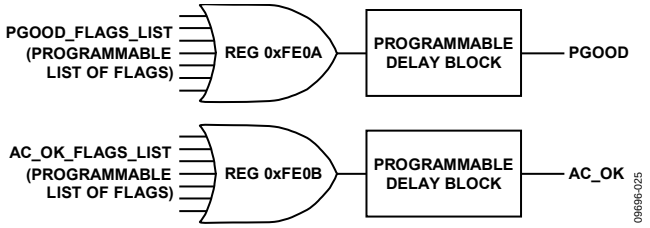


Figure 27. AC_OK and PGOOD Signals

Table 13. Flags Available to Program the AC_OK and PGOOD Pins

AC_OK_FLAGS_LIST (Register 0xFE0B)[1]	PGOOD_FLAGS_LIST (Register 0xFE0A)[1]
VIN_LOW (always checked)	VOUT_OV_FAULT (always checked)
VIN_UV_FAULT (Bit 7)	VOUT_UV_FAULT (Bit 7)
VIN_UV_WARN (Bit 6)	VOUT_OV_WARN (Bit 6)
IIN_OC_FAULT (Bit 5)	FAST_OVP (Bit 5)
IIN_OC_WARN (Bit 4)	OLP (Bit 4)
FAST_OCP (Bit 3)	FAST_OCP (Bit 3)
AC_LINE_PERIOD (Bit 2)	IIN_OC_FAULT (Bit 2)
BROWN_OUT (Bit 1)	OT_FAULT (Bit 1)
INRUSH (Bit 0)	FAST_LOOP (Bit 0)

[1] To blank one or more flags so that the AC_OK or PGOOD pin ignores it, set the corresponding bit to 1 in Register 0xFE0A or Register 0xFE0B.

ADVANCED FEATURES

The advanced features of the ADP1047/ADP1048 include

- Frequency dithering for EMI noise minimization
- PWM frequency synchronization with external source
- Smart output voltage: real-time efficiency optimization by changing the output voltage based on ac line and output power
- Smart switching frequency: real-time efficiency optimization by changing the switching frequency
- Current loop filter for light load: real-time THD optimization at light load conditions
- Phase shedding (ADP1048 only): real-time efficiency optimization by shutting down one phase
- Current loop feedforward: power factor and THD optimization at light load conditions
- Bridgeless boost operation (ADP1048 only)

All advanced features other than bridgeless boost operation are enabled by setting the appropriate bit in Register 0xFE4F.

FREQUENCY DITHERING (SPREAD SPECTRUM)

The PWM signal can be altered digitally to optimize for EMI reduction (see Figure 28). For a wider but lower EMI spectrum, the switching frequency varies with the rectified line voltage. The switching cycle changes linearly with time from 87.5% to 112.5% of the nominal value, resulting in a frequency variation of 114% to 89% of the nominal value.

To enable frequency dithering, set Register 0xFE4F, Bit 0, to 1. To configure the dithering period, program Register 0xFE1D.

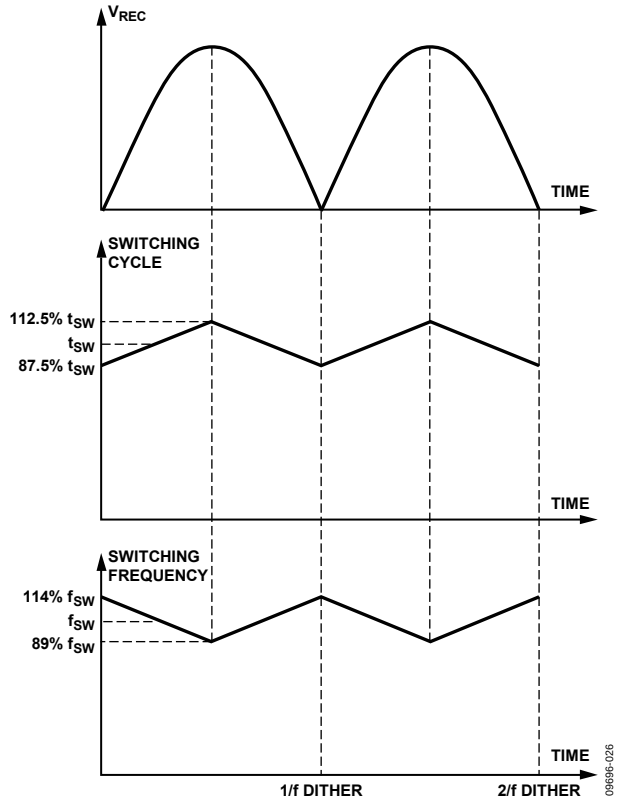


Figure 28. Switching Frequency Dithering Control

PWM FREQUENCY SYNCHRONIZATION

The part can synchronize the internal PWM clock with an external clock frequency; the external source must be within the minimum and maximum synchronization range programmed in the part. To enable PWM frequency synchronization, set Register 0xFE4F, Bit 1, to 1.

The capture range for the SYNC period is 87.5% to 112.5% of the programmed switching period. The switching frequency synchronized to the SYNC pin is limited by the frequency set in Register 0xFE1B. The maximum range for the synchronized frequency is from 89% to 114% of the programmed switching frequency. The delay between the external SYNC signal and the start of the internal switching cycle can be programmed using Register 0xFE4C.

The part synchronizes to the external clock frequency as follows:

1. The part attempts to determine the external clock period, averaging it over seven cycles (frequency capture mode).
2. After the period of the SYNC signal is determined, the internal PWM clock is adjusted until the phase is also aligned. At that point, internal and external clocks are synchronized (phase capture mode).
3. Each internal switching cycle is terminated after the SYNC rising edge is detected (pulse-by-pulse synchronization).

If the external SYNC signal is lost at any time or if the period exceeds the minimum/maximum limit, the internal clock goes back to the maximum period set in Register 0xFE1B.

During the soft start phase, the SYNC pin is ignored and the clock frequency is not synchronized.

Interleaved operation of a multiphase PFC circuit is realized by using the SYNC pin of several ADP1047/ADP1048 controllers.

The frequency synchronization feature is optional. When enabled, the switching frequency can be programmed to 1, 1/2, 1/3, or 1/4 of the SYNC frequency using Register 0xFE1E.

SMART OUTPUT VOLTAGE (LOAD LINE)

To achieve higher efficiency, the output voltage can be programmed according to the load power and input voltage condition (see Figure 29). To enable the smart output voltage feature, set Register 0xFE4F, Bit 2, to 1.

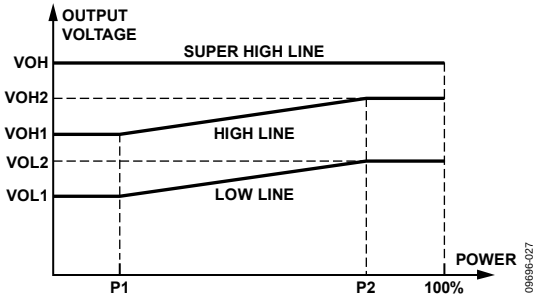


Figure 29. Smart Output Voltage Control (Load Line)

Three load lines address super high line, high line, and low line input voltage conditions.

When the rms value of the input voltage is higher than the super high line input (for example, 250 V), the load line is flat, that is, the output voltage remains at VOH, which is independent of the power. To avoid output voltage oscillation when the input voltage is around the super high line level, voltage hysteresis can be programmed using Register 0xFE4D. It is recommended that at least 16 V of hysteresis be programmed.

When the rms value of the input voltage is lower than the super high line input but higher than the high line threshold, there is a load line between P1 and P2 in terms of power. The output voltage varies between VOH1 and VOH2 as a linear function of the output power when the output power falls within the range between P1 and P2. The power levels of P1 and P2 are programmable using Register 0xFE44 and Register 0xFE45, respectively. When the power is below P1, the output voltage remains unchanged at VOH1. When the power is higher than P2, the output voltage remains unchanged at VOH2.

The bottom load line in Figure 29 applies when the rms value of the input voltage is lower than the low line threshold. The output voltage varies between VOL1 and VOL2 as a linear function of the output power when the output power falls within the range between P1 and P2. When the power is below P1, the output voltage remains unchanged at VOL1. When the power is higher than P2, the output voltage remains unchanged at VOL2.

The user can program values for VOH, VOH2, VOH1, VOL2, and VOL1 using Register 0xFE4A, Register 0xFE49, Register 0xFE48, Register 0xFE47, and Register 0xFE46, respectively.

SMART SWITCHING FREQUENCY

For higher efficiency, the switching frequency of the ADP1047/ADP1048 can be programmed according to the load power condition (see Figure 30). To enable the smart switching frequency feature, set Register 0xFE4F, Bit 3, to 1.

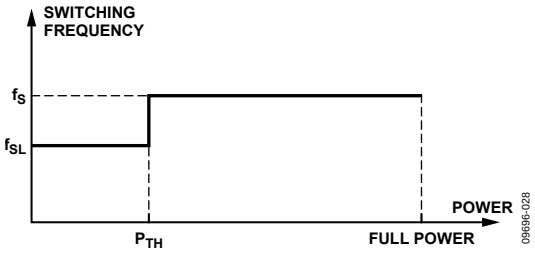


Figure 30. Smart Switching Frequency Control

The smart switching frequency feature uses two different switching frequencies for heavy load and light load conditions. When the output power is lower than the low power threshold, P_{TH}, the PFC circuit switches at the f_{SL} frequency. When the output power is higher than P_{TH} plus power hysteresis, the circuit switches at the normal set frequency, f_S.

Hysteresis can be programmed in Register 0xFE4E. The user can program the values for f_{SL} and P_{TH} in Register 0xFE1C and Register 0xFE32, respectively.

CURRENT LOOP FILTER FOR LIGHT LOAD

To achieve low THD under light load conditions, the ADP1047/ADP1048 offer current loop filter presets for light load operation under both high line input and low line input (see Figure 31). To enable the current loop filter for light load feature, set Register 0xFE4F, Bit 5, to 1.

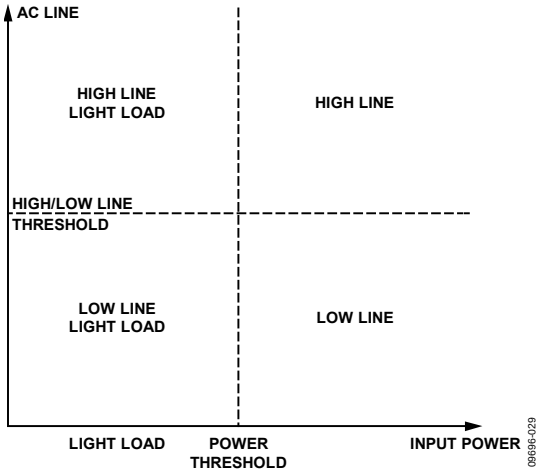


Figure 31. Current Loop Filter at Light Load Condition

When the input power drops below the low power threshold, P_{TH} (set in Register 0xFE32), the current loop filter switches to the light load filter after four full line cycles. When the input power goes above P_{TH} plus the programmed hysteresis, the current loop filter switches back to the normal mode filter immediately. This applies to both high line and low line input.

PHASE SHEDDING (ADP1048 ONLY)

To achieve high efficiency at light load, the ADP1048 can shut down one PWM output under light load conditions. When the input power drops below the low power threshold, P_{TH} (set in Register 0xFE32), one PWM output is disabled. When the input power goes above the low power threshold plus power hysteresis (set in Register 0xFE4E), the PWM resumes operation. To enable phase shedding for the ADP1048, set Register 0xFE4F, Bit 4, to 1.

CURRENT LOOP FEEDFORWARD

Current loop feedforward is implemented in the ADP1047/ADP1048 to improve the power factor and reduce THD under light load conditions (see Figure 32). To enable current loop feedforward, set Register 0xFE4F, Bit 6, to 1.

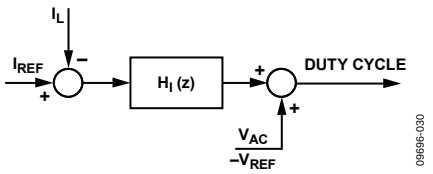


Figure 32. Current Loop Feedforward

BRIDGELESS BOOST OPERATION (ADP1048 ONLY)

The bridgeless boost configuration allows removal of the conduction losses caused by the input bridge of the PFC converter. In this configuration, it is necessary to drive the two power MOSFETs separately to achieve the highest efficiency. The ADP1048 can provide such signals. The IBAL pin is used to detect the ac line phase and zero crossings. Note that the maximum rating on the IBAL pin is VDD + 0.3 V; therefore, a clamp circuit must be connected to the IBAL pin.

During the positive ac line phase, only one boost stage is effectively working. The second one is passive, and the current flows in Q2 from the source to the drain. Turning the Q2 FET fully on during this phase allows conduction losses in Q2 to be minimized.

When the ac line phase becomes negative, the roles of Q1 and Q2 are reversed, and Q2 actively switches while Q1 is always on. The phase information is detected from the ac line via the IBAL pin.

During the soft start phase, both FETs are switching as a precautionary measure; the same happens when the phase information on the IBAL pin becomes corrupted or inaccurate.

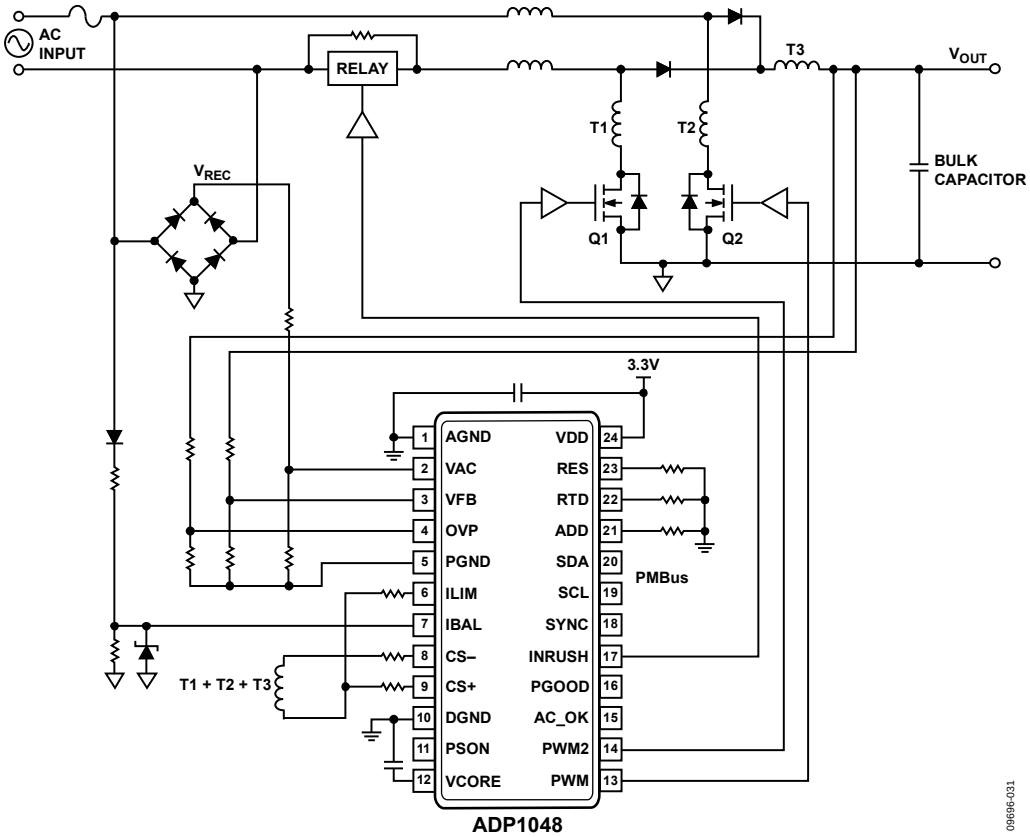


Figure 33. Schematic of Bridgeless PFC Circuit with the ADP1048

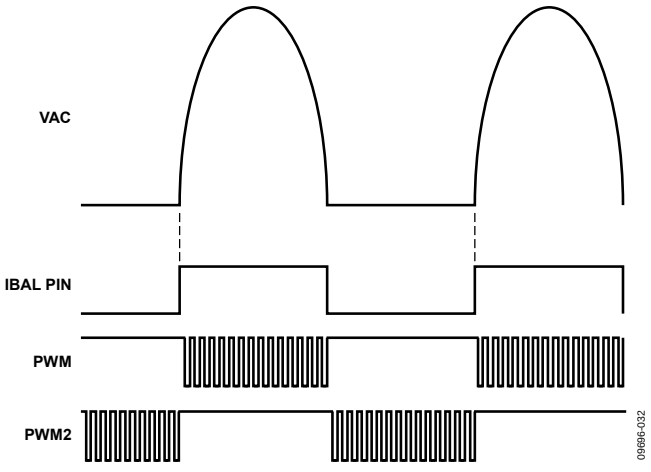


Figure 34. Bridgeless Boost Operation

POWER SUPPLY SYSTEM CALIBRATION AND TRIM

The ADP1047/ADP1048 allow the entire power supply to be calibrated and trimmed digitally in the production environment. The device can calibrate items including the output voltage, input voltage, input current, and input power, and it can trim for tolerance errors introduced by sense resistors, current transformers, and resistor dividers, as well as for its own internal circuitry.

The part comes factory trimmed at 90% of the input range at a 3.3 V supply, but it can be re-trimmed by the user to compensate for the errors introduced by external components. With the exception of the gain and offset trim registers for input power, the trim registers must be unlocked for write access. To unlock the trim registers, write to the TRIM_PASSWORD register (Register 0xD6).

OUTPUT VOLTAGE (VFB) CALIBRATION AND TRIM

The voltage sense inputs are optimized for sensing signals at 90% of the input range and cannot sense signals greater than 1.6 V. In a high voltage system, a resistor divider is required to reduce the high voltage signal to below 1.6 V. It is recommended that the high voltage signal be reduced to 1 V for best performance. The resistor divider can introduce errors, which must be trimmed out as follows:

1. Turn on the power supply with no load attached.

   The output voltage is divided down by the feedback resistor divider to supply 1 V across the VFB and AGND pins.
2. Use a calibrated multimeter to perform the output voltage reading.
3. Adjust the VFB ADC gain trim register (Register 0xFE41) until the power supply outputs the exact value in the READ_VOUT register (Register 0x8B).

INPUT VOLTAGE (VAC) GAIN AND OFFSET TRIM

The input voltage sense point on the power rail requires an external resistor divider to bring the signal within the operating input range of the VAC ADC (0 V to 1.6 V). The resistor divider can introduce errors, which must be trimmed out as follows:

1. Apply the maximum line voltage value to the input of the power supply.

   The VAC resistor divider divides this voltage down at the VAC pin. The VAC resistor divider is programmed in linear format using the VIN scale monitor register (Register 0xFE3B).
2. Adjust the VAC ADC gain trim register (Register 0xFE40) until the VAC value (Register 0x88, READ_VIN) equals the input voltage reading from a calibrated multimeter. This step trims for errors in the resistor divider network.

For VAC offset trim, adjust the value in Register 0xFE53.

CURRENT SENSE GAIN AND OFFSET TRIM

The current sense can be calibrated digitally to remove any errors due to external components.

1. Apply the maximum load to the output with the low line input voltage.
2. To match the input current reading at the maximum nominal input current, adjust the CS ADC gain trim register until the CS value (Register 0x89, READ_IIN) equals the measured result of the input current from calibrated equipment.

   If the 500 mV input range is used, adjust Register 0xFE42. If the 750 mV range is used, adjust Register 0xFE7E.

For CS offset trim, adjust the values in Register 0xFE54 (500 mV input range) or Register 0xFE7F (750 mV input range).

INPUT POWER GAIN AND OFFSET TRIM

The input power trim has separate trim registers for high line and low line input.

1. Apply the maximum load to the output with the low line input voltage.
2. Adjust the power metering gain trim for low line input register (Register 0xFE34) until the input power value in the READ_PIN register (Register 0x97) equals the measured result of the input power from calibrated equipment.
3. Apply the maximum load to the output with the high line input voltage.
4. Adjust the power metering gain trim for high line input register (Register 0xFE8F) until the input power value in the READ_PIN register (Register 0x97) equals the measured result of the input power from the calibrated equipment.

For input power offset trim, adjust the values in Register 0xFE33 (for low line input) and Register 0xFE8E (for high line input).

PMBus DIGITAL COMMUNICATION

The PMBus slave allows a device to interface to a PMBus-compliant master device as specified by the *PMBus Power System Management Protocol Specification* (Revision 1.1, February 5, 2007). The PMBus slave is a 2-wire interface that can be used to communicate with other PMBus-compliant devices and is compatible in a multimaster, multislave bus configuration.

FEATURES

The function of the PMBus slave is to decode the command sent from the master device and respond as requested. Communication is established using an I²C-like 2-wire interface with a clock line (SCL) and data line (SDA). The PMBus slave is designed to externally move chunks of 8-bit data (bytes) while maintaining compliance with the PMBus protocol. The PMBus protocol is based on the *SMBus Specification* (Version 2.0, August 2000). The SMBus specification is, in turn, based on the Philips *I²C Bus Specification* (Version 2.1, January 2000). The PMBus incorporates the following features:

- Slave operation on multiple device systems
- 7-bit addressing
- 100 kHz and 400 kHz data rates
- General call address support
- Support for clock low extension
- Separate multiple byte receive and transmit FIFO
- Extensive fault monitoring

OVERVIEW

The PMBus slave module is a 2-wire interface that can be used to communicate with other PMBus-compliant devices. Its transfer protocol is based on the Philips I²C transfer mechanism. The ADP1047/ADP1048 are always configured as slave devices in the overall system. The ADP1047/ADP1048 communicate with the master device using one data pin (SDA) and one clock pin (SCL). Because the ADP1047/ADP1048 are slave devices, they cannot generate the clock signal. However, they are capable of clock-stretching the SCL line to put the master device in a wait state when they are not ready to respond to the master's request.

Communication is initiated when the master device sends a command to the PMBus slave device. Commands can be read or write commands, in which case, data is transferred between the devices in a byte wide format. Commands can also be send commands, in which case, the command is executed by the slave device upon receiving the stop bit. The stop bit is the last bit in a complete data transfer, as defined in the PMBus/I²C communication protocol. During communication, the master and slave devices send acknowledge (A) or no acknowledge ($\overline{A}$) bits as a method of handshaking between devices. See the PMBus specification for a more detailed description of the communication protocol.

When communicating with the master device, it is possible for illegal or corrupted data to be received by the PMBus slave device. In this case, the PMBus slave device should respond to the invalid command or data, as defined by the PMBus specification, and indicate to the master device that an error or fault condition has occurred. This method of handshaking can be used as a first level of defense against programming of the slave device that can potentially damage the chip or system.

The PMBus specification defines a set of generic PMBus commands that is recommended for a power management system. However, each PMBus device manufacturer can choose to implement and support certain commands as it deems fit for its system. In addition, the PMBus device manufacturer can choose to implement manufacturer-specific commands whose functions are not included in the generic PMBus command set. The list of standard PMBus and manufacturer-specific commands can be found in the Standard PMBus Commands Supported by the ADP1047/ADP1048 section and the Manufacturer-Specific PMBus Command section.

PMBus ADDRESS

Control of the ADP1047/ADP1048 is implemented via the I²C interface. The ADP1047/ADP1048 are connected to the bus as slave devices under the control of a master device.

The PMBus address of the ADP1047/ADP1048 is set by connecting an external resistor from the ADD pin to ground. Table 14 lists the recommended resistor values and associated PMBus addresses. Eight different addresses can be used.

Table 14. PMBus Address Settings

Address	ADD Pin Resistor Value (kΩ)
0x58	10 (or connect directly to AGND)
0x59	30
0x5A	50
0x5B	69
0x5C	89
0x5D	109
0x5E	128
0x5F	148 (or connect directly to VDD)

If an incorrect resistor value is used and the resulting I²C address is close to a threshold between two addresses, the I2C_ADDRESS flag is set (Bit 4 of Register 0xFE81). The recommended resistor values in Table 14 can vary by ±2 kΩ. Therefore, it is recommended that 1% tolerance resistors be used on the ADD pin.

The part responds to the standard PMBus broadcast address (general call) of 0x00.

DATA TRANSFER

Format Overview

The PMBus slave follows the transfer protocol of the SMBus specification, which is based on the fundamental transfer protocol format of the Philips *I²C Bus Specification*, dated January 2000. Data transfers are byte wide, lower byte first. Each byte is transmitted serially, most significant bit (MSB) first. A typical transfer is diagrammed in Figure 35. See the SMBus and I²C specifications for an in-depth discussion of the transfer protocols.

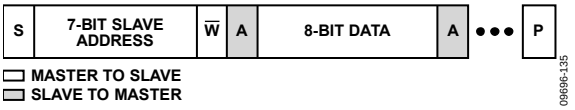


Figure 35. Basic Data Transfer

Figure 35 through Figure 42 use the following abbreviations:

S = start condition
Sr = repeated start condition
P = stop condition
R = read bit
$\overline{W}$ = write bit
A = acknowledge bit (0)
$\overline{A}$ = acknowledge bit (1)

"A" represents the ACK (acknowledge) bit. The ACK bit is typically active low (Logic 0) if the transmitted byte is successfully received by a device. However, when the receiving device is the bus master, the acknowledge bit for the last byte read is a Logic 1, indicated by $\overline{A}$.

Command Overview

Data transfer using the PMBus slave is established using PMBus commands. The PMBus specification requires that all PMBus commands start with a slave address with the R/$\overline{W}$ bit cleared (set to 0), followed by the command code. All PMBus commands supported by the ADP1047/ADP1048 follow one of the protocol types shown in Figure 36 through Figure 42.

The PMBus slave module also supports manufacturer-specific extended commands. These commands follow the same protocol as the standard PMBus commands. However, the command code consists of the following two bytes:

- The command code extension, 0xFE
- The extended command code, 0x00 to 0xFF

Using the manufacturer-specific extended commands, the PMBus device manufacturer can add an additional 256 manufacturer-specific commands to its PMBus command set.

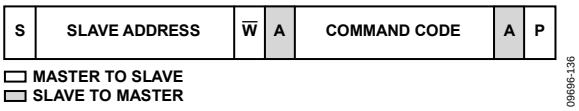


Figure 36. Send Byte Protocol

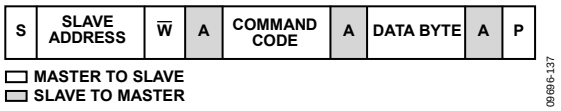


Figure 37. Write Byte Protocol

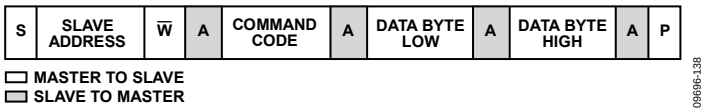


Figure 38. Write Word Protocol

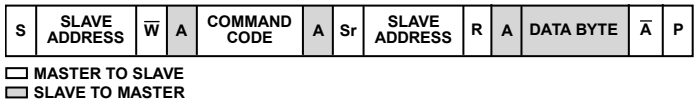


Figure 39. Read Byte Protocol

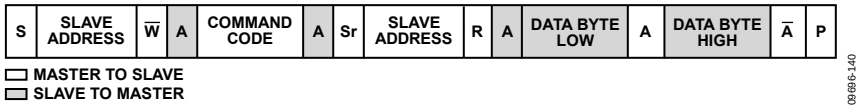


Figure 40. Read Word Protocol

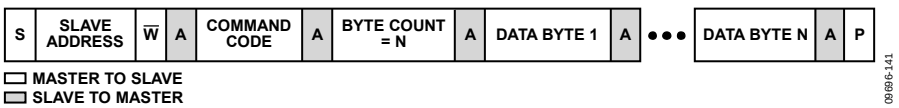


Figure 41. Block Write Protocol

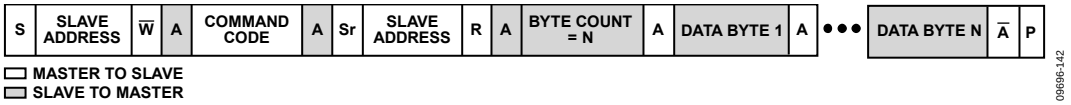


Figure 42. Block Read Protocol

Clock Generation and Stretching

The ADP1047/ADP1048 are always PMBus slave devices in the overall system; therefore, the device never needs to generate the clock, which is done by the master device in the system. However, the PMBus slave device is capable of clock stretching to put the master in a wait state. By stretching the SCL signal during the low period, the slave device communicates to the master device that it is not ready and that the master device must wait.

Conditions where the PMBus slave device stretches the SCL line low include the following:

- The master device is transmitting at a higher baud rate than the slave device.
- The receive buffer of the slave device is full and must be read before continuing. This prevents a data overflow condition.
- The slave device is not ready to send data that the master has requested.

Note that the slave device can stretch the SCL line only during the low period. Also, whereas the I²C specification allows indefinite stretching of the SCL line, the PMBus specification limits the maximum time that the SCL line can be stretched, or held low, to 25 ms, after which the device must release the communication lines and reset its state machine.

GENERAL CALL SUPPORT

The PMBus slave is capable of decoding and acknowledging a general call address. The PMBus device responds to both its own address and the general call address (0x00). The general call address enables all devices on the PMBus to be written to simultaneously.

Note that all PMBus commands must start with the slave address with the R/$\overline{W}$ bit cleared (set to 0), followed by the command code. This is also true when using the general call address to communicate with the PMBus slave device.

FAST MODE

Fast mode (400 kHz) uses essentially the same mechanics as the standard mode of operation; the electrical specifications and timing are most affected. The PMBus slave is capable of communicating with a master device operating in standard mode (100 kHz) or fast mode.

FAULT CONDITIONS

The PMBus protocol provides a comprehensive set of fault conditions that must be monitored and reported. These fault conditions can be grouped into two major categories: communication faults and monitoring faults.

Communication faults are error conditions associated with the data transfer mechanism of the PMBus protocol. Monitoring faults are error conditions associated with the operation of the PMBus device, such as output overvoltage protection, and are specific to each PMBus device. These fault conditions are described in the Power Supply System and Fault Monitoring section.

TIMEOUT CONDITION

A timeout condition occurs if any single SCL clock pulse is held low for longer than the $t_{TIMEOUT}$ of 25 ms (min). Upon detecting the timeout condition, the PMBus slave device has 10 ms to abort the transfer, release the bus lines, and be ready to accept a new start condition. The device initiating the timeout is required to hold the SCL clock line low for at least $t_{TIMEOUT\ MAX}$ = 35 ms, guaranteeing that the slave device is given enough time to reset its communication protocol.

DATA TRANSMISSION FAULTS

Data transmission faults occur when two communicating devices violate the PMBus communication protocol, as specified in the PMBus specification. See the PMBus specification for more information about each fault condition.

Corrupted Data, PEC (Item 10.8.1)

Parity error checking. Not supported.

Sending Too Few Bits (Item 10.8.2)

Transmission is interrupted by a start or stop condition before a complete byte (eight bits) has been sent. Not supported; any transmitted data is ignored.

Reading Too Few Bits (Item 10.8.3)

Transmission is interrupted by a start or stop condition before a complete byte (eight bits) has been read. Not supported; any received data is ignored.

Host Sends or Reads Too Few Bytes (Item 10.8.4)

If a host ends a packet with a stop condition before the required bytes are sent/received, it is assumed that the host intended to stop the transfer. Therefore, the PMBus does not consider this to be an error and takes no action, except to flush any remaining bytes in the transmit FIFO.

Host Sends Too Many Bytes (Item 10.8.5)

If a host sends more bytes than are expected for the corresponding command, the PMBus slave considers this a data transmission fault and responds as follows:

- NACKs all unexpected bytes as they are received
- Flushes and ignores the received command and data
- Sets the CML bit in the STATUS_BYTE register

Host Reads Too Many Bytes (Item 10.8.6)

If a host reads more bytes than are expected for the corresponding command, the PMBus slave considers this a data transmission fault and responds as follows:

- Sends all 1s (0xFF) as long as the host continues to request data
- Sets the CML bit in the STATUS_BYTE register

Device Busy (Item 10.8.7)

The PMBus slave device is too busy to respond to a request from the master device. Not supported.

DATA CONTENT FAULTS

Data content faults occur when data transmission is successful, but the PMBus slave device cannot process the data that is received from the master device.

Improperly Set Read Bit in the Address Byte (Item 10.9.1)

All PMBus commands start with a slave address with the R/$\overline{W}$ bit cleared (set to 0), followed by the command code. If a host starts a PMBus transaction with R/$\overline{W}$ set in the address phase (equivalent to an I²C read), the PMBus slave considers this a data content fault and responds as follows:

- ACKs the address byte
- NACKs the command and data bytes
- Sends all 1s (0xFF) as long as the host continues to request data
- Sets the CML bit in the STATUS_BYTE register

Invalid or Unsupported Command Code (Item 10.9.2)

If an invalid or unsupported command code is sent to the PMBus slave, the code is considered to be a data content fault, and the PMBus slave responds as follows:

- NACKs the illegal/unsupported command byte and data bytes
- Flushes and ignores the received command and data
- Sets the CML bit in the STATUS_BYTE register

Reserved Bits (Item 10.9.5)

Accesses to reserved bits are not a fault. Writes to reserved bits are ignored, and reads from reserved bits return 0.

Write to Read-Only Commands

If a host performs a write to a read-only command, the PMBus slave considers this a data content fault and responds as follows:

- NACKs all unexpected data bytes as they are received
- Flushes and ignores the received command and data
- Sets the CML bit in the STATUS_BYTE register

Note that this is the same error described in the Host Sends Too Many Bytes (Item 10.8.5) section.

Read from Write-Only Commands

If a host performs a read from a write-only command, the PMBus slave considers this a data content fault and responds as follows:

- Sends all 1s (0xFF) as long as the host continues to request data
- Sets the CML bit in the STATUS_BYTE register

Note that this is the same error described in the Host Reads Too Many Bytes (Item 10.8.6) section.

EEPROM

The ADP1047/ADP1048 have a built-in EEPROM controller that is used to communicate with the embedded 8K × 8-byte EEPROM. The EEPROM, also called Flash®/EE, is partitioned into two major blocks: the INFO block and the main block. The INFO block contains 128 8-bit bytes, and the main block contains 8K 8-bit bytes. The main block is further partitioned into 16 pages, each page containing 512 bytes.

OVERVIEW

The EEPROM controller provides an interface between the ADP1047/ADP1048 core logic and the built-in Flash/EE. The user can control data access to and from the EEPROM through this controller interface. Separate PMBus commands are available for the read, write, and erase operations to the EEPROM.

Communication is initiated by the master device sending a command to the PMBus slave device to access data from or send data to the EEPROM. Read, write, and erase commands are supported. Data is transferred between devices in a byte wide format. Using a read command, data is received from the EEPROM and transmitted to the master device. Using a write command, data is received from the master device and stored in the EEPROM through the EEPROM controller.

PAGE ERASE OPERATION

The main block consists of 16 equivalent pages of 512 bytes each, numbered Page 0 to Page 15. Page 0 and Page 1 of the main block are reserved for storing the default settings and user settings, respectively. The user cannot perform a page erase operation to Page 0 or Page 1.

Main Block Page Erase (Page 2 to Page 15)

To erase any page from Page 2 to Page 15 of the main block, the EEPROM must first be unlocked for access. For instructions on how to unlock the EEPROM, see the Unlock EEPROM section.

Page 2 to Page 15 of the main block can be individually erased using the EEPROM_PAGE_ERASE command (Register 0xD4). For example, to perform a page erase of Page 10, execute the following command:

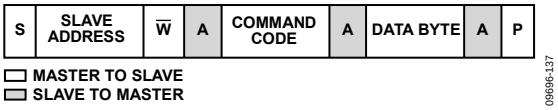


Figure 43. Example Erase Command

In this example, Command Code = 0xD4 and Data Byte = 0x0A.

Note that it is important to wait at least 35 ms for the page erase operation to complete before executing the next PMBus command.

The EEPROM allows erasing of whole pages only; therefore, to change the data of any single byte in a page, the entire page must first be erased (set high) for that byte to be writable. Subsequent writes to any bytes in that page are allowed as long as that byte has not been written to a low previously.

READ OPERATION (BYTE READ AND BLOCK READ)

Read from Page 0 and Page 1

Page 0 and Page 1 of the main block are reserved for storing the default settings and user settings, respectively, and are meant to prevent third-party access to this data. To read from Page 0 or Page 1, the user must first unlock the EEPROM (see the Unlock EEPROM section). After they are unlocked, Page 0 and Page 1 are readable using the EEPROM_DATA_xx commands, as described in the Read from Page 2 to Page 15 section. Note that when the EEPROM is locked, a read from Page 0 and Page 1 returns invalid data.

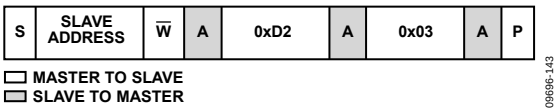
Read from Page 2 to Page 15

Data in Page 2 to Page 15 is always readable, even with the EEPROM locked. The data in the EEPROM main block can be read one byte at a time or in multiple bytes in series using the EEPROM_DATA_xx commands (Command Code 0xB0 to Command Code 0xBF).

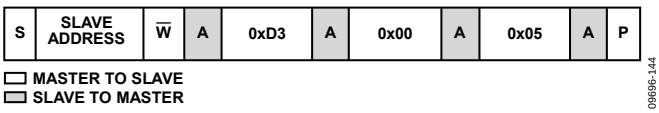
Before executing this command, the user must program the number of bytes to read using the EEPROM_NUM_RD_BYTES command (Register 0xD2). Also, the user can program the offset from the page boundary where the first read byte is returned using the EEPROM_ADDR_OFFSET command (Register 0xD3).

In the following example, three bytes from Page 4 are read from EEPROM, starting from the fifth byte of that page.

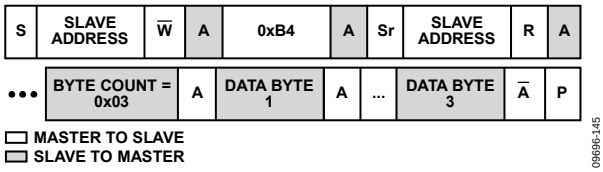
1. Set number of return bytes = 3.



2. Set address offset = 5.



3. Read three bytes from Page 4.



Note that the block read command can read a maximum of 256 bytes for any single transaction.

WRITE OPERATION (BYTE WRITE AND BLOCK WRITE)

Before performing a write to Page 2 through Page 15 of the main block, the user must first unlock the EEPROM (see the Unlock EEPROM section).

Write to Page 0 and Page 1

Page 0 and Page 1 of the main block are reserved for storing the default settings and user settings, respectively. The user cannot perform a direct write operation to Page 0 or Page 1 using the EEPROM_DATA_xx commands. If the user writes to Page 0, Page 1 returns a no acknowledge. To program the register contents of Page 1 of the main block, it is recommended that the STORE_USER_ALL command be used (Command Code 0x15). See the Save Register Settings to the User Scratch Pad section.

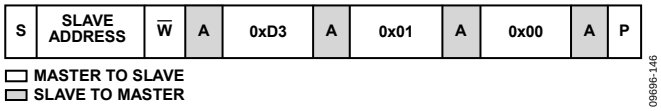
Write to Page 2 Through Page 15

The data in the EEPROM main block can be programmed (written to) one byte at a time or in multiple bytes in series using the EEPROM_DATA_xx commands (Command Code 0xB0 to Command Code 0xBF). Before executing this command, the user can program the offset from the page boundary where the first byte is written using the EEPROM_ADDR_OFFSET command (Register 0xD3).

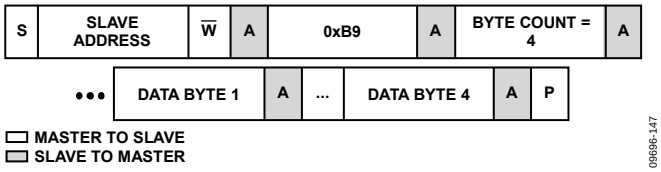
If the targeted page has not yet been erased, the user can erase the page as described in the Main Block Page Erase (Page 2 to Page 15) section.

In the following example, four bytes are written to Page 9, starting from the 256th byte of that page.

1. Set address offset = 256.



2. Write four bytes to Page 9.



Note that the block write command can write a maximum of 256 bytes for any single transaction.

EEPROM PASSWORD

On power-up, the EEPROM is locked and protected from accidental writes or erases. Only reads from Page 2 to Page 15 are allowed when the EEPROM is locked. Before any data can be written (programmed) to the EEPROM, the EEPROM must be unlocked for write access. After it is unlocked, the EEPROM is opened for reading, writing, and erasing.

On power-up, Page 0 and Page 1 are also protected from read access, and the EEPROM must first be unlocked to read these pages.

Unlock EEPROM

To unlock the EEPROM, perform two consecutive writes with the correct password (default = 0xFF) using the EEPROM_PASSWORD command (Register 0xD5). The EEPROM_UNLOCKED flag (Bit 6 of Register 0xFE81) is set to indicate that the EEPROM is unlocked for write access.

Lock EEPROM

To lock the EEPROM, write any byte other than the correct password using the EEPROM_PASSWORD command (Register 0xD5). The EEPROM unlock flag is cleared to indicate that the EEPROM is locked from write access.

Change EEPROM Password

To change the EEPROM password, the EEPROM must first be unlocked. To change the EEPROM password, first write the correct password using the EEPROM_PASSWORD command (Register 0xD5). Immediately write the new password using the EEPROM_PASSWORD command. The password is now changed to the new password.

DOWNLOADING EEPROM SETTINGS TO INTERNAL REGISTERS

Download User Settings to Registers

The user settings are stored in Page 1 of the EEPROM main block. These settings are downloaded from the EEPROM into the registers under the following conditions:

- On power-up. The user settings are automatically downloaded into the internal registers, powering the part up in a state previously saved by the user.
- On execution of the RESTORE_USER_ALL command (Command Code 0x16). This command allows the user to force a download of the user settings from the EEPROM main block, Page 1, into the internal registers.

Download Factory Settings to Registers

The factory default settings are stored in Page 0 of the EEPROM main block. The factory settings can be downloaded from the EEPROM into the internal registers using the RESTORE_DEFAULT_ALL command (Command Code 0x12).

When this command is executed, the EEPROM password is also reset to the factory default setting of 0xFF.

SAVING REGISTER SETTINGS INTO EEPROM

The register settings cannot be saved to the factory scratch pad located in Page 0 of the EEPROM main block. This is to prevent the user from accidentally overriding the factory trim settings and default register settings.

Save Register Settings to the User Scratch Pad

The register settings can be saved to the user scratch pad located in Page 1 of the EEPROM main block using the STORE_USER_ALL command (Command Code 0x15). Before this command can be executed, the EEPROM must first be unlocked for writing (see the Unlock EEPROM section).

After the register settings are saved to the user scratch pad, any subsequent power cycle automatically downloads the latest stored user information from the EEPROM into the internal registers.

Note that execution of the STORE_USER_ALL command automatically performs a page erase to Page 1 of the EEPROM main block, after which the registers are stored in EEPROM. Therefore, it is important to wait at least 35 ms for the operation to complete before executing the next PMBus command.

EEPROM CRC CHECKSUM

As a simple method of checking that the values downloaded from EEPROM and the internal registers are consistent, a CRC checksum is implemented.

- When the data from the internal registers is saved to the EEPROM (Page 1 of the main block), the total number of 1s from all the registers is counted and written into the EEPROM as the last byte of information. This is called the CRC checksum.
- When the data is downloaded from the EEPROM into the internal registers, a similar counter that sums all 1s from the values loaded into the registers is saved. This value is compared with the CRC checksum from the previous upload operation.

If the values match, the download operation was successful. If the values differ, the EEPROM download operation failed, and the EEPROM_CRC fault flag is set (Register 0xFE81, Bit 5).

To read the EEPROM CRC checksum value, execute the EEPROM_CRC_CHKSUM command (Register 0xD1). This command returns the CRC checksum accumulated in the counter during the download operation.

Note that the CRC checksum is an 8-bit cyclical accumulator that wraps around to 0 when 255 is reached.

SOFTWARE GUI

A free software GUI is available for programming and configuring the ADP1047/ADP1048. The GUI is designed to be intuitive and dramatically reduces power supply design and development time.

The software includes filter design and power supply PWM topology windows. The GUI is also an information center, displaying the status of all readings, monitoring, and flags on the ADP1047/ADP1048.

For more information about the GUI, contact Analog Devices for the latest software and a user guide.

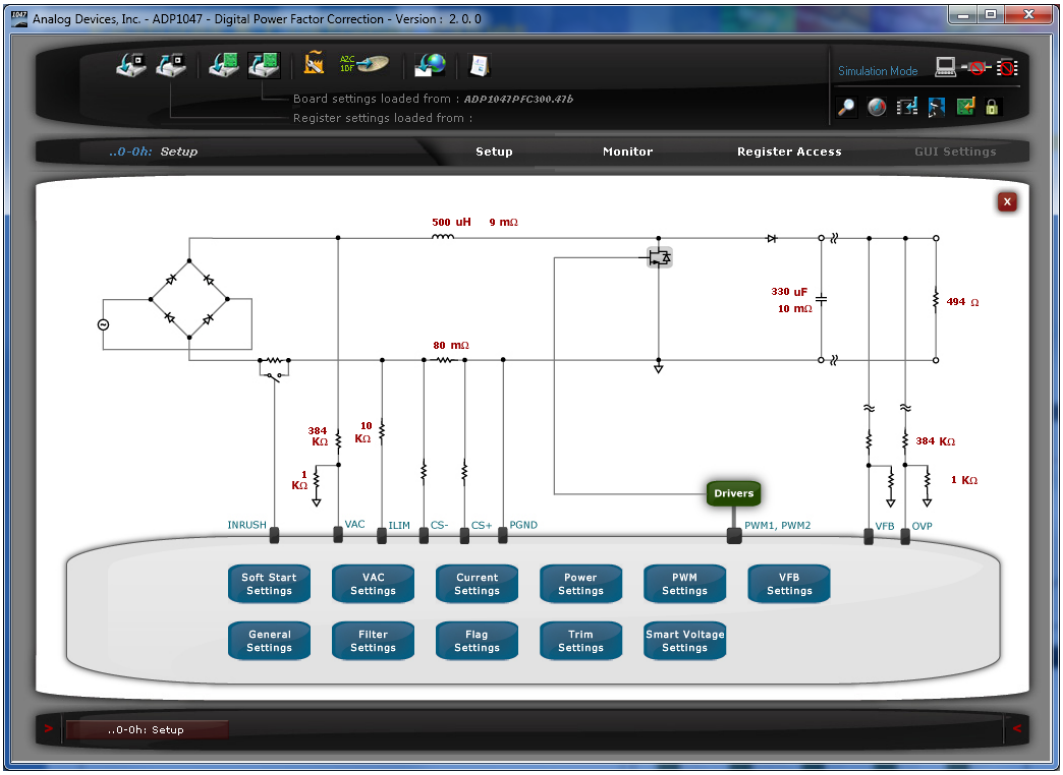


Figure 44. ADP1047/ADP1048 GUI Main Window

STANDARD PMBus COMMANDS SUPPORTED BY THE ADP1047/ADP1048

Table 15 lists the standard PMBus commands that are implemented on the ADP1047/ADP1048. Many of these commands are implemented in registers, which share the same hexadecimal value as the PMBus command code.

Table 15. Standard PMBus Commands

Command Code	Command Name
0x01	OPERATION
0x02	ON_OFF_CONFIG
0x03	CLEAR_FAULTS
0x10	WRITE_PROTECT
0x12	RESTORE_DEFAULT_ALL
0x15	STORE_USER_ALL
0x16	RESTORE_USER_ALL
0x19	CAPABILITY
0x20	VOUT_MODE
0x21	VOUT_COMMAND
0x29	VOUT_SCALE_LOOP
0x2A	VOUT_SCALE_MONITOR
0x35	VIN_ON
0x36	VIN_OFF
0x40	VOUT_OV_FAULT_LIMIT
0x41	VOUT_OV_FAULT_RESPONSE
0x42	VOUT_OV_WARN_LIMIT
0x43	VOUT_UV_WARN_LIMIT
0x44	VOUT_UV_FAULT_LIMIT
0x45	VOUT_UV_FAULT_RESPONSE
0x50	OT_FAULT_RESPONSE
0x55	VIN_OV_FAULT_LIMIT
0x56	VIN_OV_FAULT_RESPONSE
0x58	VIN_UV_WARN_LIMIT
0x59	VIN_UV_FAULT_LIMIT
0x5A	VIN_UV_FAULT_RESPONSE
0x5B	IIN_OC_FAULT_LIMIT
0x5C	IIN_OC_FAULT_RESPONSE
0x5D	IIN_OC_WARN_LIMIT
0x6B	PIN_OP_WARN_LIMIT
0x78	STATUS_BYTE
0x79	STATUS_WORD
0x7A	STATUS_VOUT
0x7C	STATUS_INPUT
0x7D	STATUS_TEMPERATURE
0x88	READ_VIN
0x89	READ_IIN
0x8B	READ_VOUT
0x97	READ_PIN
0x98	PMBUS_REVISION
0x99	MFR_ID
0x9A	MFR_MODEL
0x9B	MFR_REVISION
0xB0	EEPROM_DATA_00
0xB1	EEPROM_DATA_01
0xB2	EEPROM_DATA_02
0xB3	EEPROM_DATA_03
0xB4	EEPROM_DATA_04
0xB5	EEPROM_DATA_05
0xB6	EEPROM_DATA_06
0xB7	EEPROM_DATA_07
0xB8	EEPROM_DATA_08
0xB9	EEPROM_DATA_09
0xBA	EEPROM_DATA_10
0xBB	EEPROM_DATA_11
0xBC	EEPROM_DATA_12
0xBD	EEPROM_DATA_13
0xBE	EEPROM_DATA_14
0xBF	EEPROM_DATA_15
0xD1	EEPROM_CRC_CHKSUM
0xD2	EEPROM_NUM_RD_BYTES
0xD3	EEPROM_ADDR_OFFSET
0xD4	EEPROM_PAGE_ERASE
0xD5	EEPROM_PASSWORD
0xD6	TRIM_PASSWORD
0xF1	EEPROM_INFO

MANUFACTURER-SPECIFIC PMBus COMMANDS

Table 16 lists the manufacturer-specific PMBus commands that are implemented on the ADP1047/ADP1048. These commands are implemented in registers, which share the same hexadecimal value as the PMBus command code.

Table 16. Manufacturer-Specific Commands

Command Code	Command Name
0xFE00	CS_FAST_OCP_RESPONSE
0xFE01	OVP_FAST_OVP_RESPONSE
0xFE02	OLP_RESPONSE
0xFE03	VDD3P3_RESPONSE
0xFE04	VCORE_RESPONSE
0xFE05	PGOOD_AC_OK_DEBOUNCE_SET
0xFE06	PSON_SET
0xFE07	FLAG_FAULT_ID
0xFE08	SOFTSTART_FLAGS_BLANK1
0xFE09	SOFTSTART_FLAGS_BLANK2
0xFE0A	PGOOD_FLAGS_LIST
0xFE0B	AC_OK_FLAGS_LIST
0xFE0C	PWM rising edge timing (PWM pin)
0xFE0D	PWM rising edge setting (PWM pin)
0xFE0E	PWM falling edge timing (PWM pin)
0xFE0F	PWM falling edge setting (PWM pin)
0xFE10	PWM2 rising edge timing (PWM2 pin)
0xFE11	PWM2 rising edge setting (PWM2 pin)
0xFE12	PWM2 falling edge timing (PWM2 pin)
0xFE13	PWM2 falling edge setting (PWM2 pin)
0xFE14	PWM_SET
0xFE15	PWM_LIMIT
0xFE16	RTD ADC offset trim setting (MSB)
0xFE17	RTD ADC offset trim setting (LSB)
0xFE18	RTD ADC gain trim setting
0xFE19	OT_FAULT_LIMIT
0xFE1A	OT_WARN_LIMIT
0xFE1B	Switching frequency setting
0xFE1C	Low power switching frequency setting
0xFE1D	Frequency dithering set
0xFE1E	Frequency synchronization set
0xFE20	Voltage loop filter gain
0xFE21	Voltage loop filter zero
0xFE22	Fast voltage loop filter gain
0xFE23	Fast voltage loop filter zero
0xFE24	Fast voltage loop enable
0xFE25	VAC_THRESHOLD_SET
0xFE26	VAC_THRESHOLD_READ
0xFE27	MIN_AC_PERIOD_SET
0xFE28	MAX_AC_PERIOD_SET
0xFE29	Current loop filter gain for low line input
0xFE2A	Current loop filter zero for low line input
0xFE2B	Current loop filter gain for high line input
0xFE2C	Current loop filter zero for high line input
0xFE2D	Soft start set
0xFE2E	Inrush set
0xFE2F	FAST_OVP_FAULT_RISE
0xFE30	FAST_OVP_FAULT_FALL
0xFE31	Fast OVP debounce time setting
0xFE32	Low power mode operation threshold
0xFE33	Power metering offset trim for low line input
0xFE34	Power metering gain trim for low line input
0xFE35	High line limit
0xFE36	Low line limit
0xFE37	ILIM_TRIM
0xFE38	Voltage loop output
0xFE39	Exponent
0xFE3A	Read update rate
0xFE3B	VIN scale monitor
0xFE3C	IIN_GSENSE
0xFE3D	CS fast OCP blank
0xFE3E	CS fast OCP setting
0xFE3F	Temperature hysteresis
0xFE40	VAC ADC gain trim
0xFE41	VFB ADC gain trim
0xFE42	CS ADC gain trim for 500 mV range
0xFE43	IBAL gain (ADP1048 only)
0xFE44	Smart VOUT low power threshold (P1)
0xFE45	Smart VOUT high power threshold (P2)
0xFE46	Smart VOUT low line (VOL1)
0xFE47	Smart VOUT low line (VOL2)
0xFE48	Smart VOUT high line (VOH1)
0xFE49	Smart VOUT high line (VOH2)
0xFE4A	Smart VOUT upper limit (VOH)
0xFE4B	Smart VOUT super high line
0xFE4C	SYNC delay
0xFE4D	SMART_VOUT_SUPER_HIGH_LINE_HYS
0xFE4E	POWER_HYS
0xFE4F	Advanced feature enable
0xFE50	VOUT_OV_FAULT_HYS
0xFE51	VIN_UV_FAULT_HYS
0xFE53	VAC ADC offset trim
0xFE54	CS ADC offset trim for 500 mV range
0xFE7E	CS ADC gain trim for high (750 mV) range
0xFE7F	CS ADC offset trim for high (750 mV) range
0xFE80	Latched Flag 0
0xFE81	Latched Flag 1
0xFE82	Latched Flag 2
0xFE84	PWM value
0xFE85	VAC_LINE_PERIOD
0xFE86	Read temperature ADC
0xFE8E	Power metering offset trim for high line input

Command Code	Command Name
0xFE8F	Power metering gain trim for high line input
0xFE90	Current loop filter gain for low line input and light load
0xFE91	Current loop filter zero for low line input and light load
0xFE92	Current loop filter gain for high line input and light load
0xFE93	Current loop filter zero for high line input and light load

Command Code	Command Name
0xFE94	Smart VOUT power reading
0xFE95	IBAL configuration (ADP1048 only)
0xFE96	Debug Flag 0
0xFE97	Debug Flag 1
0xFE98	Debug Flag 2
0xFE99	Debug Flag 3
0xFE9A	Debug Flag 4
0xFE9B	Debug Flag 5

DETAILED REGISTER DESCRIPTIONS

OPERATION REGISTER

Table 17. Register 0x01—OPERATION

Bits	Bit Name	R/W	Description
7	Enable	R/W	This bit determines the device response to the OPERATION command. 0 = immediate off (no sequencing). 1 = device on.
6	RSVD	R	Always reads as 0.
[5:4]	Margin control	R	These bits set the output voltage margin level and are hardcoded to a value of 00.
[3:2]	Margin fault response	R	These bits set the device response to an output OVP/UVP warning or fault after the output is margined. These bits are hardcoded to a value of 01.
[1:0]	RSVD	R	Reserved.

ON_OFF_CONFIG REGISTER

Table 18. Register 0x02—ON_OFF_CONFIG

Bits	Bit Name	R/W	Description
[7:5]	RSVD	R	Reserved.
4	Power-up control	R/W	Set the device power-up response. 0 = device powers up when power is present. 1 = device powers up only when commanded by the control pin (PSON) and the OPERATION command.
3	Command enable	R/W	Control how the device responds to the OPERATION command. 0 = ignore the OPERATION command. 1 = the OPERATION command must be set to 1 to enable the device (in addition to setting Bit 2).
2	Pin enable	R/W	Control how the device responds to the value of the control pin (PSON). 0 = ignore the control pin (PSON). 1 = the control pin must be asserted to enable the device (in addition to setting Bit 3).
1	Control pin polarity	R/W	Set the polarity of the control pin (PSON). 0 = active low. 1 = active high.
0	Power-down delay	R	Actions to take on power-down. This bit always reads as 1 (turn off the output and stop energy transfer to the output as fast as possible).

CLEAR_FAULTS COMMAND

Code 0x03, send byte, no data. This command clears all fault bits in all registers simultaneously.

WRITE_PROTECT REGISTER

Table 19. Register 0x10—WRITE_PROTECT

Bits	Bit Name	R/W	Description
7	Write Protect 1	R/W	Setting this bit disables writes to all commands except for WRITE_PROTECT.
6	Write Protect 2	R/W	Setting this bit disables writes to all commands except for WRITE_PROTECT, OPERATION, and EEPROM_PAGE_ERASE.
5	Write Protect 3	R/W	Setting this bit disables writes to all commands except for WRITE_PROTECT, OPERATION, EEPROM_PAGE_ERASE, ON_OFF_CONFIG, and VOUT_COMMAND.
[4:0]	RSVD	R	Reserved.

RESTORE_DEFAULT_ALL COMMAND

Code 0x12, send byte, no data. This command downloads the factory default parameters from EEPROM into operating memory.

STORE_USER_ALL COMMAND

Code 0x15, send byte, no data. This command copies the entire contents of operating memory into EEPROM (Page 1 of the main block).

RESTORE_USER_ALL COMMAND

Code 0x16, send byte, no data. This command downloads the stored user settings from EEPROM into operating memory.

CAPABILITY REGISTER

This register allows host systems to determine the capabilities of the PMBus device.

Table 20. Register 0x19—CAPABILITY

Bits	Bit Name	R/W	Description
7	Packet error checking	R	Always reads as 0. Packet error checking (PEC) is not supported.
[6:5]	Maximum bus speed	R	Return the device PMBus speed capability. These bits are hardcoded to a value of 01 (use the 400 kHz maximum bus speed).
4	SMBALERT#	R	Always reads as 0. SMBALERT# pin and SMBus alert response protocol not supported.
[3:0]	RSVD	R	Reserved.

VOUT_MODE REGISTER

This register sets and reads the format (linear, VID, direct) and exponents for VOUT related commands.

Table 21. Register 0x20—VOUT_MODE

Bits	Bit Name	R/W	Description
[7:5]	Mode	R	Return the output voltage data format. This bit is hardcoded to use linear format.
[4:3]	RSVD	R	Reserved.
[2:0]	Exponent	R/W	Specify the exponent (N) used in VOUT linear mode format ($X = Y \times 2^N$). The exponent is in twos complement format.

VOUT_COMMAND REGISTER

This register sets VOUT to the configured value.

Table 22. Register 0x21—VOUT_COMMAND

Bits	Bit Name	R/W	Description
[15:12]	RSVD	R	Reserved. Always reads as 0000.
[11:0]	Mantissa	R/W	Mantissa (Y[11:0]) used in VOUT linear mode format ($X = Y \times 2^N$).

VOUT_SCALE_LOOP REGISTER

This register sets the K factor = VADC/VOUT.

Table 23. Register 0x29—VOUT_SCALE_LOOP

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R/W	Write the exponent (N) in twos complement format for $K = Y \times 2^N$.
10	RSVD	R	Always reads as 0.
[9:0]	Mantissa	R/W	Mantissa (Y[9:0]) used in K linear mode format ($K = Y \times 2^N$).

VOUT_SCALE_MONITOR REGISTER

This register sets the Kr factor = VOUT/VADC.

Table 24. Register 0x2A—VOUT_SCALE_MONITOR

Bits	Bit Name	R/W	Description
[15:14]	RSVD	R	Reserved.
[13:11]	Exponent	R/W	Write the exponent (N) in twos complement format for Kr = Y × 2^N.
10	RSVD	R	Always reads as 0.
[9:0]	Mantissa	R/W	Mantissa (Y[9:0]) used in Kr linear mode format (Kr = Y × 2^N).

VIN_ON REGISTER

This register sets the value of the input voltage to start power conversion.

Table 25. Register 0x35—VIN_ON

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R	Return the exponent (N) used in VIN linear mode format (X = Y × 2^N). The exponent (N) is set in the exponent register (Register 0xFE39, Bits[5:3]).
[10:8]	High bits	R/W	Mantissa high bits (Y[10:8]) used in VIN linear mode format (X = Y × 2^N).
[7:0]	Low byte	R/W	Mantissa low byte (Y[7:0]) used in VIN linear mode format (X = Y × 2^N). The exponent (N) is set in the exponent register (Register 0xFE39, Bits[5:3]).

VIN_OFF REGISTER

This register sets the value of the input voltage to stop power conversion.

Table 26. Register 0x36—VIN_OFF

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R	Return the exponent (N) used in VIN linear mode format (X = Y × 2^N). The exponent (N) is set in the exponent register (Register 0xFE39, Bits[5:3]).
[10:8]	High bits	R/W	Mantissa high bits (Y[10:8]) used in VIN linear mode format (X = Y × 2^N).
[7:0]	Low byte	R/W	Mantissa low byte (Y[7:0]) used in VIN linear mode format (X = Y × 2^N). The exponent (N) is set in the exponent register (Register 0xFE39, Bits[5:3]).

VOUT_OV_FAULT_LIMIT REGISTER

This register sets the accurate overvoltage threshold measured at the PFC output that causes an overvoltage fault condition.

Table 27. Register 0x40—VOUT_OV_FAULT_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R	Return the exponent (N) used in VOUT linear mode format (X = Y × 2^N). The exponent (N) is set in the VOUT_MODE register (Register 0x20, Bits[2:0]). The exponent is in twos complement format.
[10:8]	High bits	R/W	Mantissa high bits (Y[10:8]) used in VOUT linear mode format (X = Y × 2^N).
[7:0]	Low byte	R/W	Mantissa low byte (Y[7:0]) used in VOUT linear mode format (X = Y × 2^N).

VOUT_OV_FAULT_RESPONSE REGISTER

This register instructs the device on actions to take due to an output overvoltage fault condition.

Table 28. Register 0x41—VOUT_OV_FAULT_RESPONSE

Bits	Bit Name	R/W	Description		
[7:6]	Response	R/W	These bits determine the device response to an output overvoltage fault condition.		
			Bit 7	**Bit 6**	**Response**
			0	0	Do nothing.
			0	1	Continue operation for the time specified by Delay Time 1 (Bits[2:0]). If the fault persists, retry the number of times specified by the retry setting (Bits[5:3]).
			1	0	Shut down, disable the output, and retry the number of times specified by the retry setting (Bits[5:3]).
			1	1	Disable the output and wait for the fault to clear. After the fault is cleared, reenable the output.

Bits	Bit Name	R/W	Description
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. If the fault persists after the programmed number of attempts, the output is disabled and remains off until the fault is cleared. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power. The time between restart attempts is specified by Delay Time 2 (Bits[2:0]).

Bit 5	Bit 4	Bit 3	Number of Retries
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	Infinite

Bits	Bit Name	R/W	Description
[2:0]	Delay times	R/W	Delay Time 1 is the delay before the device disables the output after a fault condition is detected. Delay Time 2 is the time between restart attempts.

Bit 2	Bit 1	Bit 0	Delay Time 1	Delay Time 2
0	0	0	10 ms	252 ms
0	0	1	20 ms	558 ms
0	1	0	40 ms	924 ms
0	1	1	80 ms	1260 ms
1	0	0	160 ms	1596 ms
1	0	1	320 ms	1932 ms
1	1	0	640 ms	2268 ms
1	1	1	1280 ms	2604 ms

VOUT_OV_WARN_LIMIT REGISTER

This register sets the accurate overvoltage threshold measured at the PFC output that causes an overvoltage warning condition.

Table 29. Register 0x42—VOUT_OV_WARN_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R	Return the exponent (N) used in VOUT linear mode format ($X = Y \times 2^N$). The exponent (N) is set in the VOUT_MODE register (Register 0x20, Bits[2:0]). The exponent is in twos complement format.
[10:8]	High bits	R/W	Mantissa high bits (Y[10:8]) used in VOUT linear mode format ($X = Y \times 2^N$).
[7:0]	Low byte	R/W	Mantissa low byte (Y[7:0]) used in VOUT linear mode format ($X = Y \times 2^N$).

VOUT_UV_WARN_LIMIT REGISTER

This register sets the undervoltage threshold measured at the PFC output that causes an undervoltage warning condition.

Table 30. Register 0x43—VOUT_UV_WARN_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R	Return the exponent (N) used in VOUT linear mode format ($X = Y \times 2^N$). The exponent (N) is set in the VOUT_MODE register (Register 0x20, Bits[2:0]). The exponent is in twos complement format.
[10:8]	High bits	R/W	Mantissa high bits (Y[10:8]) used in VOUT linear mode format ($X = Y \times 2^N$).
[7:0]	Low byte	R/W	Mantissa low byte (Y[7:0]) used in VOUT linear mode format ($X = Y \times 2^N$).

VOUT_UV_FAULT_LIMIT REGISTER

This register sets the undervoltage threshold measured at the PFC output that causes an undervoltage fault condition.

Table 31. Register 0x44—VOUT_UV_FAULT_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R	Return the exponent (N) used in VOUT linear mode format ($X = Y \times 2^N$). The exponent (N) is set in the VOUT_MODE register (Register 0x20, Bits[2:0]). The exponent is in twos complement format.
[10:8]	High bits	R/W	Mantissa high bits (Y[10:8]) used in VOUT linear mode format ($X = Y \times 2^N$).
[7:0]	Low byte	R/W	Mantissa low byte (Y[7:0]) used in VOUT linear mode format ($X = Y \times 2^N$).

VOUT_UV_FAULT_RESPONSE REGISTER

This register instructs the device on actions to take due to an output undervoltage fault condition.

Table 32. Register 0x45—VOUT_UV_FAULT_RESPONSE

Bits	Bit Name	R/W	Description				
[7:6]	Response	R/W	These bits determine the device response to an output undervoltage fault condition.				
			Bit 7	**Bit 6**	**Response**		
			0	0	Do nothing.		
			0	1	Continue operation for the time specified by Delay Time 1 (Bits[2:0]). If the fault persists, retry the number of times specified by the retry setting (Bits[5:3]).		
			1	0	Shut down, disable the output, and retry the number of times specified by the retry setting (Bits[5:3]).		
			1	1	Disable the output and wait for the fault to clear. After the fault is cleared, reenable the output.		
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. If the fault persists after the programmed number of attempts, the output is disabled and remains off until the fault is cleared. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power. The time between restart attempts is specified by Delay Time 2 (Bits[2:0]).				
			Bit 5	**Bit 4**	**Bit 3**	**Number of Retries**	
			0	0	0	0	
			0	0	1	1	
			0	1	0	2	
			0	1	1	3	
			1	0	0	4	
			1	0	1	5	
			1	1	0	6	
			1	1	1	Infinite	
[2:0]	Delay times	R/W	Delay Time 1 is the delay before the device disables the output after a fault condition is detected. Delay Time 2 is the time between restart attempts.				
			Bit 2	**Bit 1**	**Bit 0**	**Delay Time 1**	**Delay Time 2**
			0	0	0	10 ms	252 ms
			0	0	1	20 ms	558 ms
			0	1	0	40 ms	924 ms
			0	1	1	80 ms	1260 ms
			1	0	0	160 ms	1596 ms
			1	0	1	320 ms	1932 ms
			1	1	0	640 ms	2268 ms
			1	1	1	1280 ms	2604 ms

OT_FAULT_RESPONSE REGISTER

This register instructs the device on actions to take due to an overtemperature fault condition.

Table 33. Register 0x50—OT_FAULT_RESPONSE

Bits	Bit Name	R/W	Description		
[7:6]	Response	R/W	These bits determine the device response to an overtemperature fault condition.		
			Bit 7	**Bit 6**	**Response**
			0	0	Do nothing.
			0	1	Continue operation for the time specified by Delay Time 1 (Bits[2:0]). If the fault persists, retry the number of times specified by the retry setting (Bits[5:3]).
			1	0	Shut down, disable the output, and retry the number of times specified by the retry setting (Bits[5:3]).
			1	1	Disable the output and wait for the fault to clear. After the fault is cleared, reenable the output.

Bits	Bit Name	R/W	Description				
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. If the fault persists after the programmed number of attempts, the output is disabled and remains off until the fault is cleared. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power. The time between restart attempts is specified by Delay Time 2 (Bits[2:0]).				
			Bit 5	**Bit 4**	**Bit 3**	**Number of Retries**	
			0	0	0	0	
			0	0	1	1	
			0	1	0	2	
			0	1	1	3	
			1	0	0	4	
			1	0	1	5	
			1	1	0	6	
			1	1	1	Infinite	
[2:0]	Delay times	R/W	Delay Time 1 is the delay before the device disables the output after a fault condition is detected. Delay Time 2 is the time between restart attempts.				
			Bit 2	**Bit 1**	**Bit 0**	**Delay Time 1**	**Delay Time 2**
			0	0	0	10 ms	252 ms
			0	0	1	20 ms	558 ms
			0	1	0	40 ms	924 ms
			0	1	1	80 ms	1260 ms
			1	0	0	160 ms	1596 ms
			1	0	1	320 ms	1932 ms
			1	1	0	640 ms	2268 ms
			1	1	1	1280 ms	2604 ms

VIN_OV_FAULT_LIMIT REGISTER

This register sets the overvoltage threshold measured at the PFC input that causes an overvoltage fault condition.

Table 34. Register 0x55—VIN_OV_FAULT_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R	Return the exponent (N) used in VIN linear mode format ($X = Y \times 2^N$). The exponent (N) is set in the exponent register (Register 0xFE39, Bits[5:3]).
[10:8]	High bits	R/W	Mantissa high bits (Y[10:8]) used in VIN linear mode format ($X = Y \times 2^N$).
[7:0]	Low byte	R/W	Mantissa low byte (Y[7:0]) used in VIN linear mode format ($X = Y \times 2^N$). The exponent (N) is set in the exponent register (Register 0xFE39, Bits[5:3]).

VIN_OV_FAULT_RESPONSE REGISTER

This register instructs the device on actions to take due to an input overvoltage fault condition.

Table 35. Register 0x56—VIN_OV_FAULT_RESPONSE

Bits	Bit Name	R/W	Description		
[7:6]	Response	R/W	These bits determine the device response to an input overvoltage fault condition.		
			Bit 7	**Bit 6**	**Response**
			0	0	Do nothing.
			0	1	Continue operation for the time specified by Delay Time 1 (Bits[2:0]). If the fault persists, retry the number of times specified by the retry setting (Bits[5:3]).
			1	0	Shut down, disable the output, and retry the number of times specified by the retry setting (Bits[5:3]).
			1	1	Disable the output and wait for the fault to clear. After the fault is cleared, reenable the output.

Bits	Bit Name	R/W	Description
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. If the fault persists after the programmed number of attempts, the output is disabled and remains off until the fault is cleared. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power. The time between restart attempts is specified by Delay Time 2 (Bits[2:0]).

Bit 5	Bit 4	Bit 3	Number of Retries
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	Infinite

Bits	Bit Name	R/W	Description
[2:0]	Delay times	R/W	Delay Time 1 is the delay before the device disables the output after a fault condition is detected. Delay Time 2 is the time between restart attempts.

Bit 2	Bit 1	Bit 0	Delay Time 1	Delay Time 2
0	0	0	10 ms	252 ms
0	0	1	20 ms	558 ms
0	1	0	40 ms	924 ms
0	1	1	80 ms	1260 ms
1	0	0	160 ms	1596 ms
1	0	1	320 ms	1932 ms
1	1	0	640 ms	2268 ms
1	1	1	1280 ms	2604 ms

VIN_UV_WARN_LIMIT REGISTER

This register sets the undervoltage threshold measured at the PFC input that causes an undervoltage warning condition.

Table 36. Register 0x58—VIN_UV_WARN_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R	Return the exponent (N) used in VIN linear mode format ($X = Y \times 2^N$). The exponent is set in the exponent register (Register 0xFE39, Bits[5:3]).
[10:8]	High bits	R/W	Mantissa high bits (Y[10:8]) used in VIN linear mode format ($X = Y \times 2^N$).
[7:0]	Low byte	R/W	Mantissa low byte (Y[7:0]) used in VIN linear mode format ($X = Y \times 2^N$). The exponent (N) is set in the exponent register (Register 0xFE39, Bits[5:3]).

VIN_UV_FAULT_LIMIT REGISTER

This register sets the undervoltage threshold measured at the PFC input that causes an undervoltage fault condition.

Table 37. Register 0x59—VIN_UV_FAULT_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R	Return the exponent (N) used in VIN linear mode format ($X = Y \times 2^N$). The exponent is set in the exponent register (Register 0xFE39, Bits[5:3]).
[10:8]	High bits	R/W	Mantissa high bits (Y[10:8]) used in VIN linear mode format ($X = Y \times 2^N$).
[7:0]	Low byte	R/W	Mantissa low byte (Y[7:0]) used in VIN linear mode format ($X = Y \times 2^N$). The exponent (N) is set in the exponent register (Register 0xFE39, Bits[5:3]).

VIN_UV_FAULT_RESPONSE REGISTER

This register instructs the device on actions to take due to an input undervoltage fault condition.

Table 38. Register 0x5A—VIN_UV_FAULT_RESPONSE

Bits	Bit Name	R/W	Description				
[7:6]	Response	R/W	These bits determine the device response to an input undervoltage fault condition.				
			Bit 7	**Bit 6**	**Response**		
			0	0	Do nothing.		
			0	1	Continue operation for the time specified by Delay Time 1 (Bits[2:0]). If the fault persists, retry the number of times specified by the retry setting (Bits[5:3]).		
			1	0	Shut down, disable the output, and retry the number of times specified by the retry setting (Bits[5:3]).		
			1	1	Disable the output and wait for the fault to clear. After the fault is cleared, reenable the output.		
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. If the fault persists after the programmed number of attempts, the output is disabled and remains off until the fault is cleared. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power. The time between restart attempts is specified by Delay Time 2 (Bits[2:0]).				
			Bit 5	**Bit 4**	**Bit 3**	**Number of Retries**	
			0	0	0	0	
			0	0	1	1	
			0	1	0	2	
			0	1	1	3	
			1	0	0	4	
			1	0	1	5	
			1	1	0	6	
			1	1	1	Infinite	
[2:0]	Delay times	R/W	Delay Time 1 is the delay before the device disables the output after a fault condition is detected. Delay Time 2 is the time between restart attempts.				
			Bit 2	**Bit 1**	**Bit 0**	**Delay Time 1**	**Delay Time 2**
			0	0	0	10 ms	252 ms
			0	0	1	20 ms	558 ms
			0	1	0	40 ms	924 ms
			0	1	1	80 ms	1260 ms
			1	0	0	160 ms	1596 ms
			1	0	1	320 ms	1932 ms
			1	1	0	640 ms	2268 ms
			1	1	1	1280 ms	2604 ms

IIN_OC_FAULT_LIMIT REGISTER

This register sets the accurate overcurrent threshold measured at the PFC input that causes an overcurrent fault condition.

Table 39. Register 0x5B—IIN_OC_FAULT_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R	Return the exponent (N) used in current linear mode format ($X = Y \times 2^N$). The exponent is set in the exponent register (Register 0xFE39, Bits[10:6]).
[10:8]	High bits	R/W	Mantissa high bits (Y[10:8]) used in current linear mode format ($X = Y \times 2^N$).
[7:0]	Low byte	R/W	Mantissa low byte (Y[7:0]) used in current linear mode format ($X = Y \times 2^N$).

IIN_OC_FAULT_RESPONSE REGISTER

This register instructs the device on actions to take due to an input overcurrent fault condition.

Table 40. Register 0x5C—IIN_OC_FAULT_RESPONSE

Bits	Bit Name	R/W	Description				
[7:6]	Response	R/W	These bits determine the device response to an input overcurrent fault condition.				
			Bit 7	**Bit 6**	**Response**		
			0	0	Do nothing.		
			0	1	Continue operation for the time specified by Delay Time 1 (Bits[2:0]). If the fault persists, retry the number of times specified by the retry setting (Bits[5:3]).		
			1	0	Shut down, disable the output, and retry the number of times specified by the retry setting (Bits[5:3]).		
			1	1	Disable the output and wait for the fault to clear. After the fault is cleared, reenable the output.		
[5:3]	Retry setting	R/W	Number of retry attempts following a fault condition. If the fault persists after the programmed number of attempts, the output is disabled and remains off until the fault is cleared. A fault condition can be cleared by a reset, a power-off/power-on sequence, or a loss of bias power. The time between restart attempts is specified by Delay Time 2 (Bits[2:0]).				
			Bit 5	**Bit 4**	**Bit 3**	**Number of Retries**	
			0	0	0	0	
			0	0	1	1	
			0	1	0	2	
			0	1	1	3	
			1	0	0	4	
			1	0	1	5	
			1	1	0	6	
			1	1	1	Infinite	
[2:0]	Delay times	R/W	Delay Time 1 is the delay before the device disables the output after a fault condition is detected. Delay Time 2 is the time between restart attempts.				
			Bit 2	**Bit 1**	**Bit 0**	**Delay Time 1**	**Delay Time 2**
			0	0	0	10 ms	252 ms
			0	0	1	20 ms	558 ms
			0	1	0	40 ms	924 ms
			0	1	1	80 ms	1260 ms
			1	0	0	160 ms	1596 ms
			1	0	1	320 ms	1932 ms
			1	1	0	640 ms	2268 ms
			1	1	1	1280 ms	2604 ms

IIN_OC_WARN_LIMIT REGISTER

This register sets the accurate overcurrent threshold measured at the PFC input that causes an overcurrent warning condition.

Table 41. Register 0x5D—IIN_OC_WARN_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R	Return the exponent (N) used in current linear mode format ($X = Y \times 2^N$). The exponent is set in the exponent register (Register 0xFE39, Bits[10:6]).
[10:8]	High bits	R/W	Mantissa high bits (Y[10:8]) used in current linear mode format ($X = Y \times 2^N$).
[7:0]	Low byte	R/W	Mantissa low byte (Y[7:0]) used in current linear mode format ($X = Y \times 2^N$).

PIN_OP_WARN_LIMIT REGISTER

This register sets the upper input power (W) threshold that causes an input overpower warning condition.

Table 42. Register 0x6B—PIN_OP_WARN_LIMIT

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R	Return the exponent (N) used in power linear mode format ($X = Y \times 2^N$). The exponent is set in the exponent register (Register 0xFE39, Bits[2:0]).
[10:8]	High bits	R/W	Mantissa high bits (Y[10:8]) used in power linear mode format ($X = Y \times 2^N$).
[7:0]	Low byte	R/W	Mantissa low byte (Y[7:0]) used in power linear mode format ($X = Y \times 2^N$).

STATUS_BYTE REGISTER

This register returns the lower byte of the STATUS_WORD register. A value of 1 in this register indicates that a fault has occurred.

Table 43. Register 0x78—STATUS_BYTE

Bits	Bit Name	R/W	Description
7	BUSY	R	1 = device was busy and unable to respond.
6	PSON_OFF	R	1 = device is not providing power to the output.
5	VOUT_OV	R	1 = output overvoltage fault.
4	IOUT_OC	R	1 = output overcurrent fault.
3	VIN_UV	R	1 = input undervoltage fault.
2	TEMPERATURE	R	1 = temperature fault or warning.
1	CML	R	1 = communications, memory, or logic fault.
0	NONE_OF_THE_ ABOVE	R	1 = fault or warning not listed in Bits[7:1].

STATUS_WORD REGISTER

A value of 1 in this register indicates that a fault has occurred.

Table 44. Register 0x79—STATUS_WORD

Bits	Bit Name	R/W	Description
15	VOUT	R	1 = output voltage fault or warning.
14	IOUT/POUT	R	1 = output current or output power fault or warning.
13	INPUT	R	1 = input voltage, input current, or input power fault or warning.
12	MFR	R	1 = manufacturer-specific fault or warning.
11	POWER_GOOD#	R	1 = POWER_GOOD is negated.
10	FANS	R	1 = fan or airflow fault or warning.
9	OTHER	R	Always reads as 0.
8	UNKNOWN	R	1 = fault or warning not listed in Bits[15:1].
7	BUSY	R	1 = device was busy and unable to respond.
6	PSON_OFF	R	1 = device is not providing power to the output.
5	VOUT_OV	R	1 = output overvoltage fault.
4	IOUT_OC	R	1 = output overcurrent fault.
3	VIN_UV	R	1 = input undervoltage fault.
2	TEMPERATURE	R	1 = temperature fault or warning.
1	CML	R	1 = communications, memory, or logic fault.
0	NONE_OF_THE_ ABOVE	R	1 = fault or warning not listed in Bits[7:1].

STATUS_VOUT REGISTER

A value of 1 in this register indicates that a fault has occurred.

Table 45. Register 0x7A—STATUS_VOUT

Bits	Bit Name	R/W	Description
7	VOUT_OV_FAULT	R	1 = output overvoltage fault.
6	VOUT_OV_WARN	R	1 = output overvoltage warning.
5	VOUT_UV_WARN	R	1 = output undervoltage warning.
4	VOUT_UV_FAULT	R	1 = output undervoltage fault.

STATUS_INPUT REGISTER

A value of 1 in this register indicates that a fault has occurred.

Table 46. Register 0x7C—STATUS_INPUT

Bits	Bit Name	R/W	Description
7	VIN_OV_FAULT	R	1 = input overvoltage fault.
5	VIN_UV_WARN	R	1 = input undervoltage warning.
4	VIN_UV_FAULT	R	1 = input undervoltage fault.
3	VIN_LOW	R	1 = device is off due to insufficient input voltage; that is, input voltage is below the turn-off threshold.
2	IIN_OC_FAULT	R	1 = input overcurrent fault.
1	IIN_OC_WARN	R	1 = input overcurrent warning.
0	PIN_OP_WARN	R	1 = input overpower warning.

STATUS_TEMPERATURE REGISTER

A value of 1 in this register indicates that a fault has occurred.

Table 47. Register 0x7D—STATUS_TEMPERATURE

Bits	Bit Name	R/W	Description
7	OT_FAULT	R	1 = overtemperature fault.
6	OT_WARN	R	1 = overtemperature warning.
[5:0]	RSVD	R	Reserved.

READ_VIN REGISTER

This register returns the input voltage (V) in VIN linear mode format ($X = Y \times 2^N$).

Table 48. Register 0x88—READ_VIN

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R	Return the exponent (N) used in VIN linear mode format ($X = Y \times 2^N$). The exponent is set in the exponent register (Register 0xFE39, Bits[5:3]).
[10:8]	High bits	R	Mantissa high bits (Y[10:8]) used in VIN linear mode format ($X = Y \times 2^N$).
[7:0]	Low byte	R	Mantissa low byte (Y[7:0]) used in VIN linear mode format ($X = Y \times 2^N$). The exponent (N) is set in the exponent register (Register 0xFE39, Bits[5:3]).

READ_IIN REGISTER

This register returns the input current (A) in current linear mode format ($X = Y \times 2^N$).

Table 49. Register 0x89—READ_IIN

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R	Return the exponent (N) used in current linear mode format ($X = Y \times 2^N$). The exponent is set in the exponent register (Register 0xFE39, Bits[10:6]).
[10:8]	High bits	R	Mantissa high bits (Y[10:8]) used in current linear mode format ($X = Y \times 2^N$).
[7:0]	Low byte	R	Mantissa low byte (Y[7:0]) used in current linear mode format ($X = Y \times 2^N$).

READ_VOUT REGISTER

This register returns the output voltage (V) in VIN linear mode format ($X = Y \times 2^N$).

Table 50. Register 0x8B—READ_VOUT

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R	Return the exponent (N) used in VOUT linear mode format ($X = Y \times 2^N$). The exponent (N) is set in the VOUT_MODE register (Register 0x20, Bits[2:0]). The exponent is in twos complement format.
[10:8]	High bits	R	Mantissa high bits (Y[10:8]) used in VOUT linear mode format ($X = Y \times 2^N$).
[7:0]	Low byte	R	Mantissa low byte (Y[7:0]) used in VOUT linear mode format ($X = Y \times 2^N$).

READ_PIN REGISTER

This register returns the input power (W) in power linear mode format ($X = Y \times 2^N$).

Table 51. Register 0x97—READ_PIN

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R	Return the exponent (N) used in power linear mode format ($X = Y \times 2^N$). The exponent (N) is set in the exponent register (Register 0xFE39, Bits[2:0]).
[10:8]	High bits	R	Mantissa high bits (Y[10:8]) used in power linear mode format ($X = Y \times 2^N$).
[7:0]	Low byte	R	Mantissa low byte (Y[7:0]) used in power linear mode format ($X = Y \times 2^N$).

PMBUS_REVISION REGISTER

Table 52. Register 0x98—PMBUS_REVISION

Bits	Bit Name	R/W	Description
[7:0]	Revision	R	Return the revision of PMBus that the device is compliant with.

MFR_ID REGISTER

Table 53. Register 0x99—MFR_ID

Bits	Bit Name	R/W	Description
[7:0]	MFR_ID	R	Return the manufacturer's ID.

MFR_MODEL REGISTER

Table 54. Register 0x9A—MFR_MODEL

Bits	Bit Name	R/W	Description
[7:0]	Model	R	Return the manufacturer's model number.

MFR_REVISION REGISTER

Table 55. Register 0x9B—MFR_REVISION

Bits	Bit Name	R/W	Description
[7:0]	Revision	R	Return the manufacturer's revision number.

EEPROM_DATA_00 Through EEPROM_DATA_15 COMMANDS

Code 0xB0 through Code 0xBF, read/write block. The EEPROM_DATA_00 through EEPROM_DATA_15 commands are used to read data from the EEPROM and write data to the EEPROM. EEPROM_DATA_00 reads from and writes to Page 0 of the EEPROM main block; EEPROM_DATA_01 reads from and writes to Page 1 of the EEPROM main block, and so on.

EEPROM_CRC_CHKSUM REGISTER

Table 56. Register 0xD1—EEPROM_CRC_CHKSUM

Bits	Bit Name	R/W	Description
[7:0]	CRC checksum	R	Return the CRC checksum value from the EEPROM download operation.

EEPROM_NUM_RD_BYTES REGISTER

Table 57. Register 0xD2—EEPROM_NUM_RD_BYTES

Bits	Bit Name	R/W	Description
[7:0]	Number of read bytes returned	R/W	These bits set the number of read bytes returned when using the EEPROM_DATA_xx commands.

EEPROM_ADDR_OFFSET REGISTER

Table 58. Register 0xD3—EEPROM_ADDR_OFFSET

Bits	Bit Name	R/W	Description
[15:0]	Address offset	R/W	These bits set the address offset of the current EEPROM page.

EEPROM_PAGE_ERASE REGISTER

Table 59. Register 0xD4—EEPROM_PAGE_ERASE

Bits	Bit Name	R/W	Description
[7:0]	Page erase	W	Perform a page erase on the selected EEPROM page. (Wait 35 ms after each page erase operation.) EEPROM must first be unlocked. Page 0 and Page 1 erase are allowed only in manufacturing test mode.

EEPROM_PASSWORD REGISTER

Table 60. Register 0xD5—EEPROM_PASSWORD

Bits	Bit Name	R/W	Description
[7:0]	EEPROM password	W	Write the password to this register to unlock EEPROM and/or to change the EEPROM password.

TRIM_PASSWORD REGISTER

Table 61. Register 0xD6—TRIM_PASSWORD

Bits	Bit Name	R/W	Description
[7:0]	Trim password	W	Write the password to this register to unlock the trim registers for write access. Write the trim password twice (default 0x00) to unlock the register; write any other value to exit.

EEPROM_INFO COMMAND

Code 0xF1, block read/write. This command reads the manufacturer's data from the EEPROM.

CS_FAST_OCP_RESPONSE REGISTER

This register instructs the device on actions to take due to a fast overcurrent protection condition.

Table 62. Register 0xFE00—CS_FAST_OCP_RESPONSE

Bits	Bit Name	R/W	Description		
[7:6]	Response	R/W	These bits determine the device response to a fast overcurrent protection condition.		
			Bit 7	**Bit 6**	**Response**
			0	0	Ignore (still terminate the PWM pulse).
			0	1	Allow the number of switching cycles specified in Bits[5:4], then shut down and soft start (use the soft start delay time specified in Register 0x5C, Bits[2:0]).
			1	0	Allow the number of switching cycles specified in Bits[5:4] (terminating the PWM pulse each time), then shut down and wait for the PSON signal to soft start.
			1	1	Disable the PWM output after the number of switching cycles specified in Bits[5:4] and wait for the flag to be cleared.
[5:4]	N-time	R/W	These bits determine the number of switching cycles allowed before the device disables the PWM output after a fast overcurrent condition is detected.		
			Bit 5	**Bit 4**	**Number of Switching Cycles**
			0	0	1
			0	1	2
			1	0	4
			1	1	8
[3:0]	RSVD	R	Reserved.		

OVP_FAST_OVP_RESPONSE REGISTER

This register instructs the device on actions to take due to a fast overvoltage fault condition.

Table 63. Register 0xFE01—OVP_FAST_OVP_RESPONSE

Bits	Bit Name	R/W	Description		
[7:6]	Response	R/W	These bits determine the device response to a fast overvoltage condition.		
			Bit 7	**Bit 6**	**Response**
			0	0	Ignore (do nothing; PWM continues).
			0	1	Shut down and soft start.
			1	0	Shut down immediately and wait for the PSON signal.
			1	1	Disable the PWM output until the unlatched flag is cleared.
[5:0]	RSVD	R	Reserved.		

OLP_RESPONSE REGISTER

This register instructs the device on actions to take due to an open-loop fault condition.

Table 64. Register 0xFE02—OLP_RESPONSE

Bits	Bit Name	R/W	Description		
[7:6]	Response	R/W	These bits determine the device response to an open-loop fault condition.		
			Bit 7	**Bit 6**	**Response**
			0	0	Ignore (do nothing; PWM continues).
			0	1	Shut down and soft start.
			1	0	Shut down immediately and wait for the PSON signal.
			1	1	Disable the PWM output until the unlatched flag is cleared.
[5:0]	RSVD	R	Reserved.		

VDD3P3_RESPONSE REGISTER

This register instructs the device on actions to take due to a VDD overvoltage fault condition.

Table 65. Register 0xFE03—VDD3P3_RESPONSE

Bits	Bit Name	R/W	Description
7	RSVD	R	Reserved.
6	Save first flag ID to EEPROM	R/W	1 = save the first flag ID to EEPROM when the device shuts down. 0 = do not save the first flag ID to EEPROM when the device shuts down.
[5:3]	Retry wait time	R/W	These bits determine the retry wait time before the next soft start. Each LSB = 588 ms.
2	Reload EEPROM	R/W	1 = reload the contents of EEPROM. 0 = do not reload the contents of EEPROM.
1	Debounce time	R/W	1 = 2.56 µs. 0 = 660 µs.
0	Ignore VDD OV	R/W	1 = ignore the VDD 3.3 V overvoltage fault. 0 = do not ignore the VDD 3.3 V overvoltage fault.

VCORE_RESPONSE REGISTER

This register instructs the device on actions to take due to a VCORE overvoltage fault condition.

Table 66. Register 0xFE04—VCORE_RESPONSE

Bits	Bit Name	R/W	Description
7	RSVD	R	Reserved.
6	Save first flag ID to EEPROM	R/W	1 = save the first flag ID to EEPROM when the device shuts down. 0 = do not save the first flag ID to EEPROM when the device shuts down.
[5:3]	Retry wait time	R/W	These bits determine the retry wait time before the next soft start. Each LSB = 588 ms.
2	Reload EEPROM	R/W	1 = reload the contents of EEPROM. 0 = do not reload the contents of EEPROM.
1	Debounce time	R/W	1 = 2.56 µs. 0 = 660 µs.
0	Ignore VCORE OV	R/W	1 = ignore the VCORE overvoltage fault. 0 = do not ignore the VCORE overvoltage fault.

PGOOD_AC_OK_DEBOUNCE_SET REGISTER

This register sets the debounce times for the PGOOD and AC_OK pins.

Table 67. Register 0xFE05—PGOOD_AC_OK_DEBOUNCE_SET

Bits	Bit Name	R/W	Description		
[7:6]	Debounce time, AC_OK pin (low to high)	R/W	Debounce from low to high for the AC_OK pin.		
			Bit 7	**Bit 6**	**Time**
			0	0	0 ms
			0	1	200 ms
			1	0	320 ms
			1	1	600 ms
[5:4]	Debounce time, AC_OK pin (high to low)	R/W	Debounce from high to low for the AC_OK pin.		
			Bit 5	**Bit 4**	**Time**
			0	0	0 ms
			0	1	200 ms
			1	0	320 ms
			1	1	600 ms

Bits	Bit Name	R/W	Description		
[3:2]	Debounce time, PGOOD pin (low to high)	R/W	Debounce from low to high for the PGOOD pin.		
			Bit 3	**Bit 2**	**Time**
			0	0	0 ms
			0	1	200 ms
			1	0	320 ms
			1	1	600 ms
[1:0]	Debounce time, PGOOD pin (high to low)	R/W	Debounce from high to low for the PGOOD pin.		
			Bit 1	**Bit 0**	**Time**
			0	0	0 ms
			0	1	200 ms
			1	0	320 ms
			1	1	600 ms

PSON_SET REGISTER

This register sets the delay time for PSON and PSOFF.

Table 68. Register 0xFE06—PSON_SET

Bits	Bit Name	R/W	Description				
[7:4]	RSVD	R	Reserved.				
[3:2]	PSON delay	R/W	These bits specify the time from when the PSON signal is active to when soft start begins.				
					Delay Time		
			Bit 3	**Bit 2**	**Min**	**Typ**	**Max**
			0	0	0 ms	0 ms	0 ms
			0	1	40 ms	50 ms	82 ms
			1	0	209 ms	250 ms	252 ms
			1	1	964 ms	1000 ms	1007 ms
[1:0]	PSOFF delay	R/W	These bits specify the time from when the PSON signal is cleared to when the device is turned off.				
					Delay Time		
			Bit 1	**Bit 0**	**Min**	**Typ**	**Max**
			0	0	0 ms	0 ms	0 ms
			0	1	40 ms	50 ms	82 ms
			1	0	209 ms	250 ms	252 ms
			1	1	964 ms	1000 ms	1007 ms

FLAG_FAULT_ID REGISTER

This register records the first fault ID that caused the system to shut down.

Table 69. Register 0xFE07—FLAG_FAULT_ID

Bits	Bit Name	R/W	Description				
[7:4]	Previous fault flag ID	R	Return the flag fault ID value of the fault that occurred just before the flag that caused the shutdown (identified in Bits[3:0]).				
[3:0]	Fault flag ID	R	Return the flag fault ID value of the fault that caused the shutdown.				
			Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Fault**
			0	0	0	1	VOUT_OV_FAULT
			0	0	1	0	VOUT_UV_FAULT
			0	0	1	1	OT_FAULT
			0	1	0	0	VIN_OV_FAULT
			0	1	0	1	VIN_UV_FAULT
			0	1	1	0	IIN_OC_FAULT
			0	1	1	1	OLP_FAULT
			1	0	0	0	FAST_OVP_FAULT
			1	0	0	1	FAST_OCP_FAULT
			1	0	1	0	VDD_33V_OV_FAULT
			1	0	1	1	VCORE_25V_OV_FAULT

SOFTSTART_FLAGS_BLANK1 REGISTER

This register blanks the specified flags during soft start (1 = blank, 0 = don't blank).

Table 70. Register 0xFE08—SOFTSTART_FLAGS_BLANK1

Bits	Bit Name	R/W	Description
7	BLANK_FAST_OVP	R/W	1 = ignore fast OVP flag.
6	BLANK_OLP	R/W	1 = ignore OLP flag.
5	BLANK_IIN_OC	R/W	1 = ignore IIN_OC_FAULT flag.
4	BLANK_VIN_OFF	R/W	1 = ignore VIN_OFF flag.
3	BLANK_VIN_OV	R/W	1 = ignore VIN_OV flag.
2	BLANK_OT	R/W	1 = ignore OT flag.
1	BLANK_VOUT_UV	R/W	1 = ignore VOUT_UV flag.
0	BLANK_VOUT_OV	R/W	1 = ignore VOUT_OV flag.

SOFTSTART_FLAGS_BLANK2 REGISTER

This register blanks the specified flag during soft start (1 = blank, 0 = don't blank).

Table 71. Register 0xFE09—SOFTSTART_FLAGS_BLANK2

Bits	Bit Name	R/W	Description
0	BLANK_FAST_OCP	R/W	1 = ignore fast OCP flag.

PGOOD_FLAGS_LIST REGISTER

This register specifies the flags that are checked to determine the PGOOD pin voltage (1 = ignore flag, 0 = check flag).

Table 72. Register 0xFE0A—PGOOD_FLAGS_LIST

Bits	Bit Name	R/W	Description
7	VOUT_UV_FAULT	R/W	1 = ignore VOUT_UV_FAULT flag.
6	VOUT_OV_WARN	R/W	1 = ignore VOUT_OV_WARN flag.
5	FAST_OVP	R/W	1 = ignore FAST_OVP flag.
4	OLP	R/W	1 = ignore OLP flag.
3	FAST_OCP	R/W	1 = ignore FAST_OCP flag.
2	IIN_OC_FAULT	R/W	1 = ignore IIN_OC_FAULT flag.
1	OT_FAULT	R/W	1 = ignore OT_FAULT flag.
0	FAST_LOOP	R/W	1 = ignore FAST_LOOP flag.

AC_OK_FLAGS_LIST REGISTER

This register specifies the flags that are checked to determine the AC_OK pin voltage (1 = ignore flag, 0 = check flag).

Table 73. Register 0xFE0B—AC_OK_FLAGS_LIST

Bits	Bit Name	R/W	Description
7	VIN_UV_FAULT	R/W	1 = ignore VIN_UV_FAULT flag.
6	VIN_UV_WARN	R/W	1 = ignore VIN_UV_WARN flag.
5	IIN_OC_FAULT	R/W	1 = ignore IIN_OC_FAULT flag.
4	IIN_OC_WARN	R/W	1 = ignore IIN_OC_WARN flag.
3	FAST_OCP	R/W	1 = ignore FAST_OCP flag.
2	AC_LINE_PERIOD	R/W	1 = ignore AC_LINE_PERIOD flag.
1	BROWN_OUT	R/W	1 = ignore BROWN_OUT flag.
0	INRUSH	R/W	1 = ignore INRUSH flag.

PWM AND PWM2 TIMING REGISTERS

Register 0xFE0C through Register 0xFE13 configure the rising and falling edges of the PWM outputs.

Table 74. Register 0xFE0C—PWM Rising Edge Timing (PWM Pin)

Bits	Bit Name	R/W	Description
[7:0]	t_1	R/W	This register contains the eight MSBs of the 10-bit t_1 time.

Table 75. Register 0xFE0D—PWM Rising Edge Setting (PWM Pin)

Bits	Bit Name	R/W	Description
[7:4]	RSVD	R	Reserved.
[3:2]	t_1	R/W	These bits contain the two LSBs of the 10-bit t_1 time. This value is always used with the eight bits of Register 0xFE0C, which contains the eight MSBs of the t_1 time.
1	Modulate enable	R/W	1 = PWM modulation acts on the t_1 edge. 0 = no PWM modulation of the t_1 edge.
0	t_1 sign	R/W	1 = positive sign. Increase of PWM modulation moves t_1 right. 0 = negative sign. Increase of PWM modulation moves t_1 left.

Table 76. Register 0xFE0E—PWM Falling Edge Timing (PWM Pin)

Bits	Bit Name	R/W	Description
[7:0]	t_2	R/W	This register contains the eight MSBs of the 10-bit t_2 time.

Table 77. Register 0xFE0F—PWM Falling Edge Setting (PWM Pin)

Bits	Bit Name	R/W	Description
[7:4]	RSVD	R	Reserved.
[3:2]	t_2	R/W	These bits contain the two LSBs of the 10-bit t_2 time. This value is always used with the eight bits of Register 0xFE0E, which contains the eight MSBs of the t_2 time.
1	Modulate enable	R/W	1 = PWM modulation acts on the t_2 edge. 0 = no PWM modulation of the t_2 edge.
0	t_2 sign	R/W	1 = positive sign. Increase of PWM modulation moves t_2 right. 0 = negative sign. Increase of PWM modulation moves t_2 left.

Table 78. Register 0xFE10—PWM2 Rising Edge Timing (PWM2 Pin)

Bits	Bit Name	R/W	Description
[7:0]	t_1	R/W	This register contains the eight MSBs of the 10-bit t_1 time.

Table 79. Register 0xFE11—PWM2 Rising Edge Setting (PWM2 Pin)

Bits	Bit Name	R/W	Description
[7:4]	RSVD	R	Reserved.
[3:2]	t_1	R/W	These bits contain the two LSBs of the 10-bit t_1 time. This value is always used with the eight bits of Register 0xFE10, which contains the eight MSBs of the t_1 time.
1	Modulate enable	R/W	1 = PWM modulation acts on the t_1 edge. 0 = no PWM modulation of the t_1 edge.
0	t_1 sign	R/W	1 = positive sign. Increase of PWM modulation moves t_1 right. 0 = negative sign. Increase of PWM modulation moves t_1 left.

Table 80. Register 0xFE12—PWM2 Falling Edge Timing (PWM2 Pin)

Bits	Bit Name	R/W	Description
[7:0]	t_2	R/W	This register contains the eight MSBs of the 10-bit t_2 time.

Table 81. Register 0xFE13—PWM2 Falling Edge Setting (PWM2 Pin)

Bits	Bit Name	R/W	Description
[7:4]	RSVD	R	Reserved.
[3:2]	t_2	R/W	These bits contain the two LSBs of the 10-bit t_2 time. This value is always used with the eight bits of Register 0xFE12, which contains the eight MSBs of the t_2 time.
1	Modulate enable	R/W	1 = PWM modulation acts on the t_2 edge. 0 = no PWM modulation of the t_2 edge.
0	t_2 sign	R/W	1 = positive sign. Increase of PWM modulation moves t_2 right. 0 = negative sign. Increase of PWM modulation moves t_2 left.

PWM_SET REGISTER

Table 82. Register 0xFE14—PWM_SET

Bits	Bit Name	R/W	Description
[7:5]	RSVD	R	Reserved.
4	ADP1048 operation	R/W	Reserved for the ADP1048 only. 1 = bridgeless PFC operation. 0 = interleaved PFC operation.
3	PWM resolution	R/W	1 = 5 ns. 0 = 40 ns.
2	PWM enable	R/W	1 = disable the PWM output. 0 = enable the PWM output.
1	PWM2 enable	R/W	1 = disable the PWM2 output. 0 = enable the PWM2 output.
0	Go button	R/W	The PWM settings are updated during the transition of this bit from low to high.

PWM_LIMIT REGISTER

Table 83. Register 0xFE15—PWM_LIMIT

Bits	Bit Name	R/W	Description
[7:4]	Limit minimum on time	R/W	These bits set the minimum on time for the PWM outputs in steps of 80 ns: 0000 = 0 ns and 1111 = 1200 ns.
[3:0]	Limit minimum off time	R/W	These bits set the minimum off time for the PWM outputs: 0000 = 40 ns, 0001 = 80 ns, 1111 = 1200 ns.

RTD ADC OFFSET TRIM SETTING (MSB) REGISTER

This register must be unlocked for write access; see Table 61.

Table 84. Register 0xFE16—RTD ADC Offset Trim Setting (MSB)

Bits	Bit Name	R/W	Description
[7:2]	RSVD	R/W	Reserved.
1	Trim polarity	R/W	1 = negative offset trim is introduced. 0 = positive offset trim is introduced.
0	RTD ADC offset trim	R/W	This bit is the MSB of the 9-bit value that sets the amount of offset trim applied to the RTD ADC reading. The LSBs are specified in Register 0xFE17.

RTD ADC OFFSET TRIM SETTING (LSB) REGISTER

This register must be unlocked for write access; see Table 61.

Table 85. Register 0xFE17—RTD ADC Offset Trim Setting (LSB)

Bits	Bit Name	R/W	Description
[7:0]	RTD ADC offset trim	R/W	These eight bits are the LSBs of the 9-bit value that sets the amount of offset trim applied to the RTD ADC reading. The MSB is specified in Register 0xFE16, Bit 0.

RTD ADC GAIN TRIM SETTING REGISTER

This register must be unlocked for write access; see Table 61.

Table 86. Register 0xFE18—RTD ADC Gain Trim Setting

Bits	Bit Name	R/W	Description
7	Gain polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	RTD ADC gain trim	R/W	This value sets the amount of gain trim that is applied to the RTD sensing gain.

OT_FAULT_LIMIT REGISTER

This register sets the overtemperature fault threshold. The debounce time of the overtemperature fault flag is 100 ms.

Table 87. Register 0xFE19—OT_FAULT_LIMIT

Bits	Bit Name	R/W	Description
[7:0]	OT fault threshold	R/W	Overtemperature fault threshold. This register, adding 0 as the MSB, results in a 9-bit threshold value. This 9-bit value is compared to the nine MSBs of the RTD ADC reading. If the RTD ADC reading is lower than the threshold set by these bits, the overtemperature fault flag is set. These eight bits provide 256 threshold settings from 0 mV to 800 mV (one LSB = 800 mV/256 = 3.125 mV). However, the lowest allowed value is 9.375 mV (0x03), and the highest allowed value is 781.25 mV (0xFA).

Bit 7	Bit 6	…	Bit 3	Bit 2	Bit 1	Bit 0	OTP Threshold (mV)
0	0	…	0	0	1	1	9.375
0	0	…	0	1	0	0	12.5
0	0	…	0	1	0	1	15.875
…	…	…	…	…	…	…	…
1	1	…	1	0	0	1	778.125
1	1	…	1	0	1	0	781.25

OT_WARN_LIMIT REGISTER

This register sets the overtemperature warning threshold. The debounce time of the overtemperature warning flag is 100 ms.

Table 88. Register 0xFE1A—OT_WARN_LIMIT

Bits	Bit Name	R/W	Description
[7:0]	OT warning threshold	R/W	Overtemperature warning threshold. This register, adding 0 as the MSB, results in a 9-bit threshold value. This 9-bit value is compared to the nine MSBs of the RTD ADC reading. If the RTD ADC reading is lower than the threshold set by these bits, the overtemperature warning flag is set. These eight bits provide 256 threshold settings from 0 mV to 800 mV (one LSB = 800 mV/256 = 3.125 mV). However, the lowest allowed value is 9.375 mV (0x03), and the highest allowed value is 781.25 mV (0xFA).

Bit 7	Bit 6	…	Bit 3	Bit 2	Bit 1	Bit 0	OTP Threshold (mV)
0	0	…	0	0	1	1	9.375
0	0	…	0	1	0	0	12.5
0	0	…	0	1	0	1	15.875
…	…	…	…	…	…	…	…
1	1	…	1	0	0	1	778.125
1	1	…	1	0	1	0	781.25

SWITCHING FREQUENCY SETTING REGISTER

Table 89. Register 0xFE1B—Switching Frequency Setting

Bits	Bit Name	R/W	Description						
[7:6]	RSVD	R	Reserved.						
[5:0]	Switching frequency	R/W	This register sets the switching frequency of the PWM outputs.						
			Bit 5	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Frequency (kHz)**
			0	0	0	0	0	0	30.05
			0	0	0	0	0	1	32.55
			0	0	0	0	1	0	35.51
			0	0	0	0	1	1	39.06
			0	0	0	1	0	0	43.40
			0	0	0	1	0	1	48.83
			0	0	0	1	1	0	52.06
			0	0	0	1	1	1	55.80
			0	0	1	0	0	0	60.10
			0	0	1	0	0	1	65.10
			0	0	1	0	1	0	71.02
			0	0	1	0	1	1	78.13
			0	0	1	1	0	0	86.81
			0	0	1	1	0	1	97.66
			0	0	1	1	1	0	100.81
			0	0	1	1	1	1	104.17
			0	1	0	0	0	0	107.76
			0	1	0	0	0	1	111.61
			0	1	0	0	1	0	115.74
			0	1	0	0	1	1	120.19
			0	1	0	1	0	0	125.00
			0	1	0	1	0	1	130.21
			0	1	0	1	1	0	135.87
			0	1	0	1	1	1	142.05
			0	1	1	0	0	0	148.81
			0	1	1	0	0	1	156.25
			0	1	1	0	1	0	164.47
			0	1	1	0	1	1	173.61
			0	1	1	1	0	0	183.82
			0	1	1	1	0	1	195.31
			0	1	1	1	1	0	198.41
			0	1	1	1	1	1	201.61
			1	0	0	0	0	0	204.92
			1	0	0	0	0	1	208.33
			1	0	0	0	1	0	211.86
			1	0	0	0	1	1	215.52
			1	0	0	1	0	0	219.30
			1	0	0	1	0	1	223.21
			1	0	0	1	1	0	227.27
			1	0	0	1	1	1	231.48
			1	0	1	0	0	0	235.85
			1	0	1	0	0	1	240.38
			1	0	1	0	1	0	245.10
			1	0	1	0	1	1	250.00
			1	0	1	1	0	0	255.10
			1	0	1	1	0	1	260.42
			1	0	1	1	1	0	265.96

Bits	Bit Name	R/W	Description						
[5:0]	Switching frequency	R/W	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Frequency (kHz)**
			1	0	1	1	1	1	271.74
			1	1	0	0	0	0	277.78
			1	1	0	0	0	1	284.09
			1	1	0	0	1	0	290.70
			1	1	0	0	1	1	297.62
			1	1	0	1	0	0	304.88
			1	1	0	1	0	1	312.50
			1	1	0	1	1	0	320.51
			1	1	0	1	1	1	328.95
			1	1	1	0	0	0	337.84
			1	1	1	0	0	1	347.22
			1	1	1	0	1	0	357.14
			1	1	1	0	1	1	367.65
			1	1	1	1	0	0	378.79
			1	1	1	1	0	1	390.63
			1	1	1	1	1	0	403.23
			1	1	1	1	1	1	403.23

LOW POWER SWITCHING FREQUENCY SETTING REGISTER

This register sets the PFC switching frequency when the PFC is running under low power mode and the smart switching frequency operation is enabled.

Table 90. Register 0xFE1C—Low Power Switching Frequency Setting

Bits	Bit Name	R/W	Description						
[7:6]	RSVD	R	Reserved.						
[5:0]	Switching frequency	R/W	This register sets the switching frequency when the power is lower than the low power threshold set in Register 0xFE32 and the smart switching frequency is enabled.						
			Bit 5	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Frequency (kHz)**
			0	0	0	0	0	0	30.05
			0	0	0	0	0	1	32.55
			0	0	0	0	1	0	35.51
			0	0	0	0	1	1	39.06
			0	0	0	1	0	0	43.40
			0	0	0	1	0	1	48.83
			0	0	0	1	1	0	52.06
			0	0	0	1	1	1	55.80
			0	0	1	0	0	0	60.10
			0	0	1	0	0	1	65.10
			0	0	1	0	1	0	71.02
			0	0	1	0	1	1	78.13
			0	0	1	1	0	0	86.81
			0	0	1	1	0	1	97.66
			0	0	1	1	1	0	100.81
			0	0	1	1	1	1	104.17
			0	1	0	0	0	0	107.76
			0	1	0	0	0	1	111.61
			0	1	0	0	1	0	115.74
			0	1	0	0	1	1	120.19
			0	1	0	1	0	0	125.00
			0	1	0	1	0	1	130.21
			0	1	0	1	1	0	135.87
			0	1	0	1	1	1	142.05

Bits	Bit Name	R/W	Description						
[5:0]	Switching frequency	R/W	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Frequency (kHz)**
			0	1	1	0	0	0	148.81
			0	1	1	0	0	1	156.25
			0	1	1	0	1	0	164.47
			0	1	1	0	1	1	173.61
			0	1	1	1	0	0	183.82
			0	1	1	1	0	1	195.31
			0	1	1	1	1	0	198.41
			0	1	1	1	1	1	201.61
			1	0	0	0	0	0	204.92
			1	0	0	0	0	1	208.33
			1	0	0	0	1	0	211.86
			1	0	0	0	1	1	215.52
			1	0	0	1	0	0	219.30
			1	0	0	1	0	1	223.21
			1	0	0	1	1	0	227.27
			1	0	0	1	1	1	231.48
			1	0	1	0	0	0	235.85
			1	0	1	0	0	1	240.38
			1	0	1	0	1	0	245.10
			1	0	1	0	1	1	250.00
			1	0	1	1	0	0	255.10
			1	0	1	1	0	1	260.42
			1	0	1	1	1	0	265.96
			1	0	1	1	1	1	271.74
			1	1	0	0	0	0	277.78
			1	1	0	0	0	1	284.09
			1	1	0	0	1	0	290.70
			1	1	0	0	1	1	297.62
			1	1	0	1	0	0	304.88
			1	1	0	1	0	1	312.50
			1	1	0	1	1	0	320.51
			1	1	0	1	1	1	328.95
			1	1	1	0	0	0	337.84
			1	1	1	0	0	1	347.22
			1	1	1	0	1	0	357.14
			1	1	1	0	1	1	367.65
			1	1	1	1	0	0	378.79
			1	1	1	1	0	1	390.63
			1	1	1	1	1	0	403.23
			1	1	1	1	1	1	403.23

FREQUENCY DITHERING SET REGISTER

Table 91. Register 0xFE1D—Frequency Dithering Set

Bits	Bit Name	R/W	Description
7	RSVD	R	Reserved.
[6:0]	Dithering period	R/W	Sets the period for updating the switching frequency. Each LSB corresponds to 40 µs.

FREQUENCY SYNCHRONIZATION SET REGISTER

Table 92. Register 0xFE1E—Frequency Synchronization Set

Bits	Bit Name	R/W	Description		
[7:2]	RSVD	R/W	Reserved.		
[1:0]	Frequency division	R/W	Sets the frequency division between the switching frequency and the external SYNC clock (f_{SW}/f_{SYNC_EXT}).		
			Bit 1	**Bit 0**	**Frequency Division**
			0	0	1
			0	1	1/2
			1	0	1/3
			1	1	1/4

VOLTAGE LOOP FILTER GAIN REGISTER

Table 93. Register 0xFE20—Voltage Loop Filter Gain

Bits	Bit Name	R/W	Description
[7:0]	Voltage loop filter gain	R/W	Determines the digital filter gain of the PFC voltage loop.

VOLTAGE LOOP FILTER ZERO REGISTER

Table 94. Register 0xFE21—Voltage Loop Filter Zero

Bits	Bit Name	R/W	Description
[7:0]	Voltage loop filter zero	R/W	Determines the position of the digital filter zero of the PFC voltage loop.

FAST VOLTAGE LOOP FILTER GAIN REGISTER

Table 95. Register 0xFE22—Fast Voltage Loop Filter Gain

Bits	Bit Name	R/W	Description
[7:0]	Fast voltage loop filter gain	R/W	Determines the digital filter gain of the PFC fast voltage loop.

FAST VOLTAGE LOOP FILTER ZERO REGISTER

Table 96. Register 0xFE23—Fast Voltage Loop Filter Zero

Bits	Bit Name	R/W	Description
[7:0]	Fast voltage loop filter zero	R/W	Determines the position of the digital filter zero of the PFC fast voltage loop.

FAST VOLTAGE LOOP ENABLE REGISTER

Table 97. Register 0xFE24—Fast Voltage Loop Enable

Bits	Bit Name	R/W	Description		
7	Enable fast loop for line transient	R/W	Enables fast loop mode immediately after the overshoot becomes larger than the regulation band plus 3%. 1 = enable fast loop mode. 0 = disable fast loop mode.		
[6:5]	Regulation band limit	R/W	Sets the threshold of the regulation band limit for switching from the normal filter to the fast loop filter.		
			Bit 6	**Bit 5**	**Threshold**
			0	0	±1.5625%
			0	1	±3.125%
			1	0	±6.25%
			1	1	±12.5%

Bits	Bit Name	R/W	Description
[4:2]	Delay time	R/W	Delay time before switching from the fast loop filter back to the normal filter after the output voltage is within the regulation band (Bits[6:5]).

Bit 4	Bit 3	Bit 2	Number of Half AC Line Cycles
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

1	Enable fast loop during soft start	R/W	Enables the fast loop filter during soft start. 1 = fast loop filter is used during soft start. 0 = normal filter is used during soft start.
0	Enable fast loop	R/W	Enables the fast loop filter with a delay. The threshold is programmed in Bits[6:5]. 1 = enable fast loop filter. 0 = disable fast loop filter.

VAC_THRESHOLD_SET REGISTER

This register sets the input voltage threshold for input ac line period measurement and zero-crossing detection.

Table 98. Register 0xFE25—VAC_THRESHOLD_SET

Bits	Bit Name	R/W	Description
7	Enable automatic threshold	R/W	1 = enable automatic threshold. 0 = disable automatic threshold.
[6:0]	Threshold voltage	R/W	These bits set the threshold voltage to detect the ac line frequency and period if Bit 7 is set to 0.

VAC_THRESHOLD_READ REGISTER

Table 99. Register 0xFE26—VAC_THRESHOLD_READ

Bits	Bit Name	R/W	Description
7	RSVD	R	Reserved.
[6:0]	VAC average reading	R	Return the reading of the threshold voltage to detect the ac line frequency and period if the automatic threshold is enabled in Register 0xFE25, Bit 7.

MIN_AC_PERIOD_SET REGISTER

Table 100. Register 0xFE27—MIN_AC_PERIOD_SET

Bits	Bit Name	R/W	Description
[7:0]	Minimum ac line period	R/W	These bits set the minimum ac line period of the input voltage. Each LSB corresponds to 163.84 µs resolution.

MAX_AC_PERIOD_SET REGISTER

Table 101. Register 0xFE28—MAX_AC_PERIOD_SET

Bits	Bit Name	R/W	Description
[7:0]	Maximum ac line period	R/W	These bits set the maximum ac line period of the input voltage. Each LSB corresponds to 163.84 µs resolution.

CURRENT LOOP FILTER GAIN FOR LOW LINE INPUT REGISTER

Table 102. Register 0xFE29—Current Loop Filter Gain for Low Line Input

Bits	Bit Name	R/W	Description
[7:0]	Current loop filter gain for low line	R/W	These bits set the current loop digital filter gain of the PFC current loop under the low line input voltage.

CURRENT LOOP FILTER ZERO FOR LOW LINE INPUT REGISTER

Table 103. Register 0xFE2A—Current Loop Filter Zero for Low Line Input

Bits	Bit Name	R/W	Description
[7:0]	Current loop filter zero for low line	R/W	These bits set the current loop digital filter zero of the PFC current loop under the low line input voltage.

CURRENT LOOP FILTER GAIN FOR HIGH LINE INPUT REGISTER

Table 104. Register 0xFE2B—Current Loop Filter Gain for High Line Input

Bits	Bit Name	R/W	Description
[7:0]	Current loop filter gain for high line	R/W	These bits set the current loop digital filter gain of the PFC current loop under the high line input voltage.

CURRENT LOOP FILTER ZERO FOR HIGH LINE INPUT REGISTER

Table 105. Register 0xFE2C—Current Loop Filter Zero for High Line Input

Bits	Bit Name	R/W	Description
[7:0]	Current loop filter zero for high line	R/W	These bits set the current loop digital filter zero of the PFC current loop under the high line input voltage.

SOFT START SET REGISTER

Table 106. Register 0xFE2D—Soft Start Set

Bits	Bit Name	R/W	Description			
[7:6]	RSVD	R	Reserved.			
[5:3]	Soft start delay time	R/W	These bits set the delay time between the inrush signal and the beginning of the soft start.			
			Bit 5	**Bit 4**	**Bit 3**	**Number of Full AC Line Cycles**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	7
[2:0]	Soft start time	R/W	These bits set the soft start time.			
			Bit 2	**Bit 1**	**Bit 0**	**Time**
			0	0	0	112 ms
			0	0	1	168 ms
			0	1	0	224 ms
			0	1	1	280 ms
			1	0	0	392 ms
			1	0	1	504 ms
			1	1	0	616 ms
			1	1	1	728 ms

INRUSH SET REGISTER

Table 107. Register 0xFE2E—Inrush Set

Bits	Bit Name	R/W	Description			
[7:5]	RSVD	R	Reserved.			
[4:3]	Timer	R/W	These bits set the timer for the VIN_LOW flag measurement.			
			Bit 4	**Bit 3**	**Timer**	
			0	0	Quarter line cycle	
			0	1	Half line cycle	
			1	0	2 ms	
			1	1	4 ms	
[2:0]	Inrush delay time	R/W	These bits set the inrush signal delay time after the BROWN_OUT flag goes low.			
			Bit 2	**Bit 1**	**Bit 0**	**Number of Full AC Line Cycles**
			0	0	0	0
			0	0	1	1
			0	1	0	2
			0	1	1	3
			1	0	0	4
			1	0	1	5
			1	1	0	6
			1	1	1	7

FAST_OVP_FAULT_RISE REGISTER

Table 108. Register 0xFE2F—FAST_OVP_FAULT_RISE

Bits	Bit Name	R/W	Description
7	RSVD	R	Reserved.
[6:0]	Fast OVP rise threshold	R/W	These bits set the rising threshold for the analog comparator at the OVP pin input as follows: *OVP threshold* = (*Code* × 0.492/128) + 1. This threshold is programmable from 1 V to 1.5 V. Each LSB increments the threshold by 3.844 mV. A value of 0x00 corresponds to a 1 V threshold; a value of 0x3F corresponds to a 1.492 V threshold.

FAST_OVP_FAULT_FALL REGISTER

Table 109. Register 0xFE30—FAST_OVP_FAULT_FALL

Bits	Bit Name	R/W	Description
7	RSVD	R	Reserved.
[6:0]	Fast OVP fall threshold	R/W	These bits set the falling threshold for the analog comparator at the OVP pin input as follows: *OVP threshold* = (*Code* × 0.492/128) + 1. This threshold is programmable from 1 V to 1.5 V. Each LSB increments the threshold by 3.844 mV. A value of 0x00 corresponds to a 1 V threshold; a value of 0x3F corresponds to a 1.492 V threshold.

FAST OVP DEBOUNCE TIME SETTING REGISTER

Table 110. Register 0xFE31—Fast OVP Debounce Time Setting

Bits	Bit Name	R/W	Description		
[7:2]	RSVD	R	Reserved.		
[1:0]	OVP debounce time	R/W	These bits set the fast OVP debounce time.		
			Bit 1	**Bit 0**	**Time**
			0	0	120 ns
			0	1	240 ns
			1	0	480 ns
			1	1	640 ns

LOW POWER MODE OPERATION THRESHOLD REGISTER

Table 111. Register 0xFE32—Low Power Mode Operation Threshold

Bits	Bit Name	R/W	Description
[7:0]	Low power threshold	R/W	These bits set the threshold value (P_{TH}) for low power mode detection. When the input power is lower than this value, the PFC enters low power mode.

POWER METERING OFFSET TRIM FOR LOW LINE INPUT REGISTER

Table 112. Register 0xFE33—Power Metering Offset Trim for Low Line Input

Bits	Bit Name	R/W	Description
7	Offset trim polarity	R/W	1 = negative offset trim is introduced. 0 = positive offset trim is introduced.
[6:0]	Power meter offset trim	R/W	This value calibrates the power meter offset at the low line input voltage. Each LSB corresponds to 0.0625/128 of the full input power.

POWER METERING GAIN TRIM FOR LOW LINE INPUT REGISTER

Table 113. Register 0xFE34—Power Metering Gain Trim for Low Line Input

Bits	Bit Name	R/W	Description
7	Gain trim polarity	R/W	1 = negative gain trim is introduced. 0 = positive gain trim is introduced.
[6:0]	Power meter gain trim	R/W	This value calibrates the power meter gain at the low line input voltage. Each LSB corresponds to 0.0625/128 of the input power.

HIGH LINE LIMIT REGISTER

Table 114. Register 0xFE35—High Line Limit

Bits	Bit Name	R/W	Description
[7:0]	VAC high line threshold	R/W	When the input voltage is higher than this value, the current loop filter for high line input is used.

LOW LINE LIMIT REGISTER

Table 115. Register 0xFE36—Low Line Limit

Bits	Bit Name	R/W	Description
[7:0]	VAC low line threshold	R/W	When the input voltage is lower than this value, the current loop filter for low line input is used.

ILIM_TRIM REGISTER

This register must be unlocked for write access; see Table 61.

Table 116. Register 0xFE37—ILIM_TRIM

Bits	Bit Name	R/W	Description
[7:5]	RSVD	R	Reserved.
4	Trim current direction	R/W	1 = source trim current (ILIM + ILIM_TRIM). 0 = sink trim current (ILIM − ILIM_TRIM).
[3:0]	ILIM trim	R/W	These bits set the trim current. Each LSB corresponds to ILIM/64.

VOLTAGE LOOP OUTPUT REGISTER

Table 117. Register 0xFE38—Voltage Loop Output

Bits	Bit Name	R/W	Description
[7:0]	Voltage loop output	R	Return the output of the voltage control loop.

EXPONENT REGISTER

This register reads and writes exponents (N) for PIN, VIN, and IIN.

Table 118. Register 0xFE39—Exponent

Bits	Bit Name	R/W	Description
[15:11]	RSVD	R	Reserved.
[10:6]	Input current exponent	R/W	Sets the exponent for the input current.
[5:3]	Input voltage exponent	R/W	Sets the exponent for the input voltage.
[2:0]	Input power exponent	R/W	Sets the exponent for the input power.

READ UPDATE RATE REGISTER

Table 119. Register 0xFE3A—Read Update Rate

Bits	Bit Name	R/W	Description			
[7:3]	RSVD	R	Reserved.			
[2:0]	Averaging window	R/W	These bits set the averaging window for the power current and voltage readings; rms values from one half ac line cycle are averaged over the programmed number of half ac line cycles.			
			Bit 2	**Bit 1**	**Bit 0**	**Number of Half AC Line Cycles**
			0	0	0	0
			0	0	1	16
			0	1	0	64
			0	1	1	128
			1	0	0	512
			1	0	1	1024
			1	1	0	4096
			1	1	1	8192

VIN SCALE MONITOR REGISTER

Table 120. Register 0xFE3B—VIN Scale Monitor

Bits	Bit Name	R/W	Description
[15:14]	RSVD	R	Reserved.
[13:11]	Exponent	R/W	Write the exponent (N) in twos complement format ($K_{VIN} = Y \times 2^N$).
10	RSVD	R	Reserved.
[9:0]	Mantissa	R/W	Mantissa (Y[9:0]) used in K_{VIN} linear mode format ($K_{VIN} = Y \times 2^N$).

IIN_GSENSE REGISTER

Table 121. Register 0xFE3C—IIN_GSENSE

Bits	Bit Name	R/W	Description
[15:11]	Exponent	R/W	Write the exponent (N) in twos complement format (IIN_GSENSE = $Y \times 2^N$).
10	RSVD	R	Reserved.
[9:0]	Mantissa	R/W	Mantissa (Y[9:0]) used in IIN linear mode format (IIN_GSENSE = $Y \times 2^N$).

CS FAST OCP BLANK REGISTER

Table 122. Register 0xFE3D—CS Fast OCP Blank

Bits	Bit Name	R/W	Description			
[7:5]	RSVD	R	Reserved.			
[4:3]	CS OCP debounce time	R/W	These bits set the CS OCP debounce time. This value is the minimum time that the CS signal must be constantly above the ILIM threshold (set in Register 0xFE3E, Bits[7:5]). When the CS OCP debounce time is exceeded, all PWM outputs are disabled for the remainder of the switching cycle.			
			Bit 4	**Bit 3**	**Fast OCP Debounce Time**	
			0	0	40 ns	
			0	1	80 ns	
			1	0	120 ns	
			1	1	240 ns	
[2:0]	Leading edge blanking time	R/W	These bits determine the leading edge blanking time. During this time, the OCP comparator output is ignored.			
			Bit 2	**Bit 1**	**Bit 0**	**Leading Edge Blanking Time**
			0	0	0	40 ns
			0	0	1	80 ns
			0	1	0	120 ns
			0	1	1	160 ns
			1	0	0	200 ns
			1	0	1	400 ns
			1	1	0	600 ns
			1	1	1	800 ns

CS FAST OCP SETTING REGISTER

Table 123. Register 0xFE3E—CS Fast OCP Setting

Bits	Bit Name	R/W	Description			
[7:5]	ILIM absolute value	R/W	These bits determine the ILIM absolute value. Bit 7 = 0 is positive sensing, and Bit 7 = 1 is negative sensing.			
			Bit 7	**Bit 6**	**Bit 5**	**ILIM Current Value**
			0	0	0	20 µA
			0	0	1	40 µA
			0	1	0	60 µA
			0	1	1	80 µA
			1	0	0	60 µA
			1	0	1	80 µA
			1	1	0	100 µA
			1	1	1	120 µA
[4:2]	RSVD	R	Reserved.			
1	CS_RANGE_SELECT	R/W	CS ADC input range. 0 = 750 mV. 1 = 500 mV.			
0	SEL_RESVI_REF	R/W	This bit sets the reference current for the CS+ and CS− common-mode level shift. 1 = select the RES VI reference current (changing R_{RES} changes this current). 0 = select the band gap generated reference current.			

TEMPERATURE HYSTERESIS REGISTER

Table 124. Register 0xFE3F—Temperature Hysteresis

Bits	Bit Name	R/W	Description
[7:0]	Temperature hysteresis	R/W	These bits set the temperature (RTD) measurement hysteresis. The OT_FAULT flag is reset when the RTD ADC value is higher than the temperature fault limit plus hysteresis. The OT_WARN flag is reset when the RTD ADC value is higher than the temperature warning limit plus hysteresis.

VAC ADC GAIN TRIM REGISTER

This register must be unlocked for write access; see Table 61.

Table 125. Register 0xFE40—VAC ADC Gain Trim

Bits	Bit Name	R/W	Description
7	Gain polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	VAC ADC gain trim	R/W	This value calibrates the VAC voltage sense gain.

VFB ADC GAIN TRIM REGISTER

This register must be unlocked for write access; see Table 61.

Table 126. Register 0xFE41—VFB ADC Gain Trim

Bits	Bit Name	R/W	Description
7	Gain polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	VFB ADC gain trim	R/W	This value calibrates the output voltage sense gain.

CS ADC GAIN TRIM FOR 500 mV RANGE REGISTER

This register must be unlocked for write access; see Table 61.

Table 127. Register 0xFE42—CS ADC Gain Trim for 500 mV Range

Bits	Bit Name	R/W	Description
7	Gain polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	CS ADC gain trim	R/W	This value calibrates the CS current sense gain.

IBAL GAIN REGISTER (ADP1048 ONLY)

Table 128. Register 0xFE43—IBAL Gain (ADP1048 Only)

Bits	Bit Name	R/W	Description
7	IBAL enable	R/W	1 = enable current balancing. 0 = disable current balancing and reset the IBAL integrator.
[6:0]	IBAL gain	R/W	The gain can be set from 0 to 127.

SMART VOUT LOW POWER THRESHOLD (P1) REGISTER

Table 129. Register 0xFE44—Smart VOUT Low Power Threshold (P1)

Bits	Bit Name	R/W	Description
[15:13]	RSVD	R	Reserved.
[12:0]	P1	R/W	These bits set the threshold value for low power mode operation when the smart output voltage function is enabled. When the input power is lower than this value, the output voltage is VOL1 for low line input and VOH1 for high line input.

SMART VOUT HIGH POWER THRESHOLD (P2) REGISTER

Table 130. Register 0xFE45—Smart VOUT High Power Threshold (P2)

Bits	Bit Name	R/W	Description
[15:13]	RSVD	R	Reserved.
[12:0]	P2	R/W	These bits set the threshold value for high power mode operation when the smart output voltage function is enabled. When the input power is higher than this value, the output voltage is VOL2 for low line input and VOH2 for high line input.

SMART VOUT LOW LINE (VOL1) REGISTER

Table 131. Register 0xFE46—Smart VOUT Low Line (VOL1)

Bits	Bit Name	R/W	Description
[15:11]	RSVD	R	Reserved.
[10:0]	VOL1	R/W	These bits set the output voltage under low power mode operation with low line input.

SMART VOUT LOW LINE (VOL2) REGISTER

Table 132. Register 0xFE47—Smart VOUT Low Line (VOL2)

Bits	Bit Name	R/W	Description
[15:11]	RSVD	R	Reserved.
[10:0]	VOL2	R/W	These bits set the output voltage under high power mode operation with low line input.

SMART VOUT HIGH LINE (VOH1) REGISTER

Table 133. Register 0xFE48—Smart VOUT High Line (VOH1)

Bits	Bit Name	R/W	Description
[15:11]	RSVD	R	Reserved.
[10:0]	VOH1	R/W	These bits set the output voltage under low power mode operation with high line input.

SMART VOUT HIGH LINE (VOH2) REGISTER

Table 134. Register 0xFE49—Smart VOUT High Line (VOH2)

Bits	Bit Name	R/W	Description
[15:11]	RSVD	R	Reserved.
[10:0]	VOH2	R/W	These bits set the output voltage under high power mode operation with high line input.

SMART VOUT UPPER LIMIT (VOH) REGISTER

Table 135. Register 0xFE4A—Smart VOUT Upper Limit (VOH)

Bits	Bit Name	R/W	Description
[15:11]	RSVD	R	Reserved.
[10:0]	VOH	R/W	These bits set the output voltage when the VAC input voltage is higher than the value set in Register 0xFE4B.

SMART VOUT SUPER HIGH LINE REGISTER

Table 136. Register 0xFE4B—Smart VOUT Super High Line

Bits	Bit Name	R/W	Description
[15:11]	RSVD	R	Reserved.
[10:0]	Super high line voltage	R/W	These bits set the input voltage value as a super high line limit.

SYNC DELAY REGISTER

Table 137. Register 0xFE4C—SYNC Delay

Bits	Bit Name	R/W	Description
[15:0]	t_{SYNC_DELAY}	R/W	These bits set the additional delay between the external synchronization reference clock signal and the rising edge of PWM. Each LSB corresponds to 80 ns resolution.

SMART_VOUT_SUPER_HIGH_LINE_HYS REGISTER

Table 138. Register 0xFE4D—SMART_VOUT_SUPER_HIGH_LINE_HYS

Bits	Bit Name	R/W	Description
[7:0]	Super high line voltage hysteresis	R/W	These bits set the voltage hysteresis of the super high line voltage for the smart output voltage function. The output voltage is VOH2 if the input voltage is lower than the super high line voltage minus the voltage hysteresis.

POWER_HYS REGISTER

Table 139. Register 0xFE4E—POWER_HYS

Bits	Bit Name	R/W	Description
[7:0]	Power hysteresis	R/W	These bits set the power hysteresis for low power mode operation. The PFC exits the low power mode if the input power is higher than the low power threshold plus the power hysteresis.

ADVANCED FEATURE ENABLE REGISTER

Table 140. Register 0xFE4F—Advanced Feature Enable

Bits	Bit Name	R/W	Description
7	RSVD	R	Reserved.
6	Enable current loop feedforward	R/W	1 = current loop feedforward is enabled. 0 = current loop feedforward is disabled.
5	Enable light load current loop filter	R/W	1 = light load current loop filter is enabled. 0 = light load current loop filter is disabled.
4	Enable phase shedding	R/W	1 = phase shedding is enabled. 0 = phase shedding is disabled. This bit applies to the ADP1048 only.
3	Enable smart switching frequency	R/W	1 = smart switching frequency is enabled. 0 = smart switching frequency is disabled.
2	Enable smart output voltage	R/W	1 = smart output voltage is enabled. 0 = smart output voltage is disabled.
1	Enable PWM synchronization	R/W	1 = PWM frequency synchronization is enabled. 0 = PWM frequency synchronization is disabled.
0	Enable frequency dithering	R/W	1 = frequency dithering is enabled. 0 = frequency dithering is disabled.

VOUT_OV_FAULT_HYS REGISTER

Table 141. Register 0xFE50—VOUT_OV_FAULT_HYS

Bits	Bit Name	R/W	Description
[7:0]	VOUT OV fault hysteresis	R/W	This register determines the mantissa hysteresis for the VOUT_OV_FAULT_LIMIT condition. This hysteresis applies only when the disable output option is selected as the VOUT_OV_FAULT_RESPONSE (Register 0x41, Bits[7:6]). The PFC output is reenabled when the output voltage is lower than VOUT_OV_FAULT_LIMIT minus this hysteresis.

VIN_UV_FAULT_HYS REGISTER

Table 142. Register 0xFE51—VIN_UV_FAULT_HYS

Bits	Bit Name	R/W	Description
[7:0]	VIN UV fault hysteresis	R/W	This register determines the mantissa hysteresis for the VIN_UV_FAULT_LIMIT condition. This hysteresis applies only when the disable output option is selected as the VIN_UV_FAULT_RESPONSE (Register 0x5A, Bits[7:6]). The PFC output is reenabled when the input voltage is higher than VIN_UV_FAULT_LIMIT plus this hysteresis.

VAC ADC OFFSET TRIM REGISTER

This register must be unlocked for write access; see Table 61.

Table 143. Register 0xFE53—VAC ADC Offset Trim

Bits	Bit Name	R/W	Description
[7:0]	VAC ADC offset trim	R/W	This register calibrates the VAC ADC offset (the offset is always subtracted from the ADC output).

CS ADC OFFSET TRIM FOR 500 mV RANGE REGISTER

This register must be unlocked for write access; see Table 61.

Table 144. Register 0xFE54—CS ADC Offset Trim for 500 mV Range

Bits	Bit Name	R/W	Description
[7:0]	CS ADC offset trim	R/W	This register calibrates the CS current sense offset (the offset is always subtracted from the ADC output).

CS ADC GAIN TRIM FOR HIGH (750 mV) RANGE REGISTER

This register must be unlocked for write access; see Table 61.

Table 145. Register 0xFE7E—CS ADC Gain Trim for High (750 mV) Range

Bits	Bit Name	R/W	Description
7	Gain polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[6:0]	CS ADC gain trim	R/W	This register calibrates the CS current sense gain.

CS ADC OFFSET TRIM FOR HIGH (750 mV) RANGE REGISTER

This register must be unlocked for write access; see Table 61.

Table 146. Register 0xFE7F—CS ADC Offset Trim for High (750 mV) Range

Bits	Bit Name	R/W	Description
[7:0]	CS ADC offset trim	R/W	This register calibrates the CS current sense offset (the offset is always subtracted from the ADC output).

LATCHED FLAG REGISTERS

The bits in the latched flag registers remain set (latched) to allow users to detect an intermittent fault. Reading a latched flag register resets the flags in that register.

Table 147. Register 0xFE80—Latched Flag 0

Bits	Bit Name	R/W	Description
7	MAX_MODULATION	R	1 = maximum modulation limit is reached.
6	MIN_MODULATION	R	1 = minimum modulation limit is reached.
5	OLP	R	1 = one of the two voltage dividers is probably disconnected or malfunctioning.
4	FAST_OVP	R	1 = the threshold set for the comparator on the OVP pin has been crossed.
3	AC_PERIOD	R	1 = controller is not able to detect the ac line period; the maximum value of the period is used and this flag is set.
2	BROWN_OUT	R	1 = VAC is lower than the value stored in VIN_ON (Register 0x35).
1	SOFT_START	R	1 = system is in soft start sequence; fast loop filter is in use.
0	INRUSH	R	1 = INRUSH control relay is off.

Table 148. Register 0xFE81—Latched Flag 1

Bits	Bit Name	R/W	Description
7	RSVD	R	Reserved.
6	EEPROM_UNLOCKED	R	1 = EEPROM is unlocked and its contents can be written.
5	EEPROM_CRC	R	1 = downloaded EEPROM contents are incorrect.
4	I2C_ADDRESS	R	1 = the resistor on the ADD pin has a value that can cause an error in the address assignment (the address falls too close to the threshold between two addresses).
3	LOW_LINE	R	1 = input voltage is higher than the high line threshold.
2	FAST_OCP	R	1 = the threshold set for the comparator on the ILIM pin has been crossed.
1	SYNC_LOCK	R	1 = external synchronization frequency is locked.
0	AC_OK	R	This flag is a programmable combination of other internal flags and refers to the condition of the input voltage. A value of 1 means that the output of the AC_OK pin is low.

Table 149. Register 0xFE82—Latched Flag 2

Bits	Bit Name	R/W	Description
[7:6]	RSVD	R	Reserved.
5	LOW_POWER	R	1 = input power has dropped below the threshold for low power mode operation.
4	FAST_LOOP	R	1 = fast loop compensation filter is in use.
3	VCORE_OV	R	1 = an overvoltage condition is present on the VCORE rail.
2	VDD_3.3V_OV	R	1 = an overvoltage condition is present on the VDD rail.
1	VDD_3.3V_UV	R	1 = an undervoltage condition is present on the VDD rail.
0	RSVD	R	Reserved.

PWM VALUE REGISTER

Table 150. Register 0xFE84—PWM Value

Bits	Bit Name	R/W	Description
[7:0]	PWM value	R	Return the eight MSBs of the PWM value (10 bits).

VAC_LINE_PERIOD REGISTER

Table 151. Register 0xFE85—VAC_LINE_PERIOD

Bits	Bit Name	R/W	Description
[7:0]	VAC line period	R	Return the measured period on the VAC pin signal. Each LSB corresponds to 163.84 µs.

READ TEMPERATURE ADC REGISTER

Table 152. Register 0xFE86—Read Temperature ADC

Bits	Bit Name	R/W	Description
[15:0]	RTD temperature	R	Return the measured temperature in ADC 12-bit format.

POWER METERING OFFSET TRIM FOR HIGH LINE INPUT REGISTER

Table 153. Register 0xFE8E—Power Metering Offset Trim for High Line Input

Bits	Bit Name	R/W	Description
7	Offset trim polarity	R/W	1 = negative offset trim is introduced. 0 = positive offset trim is introduced.
[6:0]	Power meter offset trim	R/W	This value calibrates the power meter offset at the high line input voltage. Each LSB corresponds to 0.0625/128 of the full input power.

POWER METERING GAIN TRIM FOR HIGH LINE INPUT REGISTER

Table 154. Register 0xFE8F—Power Metering Gain Trim for High Line Input

Bits	Bit Name	R/W	Description
7	Gain trim polarity	R/W	1 = negative gain trim is introduced. 0 = positive gain trim is introduced.
[6:0]	Power meter gain trim	R/W	This value calibrates the power meter gain at the high line input voltage. Each LSB corresponds to 0.0625/128 of the input power.

CURRENT LOOP FILTER GAIN FOR LOW LINE INPUT AND LIGHT LOAD REGISTER

Table 155. Register 0xFE90—Current Loop Filter Gain for Low Line Input and Light Load

Bits	Bit Name	R/W	Description
[7:0]	Current loop filter gain for low line and light load	R/W	These bits set the current loop digital filter gain of the PFC current loop under the low line input voltage at a light load condition if Bit 5 of Register 0xFE4F is set to 1.

CURRENT LOOP FILTER ZERO FOR LOW LINE INPUT AND LIGHT LOAD REGISTER

Table 156. Register 0xFE91—Current Loop Filter Zero for Low Line Input and Light Load

Bits	Bit Name	R/W	Description
[7:0]	Current loop filter zero for low line and light load	R/W	These bits set the current loop digital filter zero of the PFC current loop under the low line input voltage at a light load condition if Bit 5 of Register 0xFE4F is set to 1.

CURRENT LOOP FILTER GAIN FOR HIGH LINE INPUT AND LIGHT LOAD REGISTER

Table 157. Register 0xFE92—Current Loop Filter Gain for High Line Input and Light Load

Bits	Bit Name	R/W	Description
[7:0]	Current loop filter gain for high line and light load	R/W	These bits set the current loop digital filter gain of the PFC current loop under the high line input voltage at a light load condition if Bit 5 of Register 0xFE4F is set to 1.

CURRENT LOOP FILTER ZERO FOR HIGH LINE INPUT AND LIGHT LOAD REGISTER

Table 158. Register 0xFE93—Current Loop Filter Zero for High Line Input and Light Load

Bits	Bit Name	R/W	Description
[7:0]	Current loop filter zero for high line and light load	R/W	These bits set the current loop digital filter zero of the PFC current loop under the high line input voltage at a light load condition if Bit 5 of Register 0xFE4F is set to 1.

SMART VOUT POWER READING REGISTER

Table 159. Register 0xFE94—Smart VOUT Power Reading

Bits	Bit Name	R/W	Description
[15:0]	Power reading	R	Return the average power reading for smart output voltage (averaged over 16 full line cycles).

IBAL CONFIGURATION REGISTER (ADP1048 ONLY)

Table 160. Register 0xFE95—IBAL Configuration (ADP1048 Only)

Bits	Bit Name	R/W	Description
7	IBAL disconnect	R/W	1 = disconnect the output of the current balance block from the PWM outputs. 0 = connect the output of the current balance block to the PWM outputs.
6	IBAL at load transient	R/W	0 = disable current balancing when the fast loop is triggered. 1 = enable current balancing when the fast loop is triggered. It is recommended that this bit be set to 0.
[5:4]	RSVD	R	Reserved.
3	IBAL at low power mode	R/W	1 = disable current balancing under low power mode if the output of the current balancing block reaches the limit. 0 = enable current balancing under low power mode even if the output of the current balancing block reaches the limit. It is recommended that this bit be set to 1.
[2:0]	RSVD	R	Reserved.

DEBUG FLAG REGISTERS

Table 161. Register 0xFE96—Debug Flag 0

Bits	Bit Name	R/W	Description
7	OT_WARN	R	1 = measured temperature is above the value of OT_WARN_LIMIT.
6	OT_FAULT	R	1 = measured temperature is above the value of OT_FAULT_LIMIT.
5	TEMPERATURE	R	1 = temperature fault or warning.
4	UNKNOWN	R	1 = fault or warning not listed in Register 0x79, Bits[15:1].
3	MFR_FAULT	R	1 = manufacturer-specific fault or warning (Register 0xFE80, Register 0xFE81, Register 0xFE82).
2	PSON	R	1 = PSON signal (hardware or software) is inactive.
1	PGOOD	R	Power good. This flag is a programmable combination of other internal flags and refers to the condition of the output voltage. A value of 1 means that the output of the PGOOD pin is low.
0	AC_OK	R	This flag is a programmable combination of other internal flags and refers to the condition of the input voltage. A value of 1 means that the output of the AC_OK pin is low.

Table 162. Register 0xFE97—Debug Flag 1

Bits	Bit Name	R/W	Description
7	EEPROM_UNLOCKED	R	1 = EEPROM is unlocked and its contents can be written.
6	EEPROM_CRC	R	1 = downloaded EEPROM contents are incorrect.
5	I2C_ADDRESS	R	1 = the resistor on the ADD pin has a value that can cause an error in the address assignment (the address falls too close to the threshold between two addresses).
4	FAST_LOOP	R	1 = fast loop compensation filter is in use.
3	MAX_MODULATION	R	1 = maximum modulation limit is reached.
2	MIN_MODULATION	R	1 = minimum modulation limit is reached.
1	SOFT_START	R	1 = system is in soft start sequence; fast loop filter is in use.
0	SYNC_LOCK	R	1 = external synchronization frequency is locked.

Table 163. Register 0xFE98—Debug Flag 2

Bits	Bit Name	R/W	Description
7	VIN_UV	R	1 = general input undervoltage fault (same as Register 0x7C, Bit 4).
6	VIN_LOW	R	1 = VAC is lower than VIN_OFF (Register 0x36). This signal shuts down the power supply.
5	VIN_UV_FAULT	R	1 = input voltage on VAC is smaller than the value in VIN_UV_FAULT_LIMIT (Register 0x59).
4	VIN_UV_WARN	R	1 = input voltage on VAC is smaller than the value in VIN_UV_WARN_LIMIT (Register 0x58).
3	LOW_LINE	R	1 = input voltage is higher than the high line threshold.
2	BROWN_OUT	R	1 = VAC is lower than the value stored in VIN_ON (Register 0x35).
1	CML	R	1 = communications, memory, or logic fault.
0	VDD_3.3V_OV	R	1 = an overvoltage condition is present on the VDD rail.

Table 164. Register 0xFE99—Debug Flag 3

Bits	Bit Name	R/W	Description
7	VIN_OV_FAULT	R	1 = input voltage on VAC is larger than the value in VIN_OV_FAULT_LIMIT (Register 0x55).
6	VCORE_OV	R	1 = an overvoltage condition is present on the VCORE rail.
5	PIN_OP_WARN	R	1 = input overpower warning.
4	AC_PERIOD	R	1 = controller is not able to detect the ac line period; the maximum value of the period is used and this flag is set.
3	IIN_OC_WARN	R	1 = input current measured on the CS ADC is larger than the value in IIN_OC_WARN_LIMIT (Register 0x5D).
2	IIN_OC_FAULT	R	1 = input current measured on the CS ADC is larger than the value in IIN_OC_FAULT_LIMIT (Register 0x5B).
1	FAST_OCP	R	1 = the threshold set for the comparator on the ILIM pin has been crossed.
0	INPUT	R	1 = input voltage, input current, or input power fault or warning.

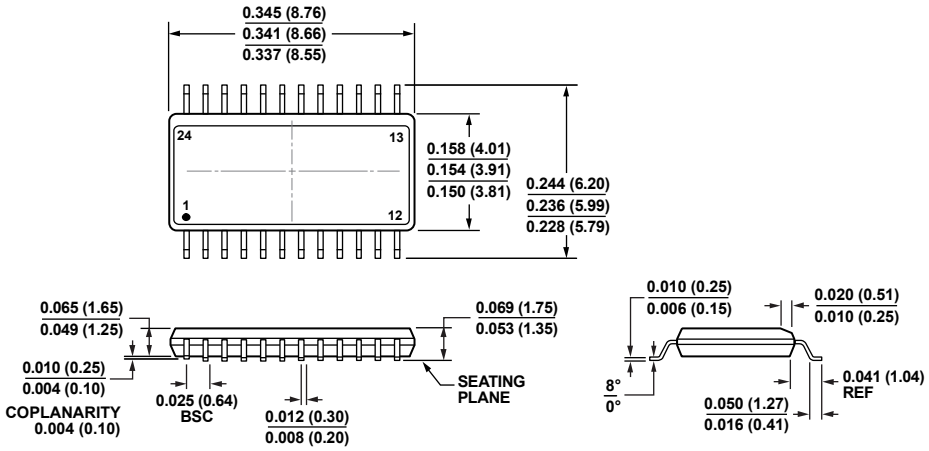
Table 165. Register 0xFE9A—Debug Flag 4

Bits	Bit Name	R/W	Description
7	OLP	R	1 = one of the two voltage dividers is probably disconnected or malfunctioning.
6	FAST_OVP	R	1 = the threshold set for the comparator on the OVP pin has been crossed.
5	VOUT_UV_FAULT	R	1 = output voltage is below the VOUT_UV_FAULT_LIMIT (Register 0x44).
4	VOUT_UV_WARN	R	1 = output voltage is below the VOUT_UV_WARN_LIMIT (Register 0x43).
3	VOUT_OV_WARN	R	1 = output voltage is above the VOUT_OV_WARN_LIMIT (Register 0x42).
2	VOUT_OV_FAULT	R	1 = output voltage is above the VOUT_OV_FAULT_LIMIT (Register 0x40).
1	VOUT_OV	R	General output overvoltage fault: this flag is a combination (OR) of any output overvoltage flag (Register 0x7A, Bit 7 and Register 0xFE80, Bit 4 (FAST_OVP)).
0	VOUT	R	1 = any fault on output voltage (overvoltage, undervoltage, fast OVP, or accurate OVP).

Table 166. Register 0xFE9B—Debug Flag 5

Bits	Bit Name	R/W	Description
[7:3]	RSVD	R	Reserved.
2	LOW_POWER	R	1 = input power has dropped below the threshold for low power mode operation.
1	VDD_3.3V_UV	R	1 = an undervoltage condition is present on the VDD rail.
0	INRUSH	R	1 = INRUSH control relay is off.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137-AE

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

01-03-2008-A

Figure 45. 24-Lead Shrink Small Outline Package [QSOP]
(RQ-24)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP1047ARQZ-R7	−40°C to +85°C	24-Lead Shrink Small Outline Package [QSOP]	RQ-24
ADP1048ARQZ-R7	−40°C to +85°C	24-Lead Shrink Small Outline Package [QSOP]	RQ-24
ADP1047-300-EVALZ		ADP1047 300 W Evaluation Board	
ADP1048-600-EVALZ		ADP1048 600 W Evaluation Board	
ADP1047DC1-EVALZ		ADP1047 Daughter Card	
ADP1048DC1-EVALZ		ADP1048 Daughter Card	
ADP-I2C-USB-Z		USB to I²C Adapter	

[1] Z = RoHS Compliant Part.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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