

# 74LVC4066-Q100

Quad bilateral switch

Rev. 1 — 7 August 2012

Product data sheet

## 1. General description

---

The 74LVC4066-Q100 is a high-speed Si-gate CMOS device.

The 74LVC4066-Q100 provides four single pole, single-throw analog switch functions. Each switch has two input/output terminals (nY and nZ) and an active HIGH enable input (nE). When nE is LOW, the analog switch is turned off.

Schmitt-trigger action at the enable inputs makes the circuit tolerant of slower input rise and fall times across the entire  $V_{CC}$  range from 1.65 V to 5.5 V.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

---

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- Wide supply voltage range from 1.65 V to 5.5 V
- Very low ON resistance:
  - ◆  $7.5\ \Omega$  (typical) at  $V_{CC} = 2.7\text{ V}$
  - ◆  $6.5\ \Omega$  (typical) at  $V_{CC} = 3.3\text{ V}$
  - ◆  $6\ \Omega$  (typical) at  $V_{CC} = 5\text{ V}$
- Switch current capability of 32 mA
- High noise immunity
- CMOS low-power consumption
- Direct interface TTL-levels
- Latch-up performance exceeds 250 mA
- ESD protection:
  - ◆ MIL-STD-883, method 3015 exceeds 2000 V
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V ( $C = 200\text{ pF}$ ,  $R = 0\ \Omega$ )
- Enable inputs accept voltages up to 5 V
- Multiple package options



### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC4066D-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC4066PW-Q100	-40 °C to +125 °C	TSSOP14	plastic thin small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC4066BQ-Q100	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

### 4. Functional diagram

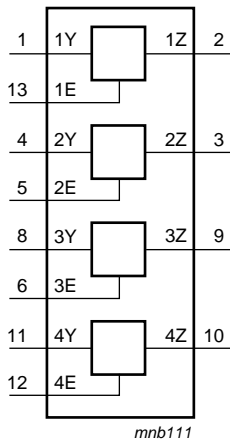


Fig 1. Logic symbol

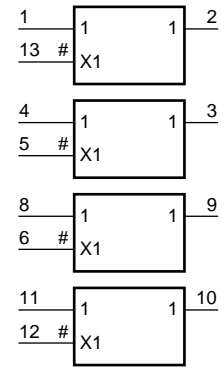
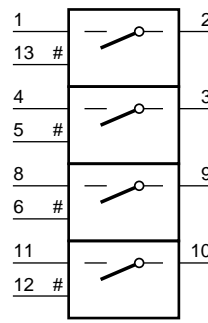


Fig 2. Logic symbol (IEEE/IEC)

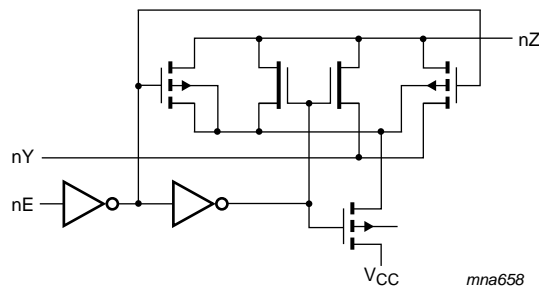
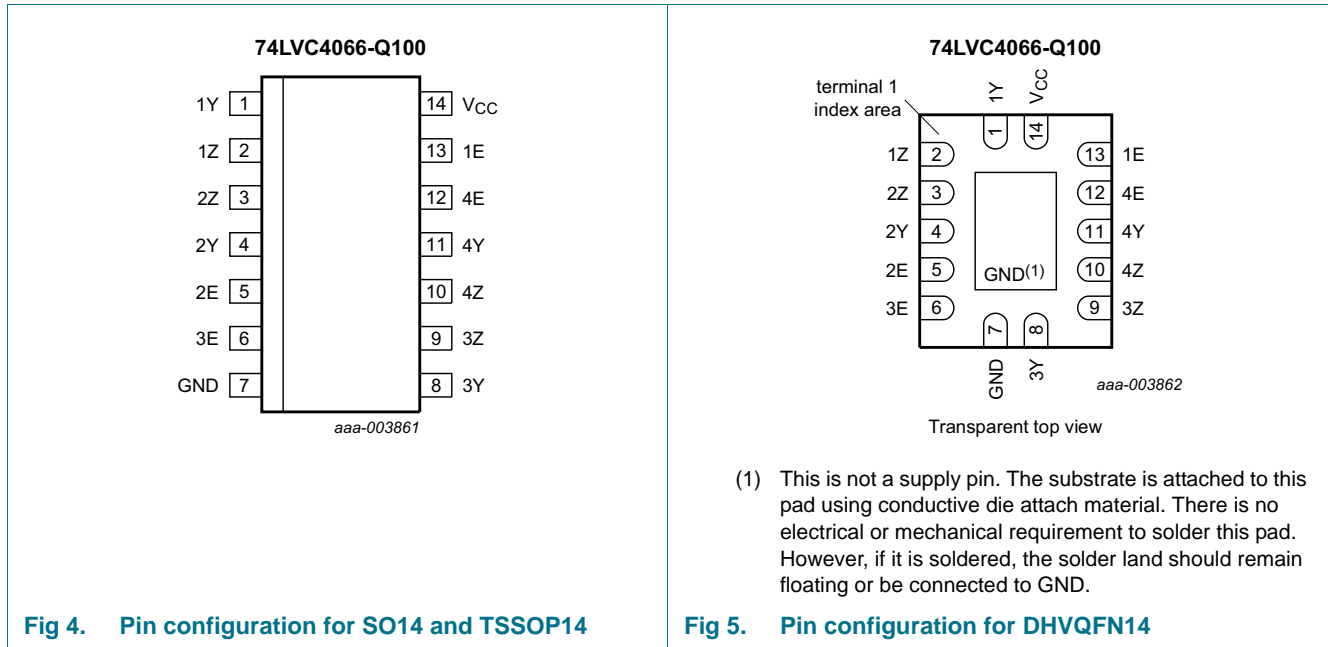


Fig 3. Logic diagram (one switch)

## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1Y	1	independent input/output
1Z	2	independent output/input
2Z	3	independent output/input
2Y	4	independent input/output
2E	5	enable input (active HIGH)
3E	6	enable input (active HIGH)
GND	7	ground (0 V)
3Y	8	independent input/output
3Z	9	independent output/input
4Z	10	independent output/input
4Y	11	independent input/output
4E	12	enable input (active HIGH)
1E	13	enable input (active HIGH)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Input nE	Switch
L	OFF
H	ON

[1] H = HIGH voltage level;  
L = LOW voltage level.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$V_I$	input voltage		<sup>[1]</sup> -0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I < V_{CC} + 0.5\text{ V}$	-50	-	mA
$I_{SK}$	switch clamping current	$V_I < -0.5\text{ V}$ or $V_I < V_{CC} + 0.5\text{ V}$	-	±50	mA
$V_{SW}$	switch voltage	enable and disable mode	<sup>[2]</sup> -0.5	+6.5	V
$I_{SW}$	switch current	$-0.5 < V_{SW} < V_{CC} + 0.5\text{ V}$	-	±50	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$	<sup>[3]</sup> -	500	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.  
For TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.  
For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		1.65	-	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_{SW}$	switch voltage		[1] 0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	[2] -	-	20	ns/V
		$V_{CC} = 2.7\text{ V to }5.5\text{ V}$	[2] -	-	10	ns/V

[1] To avoid sinking GND current from terminal nZ when switch current flows in terminal nY, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no GND current flows from terminal nY. In this case, there is no limit for the voltage drop across the switch.

[2] Applies to control signal levels.

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65V_{CC}$	-	-	$0.65V_{CC}$	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	1.7	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	2.0	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7V_{CC}$	-	-	$0.7V_{CC}$	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35V_{CC}$	-	$0.35V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	-	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	-	0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.3V_{CC}$	-	$0.3V_{CC}$	V
$I_I$	input leakage current	pin nE; $V_{CC} = 5.5\text{ V}$ ; $V_I = 5.5\text{ V or GND}$ [2]	-	$\pm 0.1$	$\pm 5$	-	$\pm 20$	$\mu\text{A}$
$I_{S(OFF)}$	OFF-state leakage current	$ V_{SW}  = V_{CC} - \text{GND}$ ; $V_{CC} = 5.5\text{ V}$ ; see <a href="#">Figure 6</a> [2]	-	$\pm 0.1$	$\pm 5$	-	$\pm 20$	$\mu\text{A}$
$I_{S(ON)}$	ON-state leakage current	$ V_{SW}  = V_{CC} - \text{GND}$ ; $V_{CC} = 5.5\text{ V}$ ; see <a href="#">Figure 7</a> [2]	-	$\pm 0.1$	$\pm 5$	-	$\pm 20$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC} \text{ or GND}$ ; $V_{SW} = \text{GND or } V_{CC}$ ; $V_{CC} = 5.5\text{ V}$ [2]	-	0.1	10	-	40	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	pin nE; $V_I = V_{CC} - 0.6\text{ V}$ ; $V_{CC} = 5.5\text{ V}$ ; $V_{SW} = \text{GND or } V_{CC}$ [2]	-	5	500	-	5000	$\mu\text{A}$

**Table 6. Static characteristics ...continued**

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
C <sub>I</sub>	input capacitance		-	12.5	-	-	-	pF
C <sub>S(OFF)</sub>	OFF-state capacitance		-	8.0	-	-	-	pF
C <sub>S(ON)</sub>	ON-state capacitance		-	14.0	-	-	-	pF

- [1] All typical values are measured at T<sub>amb</sub> = 25 °C.
- [2] These typical values are measured at V<sub>CC</sub> = 3.3 V.

### 9.1 Test circuits

001aag488

$V_I = V_{CC}$  or GND and  $V_O =$  GND or  $V_{CC}$ .

**Fig 6. Test circuit for measuring OFF-state leakage current**

001aag489

$V_I = V_{CC}$  or GND and  $V_O =$  open circuit.

**Fig 7. Test circuit for measuring ON-state leakage current**

### 9.2 ON resistance

**Table 7. ON resistance**

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see [Figure 9](#) to [Figure 14](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
R <sub>ON(peak)</sub>	ON resistance (peak)	V <sub>I</sub> = GND to V <sub>CC</sub> ; see <a href="#">Figure 8</a>						
		I <sub>SW</sub> = 4 mA; V <sub>CC</sub> = 1.65 V to 1.95 V	-	34.0	130	-	195	Ω
		I <sub>SW</sub> = 8 mA; V <sub>CC</sub> = 2.3 V to 2.7 V	-	12.0	30	-	45	Ω
		I <sub>SW</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	10.4	25	-	38	Ω
		I <sub>SW</sub> = 24 mA; V <sub>CC</sub> = 3 V to 3.6 V	-	7.8	20	-	30	Ω
		I <sub>SW</sub> = 32 mA; V <sub>CC</sub> = 4.5 V to 5.5 V	-	6.2	15	-	23	Ω

**Table 7. ON resistance ...continued**

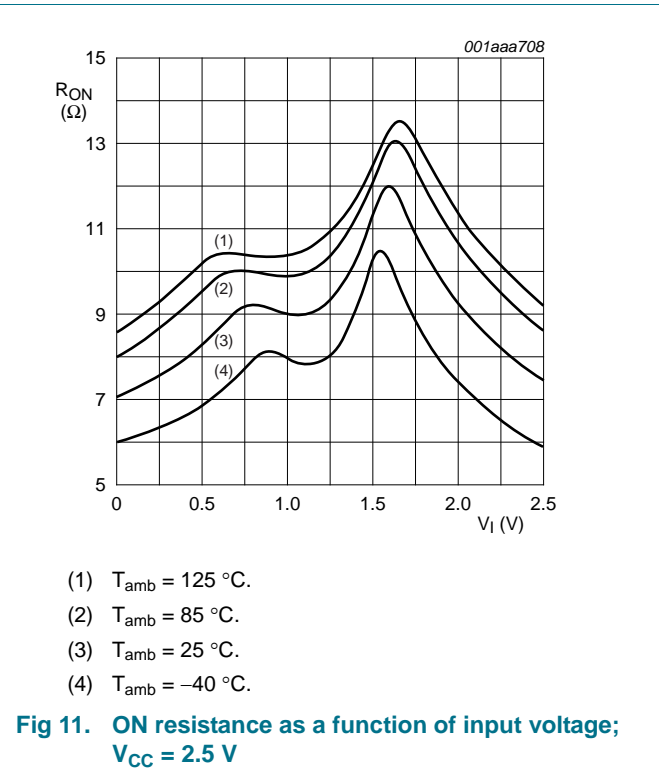
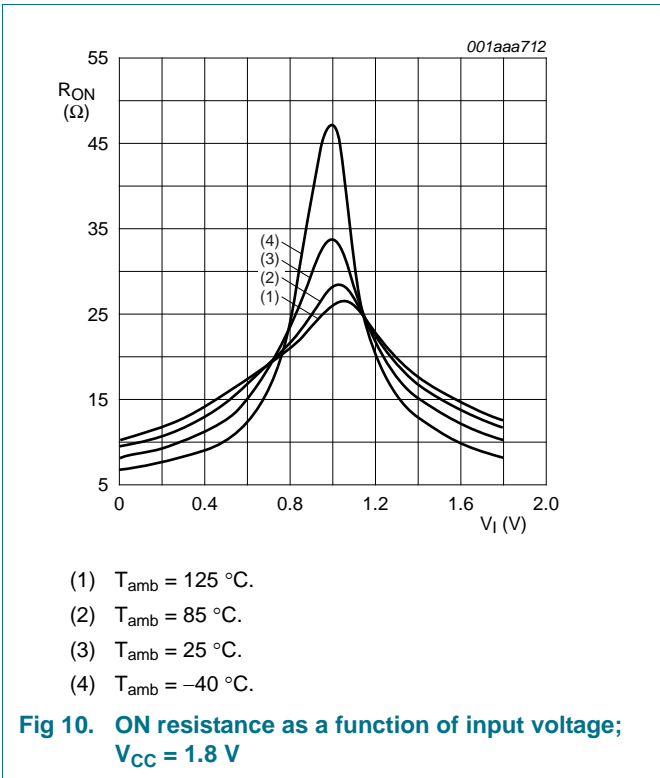
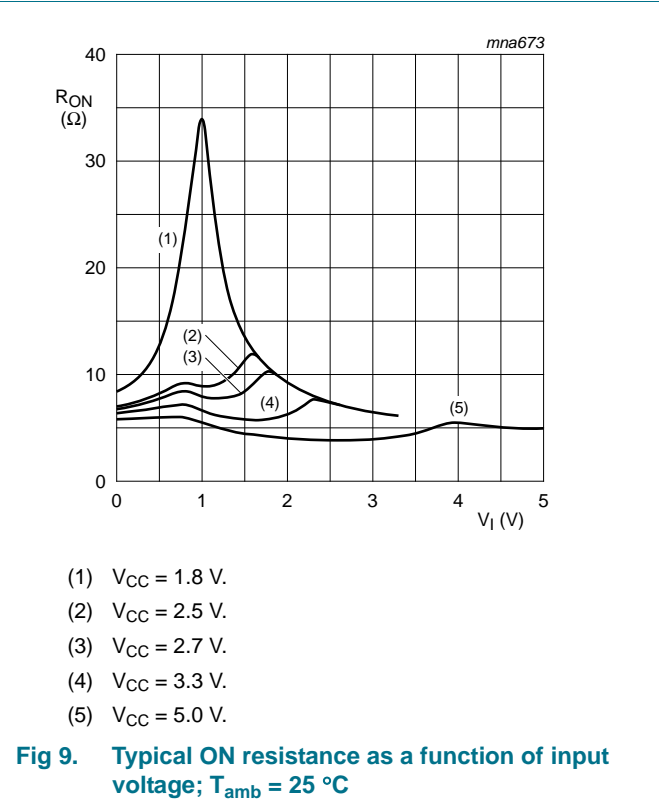
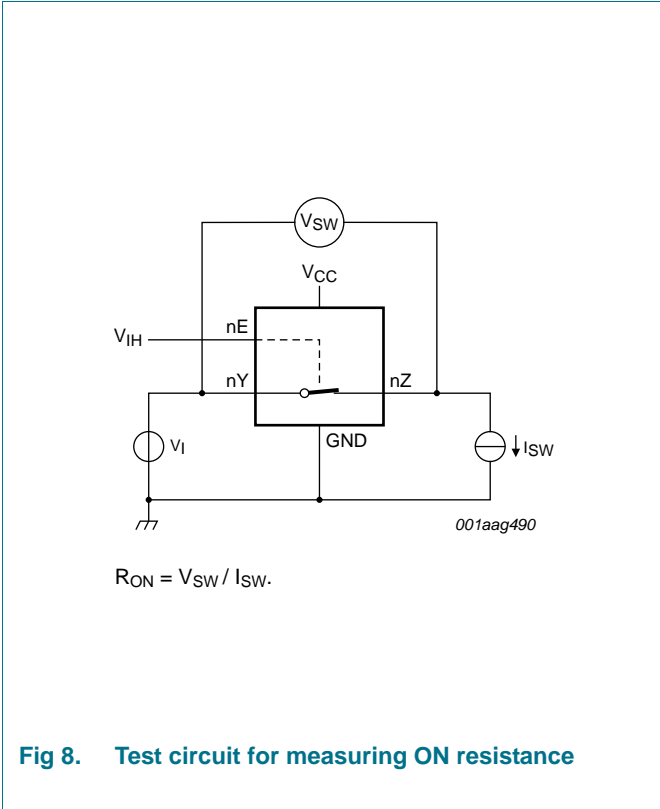
At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see [Figure 9](#) to [Figure 14](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
R <sub>ON(rail)</sub>	ON resistance (rail)	V <sub>I</sub> = GND; see <a href="#">Figure 8</a>						
		I <sub>SW</sub> = 4 mA; V <sub>CC</sub> = 1.65 V to 1.95 V	-	8.2	18	-	27	Ω
		I <sub>SW</sub> = 8 mA; V <sub>CC</sub> = 2.3 V to 2.7 V	-	7.1	16	-	24	Ω
		I <sub>SW</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	6.9	14	-	21	Ω
		I <sub>SW</sub> = 24 mA; V <sub>CC</sub> = 3 V to 3.6 V	-	6.5	12	-	18	Ω
		I <sub>SW</sub> = 32 mA; V <sub>CC</sub> = 4.5 V to 5.5 V	-	5.8	10	-	15	Ω
		V <sub>I</sub> = V <sub>CC</sub> ; see <a href="#">Figure 8</a>						
		I <sub>SW</sub> = 4 mA; V <sub>CC</sub> = 1.65 V to 1.95 V	-	10.4	30	-	45	Ω
		I <sub>SW</sub> = 8 mA; V <sub>CC</sub> = 2.3 V to 2.7 V	-	7.6	20	-	30	Ω
		I <sub>SW</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	7.0	18	-	27	Ω
		I <sub>SW</sub> = 24 mA; V <sub>CC</sub> = 3 V to 3.6 V	-	6.1	15	-	23	Ω
		I <sub>SW</sub> = 32 mA; V <sub>CC</sub> = 4.5 V to 5.5 V	-	4.9	10	-	15	Ω
R <sub>ON(flat)</sub>	ON resistance (flatness)	V <sub>I</sub> = GND to V <sub>CC</sub> <a href="#">[2]</a>						
		I <sub>SW</sub> = 4 mA; V <sub>CC</sub> = 1.65 V to 1.95 V	-	26.0	-	-	-	Ω
		I <sub>SW</sub> = 8 mA; V <sub>CC</sub> = 2.3 V to 2.7 V	-	5.0	-	-	-	Ω
		I <sub>SW</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	3.5	-	-	-	Ω
		I <sub>SW</sub> = 24 mA; V <sub>CC</sub> = 3 V to 3.6 V	-	2.0	-	-	-	Ω
		I <sub>SW</sub> = 32 mA; V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.5	-	-	-	Ω

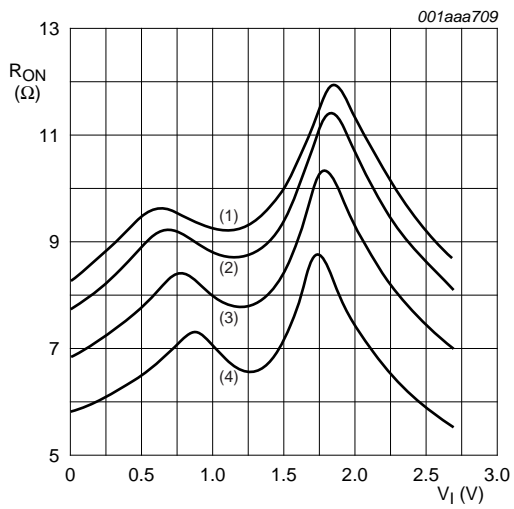
[1] Typical values are measured at T<sub>amb</sub> = 25 °C and nominal V<sub>CC</sub>.

[2] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V<sub>CC</sub> and temperature.

9.3 ON resistance test circuit and graphs

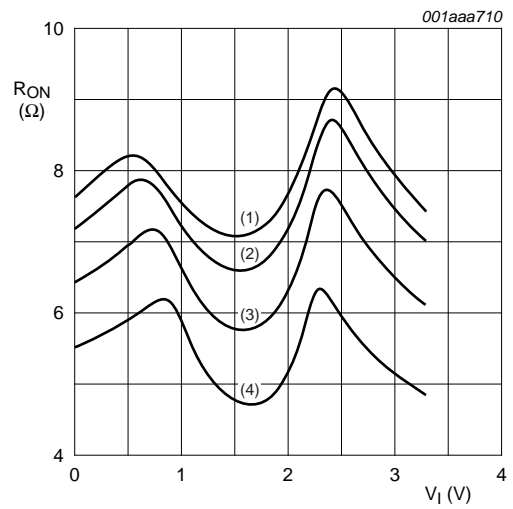






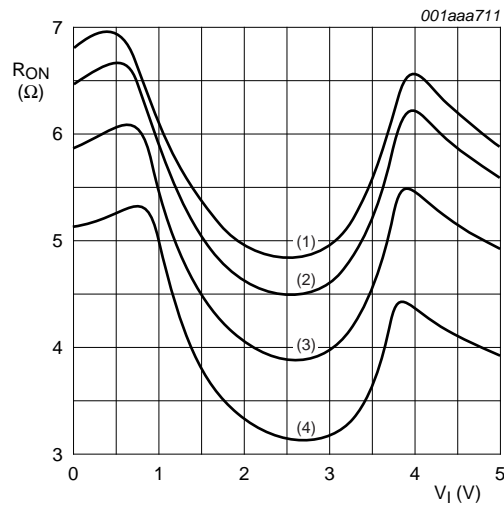
- (1)  $T_{amb} = 125$  °C.
- (2)  $T_{amb} = 85$  °C.
- (3)  $T_{amb} = 25$  °C.
- (4)  $T_{amb} = -40$  °C.

Fig 12. ON resistance as a function of input voltage;  $V_{CC} = 2.7$  V



- (1)  $T_{amb} = 125$  °C.
- (2)  $T_{amb} = 85$  °C.
- (3)  $T_{amb} = 25$  °C.
- (4)  $T_{amb} = -40$  °C.

Fig 13. ON resistance as a function of input voltage;  $V_{CC} = 3.3$  V



- (1)  $T_{amb} = 125$  °C.
- (2)  $T_{amb} = 85$  °C.
- (3)  $T_{amb} = 25$  °C.
- (4)  $T_{amb} = -40$  °C.

Fig 14. ON resistance as a function of input voltage;  $V_{CC} = 5.0$  V

## 10. Dynamic characteristics

**Table 8. Dynamic characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for load circuit [Figure 17](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nY to nZ or nZ to nY; see <a href="#">Figure 15</a> <sup>[2][3]</sup>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	0.8	2.0	-	3.0	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	0.4	1.2	-	2.0	ns
		V <sub>CC</sub> = 2.7 V	-	0.4	1.0	-	1.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	0.3	0.8	-	1.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	0.2	0.6	-	1.0	ns
t <sub>en</sub>	enable time	nE to nY or nZ; see <a href="#">Figure 16</a> <sup>[4]</sup>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	5.3	10	1.0	12.5	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	3.0	5.6	1.0	7.0	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.6	5.0	1.0	6.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.5	4.4	1.0	5.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	1.0	1.9	3.9	1.0	5.0	ns
t <sub>dis</sub>	disable time	nE to nY or nZ; see <a href="#">Figure 16</a> <sup>[5]</sup>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	4.2	9.0	1.0	11.5	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.4	5.5	1.0	7.0	ns
		V <sub>CC</sub> = 2.7 V	1.0	3.6	6.5	1.0	8.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	3.4	6.0	1.0	7.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	1.0	2.5	5.0	1.0	6.5	ns
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f <sub>i</sub> = 10 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[6]</sup>						
		V <sub>CC</sub> = 2.5 V	-	11.0	-	-	-	pF
		V <sub>CC</sub> = 3.3 V	-	12.5	-	-	-	pF
		V <sub>CC</sub> = 5.0 V	-	15.6	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and nominal V<sub>CC</sub>.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] Propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified capacitance when driven by an ideal voltage source (zero output impedance).

[4] t<sub>en</sub> is the same as t<sub>PZH</sub> and t<sub>PZL</sub>.

[5] t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

[6] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum\{(C_L + C_{S(ON)}) \times V_{CC}^2 \times f_o\}$$

where:

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

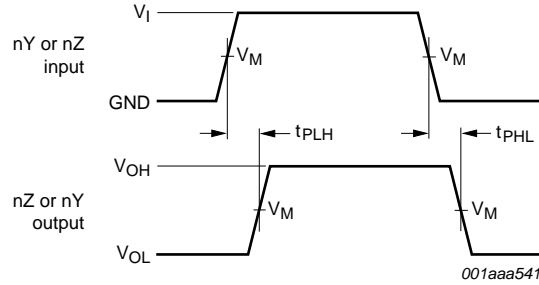
C<sub>S(ON)</sub> = maximum ON-state switch capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

∑{(C<sub>L</sub> + C<sub>S(ON)</sub>) × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>} = sum of the outputs.

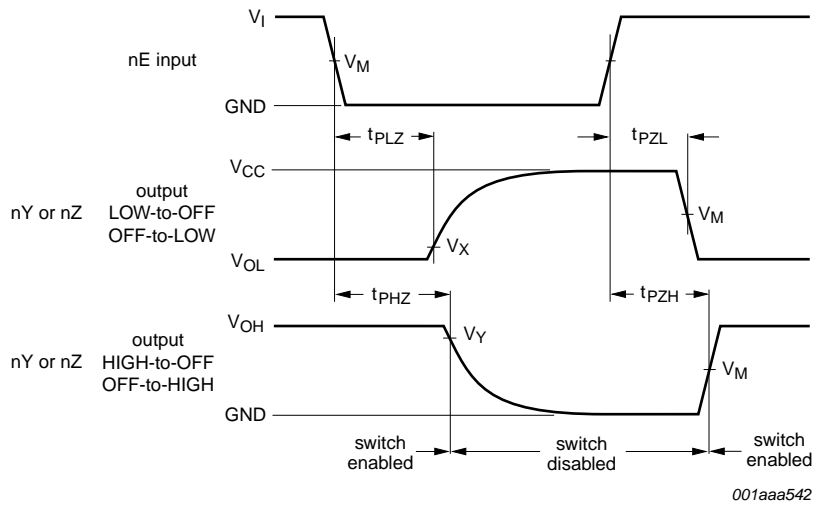
10.1 Waveforms and test circuit



Measurement points are given in [Table 9](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig 15. Input (nY or nZ) to output (nZ or nY) propagation delays



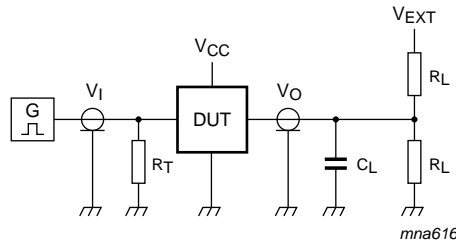
Measurement points are given in [Table 9](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig 16. Enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output		
$V_{CC}$	$V_M$	$V_M$	$V_X$	$V_Y$
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5 V_{CC}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
3.0 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



Test data is given in [Table 10](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 17. Load circuit for switching times**

**Table 10. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	1 k $\Omega$	open	GND	$2V_{CC}$
2.3 V to 2.7 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	500 $\Omega$	open	GND	$2V_{CC}$
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	GND	6 V
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	GND	6 V
4.5 V to 5.5 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	GND	$2V_{CC}$

## 10.2 Additional dynamic characteristics

**Table 11. Additional dynamic characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = 25$  °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$R_L = 10$ k $\Omega$ ; $C_L = 50$ pF; $f_i = 1$ kHz; see <a href="#">Figure 18</a>				
		$V_{CC} = 1.65$ V	-	0.032	-	%
		$V_{CC} = 2.3$ V	-	0.008	-	%
		$V_{CC} = 3$ V	-	0.006	-	%
		$V_{CC} = 4.5$ V	-	0.005	-	%
		$R_L = 10$ k $\Omega$ ; $C_L = 50$ pF; $f_i = 10$ kHz; see <a href="#">Figure 18</a>				
		$V_{CC} = 1.65$ V	-	0.068	-	%
		$V_{CC} = 2.3$ V	-	0.009	-	%
		$V_{CC} = 3$ V	-	0.008	-	%
		$V_{CC} = 4.5$ V	-	0.006	-	%

**Table 11. Additional dynamic characteristics ...continued**At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

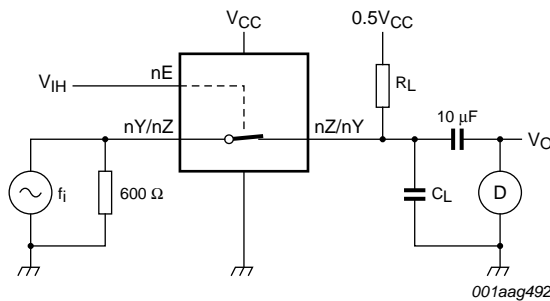
Symbol	Parameter	Conditions	Min	Typ	Max	Unit		
$f_{ -3\text{dB}}$	-3 dB frequency response	$R_L = 600\ \Omega$ ; $C_L = 50\ \text{pF}$ ; see <a href="#">Figure 19</a>						
		$V_{CC} = 1.65\ \text{V}$	-	170	-	MHz		
		$V_{CC} = 2.3\ \text{V}$	-	210	-	MHz		
		$V_{CC} = 3\ \text{V}$	-	212	-	MHz		
		$V_{CC} = 4.5\ \text{V}$	-	215	-	MHz		
		$R_L = 50\ \Omega$ ; $C_L = 5\ \text{pF}$ ; see <a href="#">Figure 19</a>						
		$V_{CC} = 1.65\ \text{V}$	-	> 500	-	MHz		
		$V_{CC} = 2.3\ \text{V}$	-	> 500	-	MHz		
		$V_{CC} = 3\ \text{V}$	-	> 500	-	MHz		
		$V_{CC} = 4.5\ \text{V}$	-	> 500	-	MHz		
		$\alpha_{\text{iso}}$	isolation (OFF-state)	$R_L = 600\ \Omega$ ; $C_L = 50\ \text{pF}$ ; $f_i = 1\ \text{MHz}$ ; see <a href="#">Figure 20</a>				
				$V_{CC} = 1.65\ \text{V}$	-	-46	-	dB
$V_{CC} = 2.3\ \text{V}$	-			-46	-	dB		
$V_{CC} = 3\ \text{V}$	-			-46	-	dB		
$V_{CC} = 4.5\ \text{V}$	-			-46	-	dB		
$R_L = 50\ \Omega$ ; $C_L = 5\ \text{pF}$ ; $f_i = 1\ \text{MHz}$ ; see <a href="#">Figure 20</a>								
$V_{CC} = 1.65\ \text{V}$	-			-42	-	dB		
$V_{CC} = 2.3\ \text{V}$	-			-42	-	dB		
$V_{CC} = 3\ \text{V}$	-			-42	-	dB		
$V_{CC} = 4.5\ \text{V}$	-			-42	-	dB		
$V_{\text{ct}}$	crosstalk voltage			between digital inputs and switch; $R_L = 600\ \Omega$ ; $C_L = 50\ \text{pF}$ ; $f_i = 1\ \text{MHz}$ ; $t_r = t_f = 2\ \text{ns}$ ; see <a href="#">Figure 21</a>				
				$V_{CC} = 1.65\ \text{V}$	-	69	-	mV
		$V_{CC} = 2.3\ \text{V}$	-	87	-	mV		
		$V_{CC} = 3\ \text{V}$	-	156	-	mV		
		$V_{CC} = 4.5\ \text{V}$	-	302	-	mV		
Xtalk	crosstalk	between switches; $R_L = 600\ \Omega$ ; $C_L = 50\ \text{pF}$ ; $f_i = 1\ \text{MHz}$ ; see <a href="#">Figure 22</a>						
		$V_{CC} = 1.65\ \text{V}$	-	-58	-	dB		
		$V_{CC} = 2.3\ \text{V}$	-	-58	-	dB		
		$V_{CC} = 3\ \text{V}$	-	-58	-	dB		
		$V_{CC} = 4.5\ \text{V}$	-	-58	-	dB		
		between switches; $R_L = 50\ \Omega$ ; $C_L = 5\ \text{pF}$ ; $f_i = 1\ \text{MHz}$ ; see <a href="#">Figure 22</a>						
		$V_{CC} = 1.65\ \text{V}$	-	-58	-	dB		
		$V_{CC} = 2.3\ \text{V}$	-	-58	-	dB		
		$V_{CC} = 3\ \text{V}$	-	-58	-	dB		
		$V_{CC} = 4.5\ \text{V}$	-	-58	-	dB		

**Table 11. Additional dynamic characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{inj}$	charge injection	$C_L = 0.1\text{ nF}$ ; $V_{gen} = 0\text{ V}$ ; $R_{gen} = 0\text{ }\Omega$ ; $f_i = 1\text{ MHz}$ ; $R_L = 1\text{ M}\Omega$ ; see <a href="#">Figure 23</a>				
		$V_{CC} = 1.8\text{ V}$	-	3.3	-	pC
		$V_{CC} = 2.5\text{ V}$	-	4.1	-	pC
		$V_{CC} = 3.3\text{ V}$	-	5.0	-	pC
		$V_{CC} = 4.5\text{ V}$	-	6.4	-	pC
		$V_{CC} = 5.5\text{ V}$	-	7.5	-	pC

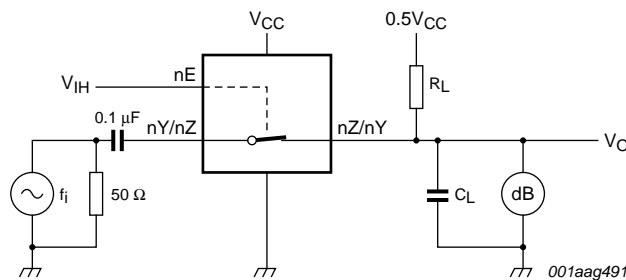
**10.2.1 Test circuits**



**Test conditions:**

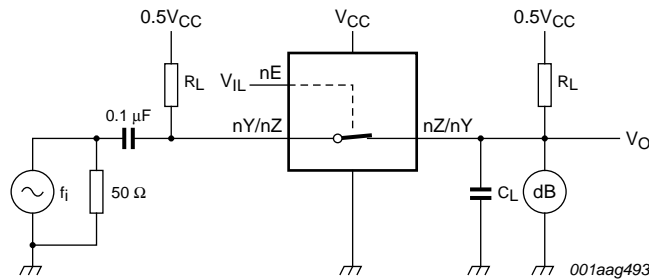
- $V_{CC} = 1.65\text{ V}$ :  $V_i = 1.4\text{ V}$  (p-p).
- $V_{CC} = 2.3\text{ V}$ :  $V_i = 2\text{ V}$  (p-p).
- $V_{CC} = 3\text{ V}$ :  $V_i = 2.5\text{ V}$  (p-p).
- $V_{CC} = 4.5\text{ V}$ :  $V_i = 4\text{ V}$  (p-p).

**Fig 18. Test circuit for measuring total harmonic distortion**



Adjust  $f_i$  voltage to obtain 0 dBm level at output. Increase  $f_i$  frequency until dB meter reads -3 dB.

**Fig 19. Test circuit for measuring the frequency response when switch is in ON-state**



Adjust  $f_i$  voltage to obtain 0 dBm level at input.

Fig 20. Test circuit for measuring isolation (OFF-state)

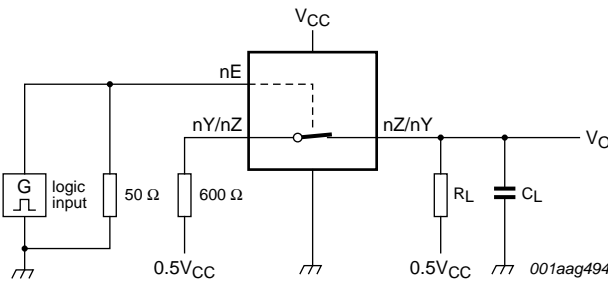
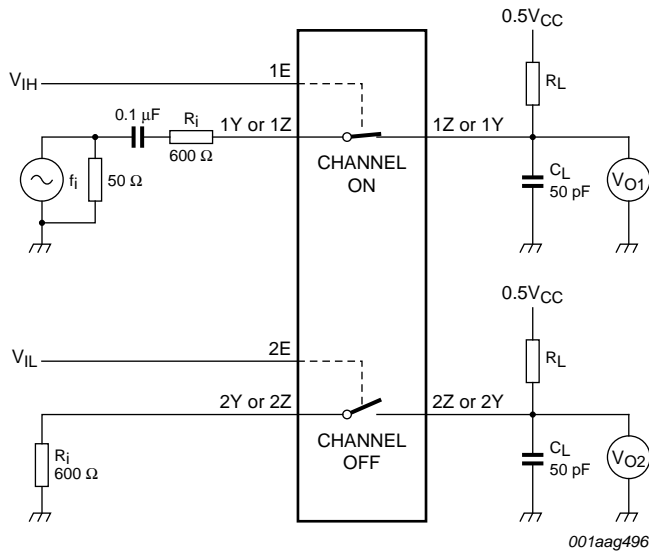
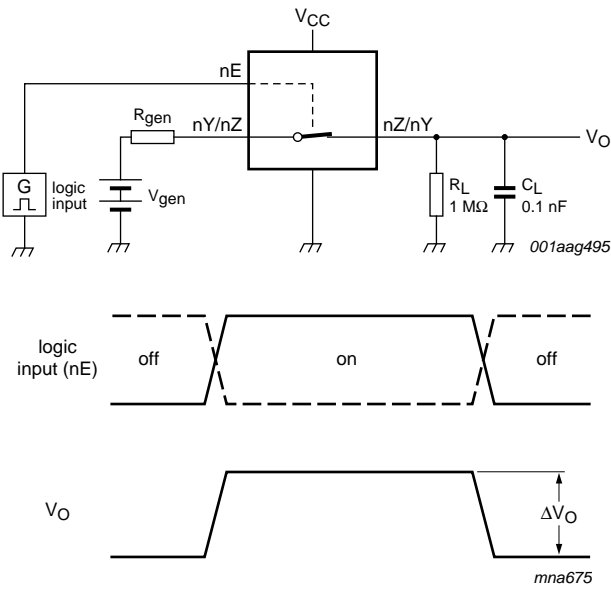


Fig 21. Test circuit for measuring crosstalk voltage (between digital inputs and switch)



$20 \log_{10} (V_{O2} / V_{O1})$  or  $20 \log_{10} (V_{O1} / V_{O2})$ .

Fig 22. Test circuit for measuring crosstalk between switches



$Q_{inj} = \Delta V_O \times C_L$ .  
 $\Delta V_O$  = output voltage variation.  
 $R_{gen}$  = generator resistance.  
 $V_{gen}$  = generator voltage.

**Fig 23. Test circuit for measuring charge injection**



11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

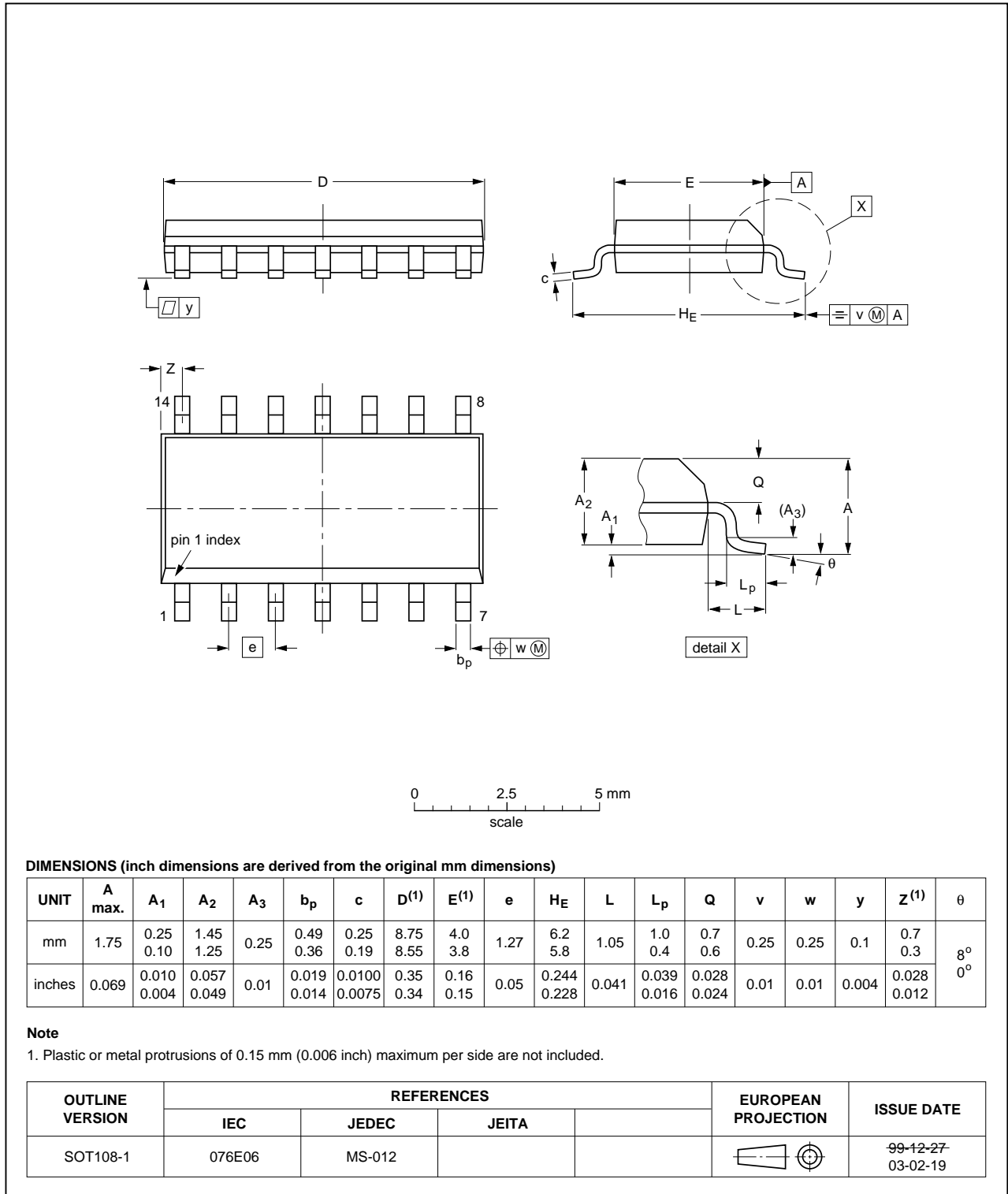


Fig 24. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

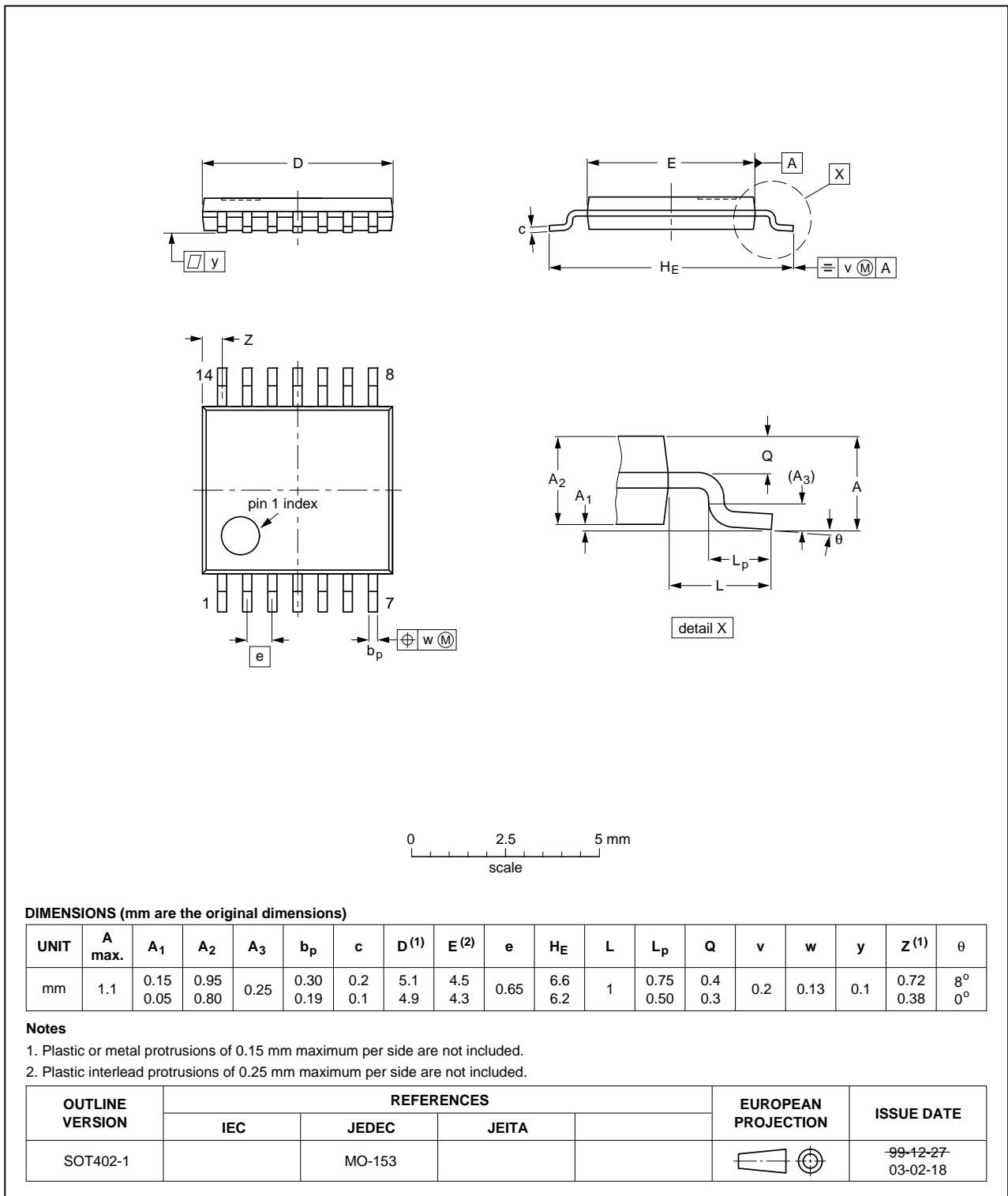


Fig 25. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

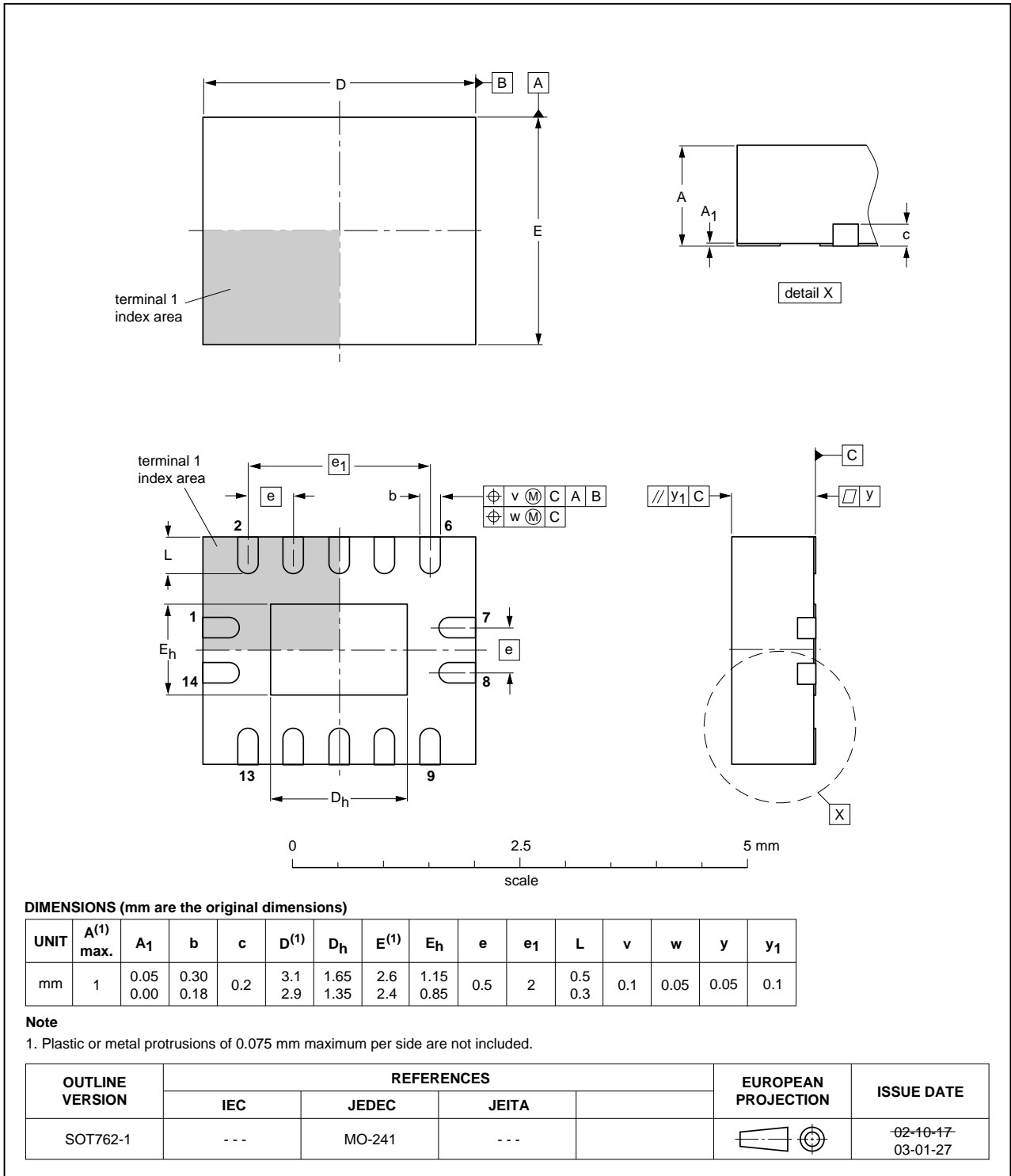


Fig 26. Package outline SOT762-1 (DHVQFN14)

## 12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
TTL	Transistor-Transistor Logic
HBM	Human Body Model
ESD	ElectroStatic Discharge
MM	Machine Model
DUT	Device Under Test
MIL	Military

## 13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC4066_Q100 v.1	20120807	Product data sheet	-	-

## 14. Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 14.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 14.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use in automotive applications** — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

#### 14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 15. Contact information

---

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

16. Contents

1 General description . . . . . 1

2 Features and benefits . . . . . 1

3 Ordering information . . . . . 2

4 Functional diagram . . . . . 2

5 Pinning information . . . . . 3

5.1 Pinning . . . . . 3

5.2 Pin description . . . . . 3

6 Functional description . . . . . 4

7 Limiting values . . . . . 4

8 Recommended operating conditions . . . . . 5

9 Static characteristics . . . . . 5

9.1 Test circuits . . . . . 6

9.2 ON resistance . . . . . 6

9.3 ON resistance test circuit and graphs . . . . . 8

10 Dynamic characteristics . . . . . 10

10.1 Waveforms and test circuit . . . . . 11

10.2 Additional dynamic characteristics . . . . . 12

10.2.1 Test circuits . . . . . 14

11 Package outline . . . . . 17

12 Abbreviations . . . . . 20

13 Revision history . . . . . 20

14 Legal information . . . . . 21

14.1 Data sheet status . . . . . 21

14.2 Definitions . . . . . 21

14.3 Disclaimers . . . . . 21

14.4 Trademarks . . . . . 22

15 Contact information . . . . . 22

16 Contents . . . . . 23

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2012. All rights reserved.

For more information, please visit: <http://www.nxp.com>  
 For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 7 August 2012  
 Document identifier: 74LVC4066\_Q100