# Precision Analog Microcontroller, Analog I/O with MDIO Interface, ARM Cortex-M3

Data Sheet

# ADuCM322

## FEATURES

- Analog input/output
  - Multichannel, 12-bit, 1 MSPS analog-to-digital converter (ADC)
    - Up to 16 ADC input channels
    - 0 V to VREF analog input range
    - Single-ended modes
    - AVDD and IOVDD monitors
  - 12-bit voltage output digital-to-analog converters (VDACs)
    - 8 VDACs with a range of 0 V to 2.5 V or $AV_{DD}$ outputs
  - Voltage comparator
- Microcontroller
  - ARM Cortex-M3 processor, 32-bit RISC architecture
  - Serial wire port supports code download and debug
- Clocking options
  - 80 MHz phase-locked loop (PLL) with programmable divider
  - Trimmed on-chip oscillator (±3%)
  - External 16 MHz crystal option
  - External clock source up to 80 MHz
- Memory
  - 2 × 128 kB independent Flash/EE memories
  - 10,000 cycle Flash/EE endurance
  - 20-year Flash/EE retention
  - 32 kB SRAM
- Software triggered in-circuit reprogrammability via management data input/output (MDIO)
- On-chip peripherals
  - MDIO slave up to 4 MHz
  - 2 × $I^2C$, 2 × SPI, UART
  - Multiple general-purpose input/output (GPIO) balls: 3.6 V compliant
  - 7 × 1.2 V compatible when used for MDIO
  - 32-element programmable logic array (PLA)
  - 3 general-purpose timers
  - Wake-up timer
  - Watchdog timer
  - 16-bit pulse width modulator (PWM)
- Power
  - Supply range: 2.9 V to 3.6 V
  - Flexible operating modes for low power applications
- Packages and temperature range
  - 6 mm × 6 mm, 96-ball CSP_BGA package
  - Fully specified for −40°C to +105°C ambient operation
- Tools
  - QuickStart development system
  - Full third-party support

## APPLICATIONS

- Optical networking

## FUNCTIONAL BLOCK DIAGRAM

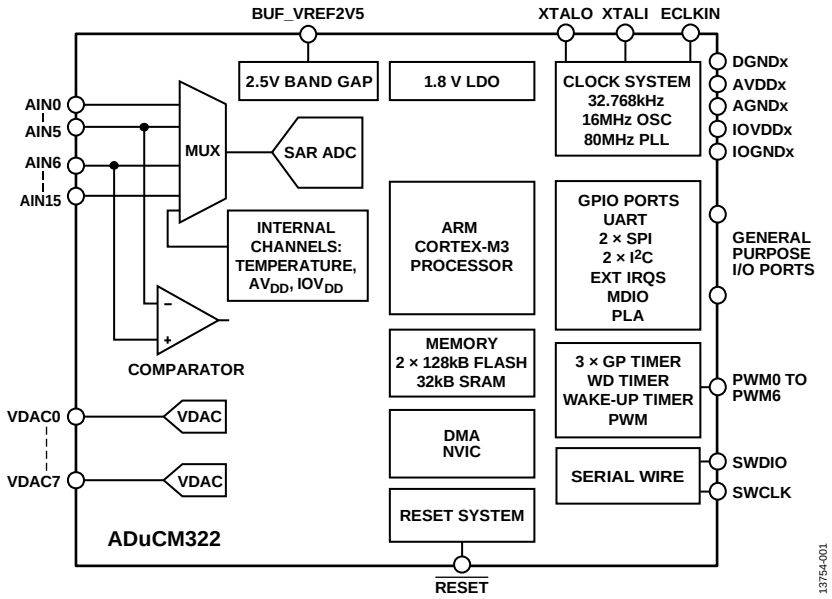


*Figure 1.*



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## REVISION HISTORY

**4/2018—Rev. 0 to Rev. A**

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**2/2016—Revision 0: Initial Version**

# GENERAL DESCRIPTION

The ADuCM322 is a fully integrated, single package device that incorporates high performance analog peripherals together with digital peripherals controlled by an 80 MHz ARM® Cortex™-M3 processor and integral flash for code and data.

The ADC on the ADuCM322 provides 12-bit, 1 MSPS data acquisition on up to 16 input balls. Additionally, chip temperature and supply voltages can be measured.

The ADC input voltage range is 0 V to VREF. A sequencer is provided, which allows a user to select a set of ADC channels to measure in sequence without software involvement during the sequence. The sequence can optionally repeat automatically at a user selectable rate. Up to eight VDACs are provided with output ranges that are programmable to one of two voltage ranges.

The ADuCM322 can be configured so that the digital and analog outputs retain their output voltages through a watchdog or software reset sequence. Thus, a product can remain functional even while the ADuCM322 is resetting itself.

The ADuCM322 has a low power ARM Cortex-M3 processor and a 32-bit RISC machine that offers up to 100 MIPS peak performance. Also integrated on-chip are 2 × 128 kB Flash/EE memory blocks and 32 kB of SRAM. The flash comprises two separate 128 kB blocks supporting execution from one flash block and simultaneous writing/erasing of the other flash block.

The ADuCM322 operates from an on-chip oscillator or a 16 MHz external crystal and a PLL at 80 MHz. This clock can optionally be divided down to reduce current consumption. Additional low power modes can be set via software. In normal operating mode, the ADuCM322 digital core consumes about 300 μA per MHz.

The device includes an MDIO interface capable of operating at up to 4 MHz. The capability to simultaneously execute from one flash block and write/erase the other flash block makes the ADuCM322 ideal for 10G, 40G, and 100G optical applications. In addition, the nonerasable kernel code plus flags in user flash provide assistance by allowing user code to robustly switch between the two blocks of user flash code and data spaces.

The ADuCM322 integrates a range of on-chip peripherals that can be configured under software control, as required in the application. These peripherals include 1 × UART, 2 × $I^2C$, and 2 × SPI serial input/output communication controllers, GPIO, 32-element PLA, three general-purpose timers, plus a wake-up timer and system watchdog timer. A 16-bit PWM with seven output channels is also provided.

GPIO balls on the device power up in high impedance input mode. In output mode, the software chooses between open-drain mode and push-pull mode. The pull-up resistors can be disabled and enabled in software. In GPIO output mode, the inputs can remain enabled to monitor the balls. The GPIO balls can also be programmed to handle digital or analog peripheral signals; in such cases, the ball characteristics are matched to the specific requirement.

A large support ecosystem is available for the ARM Cortex-M3 processor to ease product development of the ADuCM322. Access is via the ARM serial wire debug port (SW-DP). On-chip factory firmware supports in-circuit serial download via MDIO. These features are incorporated into a QuickStart™ development system, supporting this precision analog microcontroller family.

# SPECIFICATIONS

## MICROCONTROLLER ELECTRICAL SPECIFICATIONS

AVDD = IOVDD = VDD1 = 2.9 V to 3.6 V (see Figure 12), maximum difference between supplies = 0.3 V, VREF = 2.5 V internal reference, $f_{CORE}$ = 80 MHz, $T_A$ = −40°C to +105°C, unless otherwise noted. The power-up sequence must be VDD1, IOVDDx, and AVDDx, but no delays in the sequence are required.

**Table 1.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| ADC BASIC SPECIFICATIONS | | | | | | Single-ended mode, unless otherwise stated |
| ADC Power-Up Time | | | 5 | | µs | |
| Data Rate | $f_{SAMPLE}$ | | | 1 | MSPS | |
| DC Accuracy[1] | | 12 | | | Bits | 1 LSB = 2.5 V/$2^{12}$ |
| Resolution[1] | | 16 | | | Bits | Number of data bits |
| Integral Nonlinearity | INL | | ±1.75 | | LSB | 2.5 V internal reference; 1 LSB = 2.5 V/$2^{12}$ |
| | | | ±1.75 | | LSB | 2.5 V external reference; 1 LSB = 2.5 V/$2^{12}$ |
| Differential Nonlinearity | DNL | −0.99 | ±0.75 | +1.5 | LSB | 2.5 V internal reference; 1 LSB = 2.5 V/$2^{12}$ |
| | | | ±0.75 | | LSB | 2.5 V external reference; 1 LSB = 2.5 V/$2^{12}$ |
| DC Code Distribution | | | ±3 | | LSB | ADC input 1.25 V; 1 LSB = 2.5 V/$2^{12}$ |
| ADC ENDPOINT ERRORS | | | | | | |
| Offset Error | | | ±200 | | µV | |
| Drift[1] | | −3.92 | 0.3 | +1.21 | µV/°C | Using 2.5 V external reference |
| Match | | | ±1 | | LSB | Matching compared to AIN8 |
| Full-Scale Error | | | ±400 | | µV | |
| Gain Drift[1] | | −4 | | +5 | µV/°C | Full-scale error drift minus offset error drift |
| Match | | | ±1 | | LSB | |
| ADC DYNAMIC PERFORMANCE | | | | | | $f_{IN}$ = 665.25 Hz sine wave, $f_{SAMPLE}$ = 100 kSPS; input filter = 15 Ω, $C_L$ = 2 nF |
| Signal-to-Noise Ratio | SNR | | 80 | | dB | Includes distortion and noise components |
| Total Harmonic Distortion | THD | | −86 | | dB | |
| Peak Harmonic or Spurious Noise | | | −88 | | dB | |
| Channel-to-Channel Crosstalk | | | −90 | | dB | Measured on adjacent channels |
| ADC INPUT | | | | | | |
| Input Voltage Ranges | | | | | | |
| Single-Ended Mode[1] | | AGND | | VREF | | |
| Compliance[1] | | AGND4 | | AVDD4 | | |
| Leakage Current | | | ±1.5 | | nA | |
| Input Current | | | ±9 | | µA/V | At 1 MSPS |
| | | | ±6 | | µA/V | ≤800 kSPS |
| | | | ±4 | | µA/V | 500 kSPS, ADCCNVC, Bits[25:16] = 0x1E |
| Input Capacitance | | | 20 | | pF | During ADC acquisition |
| ON-CHIP VOLTAGE REFERENCE | | | 2.51 | | V | 0.47 µF from VREF_1V2 to AGND4; reference is measured with all ADC and VDACs enabled |
| Accuracy | | | | ±5 | mV | $T_A$ = 25°C |
| Reference Temperature Coefficient[1] | | −59 | ±15 | 38 | ppm/°C | |
| Power Supply Rejection Ratio | PSRR | | 60 | | dB | |
| Internal $V_{REF}$ Power-On Time | | | 50 | | ms | |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| EXTERNAL REFERENCE INPUT | | | | | | |
| Range[1] | | 1.8 | | 2.5 | V | ADC |
| Input Current | | | 200 | | μA | |
| BUFFERED REFERENCE OUTPUT | | | | | | |
| Output Voltage | | | 2.504 | | V | |
| Accuracy | | | ±8 | | mV | $T_A$ = 25°C, load = 1.2 mA |
| Reference Temperature Coefficient[1] | | −115 | ±15 | 115 | μV/°C | 100 nF from BUF_VREF2V5 to AGND4 |
| Output Impedance | | | 10 | | Ω | $T_A$ = 25°C |
| Load Current[1] | | | | 1.2 | mA | |
| VDAC CHANNEL SPECIFICATIONS | | | | | | $R_L$ = 5 kΩ, $C_L$ = 100 pF[2] |
| DC Accuracy[1] | | 12 | | | Bits | 1 LSB = 2.5 V/$2^{12}$ |
| Resolution[1] | | 12 | | | Bits | Number of data bits |
| Relative Accuracy[3] | INL | | ±4 | | LSB | 1 LSB = 2.5 V/$2^{12}$ |
| Differential Nonlinearity[3] | DNL | −0.99 | | +1 | LSB | Guaranteed monotonic, 1 LSB = 2.5 V/$2^{12}$ |
| Offset Error | | | ±3 | ±15 | mV | 2.5 V internal reference, DAC Output Code 0 |
| Drift | | | ±18 | | μV/°C | |
| Gain Error[4] | | | ±0.3 | ±0.85 | % | 0 V to internal $V_{REF}$ range |
| | | | ±0.4 | ±1 | % | 0 V to AVDD range |
| Drift | | | 6.5 | | ppm/°C | Excluding reference drift |
| Mismatch | | | 0.1 | | % | % of full scale on DAC0 |
| Analog Outputs | | | | | | |
| Output Voltage Range 1[1] | | 0.15 | | 2.5 | V | |
| Output Voltage Range 2[1] | | 0.15 | | AVDDx − 0.15 | V | |
| Output Impedance | | | 2 | | Ω | |
| DAC AC Characteristics | | | | | | |
| Output Settling Time | | | 10 | | μs | Settled to ±1 LSB |
| Glitch Energy | | | ±20 | | nV-sec | 1 LSB change when the maximum number of bits changes simultaneously in the DACxDAT register |
| COMPARATOR | | | | | | |
| Input | | | | | | |
| Offset Voltage | | | ±10 | | mV | |
| Bias Current | | | 1 | | nA | |
| Voltage Range[1] | | AGNDx | | AVDDx − 1.2 | V | |
| Capacitance | | | 7 | | pF | |
| Hysteresis[1] | | 8.5 | | 15 | mV | When enabled in software |
| Response Time | | | 7 | | μs | AFECOMP, Bits[2:1] = 0 |
| TEMPERATURE SENSOR | | | | | | Indicates die temperature, see Figure 9 |
| Resolution | | | 0.5 | | °C | When precision calibrated by the user[5] |
| Accuracy[1] | | 1.34 | | 1.43 | V | ADC measured voltage for temperature sensor channel without calibration, $T_A$ = 25°C |
| POWER-ON RESET | POR | | 2.85 | 2.9 | V | |
| WATCHDOG TIMER | WDT | | | | | |
| Timeout Period | | | 32 | | sec | Default at power-up |
| FLASH/EE MEMORY | | | | | | |
| Endurance[1] | | 10,000 | | | Cycles | |
| Data Retention[1] | | 20 | | | Years | $T_J$ = 85°C |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| DIGITAL INPUTS | | | | | | |
| Input Leakage Current | | | | | | |
| Logic 1 GPIO | | | 1 | | nA | $V_{IH} = V_{DD}$, pull-up resistor disabled |
| Logic 0 GPIO | | | 10 | | nA | $V_{IL} = 0$ V, pull-up resistor disabled |
| PRTADDRx | | | | | | |
| Input Leakage Current | | | 16 | | µA | $V_{IN}$ = 0 V to 1.8 V, due to weak pull-up resistors to 1.8 V |
| Input Voltage | | 0.84 | | 1.5 | V | External resistor 91 kΩ ± 1% to ground; range for CFP MSA high[1] |
| Input Capacitance, All Balls Except MCK, MDIO, PRTADDRx, and XTALx | | | 10 | | pF | |
| Input Capacitance | | | | | | |
| MCK, PRTADDRx | | | 6.5 | | pF | |
| MDIO | | | 8.5 | | pF | |
| Ball Capacitance | | | | | | |
| XTALI | | | 5 | | pF | |
| XTALO | | | 5 | | pF | |
| LOGIC INPUTS | | | | | | |
| GPIO Input Voltage | | | | | | |
| Low | $V_{INL}$ | | | 0.25 × IOVDDx | V | |
| High | $V_{INH}$ | 0.58 × IOVDDx | | | V | |
| MDIO | | | | | | |
| PRTADDRx Input Voltage | | | | | | |
| Low | $V_{INL}$ | | | 0.36 | V | |
| High | $V_{INH}$ | 0.84 | | | V | |
| MCK, MDIO Input Voltage | | | | | | Setup time ≥10 ns; hold time ≥10 ns; MCK/MDIO |
| Low | $V_{INL}$ | | | 0.36 | V | |
| High | $V_{INH}$ | 0.84 | | | V | |
| XTALI Input Voltage | | | | | | |
| Low | $V_{INL}$ | | 1.1 | | V | |
| High | $V_{INH}$ | | 1.7 | | V | |
| Pull-Up Current | | 30 | | 120 | µA | $V_{IN}$ = 0 V, see Figure 10 |
| Pull-Down Current | | 30 | | 100 | µA | $V_{IN}$ = 3.3 V, see Figure 10 |
| LOGIC OUTPUTS | | | | | | All digital outputs excluding XTALO |
| GPIO Output Voltage[6] | | | | | | |
| High | $V_{OH}$ | IOVDDx − 0.4 | | | V | $I_{SOURCE}$ = 2 mA |
| Low | $V_{OL}$ | | | 0.4 | V | $I_{SINK}$ = 2 mA |
| GPIO Short-Circuit Current[1] | | | 11 | | mA | See Figure 11 |
| MDIO | | | | | | |
| Output Voltage | | | | | | |
| High | $V_{OH}$ | 1.0 | | | V | $I_{SOURCE}$ = 4 mA |
| Low | $V_{OL}$ | | | 0.2 | V | $I_{SINK}$ = 4 mA |
| Delay Time | | | | 100 | ns | MCK to MDIO out |
| OSCILLATORS | | | | | | |
| Internal System Oscillator | | | 16 | | MHz | |
| Accuracy | | | ±0.5 | ±3 | % | |
| System PLL | | | 80 | | MHz | Main system clock |
| External Crystal Oscillator | | | 16 | | MHz | Can be selected in place of the internal oscillator |
| 32 kHz Internal Oscillator | | | 32.768 | | kHz | Use for watchdog |
| Accuracy | | | ±5 | ±20 | % | |
| External Clock | | 0.05 | | 80 | MHz | Can be selected in place of PLL |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| START-UP TIME | | | | | | Processor clock = 80 MHz |
| At Power-On | | | 50 | | ms | POR to first user code execution |
| After Other Reset | | | 1.5 | | ms | Reset to first user code execution |
| From All Power-Down Modes | | | 1.25 | | µs | |
| PROGRAMMABLE LOGIC ARRAY | PLA | | | | | |
| Propagation Delay | | | | | | |
| Ball | | | 17 | | ns | From input ball to output ball |
| Element | | | 1.5 | | ns | Per PLA cell |
| EXTERNAL INTERRUPTS | | | | | | |
| Pulse Width[1] | | | | | | |
| Level Triggered | | 7 | | | ns | |
| Edge Triggered | | 1 | | | ns | |
| POWER REQUIREMENTS[7] | | | | | | |
| Power Supply Voltage Range | | | | | | |
| AVDDx to AGNDx and IOVDDx to DGNDx[1] | | 2.9 | 3.3 | 3.6 | V | |
| Analog Power Supply Currents | | | | | | |
| AVDDx Current | | | 4.9 | | mA | Analog peripherals in idle mode |
| Digital Power Supply Current | | | | | | |
| IOVDDx Current in Normal Mode | | | 2.7 | | mA | All GPIO pull-up resistors enabled |
| VDDx Current | | | | | | |
| Normal Mode | | | 29 | | mA | Clock divider (CD) = 0 (80 MHz clock), executing typical code |
| | | | 20 | | mA | CD = 1, executing typical code |
| | | | 10 | | mA | CD = 7, executing typical code |
| CORE_SLEEP Mode | | | 16 | | mA | |
| SYS_SLEEP Mode | | | 8 | | mA | |
| Hibernate Mode | | | 4 | | mA | |
| Additional Power Supply Currents | | | | | | |
| ADC | | | 4.1 | | mA | Continuously converting at 100 kSPS |
| DAC | | | 340 | | µA | Per powered up DAC, excluding load current |
| Total Supply Current | | | 37 | | mA | VDD1, IOVDDx, AVDDx connected together; condition when entering user code: peripheral clocks on, peripherals idle, no load currents |
| Thermal Performance | | | | | | |
| Impedance Junction to Ambient | | | 45 | | °C/W | JEDEC 2S2P |

[1] These specifications are not production tested but are guaranteed by design and/or characterization data at production release.
[2] The data in this section also applies for a load of $R_L$ =1 kΩ and $C_L$ = 100 pF but only an output range of 0 V to 2.5 V. However, this specification is not production tested.
[3] DAC linearity is calculated using a reduced code range of 100 to 3900.
[4] DAC gain error is calculated using a reduced code range of 100 to an internal 2.5 V $V_{REF}$.
[5] Due to self heating, internal temperature measurements cannot be used to predict external temperatures. This value is only relevant after user calibration and only for internal and external conditions identical to those at calibration.
[6] The average current from all GPIO balls must not exceed 3 mA per ball.
[7] Power figures exclude any load currents to external circuits.

## TIMING SPECIFICATIONS

### *I²C Timing*

**Table 2. I²C Timing in Standard Mode (100 kHz)**

| | | Slave | | | |
|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min** | **Typ** | **Max** | **Unit** |
| $t_L$ | SCL low pulse width | 4.7 | | | µs |
| $t_H$ | SCL high pulse width | 4.0 | | | ns |
| $t_{SHD}$ | Start condition hold time | 4.0 | | | µs |
| $t_{DSU}$ | Data setup time | 250 | | | ns |
| $t_{DHD}$ | Data hold time (SDA held internally for 300 ns after falling edge of SCL) | 0 | | 3.45 | µs |
| $t_{RSU}$ | Setup time for repeated start | 4.7 | | | µs |
| $t_{PSU}$ | Stop condition setup time | 4.0 | | | µs |
| $t_{BUF}$ | Bus-free time between a stop condition and a start condition | 4.7 | | | µs |
| $t_R$ | Rise time for both SLC and SDA | | | 1 | µs |
| $t_F$ | Fall time for both SLC and SDA | | 15 | 300 | ns |
| $t_{VD;DAT}$ | Data valid time | | | 3.45 | µs |
| $t_{VD;ACK}$ | Data valid acknowledge time | | | 3.45 | µs |

**Table 3. I²C Timing in Fast Mode (400 kHz)**

| | | Slave | | | |
|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min** | **Typ** | **Max** | **Unit** |
| $t_L$ | SCL low pulse width | 1.3 | | | µs |
| $t_H$ | SCL high pulse width | 0.6 | | | ns |
| $t_{SHD}$ | Start condition hold time | 0.3 | | | µs |
| $t_{DSU}$ | Data setup time | 100 | | | ns |
| $t_{DHD}$ | Data hold time (SDA held internally for 300 ns after falling edge of SCL) | 0 | | | µs |
| $t_{RSU}$ | Setup time for repeated start | 0.6 | | | µs |
| $t_{PSU}$ | Stop condition setup time | 0.3 | | | µs |
| $t_{BUF}$ | Bus-free time between a stop condition and a start condition | 1.3 | | | µs |
| $t_R$ | Rise time for both SCL and SDA | 20 | | 300 | ns |
| $t_F$ | Fall time for both SCL and SDA | | 15 | 300 | ns |
| $t_{VD;DAT}$ | Data valid time | | | 0.9 | µs |
| $t_{VD;ACK}$ | Data valid acknowledge time | | | 0.9 | µs |

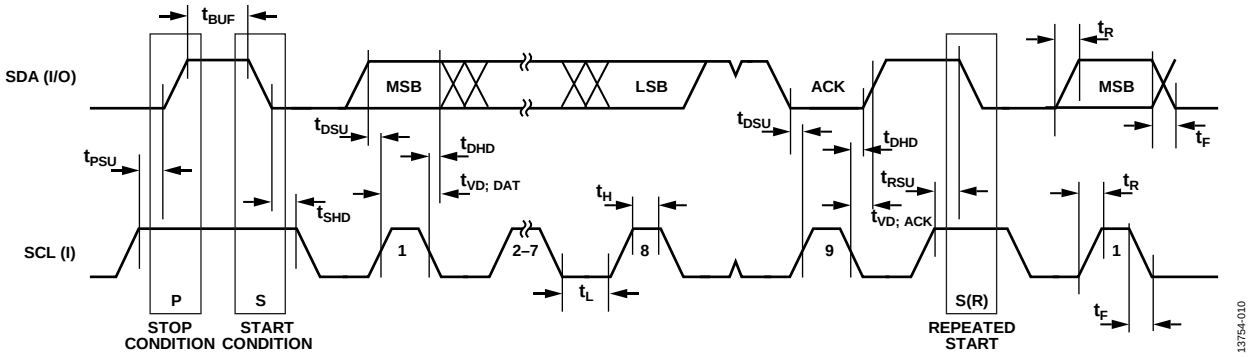


*Figure 2. I²C Compatible Interface Timing*

### *SPI Timing*

**Table 4. SPI Master Mode Timing (Phase Mode = 1)**

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SL}$ | SCLK low pulse width | | (SPIDIV + 1) × $t_{HCLK}$/2 | | ns |
| $t_{SH}$ | SCLK high pulse width | | (SPIDIV + 1) × $t_{HCLK}$/2 | | ns |
| $t_{DAV}$ | Data output valid after SCLK edge | 0 | 3 | | ns |
| $t_{DSU}$ | Data input setup time before SCLK edge | | ½ SCLK | | ns |
| $t_{DHD}$ | Data input hold time after SCLK edge | | SCLK | | ns |
| $t_{DF}$ | Data output fall time | | SCLK | | ns |
| $t_{DR}$ | Data output rise time | | 25 | | ns |
| $t_{SR}$ | SCLK rise time | | 25 | | ns |
| $t_{SF}$ | SCLK fall time | | 20 | | ns |

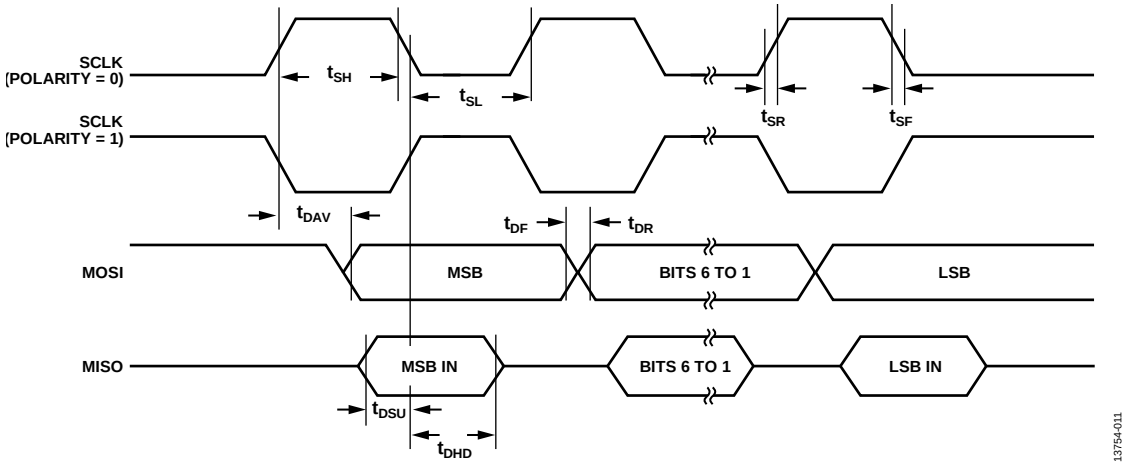


*Figure 3. SPI Master Mode Timing (Phase Mode = 1)*

**Table 5. SPI Master Mode Timing (Phase Mode = 0)**

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SL}$ | SCLK low pulse width | | (SPIDIV + 1) × $t_{HCLK}$/2 | | ns |
| $t_{SH}$ | SCLK high pulse width | | (SPIDIV + 1) × $t_{HCLK}$/2 | | ns |
| $t_{DAV}$ | Data output valid after SCLK edge | 0 | 3 | | ns |
| $t_{DOSU}$ | Data output setup before SCLK edge | | ½ SCLK | | ns |
| $t_{DSU}$ | Data input setup time before SCLK edge | | SCLK | | ns |
| $t_{DHD}$ | Data input hold time after SCLK edge | | SCLK | | ns |
| $t_{DF}$ | Data output fall time | | 25 | | ns |
| $t_{DR}$ | Data output rise time | | 25 | | ns |
| $t_{SR}$ | SCLK rise time | | 20 | | ns |
| $t_{SF}$ | SCLK fall time | | 20 | | ns |

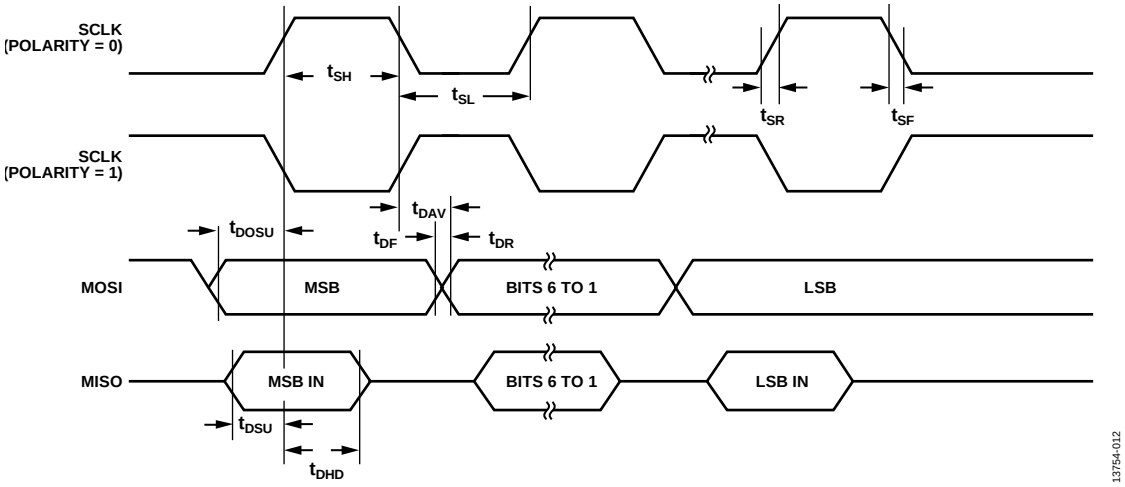


*Figure 4. SPI Master Mode Timing (Phase Mode = 0)*

**Table 6. SPI Slave Mode Timing (Phase Mode = 1)**

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{\overline{CS}}$ | $\overline{CS}$ to SCLK edge | 10 | | | ns |
| $t_{\overline{CSM}}$ | $\overline{CS}$ high time between active periods | SCLKx | | | ns |
| $t_{SL}$ | SCLK low pulse width | | (SPIDIV + 1) × $t_{HCLK}$ | | ns |
| $t_{SH}$ | SCLK high pulse width | | (SPIDIV + 1) × $t_{HCLK}$ | | ns |
| $t_{DAV}$ | Data output valid after SCLK edge | | 20 | | ns |
| $t_{DSU}$ | Data input setup time before SCLK edge | 10 | | | ns |
| $t_{DHD}$ | Data input hold time after SCLK edge | 10 | | | ns |
| $t_{DF}$ | Data output fall time | | 25 | | ns |
| $t_{DR}$ | Data output rise time | | 25 | | ns |
| $t_{SR}$ | SCLK rise time | 1 | | | ns |
| $t_{SF}$ | SCLK fall time | 1 | | | ns |
| $t_{SFS}$ | $\overline{CS}$ high after SCLK edge | 20 | | | ns |

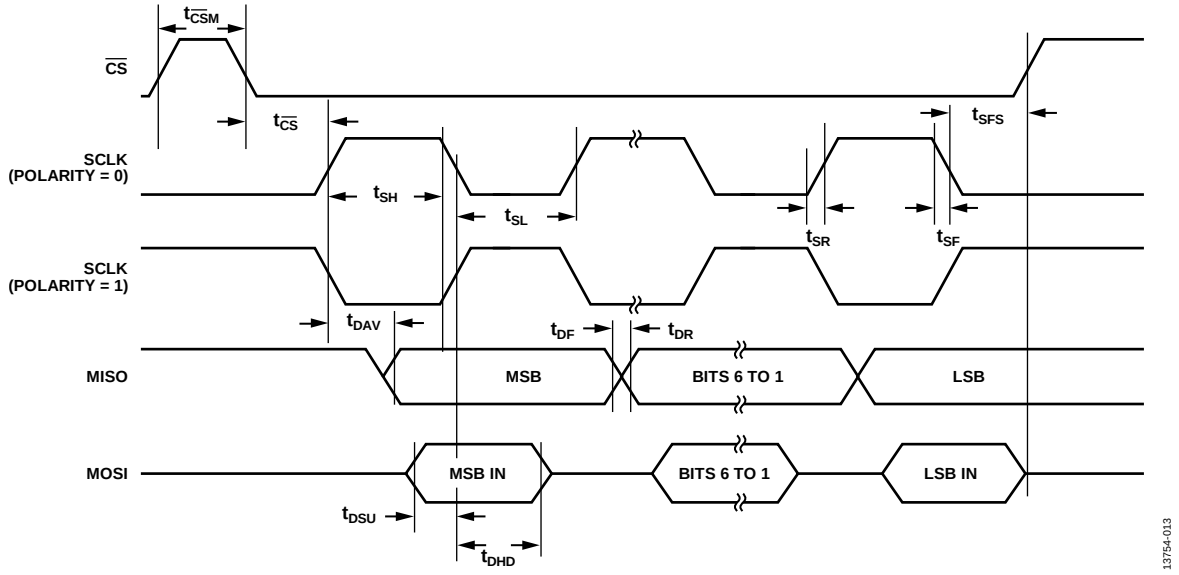


*Figure 5. SPI Slave Mode Timing (Phase Mode = 1)*

**Table 7. SPI Slave Mode Timing (Phase Mode = 0)**

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{\overline{CS}}$ | $\overline{CS}$ to SCLK edge | 10 | | | ns |
| $t_{\overline{CSM}}$ | $\overline{CS}$ high time between active periods | SCLKx | | | ns |
| $t_{SL}$ | SCLK low pulse width | | (SPIDIV + 1) × $t_{HCLK}$ | | ns |
| $t_{SH}$ | SCLK high pulse width | | (SPIDIV + 1) × $t_{HCLK}$ | | ns |
| $t_{DAV}$ | Data output valid after SCLK edge | | 20 | | ns |
| $t_{DSU}$ | Data input setup time before SCLK edge | 10 | | | ns |
| $t_{DHD}$ | Data input hold time after SCLK edge | 10 | | | ns |
| $t_{DF}$ | Data output fall time | | 25 | | ns |
| $t_{DR}$ | Data output rise time | | 25 | | ns |
| $t_{SR}$ | SCLK rise time | 1 | | | ns |
| $t_{SF}$ | SCLK fall time | 1 | | | ns |
| $t_{DOCS}$ | Data output valid after $\overline{CS}$ edge | 20 | | | ns |
| $t_{SFS}$ | $\overline{CS}$ high after SCLK edge | 10 | | | ns |

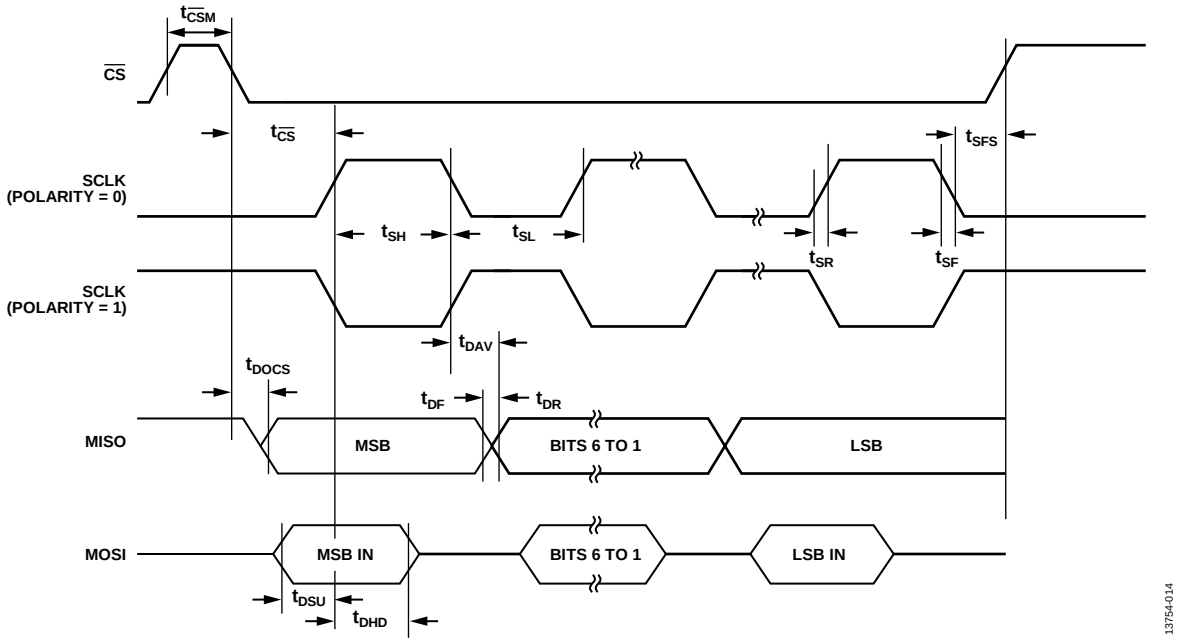


*Figure 6. SPI Slave Mode Timing (Phase Mode = 0)*

**Table 8. MDIO vs. MDC Timing**

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SETUP}$ | MDIO setup before MCK edge | 10 | | | ns |
| $t_{HOLD}$ | MDIO valid after MCK edge | 10 | | | ns |
| $t_{DELAY}$ | Data output after MCK edge | | | 100 | ns |

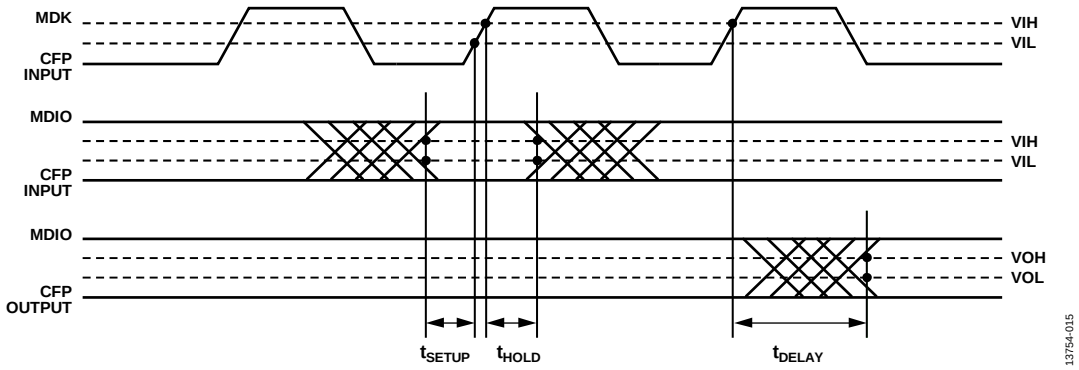


*Figure 7. MDIO Timing*

## ABSOLUTE MAXIMUM RATINGS

**Table 9.**

| Parameter | Rating |
|---|---|
| Any Ball to GND | −0.3 V to +3.9 V |
| Any RES1 Type Ball to GND | −0.3 V to +2.8 V |
| MDIO,[1] MCK and PRTADDR0 to PRTADDR4 in MDIO Mode to GND | −0.3 V to +2.1 V |
| Between Any of AVDDx, IOVDDx, and VDD1 Balls | −0.3 V to +0.3 V |
| Any I Type Ball to GND[2] | −0.3 V to IOVDDx + 0.3 V |
| Any RES Type, AI Type, or AO Type Ball to GND[3] | −0.3 V to AVDDx + 0.3 V |
| ADC_REFP to GND | −0.3 V to AVDDx + 0.3 V |
| Total Positive GPIO Ball Currents | 0 mA to 30 mA |
| Total Negative GPIO Ball Currents | −30 mA to 0 mA |
| Maximum Power Dissipation | 1 W |
| Operating Ambient Temperature Range | −40°C to +105°C |
| Storage Temperature Range | −65°C to +160°C |
| Operating Junction Temperature Range | −40°C to +150°C |
| Electrostatic Discharge (ESD) | |
| Human Body Model (HBM) | 2 kV |
| Field Induced Charged Device Mode (FICDM) | 1 kV |

[1] Note this ball is always in MDIO mode.
[2] This limit does not apply if no current can be drawn by external circuits on IOVDDx, because then IOVDD follows to a suitable level.
[3] This limit does not apply if no current can be drawn by external circuits on AVDDx, because then AVDD follows to a suitable level.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

All requirements applicable to each ball must be met. Where multiple limits apply to a ball, each one must be met individually. The limits apply according to the functionality of the balls at the time. Balls that can be either analog or digital, that is, that have two types indicated in the ball descriptions, must meet the limits for both types. For ball types, see Table 10.

When powered up, it is required that all ground balls and ADC_REFN be connected together to a node referred to as GND in Table 9. The limits that are listed must be reduced by any difference between any GNDs. Also, it is required that AVDD3 is connected to AVDD4 and that IOVDD1 to IOVDD3 are connected together.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

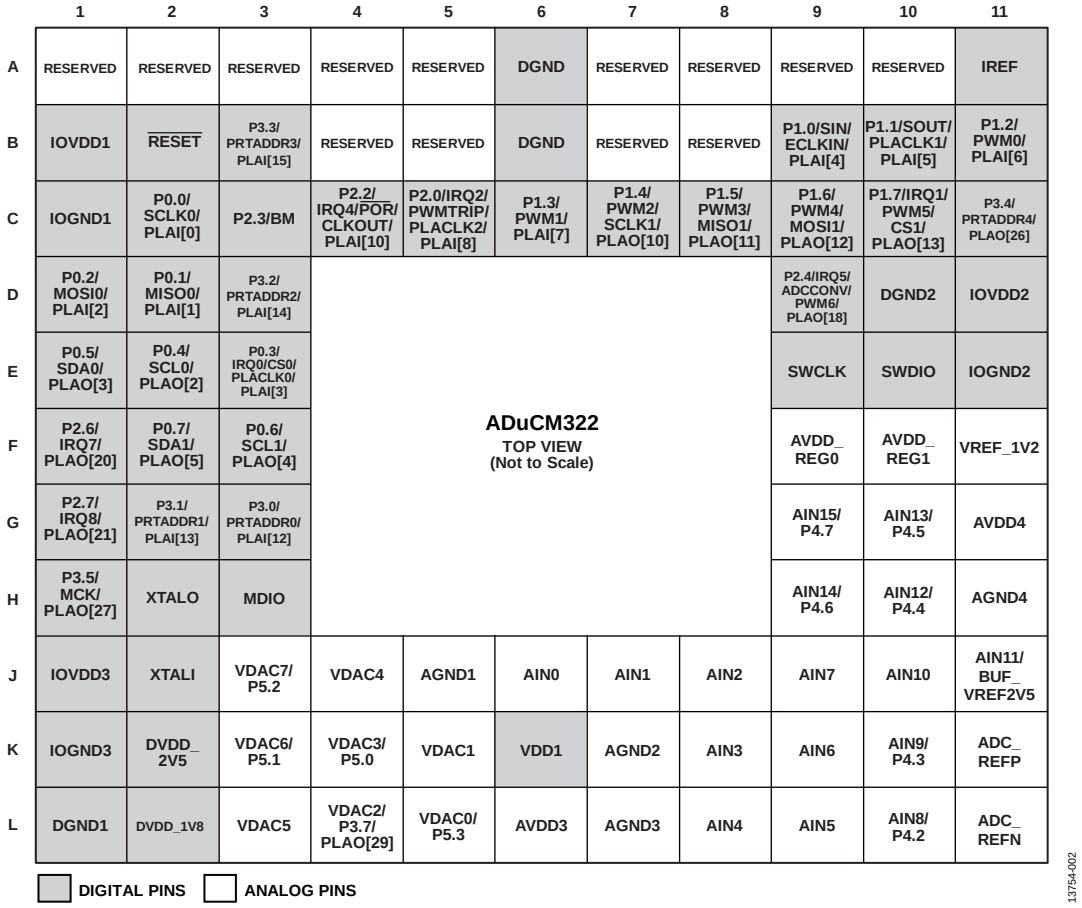


*Figure 8. Pin Configuration*

**Table 10. Pin Function Descriptions**

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| A1 | RESERVED | RES | No Connect. Leave this ball unconnected. |
| A2 | RESERVED | RES | Connect to AGND. |
| A3 | RESERVED | RES1 | Connect to AVDD_REG1. |
| A4 | RESERVED | RES1 | Connect to AVDD_REG1. |
| A5 | RESERVED | RES | Connect to AGND. |
| A6 | DGND | S | Power Supply Ground. |
| A7 | RESERVED | RES | Connect to AGND. |
| A8 | RESERVED | RES1 | Connect to AVDD_REG1. |
| A9 | RESERVED | RES1 | Connect to AVDD_REG1. |
| A10 | RESERVED | RES | Connect to AGND. |
| A11 | IREF | AI | Reference Current. This ball generates the reference current and is set by an external resistor, $R_{EXT}$. Connect a 3.3 kΩ $R_{EXT}$ from IREF to DGND. |
| B1 | IOVDD1 | S | 3.3 V GPIO Supply. |
| B2 | $\overline{\text{RESET}}$ | I | Reset Input (Active Low). An internal pull-up resistor is included. |
| B3 | P3.3/PRTADDR3/PLAI[15] | I/O | Digital Input/Output Port 3.3 (P3.3).<br>MDIO Port Address Bit 3 (PRTADDR3). See the Digital Inputs parameter in Table 1 for details.<br>Output of PLA Element 15 (PLAI[15]). |
| B4 | RESERVED | RES | No Connect. Leave this ball unconnected. |
| B5 | RESERVED | RES | No Connect. Leave this ball unconnected. |
| B6 | DGND | S | Power Supply Ground. |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| B7 | RESERVED | RES | No Connect. Leave this ball unconnected. |
| B8 | RESERVED | RES | No Connect. Leave this ball unconnected. |
| B9 | P1.0/SIN/ECLKIN/PLAI[4] | I/O | Digital Input/Output Port 1.0 (P1.0).<br>UART Input (SIN).<br>External Input Clock (ECLKIN).<br>Input to PLA Element 4 (PLAI[4]). |
| B10 | P1.1/SOUT/PLACLK1/PLAI[5] | I/O | Digital Input/Output Port 1.1 (P1.1).<br>UART Output (SOUT).<br>PLA Clock 1(PLACLK1).<br>Input to PLA Element 5 (PLAI[5]). |
| B11 | P1.2/PWM0/PLAI[6] | I/O | Digital Input/Output Port 1.2 (P1.2).<br>PWM Output 0 (PWM0).<br>Input to PLA Element 6 (PLAI[6]). |
| C1 | IOGND1 | S | Ground for IOVDD1. |
| C2 | P0.0/SCLK0/PLAI[0] | I/O | Digital Input/Output Port 0.0 (P0.0).<br>SPI0 Clock (SCLK0).<br>Input to PLA Element 0 (PLAI[0]). |
| C3 | P2.3/BM | I/O | Digital Input/Output Port 2.3 (P2.3).<br>Boot Mode (BM). This ball determines the start-up sequence after every reset. Pull-up is enabled at power-up. |
| C4 | P2.2/IRQ4/$\overline{\text{POR}}$/CLKOUT/PLAI[10] | I/O | Digital Input/Output Port 2.2 (P2.2).<br>External Interrupt 4 (IRQ4).<br>Reset Output ($\overline{\text{POR}}$). This ball function is an output and it is the default for Ball C4.<br>Clock Output (CLKOUT).<br>Input to PLA Element 10 (PLAI[10]). |
| C5 | P2.0/IRQ2/PWMTRIP/PLACLK2/PLAI[8] | I/O | Digital Input/Output Port 2.0 (P2.0).<br>External Interrupt 2 (IRQ2).<br>PWM Trip (PWMTRIP).<br>PLA Input Clock 2 (PLACLK2).<br>Input to PLA Element 8 (PLAI[8]). |
| C6 | P1.3/PWM1/PLAI[7] | I/O | Digital Input/Output Port 1.3 (P1.3).<br>PWM Output 1 (PWM1).<br>Input to PLA Element 7 (PLAI[7]). |
| C7 | P1.4/PWM2/SCLK1/PLAO[10] | I/O | Digital Input/Output Port 1.4 (P1.4).<br>PWM Output 2 (PWM2).<br>SPI1 Clock (SCLK1).<br>Output of PLA Element 10 (PLAO[10]). |
| C8 | P1.5/PWM3/MISO1/PLAO[11] | I/O | Digital Input/Output Port 1.5 (P1.5).<br>PWM Output 3 (PWM3).<br>SPI1 Master In, Slave Out (MISO1).<br>Output of PLA Element 11 (PLAO[11]). |
| C9 | P1.6/PWM4/MOSI1/PLAO[12] | I/O | Digital Input/Output Port 1.6 (P1.6).<br>PWM Output 4 (PWM4).<br>SPI1 Master Out, Slave Input (MOSI1).<br>Output of PLA Element 12 (PLAO[12]). |
| C10 | P1.7/IRQ1/PWM5/CS1/PLAO[13] | I/O | Digital Input/Output Port 1.7 (P1.7).<br>External Interrupt 1 (IRQ1).<br>PWM Output 5 (PWM5).<br>SPI1 Chip Select 1 (CS1). When using SPI1, configure this ball as CS1.<br>Output of PLA Element 13 (PLAO[13]). |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| C11 | P3.4/PRTADDR4/PLAO[26] | I/O | Digital Input/Output Port 3.4 (P3.4).<br>MDIO Port Address Bit 4 (PRTADDR4). See the Digital Inputs parameter in Table 1 for details.<br>Output of PLA Element 26 (PLAO[26]). |
| D1 | P0.2/MOSI0/PLAI[2] | I/O | Digital Input/Output Port 0.2 (P0.2).<br>SPI0 Master Out, Slave In (MOSI0).<br>Input to PLA Element 2 (PLAI[2]). |
| D2 | P0.1/MISO0/PLAI[1] | I/O | Digital Input/Output Port 0.1 (P0.1).<br>SPI0 Master In, Slave Out (MISO0).<br>Input to PLA Element 1 (PLAI[1]). |
| D3 | P3.2/PRTADDR2/PLAI[14] | I/O | Digital Input/Output Port 3.2 (P3.2).<br>MDIO Port Address Bit 2 (PRTADDR2). See the Digital Inputs parameter in Table 1 for details.<br>Input to PLA Element 14 (PLAI[14]). |
| D9 | P2.4/IRQ5/ADCCONV/PWM6/PLAO[18] | I/O | Digital Input/Output Port 2.4 (P2.4).<br>External Interrupt 5 (IRQ5).<br>External Input to Start ADC Conversions (ADCCONV).<br>PWM Output 6 (PWM6).<br>Output of PLA Element 18 (PLAO[18]). |
| D10 | DGND2 | S | Digital Ground 2. Connect to DGND1. |
| D11 | IOVDD2 | S | 3.3 V GPIO Supply. |
| E1 | P0.5/SDA0/PLAO[3] | I/O | Digital Input/Output Port 0.5 (P0.5).<br>I²C0 Serial Data (SDA0).<br>Output of PLA Element 3 (PLAO[3]). |
| E2 | P0.4/SCL0/PLAO[2] | I/O | Digital Input/Output Port 0.4 (P0.4).<br>I²C0 Serial Clock (SCL0).<br>Output of PLA Element 2 (PLAO[2]). |
| E3 | P0.3/IRQ0/CS0/PLACLK0/PLAI[3] | I/O | Digital Input/Output Port 0.3 (P0.3).<br>External Interrupt 0 (IRQ0).<br>SPI0 Chip Select 0 (CS0). When using SPI0, configure this ball as CS0.<br>PLA Clock 0 (PLACLK0).<br>Input to PLA Element 3 (PLAI[3]). |
| E9 | SWCLK | I | Serial Wire Debug Clock. |
| E10 | SWDIO | I/O | Serial Wire Bidirectional Data. |
| E11 | IOGND2 | S | Ground for IOVDD2. |
| F1 | P2.6/IRQ7/PLAO[20] | I/O | Digital Input/Output Port 2.6 (P2.6).<br>External Interrupt 7 (IRQ7).<br>Output of PLA Element 20 (PLAO[20]). |
| F2 | P0.7/SDA1/PLAO[5] | I/O | Digital Input/Output Port 0.7 (P0.7).<br>I²C1 Serial Data (SDA1).<br>Output of PLA Element 5 (PLAO[5]). |
| F3 | P0.6/SCL1/PLAO[4] | I/O | Digital Input/Output Port 0.6 (P0.6).<br>I²C1 Serial Clock (SCL1).<br>Output of PLA Element 4 (PLAO[4]). |
| F9 | AVDD_REG0 | AO | Analog Regulator 0 Supply. A 470 nF capacitor to AGND4 must be connected to this ball to stabilize the internal 2.5 V regulator that supplies the ADC. |
| F10 | AVDD_REG1 | AO | Analog Regulator 1 Supply. Output of 2.5 V on-chip LDO regulator. A 470 nF capacitor to AGND4 must be connected to this ball. |
| F11 | VREF_1V2 | S | 1.2 V Reference. This ball cannot be used to source current externally. Connect VREF_1V2 to AGNDx via a 470 nF capacitor. |
| G1 | P2.7/IRQ8/PLAO[21] | I/O | Digital Input/Output Port 2.7 (P2.7).<br>External Interrupt 8 (IRQ8).<br>Output of PLA Element 21 (PLAO[21]). |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| G2 | P3.1/PRTADDR1/PLAI[13] | I/O | Digital Input/Output Port 3.1 (P3.1).<br>MDIO Port Address Bit 1 (PRTADDR1). See the Digital Inputs parameter in Table 1 for details.<br>Input to PLA Element 13 (PLAI[13]). |
| G3 | P3.0/PRTADDR0/PLAI[12] | I/O | Digital Input/Output Port 3.0 (P3.0).<br>MDIO Port Address Bit 0 (PRTADDR0). See the Digital Inputs parameter in Table 1 for details.<br>Input to PLA Element 12 (PLAI[12]). |
| G9 | AIN15/P4.7 | AI/I/O | Analog Input 15 (AIN15).<br>Digital Input/Output Port 4.7 (P4.7). |
| G10 | AIN13/P4.5 | AI/I/O | Analog Input 13 (AIN13).<br>Digital Input/Output Port 4.5 (P4.5). |
| G11 | AVDD4 | S | ADC Supply (3.3 V). |
| H1 | P3.5/MCK/PLAO[27] | I/O | Digital Input/Output Port 3.5 (P3.5).<br>MDIO Clock (MCK). See the Digital Inputs parameter in Table 1 for more details.<br>Output of PLA Element 27 (PLAO[27]). |
| H2 | XTALO | O | Output from the Crystal Oscillator Inverter. When not using an external crystal, leave XTALO unconnected. |
| H3 | MDIO | I/O | MDIO Data. |
| H9 | AIN14/P4.6 | AI/I/O | Analog Input 14 (AIN14).<br>Digital Input/Output Port 4.6 (P4.6). |
| H10 | AIN12/P4.4 | AI/I/O | Analog Input 12 (AIN12).<br>Digital Input/Output Port 4.4 (P4.4). |
| H11 | AGND4 | S | Ground for AVDD4, AVDD_REG0, and AVDD_REG1. |
| J1 | IOVDD3 | S | 3.3 V GPIO Supply. |
| J2 | XTALI | I | Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits. When not using an external crystal, connect XTALI to DGND. |
| J3 | VDAC7/P5.2 | AO/I/O | Voltage DAC7 Output (VDAC7).<br>Digital Input/Output Port 5.2 (P5.2). |
| J4 | VDAC4 | AO | Voltage DAC4 Output (VDAC4). |
| J5 | AGND1 | S | Analog Ground for VDD1. |
| J6 | AIN0 | AI | Analog Input 0. |
| J7 | AIN1 | AI | Analog Input 1. |
| J8 | AIN2 | AI | Analog Input 2. |
| J9 | AIN7 | AI | Analog Input 7. |
| J10 | AIN10 | AI | Analog Input 10. |
| J11 | AIN11/BUF_VREF2V5 | AI/AO | Analog Input 11 (AIN11).<br>Buffered 2.5 V Bias (BUF_VREF2V5). The maximum load is 1.2 mA. Connect BUF_VREF2V5 to AGNDx via a 100 nF capacitor. |
| K1 | IOGND3 | S | Ground for IOVDD3. |
| K2 | DVDD_2V5 | AO | 2.5 V Digital Supply. A 470 nF capacitor to IOGND3 must be connected to this ball to stabilize the internal 2.5 V regulator that supplies the analog digital control. |
| K3 | VDAC6/P5.1 | AO/I/O | Voltage DAC6 Output (VDAC6).<br>Digital Input/Output Port 5.1 (P5.1). |
| K4 | VDAC3/P5.0 | AO/I/O | Voltage DAC3 Output (VDAC3).<br>Digital Input/Output Port 5.0 (P5.0). |
| K5 | VDAC1 | AO | Voltage DAC1 Output. |
| K6 | VDD1 | S | 3.3 V Supply for Digital Die. |
| K7 | AGND2 | S | ESD Ground for Pad Ring. |
| K8 | AIN3 | AI | Analog Input 3. |
| K9 | AIN6 | AI | Analog Input 6. AIN6 is also the positive input for the comparator. |
| K10 | AIN9/P4.3 | AI/I/O | Analog Input 9 (AIN9).<br>Digital Input/Output Port 4.3 (P4.3). |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| K11 | ADC_REFP | AO/A | Decoupling Capacitor Connection for ADC Reference Buffer. Connect this ball to a 4.7 µF capacitor to the ADC_REFN ball. ADC_REFP can be overdriven by an external reference. |
| L1 | DGND1 | S | Digital Ground 1 for DVDD_1V8. |
| L2 | DVDD_1V8 | AO | 1.8 V Digital Supply. A 470 nF capacitor to DGND1 must be connected to this ball to stabilize the internal 1.8 V regulator that supplies flash memory and the ARM Cortex-M3 processor. |
| L3 | VDAC5 | AO | Voltage DAC5 Output (VDAC5). |
| L4 | VDAC2/P3.7/PLAO[29] | AO/I/O | Voltage DAC2 Output (VDAC2).<br>Digital Input/Output Port 3.7 (P3.7).<br>Output of PLA Element 29 (PLAO[29]). |
| L5 | VDAC0/P5.3 | AO/I/O | Voltage DAC0 Output (VDAC0).<br>Digital Input/Output Port 5.3 (P5.3). |
| L6 | AVDD3 | S | VDAC Supply (3.3 V). |
| L7 | AGND3 | S | Ground for AVDD3. |
| L8 | AIN4 | AI | Analog Input 4. |
| L9 | AIN5 | AI | Analog Input 5. AIN5 can be the negative input for the comparator. |
| L10 | AIN8/P4.2 | AI/I/O | Analog Input 8 (AIN8).<br>Digital Input/Output Port 4.2 (P4.2). |
| L11 | ADC_REFN | AO/A | Decoupling Capacitor Connection for ADC Reference Buffer. Connect this ball to AGND4. |

[1] RES and RES1 are reserved, S is supply, AI is analog input, I is digital input, I/O is input/output, AO is analog output, and O is digital output.

# TYPICAL PERFORMANCE CHARACTERISTICS

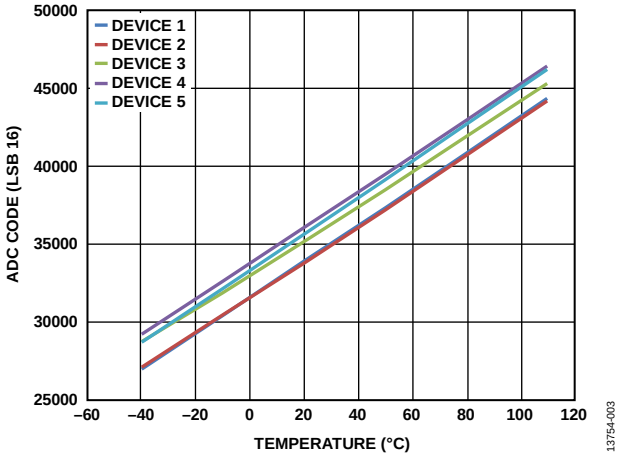


*Figure 9. Temperature Measurement vs. Internal Temperature ($V_{DD}$ = 3.3 V, 50 kSPS)*

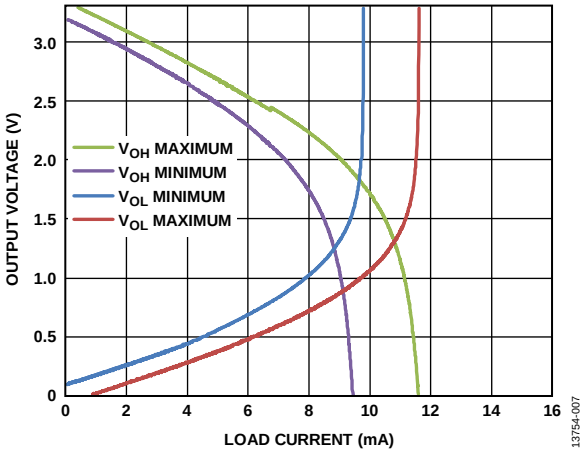


*Figure 11. Output Voltage vs. Load Current*

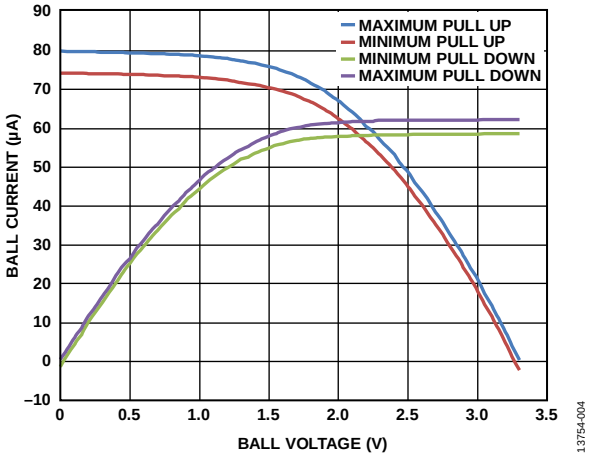


*Figure 10. Pull-Up/Pull-Down Ball Current vs. Ball Voltage ($V_{DD}$ = 3.3 V, $T_A$ = 25°C)*

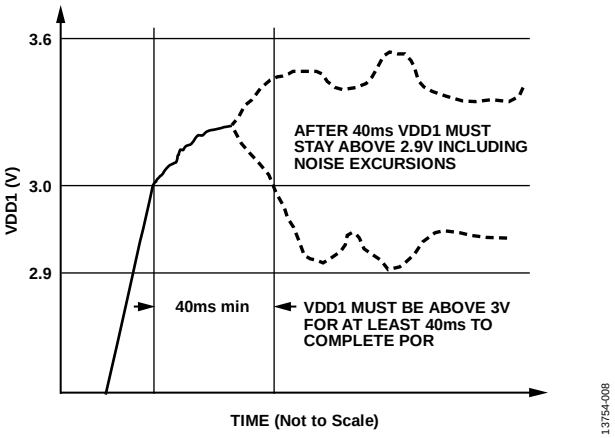


*Figure 12. VDD1 Power-On Requirements*

# APPLICATIONS INFORMATION

## RECOMMENDED CIRCUIT AND COMPONENT VALUES

Figure 13 shows a typical connection diagram for the ADuCM322.

Supplies and regulators must be adequately decoupled with capacitors connected between the AVDDx, DVDD_x, AVDD_REGx, IOVDDx, and VDD1 balls and their associated GND balls (AGNDx, IOGNDx, and DGNDx). Table 10 indicates which ground balls are paired with which supply balls.

There are four digital supply balls: IOVDD1, IOVDD2, IOVDD3, and VDD1. Decouple these balls with a 100 nF capacitor placed as near as possible to each of the four balls and their associated ground balls (IOGNDx and AGND1, respectively). In addition, place a 10 µF capacitor conveniently near to these balls.

Similarly, the analog supply balls, AVDD3 and AVDD4, each require a 100 nF capacitor placed as near as possible to each ball and its associated AGNDx ball, and place a 10 µF capacitor conveniently near to these balls.

The ADC reference requires a 4.7 µF capacitor placed between ADC_REFP and ADC_REFN and located as near as possible to each ball. ADC_REFN must be connected directly to AGND4.

The ADuCM322 contains four internal regulators. These regulators require external decoupling capacitors. The DVDD_1V8 and DVDD_2V5 balls each require a 470 nF capacitor to DGND1 and IOGND3, respectively. AVDD_REG0 and AVDD_REG1 each require a decoupling capacitor to AGND4. The AVDD_REG1 output ball must be connected to Ball A3, Ball A4, Ball A8, and Ball A9.

Connect the IREF ball to DGND via a standard 3.3 kΩ resistor.

Take care in the layout to ensure that currents flowing from the ground end of each decoupling capacitor to its associated ground ball share as little track as possible with other ground currents on the printed circuit board.

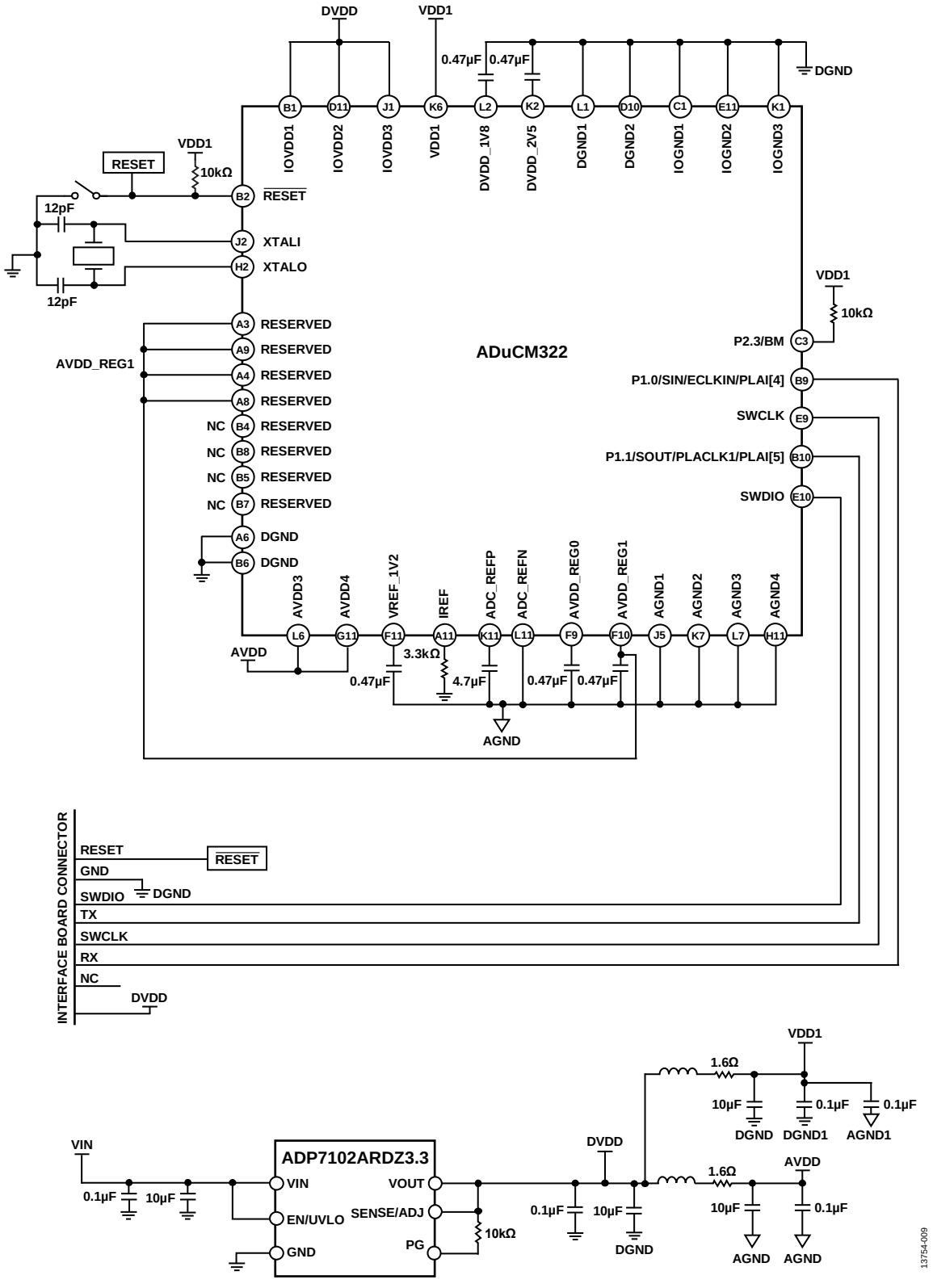


*Figure 13. Recommended Circuit and Component Values*

# OUTLINE DIMENSIONS

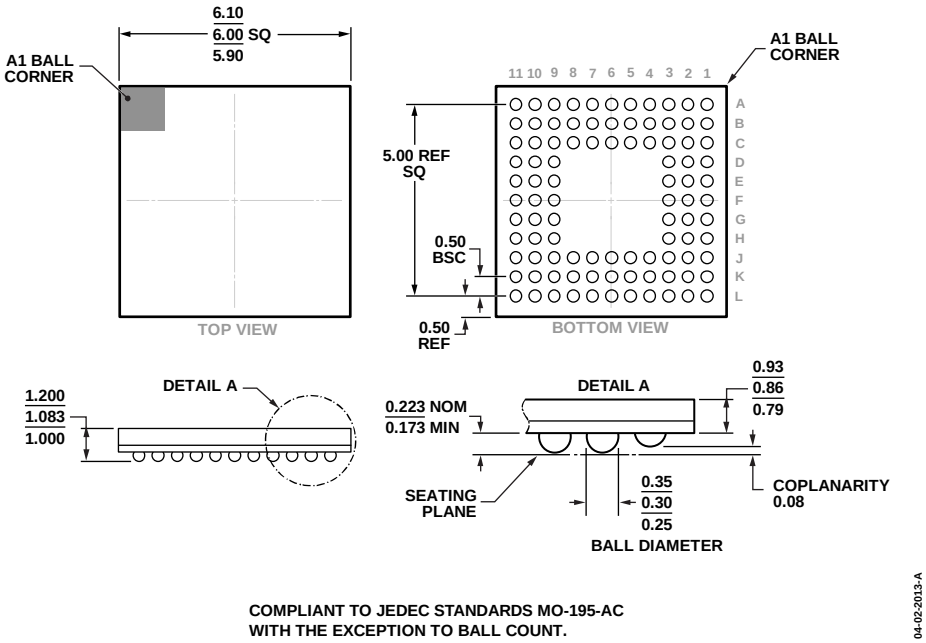


*Figure 14. 96-Ball Chip Scale Package Ball Grid Array [CSP_BGA]*
*(BC-96-2)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option | Downloader | Ordering Quantity |
|---|---|---|---|---|---|
| ADuCM322BBCZ | −40°C to +105°C | 96-Ball CSP_BGA | BC-96-2 | MDIO | 429 |
| ADuCM322BBCZ-RL | −40°C to +105°C | 96-Ball CSP_BGA | BC-96-2 | MDIO | 2,500 |
| EV-ADuCM322QSPZ | | Evaluation Board with QuickStart Development System | | MDIO | 1 |

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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