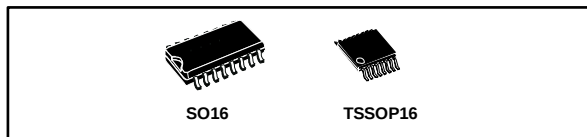


8-bit addressable latch

Datasheet - production data



Features

- High speed: $t_{PD} = 20$ ns (typ.) at $V_{CC} = 6$ V
- Low power dissipation:
 $I_{CC} = 4$ μ A (max.) at $T_A = 25$ °C
- High noise immunity:
 $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (min.)
- Symmetrical output impedance:
 $|I_{OH}| = I_{OL} = 4$ mA (min)
- Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- Wide operating voltage range:
 V_{CC} (OPR) = 2 V to 6 V
- Pin and function compatible with 74 series 259
- ESD performance
 - CDM: 1 kV
 - HBM: 1.5 kV
 - MM: 200 V

Description

The M74HC259 is a high-speed CMOS 8-bit addressable latch manufactured with silicon gate C²MOS technology.

The M74HC259 has single data input (D) 8 latch outputs (Q0-Q7), 3 address inputs (A, B, and C), common enable input (E), and a common

$\overline{CLEAR}$ input. To operate this device as an addressable latch, data is held on the D input, and the address of the latch into which the data is to be entered is held on the A, B, and C inputs.

When $\overline{ENABLE}$ is taken low, the data flows through to the address outputs. The data is stored on the positive-going edge of the $\overline{ENABLE}$ pulse. All unaddressed latches will

remain unaffected. With $\overline{ENABLE}$ in the high state, the device is deselected and all latches remain in their previous state, unaffected by changes on the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the $\overline{ENABLE}$ should be held high (inactive) while the address lines are changing. If $\overline{ENABLE}$ is held high and $\overline{CLEAR}$ is taken low, all eight latches are cleared to the low state. If $\overline{ENABLE}$ is low, all latches except the addressed latch will be cleared. The addressed latch will instead follow the D input, effectively implementing a 3-to-8 line decoder.

All inputs are equipped with protection circuits to guard against static discharge and transient excess voltage.

Table 1: Device summary

Order code	Temperature range	Package	Packaging	Marking
M74HC259YRM13TR ⁽¹⁾	-40 °C to +125 °C	SO16 (automotive grade) ¹	Tape and reel	74HC259Y
M74HC259RM13TR	-55 °C to +125 °C	SO16	Tape and reel	74HC259
M74HC259TTR	-55 °C to +125 °C	TSSOP16	Tape and reel	HC259
M74HC259YTTR ¹	-40 °C to +125 °C	TSSOP16 (automotive grade) ¹	Tape and reel	HC259Y

Notes:

⁽¹⁾Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.

Contents

1	Pin information	5
2	Functional description	6
3	Electrical characteristics	8
4	Package information	15
	4.1 SO16 package information.....	15
	4.2 TSSOP16 package information.....	17
5	Revision history	18

List of tables

Table 1: Device summary	1
Table 2: Pin description	5
Table 3: Truth table	6
Table 4: Absolute maximum ratings	8
Table 5: Recommended operating conditions	8
Table 6: DC specifications	9
Table 7: AC electrical characteristics ($C_L = 50$ pF, input $t_r = t_f = 6$ ns)	10
Table 8: Capacitive characteristics	11
Table 9: Plastic SO16 package mechanical data	16
Table 10: TSSOP16 package mechanical data	17
Table 11: Document revision history	18

List of figures

Figure 1: Pin connections and IEC logic symbols	5
Figure 2: Input and output equivalent circuit.....	6
Figure 3: Logic diagram	7
Figure 4: Test circuit	11
Figure 5: Waveform 1: propagation delay time ($f = 1$ MHz; 50% duty cycle)	12
Figure 6: Waveform 2: propagation delay time ($f = 1$ MHz; 50% duty cycle)	12
Figure 7: Waveform 3: minimum pulse width (G), setup and hold time (D to G) ($f = 1$ MHz; 50% duty cycle).....	13
Figure 8: Waveform 4: minimum pulse width (CLR) ($f = 1$ MHz; 50% duty cycle)	13
Figure 9: Waveform 5: setup and hold time ($f = 1$ MHz; 50 duty cycle).....	14
Figure 10: Waveform 6: input waveforms ($f = 1$ MHz; 50% duty cycle).....	14
Figure 11: Plastic SO16 package mechanical outline	15
Figure 12: TSSOP16 package mechanical outline	17

1 Pin information

Figure 1: Pin connections and IEC logic symbols

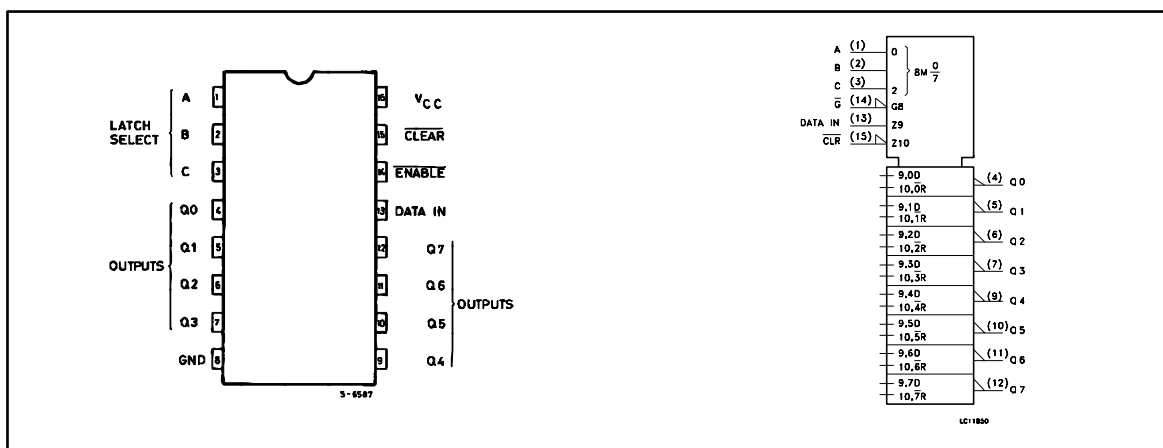


Table 2: Pin description

Pin number	Symbol	Name and function
1, 2, 3	A, B, C	Address inputs
4, 5, 6, 7, 9, 10, 11, 12	Q0 to Q7	Latch outputs
13	D	Data input
14	$\overline{\text{ENABLE}}$	Latch enable input (active low)
15	$\overline{\text{CLEAR}}$	Conditional reset input (low)
8	GND	Ground (0 V)
16	V _{CC}	Positive supply voltage

2 Functional description

Table 3: Truth table

Inputs		Outputs of addressed latch	Other output	Function
<u>CLEAR</u>	<u>ENABLE</u>			
H	L	D	Qi0	Addressable latch
H	H	Qi0	Qi0	Memory
L	L	D	L	8-line demultiplexer
L	H	L	L	Clear all bits to "L"

D: the level at the data input
Qi0: the level before the indicated steady state input conditions where established (i = 0, 1,, 7)

Inputs selected			Latch addressed
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

Figure 2: Input and output equivalent circuit

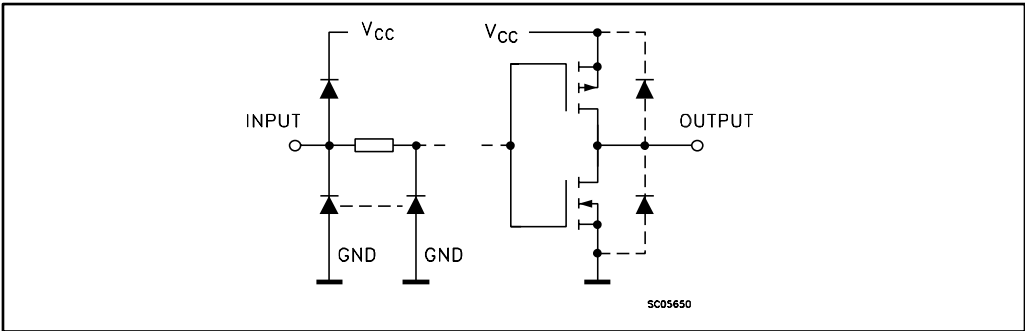
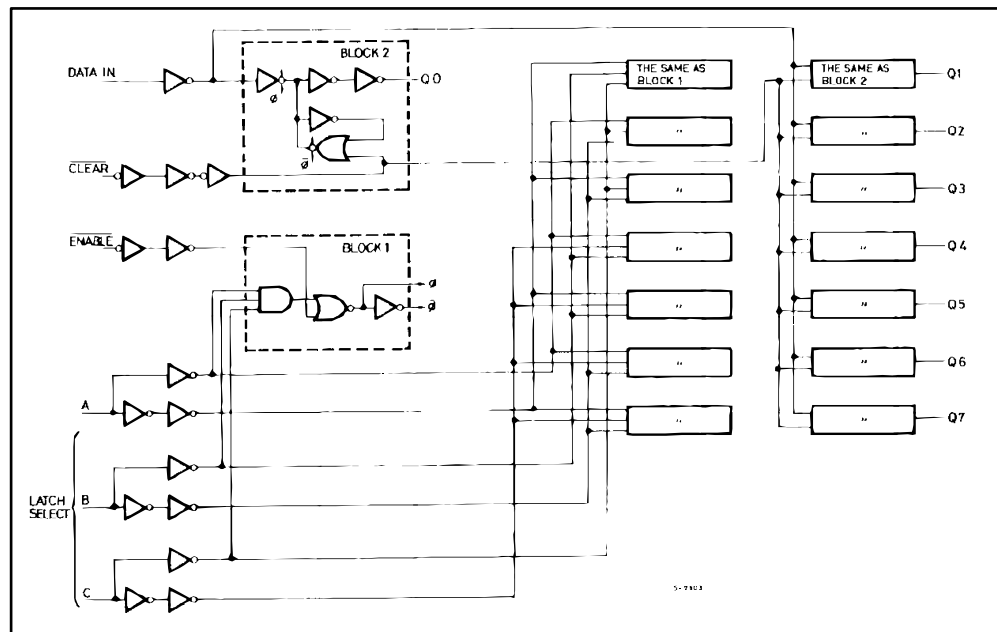


Figure 3: Logic diagram



This logic diagram has not been used to estimate propagation delays.

3 Electrical characteristics

Stressing the device above the ratings listed in the "Absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the operating sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to +7	V
V_I	DC input voltage	-0.5 to V_{CC} to +0.5	V
V_O	DC output voltage	-0.5 to V_{CC} to +0.5	V
I_{IK}	DC input diode current	± 20	mA
I_{OK}	DC output diode current	± 20	mA
I_O	DC output current	± 25	mA
I_{CC} or I_{GND}	DC VCC or ground current	± 50	mA
P_D	Power dissipation	500 ⁽¹⁾	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec.)	300	°C

Notes:

⁽¹⁾500 mW at 65 °C; derate to 300 mW by 10 mW/°C from 65 °C to 85 °C

Table 5: Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		2 to 6	V
V_I	Input voltage		0 to V_{CC}	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-55 to 125	°C
t_r, t_f	Input rise and fall time	$V_{CC} = 2.0 \text{ V}$	0 to 1000	ns
		$V_{CC} = 4.5 \text{ V}$	0 to 500	ns
		$V_{CC} = 6.0 \text{ V}$	0 to 400	ns

Table 6: DC specifications

Symbol	Parameter	Test condition		Value							Unit
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V _{IH}	High-level input voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V _{IL}	Low-level input voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V _{OH}	High-level output voltage	2.0	I _O = -20 μA	1.9	2.0		1.9		1.9		V
		4.5	I _O = -20 μA	4.4	4.5		4.4		4.4		
		6.0	I _O = -20 μA	5.9	6.0		5.9		5.9		
		4.5	I _O = -4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I _O = -5.2 mA	5.68	5.8		5.63		5.60		
V _{OL}	Low-level output voltage	2.0	I _O = 20 μA		0.0	0.1		0.1		0.1	V
		4.5	I _O = 20 μA		0.0	0.1		0.1		0.1	
		6.0	I _O = 20 μA		0.0	0.1		0.1		0.1	
		4.5	I _O = 4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I _O = 5.2 mA		0.18	0.26		0.33		0.40	
I _I	Input leakage current	6.0	V _I = V _{CC} or GND			±0.1		±1		±1	μA
I _{CC}	Quiescent supply current	6.0	V _I = V _{CC} or GND			4		40		80	μA

Table 7: AC electrical characteristics ($C_L = 50$ pF, input $t_r = t_f = 6$ ns)

Symbol	Parameter	Test condition	Value							Unit
			T _A = 25°C			-40 to 85°C		-55 to 125°C		
		V _{CC} (V)	Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _{TLH} t _{THL}	Output transition time	2.0		30	75		95		110	ns
		4.5		8	15		19		22	
		6.0		7	13		16		19	
t _{PLH} t _{PHL}	Propagation delay time (DATA – Q)	2.0		56	140		175		210	ns
		4.5		18	28		35		42	
		6.0		15	24		30		36	
t _{PLH} t _{PHL}	Propagation delay time (A, B, C – Q)	2.0		76	190		240		285	ns
		4.5		24	38		48		57	
		6.0		20	32		41		48	
t _{PLH} t _{PHL}	Propagation delay time (G – Q)	2.0		57	150		190		225	ns
		4.5		19	30		38		45	
		6.0		16	26		32		38	
t _{PLH} t _{PHL}	Propagation delay time ($\overline{\text{CLEAR}}$ – Q)	2.0		45	115		145		175	ns
		4.5		15	23		29		35	
		6.0		13	20		25		30	
t _{W(L)}	Minimum pulse width ($\overline{\text{ENABLE}}$)	2.0		28	75		90		115	ns
		4.5		7	15		19		23	
		6.0		6	13		16		20	
t _{W(L)}	Minimum pulse width ($\overline{\text{CLEAR}}$)	2.0		24	75		90		115	ns
		4.5		6	15		19		23	
		6.0		5	13		16		20	
t _S	Minimum setup time (DATA)	2.0		12	50		60		75	ns
		4.5		3	10		12		15	
		6.0		3	9		11		13	
t _S	Minimum setup time (A, B, C)	2.0			25		30		40	ns
		4.5			5		6		8	
		6.0			5		5		7	
t _H	Minimum hold time (DATA)	2.0			5		5		5	ns
		4.5			5		5		5	
		6.0			5		5		5	
t _H	Minimum hold time (A, B, C)	2.0			0		0		0	ns
		4.5			0		0		0	
		6.0			0		0		0	

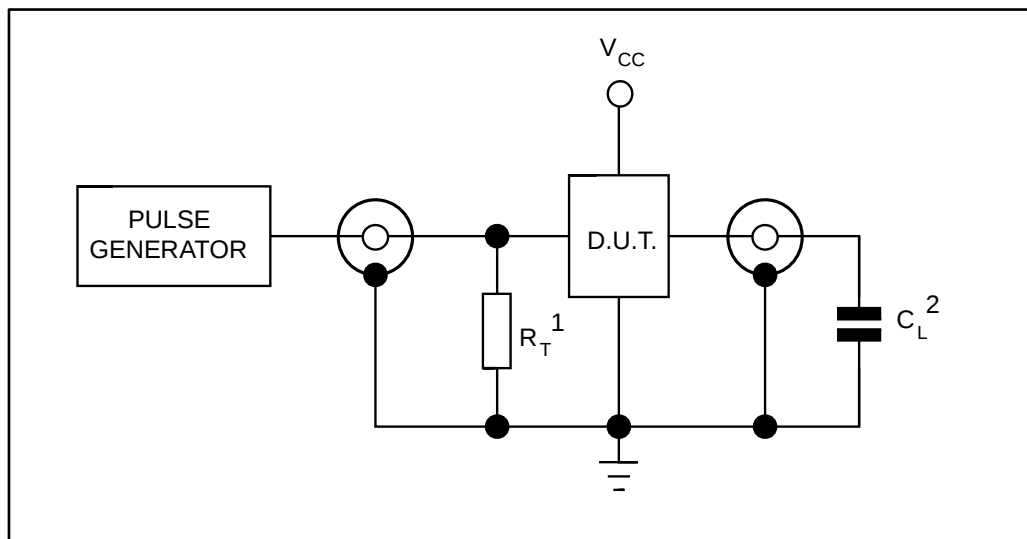
Table 8: Capacitive characteristics

Symbol	Parameter	Test condition	Value							Unit
			T _A = 25°C			-40 to 85°C		-55 to 125°C		
		V _{CC} (V)	Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C _{IN}	Input capacitance	5.0		5	10		10		10	pF
C _{PD}	Power dissipation capacitance ⁽¹⁾	5.0		66						pF

Notes:

⁽¹⁾ C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (refer to the test circuit). The average operating current can be obtained by the following equation: $I_{CC(oper)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

Figure 4: Test circuit



1. $R_T = Z_{OUT}$ of pulse generator (typically 50 ohm)
2. $C_L = 50 \text{ pF}$ or equivalent (includes jig and probe capacitance)

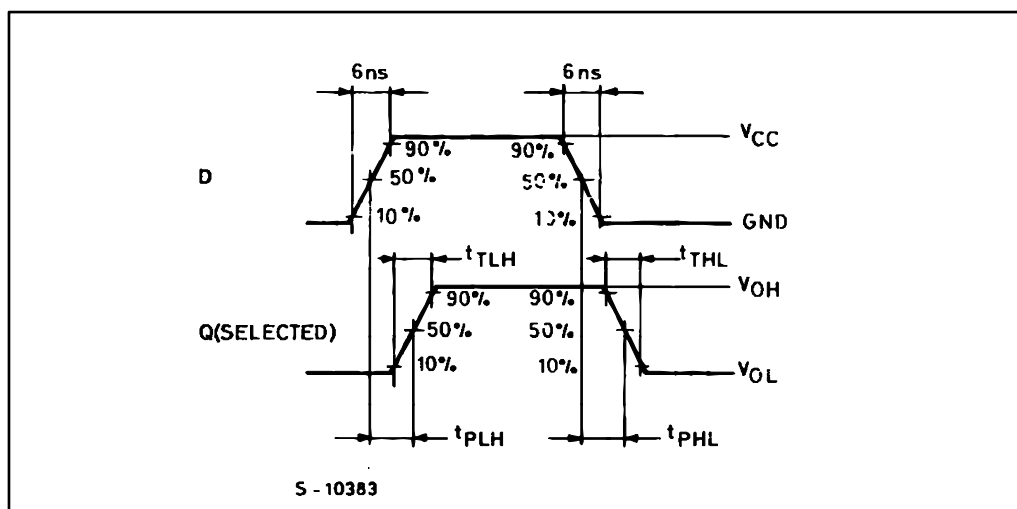
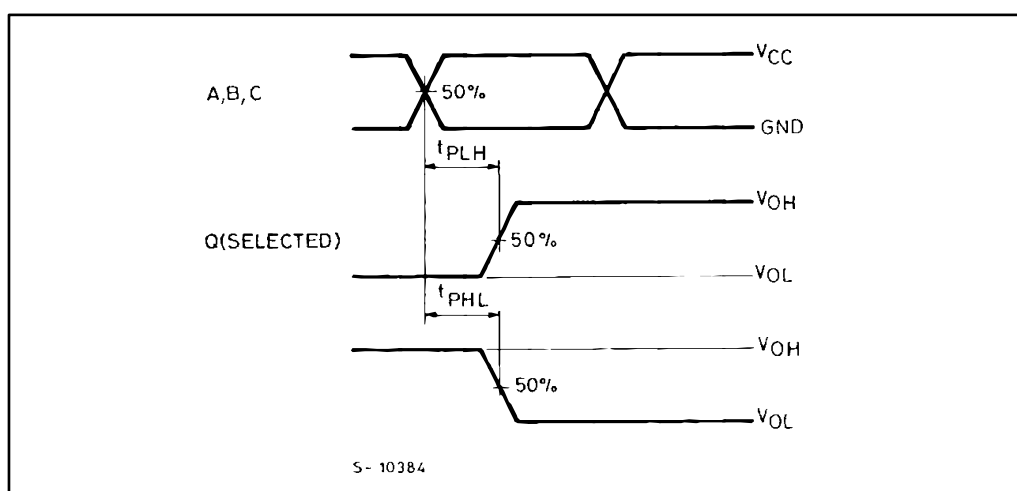
Figure 5: Waveform 1: propagation delay time ($f = 1\text{ MHz}$; 50% duty cycle)Figure 6: Waveform 2: propagation delay time ($f = 1\text{ MHz}$; 50% duty cycle)

Figure 7: Waveform 3: minimum pulse width (G), setup and hold time (D to G) ($f = 1\text{ MHz}$; 50% duty cycle)

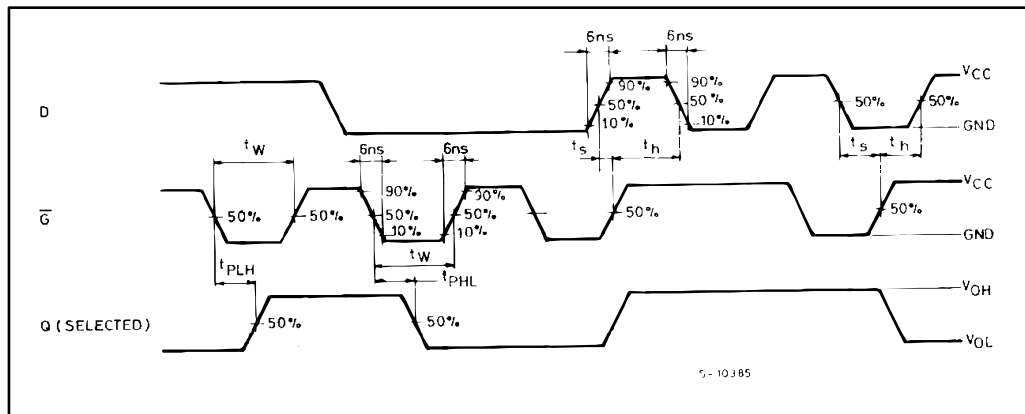


Figure 8: Waveform 4: minimum pulse width (CLR) ($f = 1\text{ MHz}$; 50% duty cycle)

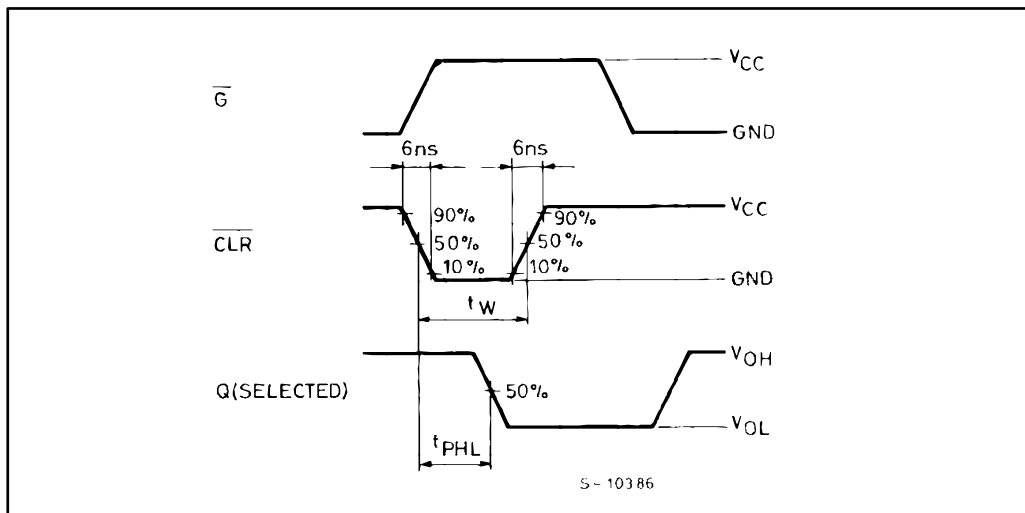
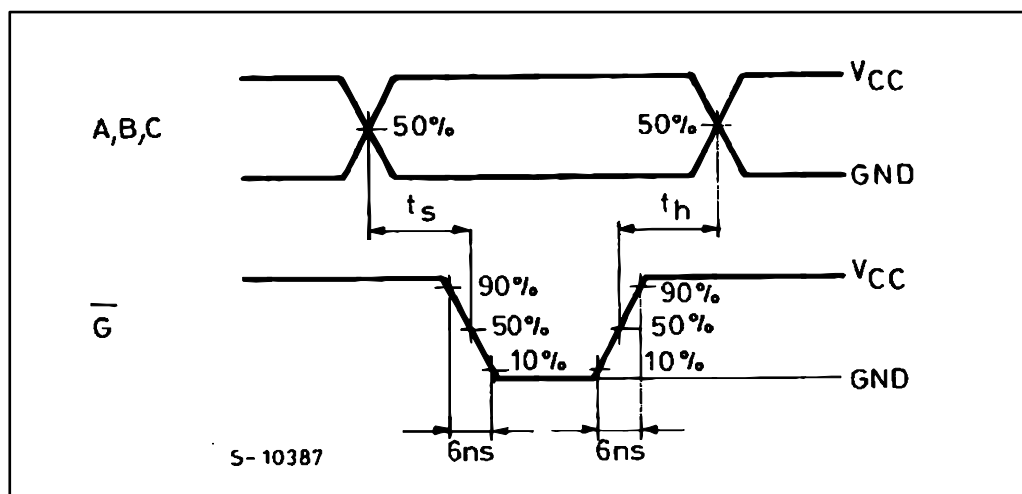
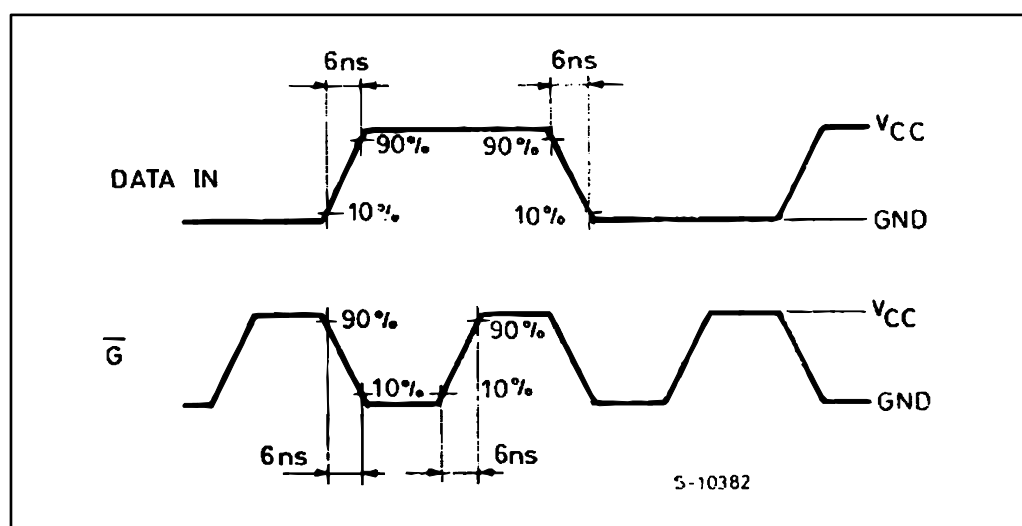


Figure 9: Waveform 5: setup and hold time ($f = 1\text{ MHz}$; 50% duty cycle)Figure 10: Waveform 6: input waveforms ($f = 1\text{ MHz}$; 50% duty cycle)

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 SO16 package information

Figure 11: Plastic SO16 package mechanical outline

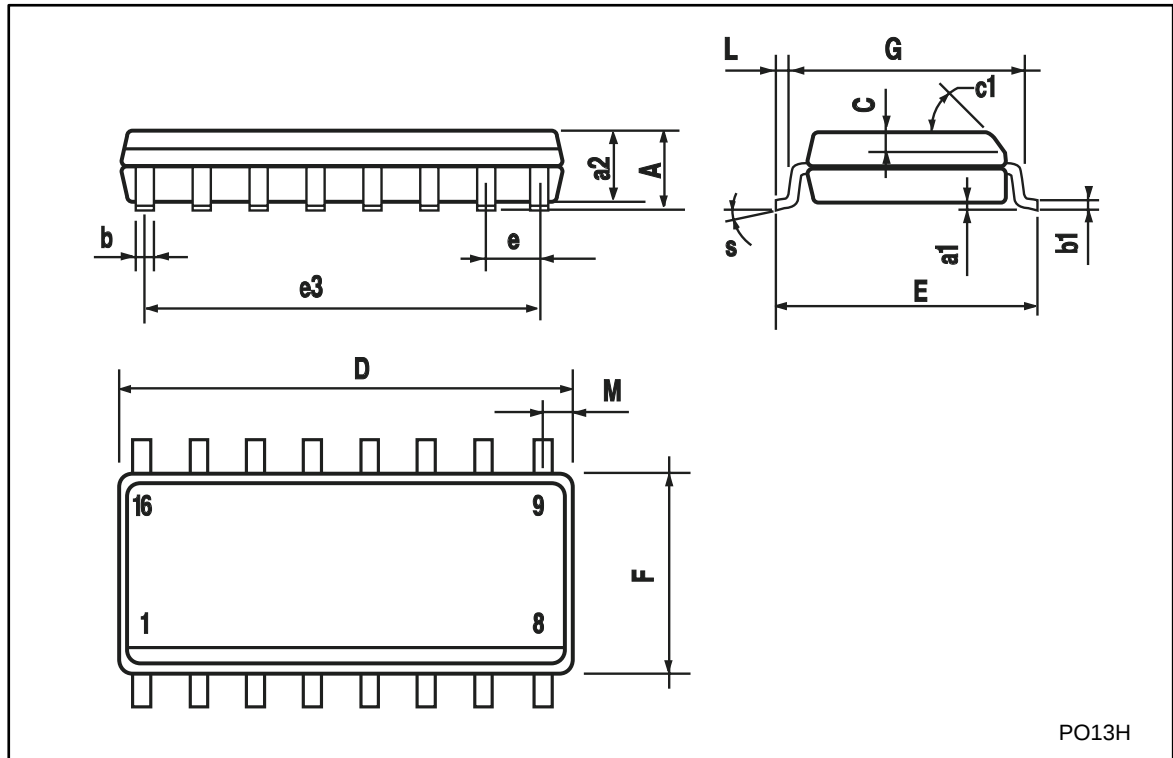


Table 9: Plastic SO16 package mechanical data

Dimensions	mm.			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 ° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8 ° (max.)					

4.3 TSSOP16 package information

Figure 12: TSSOP16 package mechanical outline

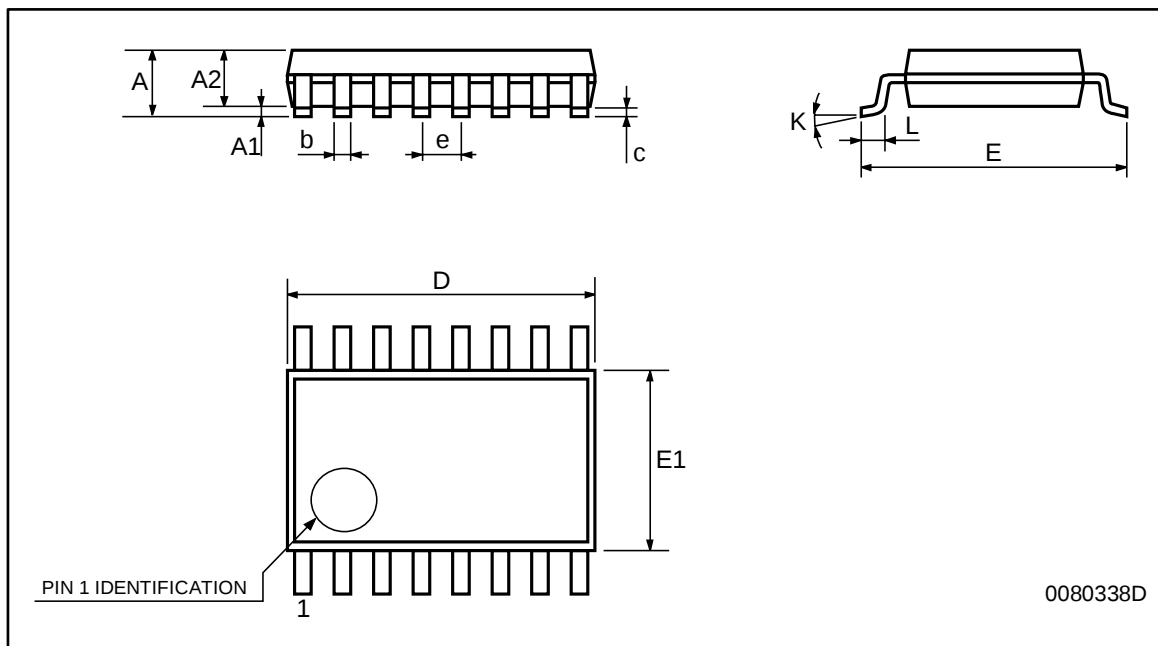


Table 10: TSSOP16 package mechanical data

Dimensions	mm.			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

5 Revision history

Table 11: Document revision history

Date	Version	Change
Jul-2001	1	Initial release
01-Nov-2013	2	Added ESD performance to Section "Features" Added automotive grade order codes, temperature ranges and marking information to Table 1: "Device summary" Removed DIP16 package option Revised document presentation, minor textual updates

Please Read Carefully

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy
- Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United
States of America

www.st.com