RM24C512C-L
512-Kbit 1.65V Minimum Non-volatile Serial EEPROM I²C Bus

Preliminary Datasheet

Features

- Memory array: 512Kbit non-volatile serial EEPROM memory
- Single supply voltage: 1.65V - 3.6V
- 2-wire I²C interface
- Compatible with I²C bus modes:
  -100kHz
  -400kHz
  -1MHz
- Page size: 128 bytes
  -Byte and Page Write from 1 to 128 bytes
- Low Energy Byte Write
  -Byte Write consuming 50 nJ
- Low power consumption
  -0.25 mA active Read current
  -1.0 mA active Write current
  -1.0 µA Standby current
- Fast Write
  -Page Write in 3 ms (128 byte page)
  -Byte Write within 60 µs
- Random and sequential Read modes
- Industry's lowest read cycle latency
- Unlimited read cycles
- Write protect of the whole memory array
- 8-lead SOIC, 8-lead TSSOP, 8-pad UDFN and 6-ball WLCSP packages
- RoHS-compliant and halogen-free packaging
- Data Retention: >40 years at 125°C
- Endurance: 100,000 Write Cycles (for both byte and page write cycles)
  - No degradation across temperature range
- Industrial Operating Temperature: -40°C to 85°C
- No data loss under UV exposure on bare die or WLCSP
- Based on Adesto's proprietary CBRAM® technology

Description

The Mavriq™ RM24C512C-L is a 512Kbit, serial EEPROM device that utilizes Adesto's CBRAM® resistive memory technology. The memory devices use a single low-voltage supply ranging from 1.65V to 3.6V.

The Mavriq I²C device is accessed through a 2-wire I²C compatible interface consisting of a Serial Data (SDA) and Serial Clock (SCL). The maximum clock (SCL) frequency is 1MHz. The devices have both byte write and page write capability. Page

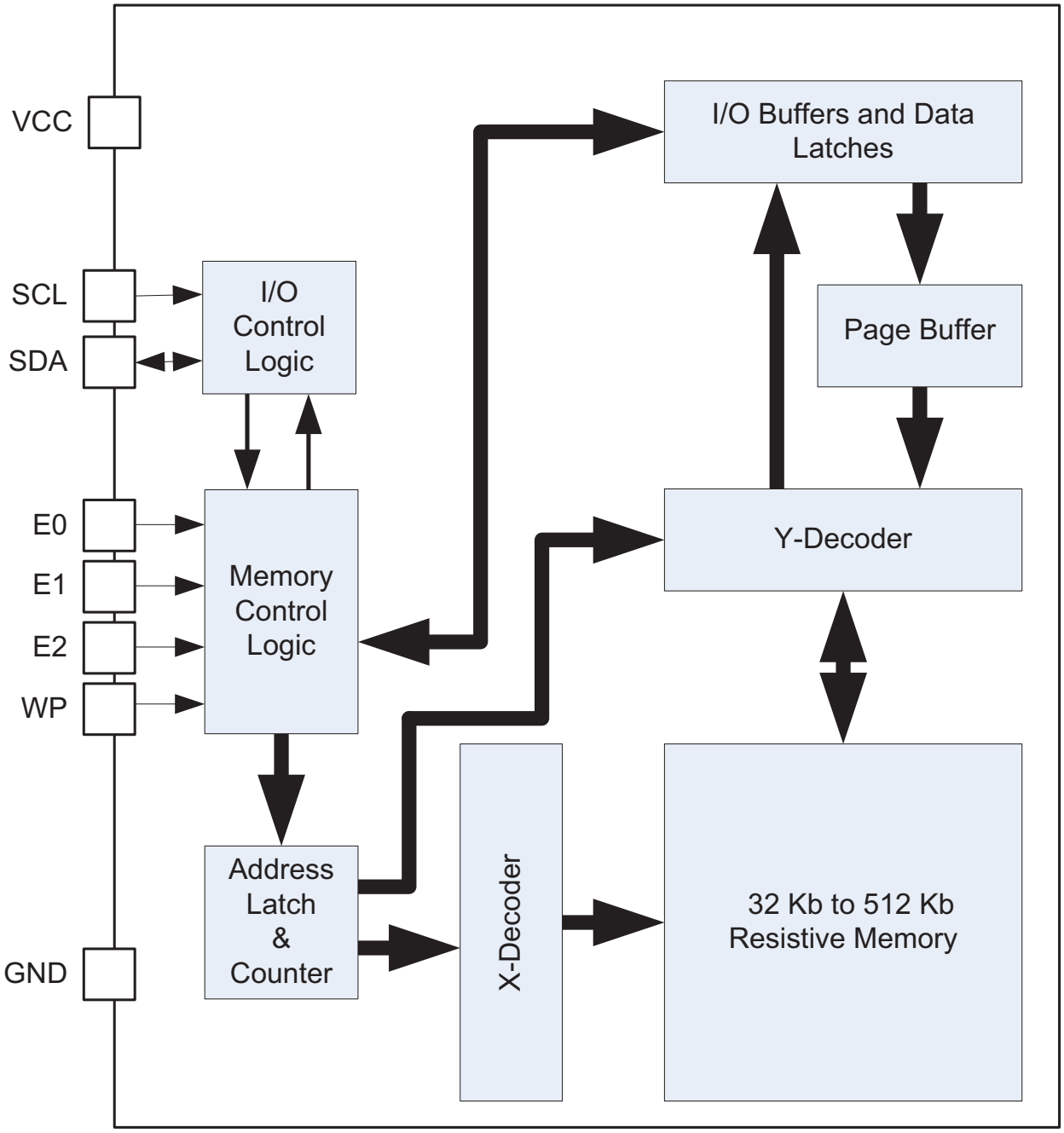
write is 128 bytes. The Byte Write operation of Mavriq memory consumes only 10% of the energy consumed by a Byte Write operation of EEPROM devices of similar size.

Adesto's EEPROM endurance can be as much as 40X higher than industry standard EEPROM devices operating in byte write mode at 85°C. Unlike EEPROMs based on floating gate technology (which require read-modify-write on a whole page for every write operation) CBRAM write endurance is based on the capability to write each byte individually, irrespective of whether the user writes single bytes or an entire page. Additionally, unlike floating gate technology, CBRAM does not experience any degradation of endurance across the full temperature range. By contrast, in order to modify a single byte, most EEPROMs modify and write full pages of 32, 64 or 128 bytes. This provides significantly less endurance for floating gate devices used in byte write mode when compared to page write mode.

The Page Write operation of Mavriq memory is 4-6 times faster than the Page Write operation of similar EEPROM devices. Both random and sequential reads are available. Sequential reads are capable of reading the entire memory in one operation. External address pins permit up to eight devices on the same data bus. The devices are available in standard 8-pin SOIC and TSSOP, UDFN and WLCSP packages.

1. Block Diagram

Figure 1-1. Block Diagram



2. Pin/Signal Descriptions

Table 2-1. Pin/Signal Descriptions

Symbol	Pin #	Name/Function	Description
E0	1	LSB - Least Significant Bit, External Enable	LSB of the three external enable bits (E0, E1 and E2). The levels of the external enable bits are compared with three enable bits in the received control byte to provide device selection. The device is selected if the comparison is true. Up to eight devices may be connected to the same bus by using different E0, E1, E2 combinations.
E1	2	External Enable	The middle of the three external enable bits (E0, E1 and E2). The levels of the enable bits are compared with three enable bits in the received control byte to provide device selection. Also see the E0, E2 pin.
E2	3	MSB - Most Significant Bit, External Enable	MSB of the three external enable bits (E0, E1 and E2). The levels of the enable bits are compared with three enable bits in the received control byte to provide device selection. Also see the E0, E1 pin.
GND	4	Ground	
SDA	5	Serial Data	Bidirectional pin used to transfer addresses and data into and data out of the device. It is an open-drain terminal, and therefore requires a pull-up resistor to VCC. Typical pull-up resistors are: 10KΩ for 100KHz, and 2KΩ for 400KHz and 1MHz. For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.
SCL	6	Serial Clock	This input is used to synchronize the data transfer from and to the device. SCL is an input only, since it is a slave-only device.
WP	7	Write Protect	Connect to either VCC or GND. If pulled low, write operations are enabled. If pulled high, write operations are inhibited, but read operations are not affected.
Vcc	8	Power	Power supply pin

2.1 Pin Out Diagram

Figure 1.

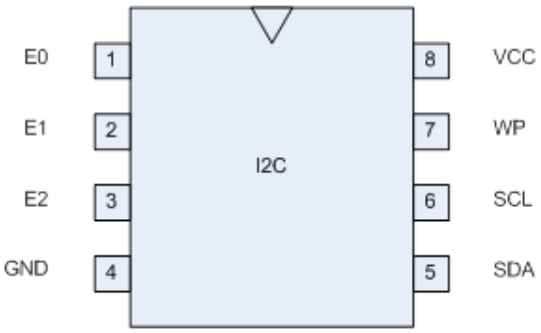


Figure 2. (Bottom-view)

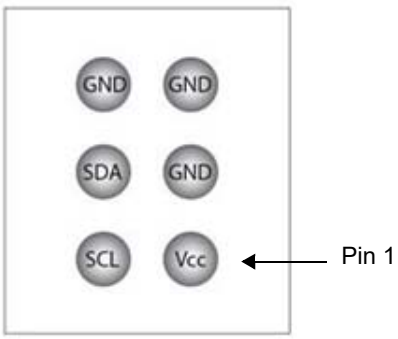


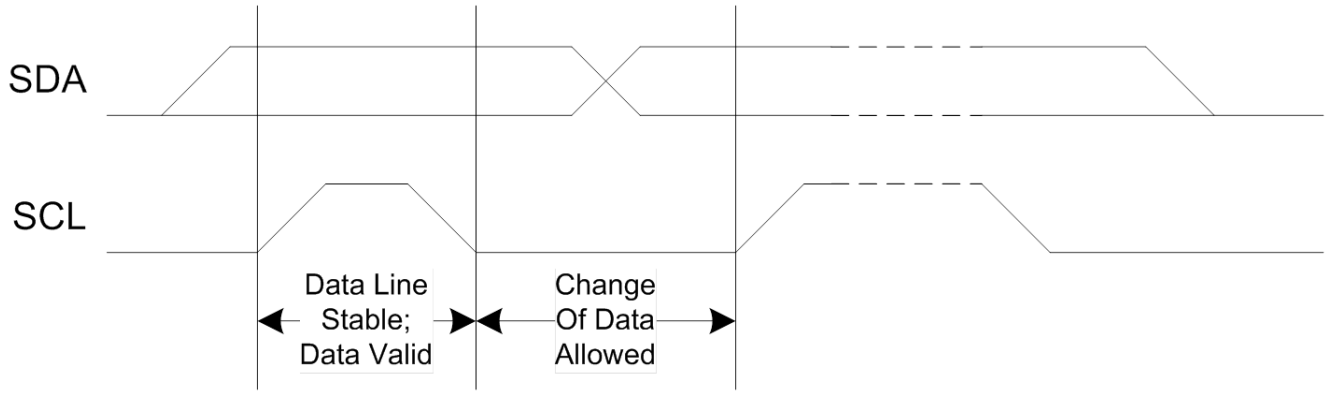
Figure 1. Pin out diagram for SOIC, TSSOP and UDFN packages. **Figure 2.** Pin out diagram for WLCSP package.

3. I²C Bus Protocol

I²C is a 2-wire serial bus architecture with a clock pin (SCL) for synchronization, and a data pin (SDA) for data transfer. On the device the SDA pin is bi-directional. The SCL pin is an input only, because the device is slave-only. The SCL and SDA pins are both externally connected to a positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are high. The output stages of devices connected to the bus must have an open drain or open collector to perform a wired-AND function. Data on the I²C bus can be transferred at rates of up to 1 Mbit/s. The number of interfaces that may be connected to the bus is solely dependent on the bus capacitance limit of 400pF.

The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 1-1).

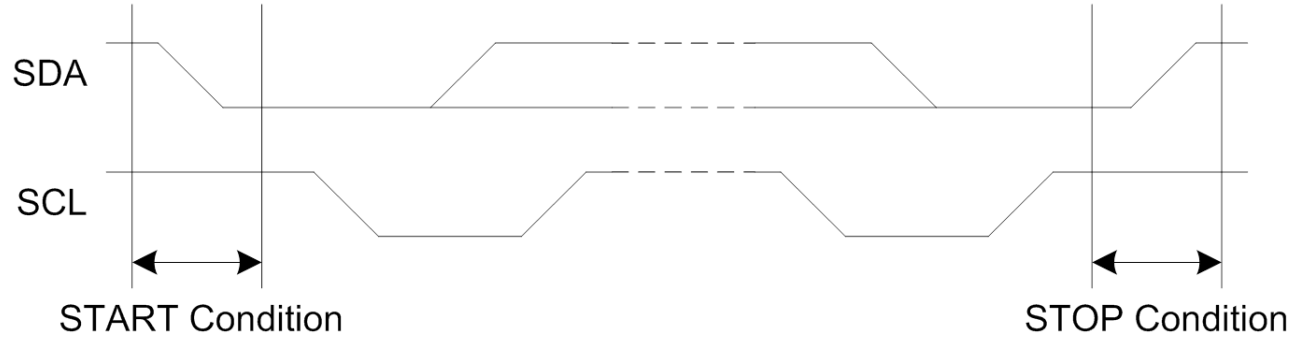
Figure 3-1. Bit Transfer on the I²C bus



A high-to-low transition on the SDA line while SCL is high indicates a START condition. A low-to-high transition on the SDA line while SCL is high defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition (see Figure 3-2).

Figure 3-2. START and STOP conditions

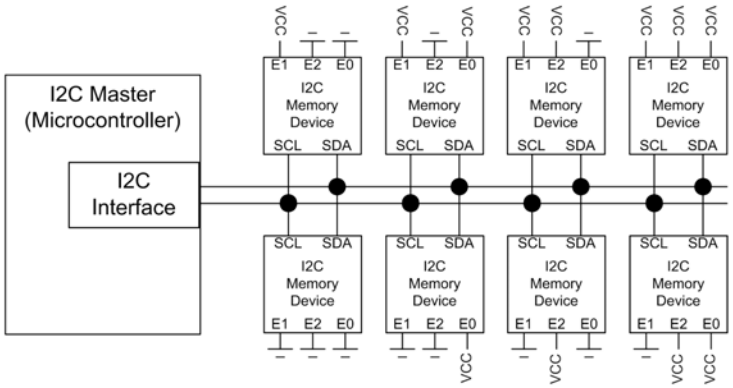


Every byte put on the SDA line must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an acknowledge bit; therefore, the number of clock cycles to transfer one byte is nine. Data is transferred with the most significant bit (MSB) first.

3.1 I²C Master and Slave Configuration

The device has a two-pin industry-standard I2C interface. It is configured as a slave-only device and therefore does not generate a clock. By connecting the E0, E1 and E2 enable pins in the configuration shown in Figure 3-3, up to eight devices can be connected onto an I2C Interface bus controlled by an I2C master device, such as a microcontroller.

Figure 3-3. Connection between I²C Master and Slaves



4. Device Timing

Figure 4-1. Bus Timing Data

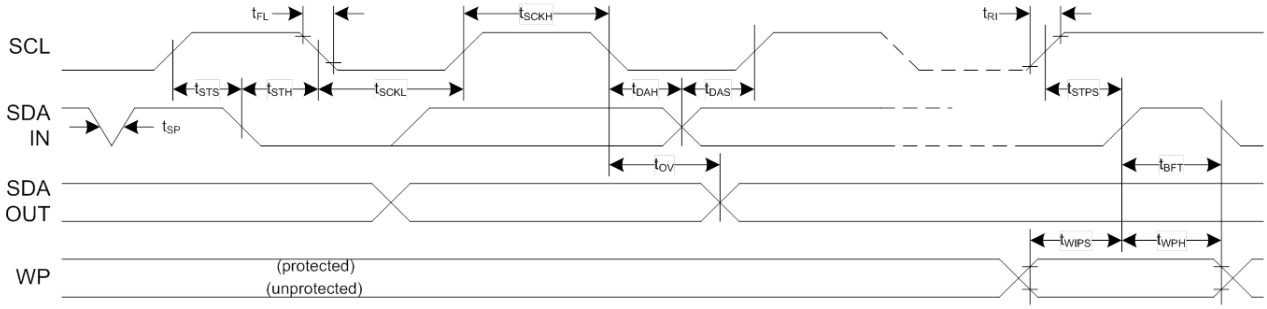
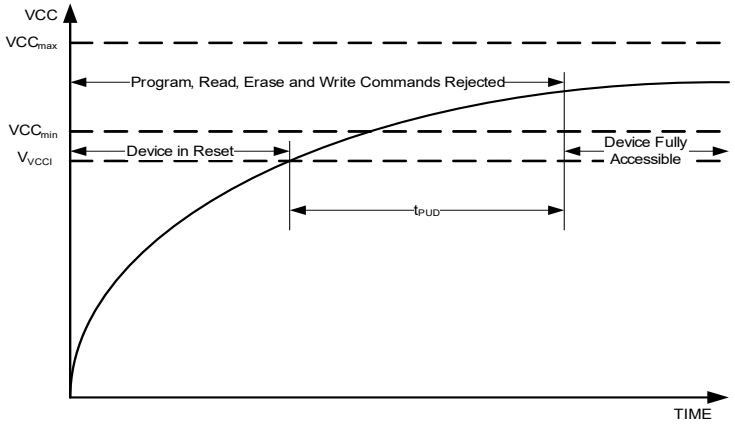


Figure 4-2. Power-up Timing

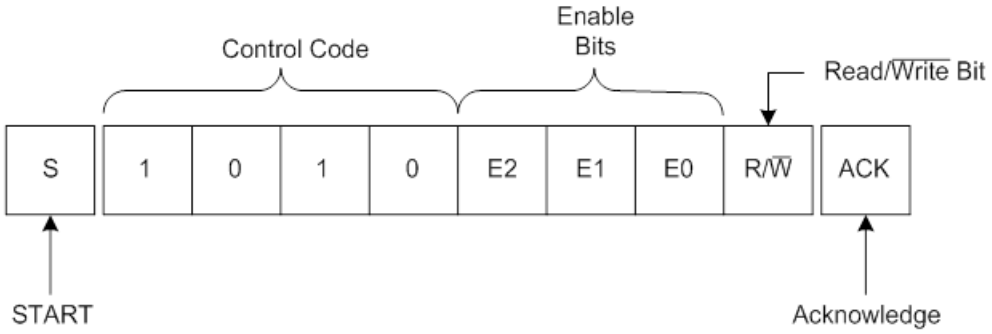


Power up delay t_{PUD} is based on V_{CCi} which is the voltage level at which the internal reset circuit releases and signals the controller to initiate the power-on reset condition for a 75µS maximum period.

5. Device Addressing

The first byte sent from the master device to the EEPROM following the START condition is the control byte (See Figure 5-1). The first four bits of the control byte is the control code. The control code is “1010” both for read and for write operations. The next three bits of the control byte are the enable bits (E2, E1 and E0), which are compared to the levels set on the E0, E1 and E2 pins. The E0, E1 and E2 bits sent in the control byte must correspond to the logic levels set on the corresponding E0, E1 and E2 pins for a device to be selected. In effect, the E0, E1 and E2 bits in the control register act as the three MSB bits of a word address. These three bits allow the use of up to eight devices on the same bus. The last bit of the control byte (R/$\overline{W}$) defines the operation to be performed, read or write: if set to a one, a read operation is selected; if set to a zero, a write operation is selected.

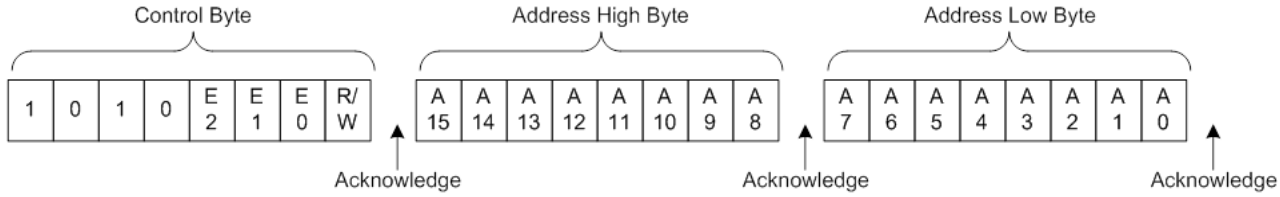
Figure 5-1. Control Byte



Upon receiving a "1010", the chip enable bits, and the R/$\overline{W}$ bit, the device performs an acknowledge by pulling the SDA line low during the 9th clock pulse. As stated above, the device will now be set for either a read or a write operation by the R/$\overline{W}$ bit.

After the device acknowledges the control byte, two additional bytes are sent by the master to the slave. These define the target address of the byte in the device to be written. The bit assignment for the address is shown in Figure 5-2.
It should be noted that not all the address bits are used. For the 512-Kbit device, only address A0 to A15 are used; the rest are don't cares and must be set to "0".

Figure 5-2. Address sequence bit assignment



The device will acknowledge each byte of data that is received by pulling the SDA line low during the 9th clock pulse. If the device does not provide an acknowledge, it has not received the data; consequently the entire sequence, starting with the control byte, must be resent.

6. Byte Write Operation

If the R/$\overline{W}$ bit in the control byte is set to zero, the device will be in write mode. Once the control byte is received, the device will perform an acknowledge; it will then be ready to receive the Address High Byte (see Figure 6-1). After receiving the Address High Byte, the device acknowledges and then is ready to receive the Address Low Byte. After receiving the Address Low Byte, the device will acknowledge and then write the address (expressed by the high and low address bytes) into its address pointer. The device is then ready to receive a byte of data to be written into the

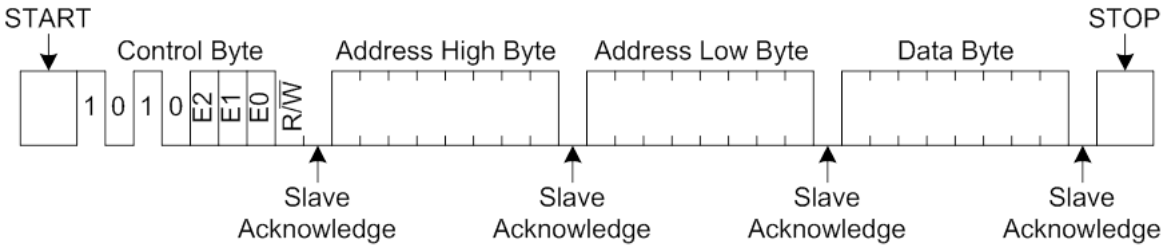
addressed memory location. After the device receives the data, it performs an acknowledge. After the master has received the last acknowledge (after the data byte) the master should send a STOP condition. The STOP condition initiates the internal write cycle in the device. If the master does not send a STOP, the device will not write the data into the addressed memory location.

While the device is in the write cycle it will not generate an acknowledge signal. Meanwhile, the master can poll the device to determine when the write cycle is complete by sending it a control byte and looking for an acknowledge. Once the write cycle has completed, the device will acknowledge a control byte sent to it.

If, in the RM24C512C-L, the byte written is the last byte in a 128-byte page, the address will wrap around to the beginning of the same page. For instance, if the byte is written to address 007Fh, the incremented address will be 0000h. If the byte is written to address 07FFh, the incremented address will be 0780h.

If a write cycle is attempted with the WP (write protect) pin held high, the device will acknowledge the command, address, and data, but no write cycle will occur following the STOP command. The data will not be written, and the device will immediately be available to accept a new command. However, the internal address pointer will be written; so after the data byte is transmitted to the device and the STOP command issued by the master, the internal address pointer will again be incremented by one.

Figure 6-1. Byte Write Cycle



7. Page Write Operation

Table 7-1. Density and Page Size

Product	Density	Page Size (byte)
RM24C512C-L	**512 Kbit**	**128**

During a Page Write cycle, a page with up to 128 bytes of data can be written in one continuous write command. The Page Write starts in the same manner as the Byte Write. In a Page Write, after the acknowledge following the first data byte, the master does not send a STOP, but continues to send additional data bytes. (See Figure 7-1.) At the end of the number of bytes to be written, the master sends a STOP command. Once the STOP command is sent, the device will write all the data bytes into memory, starting at the address location given in the address bytes.

If the master should transmit more than 128 bytes prior to generating the STOP command, the internal 128-byte data buffer in the device will wrap around and the first data bytes transmitted will be overwritten.

The internal address pointer will not increment beyond a page boundary but will instead wrap around to the first byte of the addressed page.

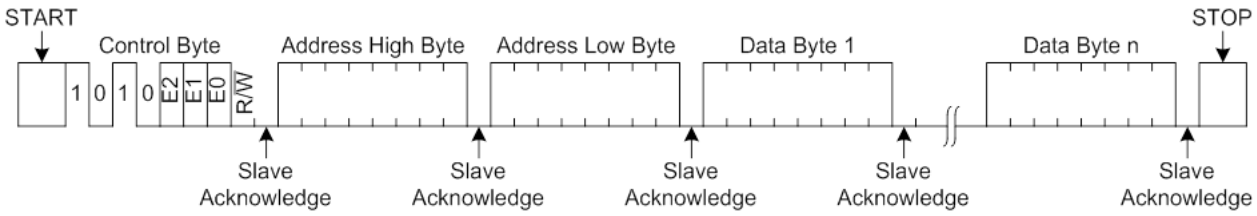
As with the Byte Write cycle, once the STOP command is received the device enters a write cycle. During the write cycle, the device will not generate an acknowledge signal. Meanwhile, the master can poll the device to determine when the write cycle is complete by sending it a control byte and looking for an acknowledge. Once the write cycle has completed, the device will acknowledge a control byte sent to it.

During the Page Write cycle, the first byte in the data byte buffer will be written in the address location indicated by the address bytes transmitted to the device. Each successive data byte will be written in the successive address locations.

If a Page Write cycle is attempted with the WP pin held high, the device will acknowledge the command, address and data bytes, but will not enter a write cycle after the STOP command is issued. No data will be written, and the device will immediately be available to accept a new command. However, the internal address pointer will be written; so after the Page Write data bytes are transmitted to the device and the STOP command issued by the master, the internal address pointer will be incremented by the number of data bytes sent (but only within the page addressed).

Note that the Page Write operation is internally executed by sequentially writing the words in the Page Buffer. Therefore the Page Write time can be estimated as Byte Write time multiplied by the Number of Words to be written.

Figure 7-1. Page Write Cycle



8. Write Protection

The WP pin allows the user to write-protect the entire memory array when the pin is tied to VCC. If the WP pin is tied to GND, write protection is disabled. The WP pin is sampled at the STOP command for every Write command. Toggling the WP pin after the STOP command will have no effect on the execution of the write cycle.

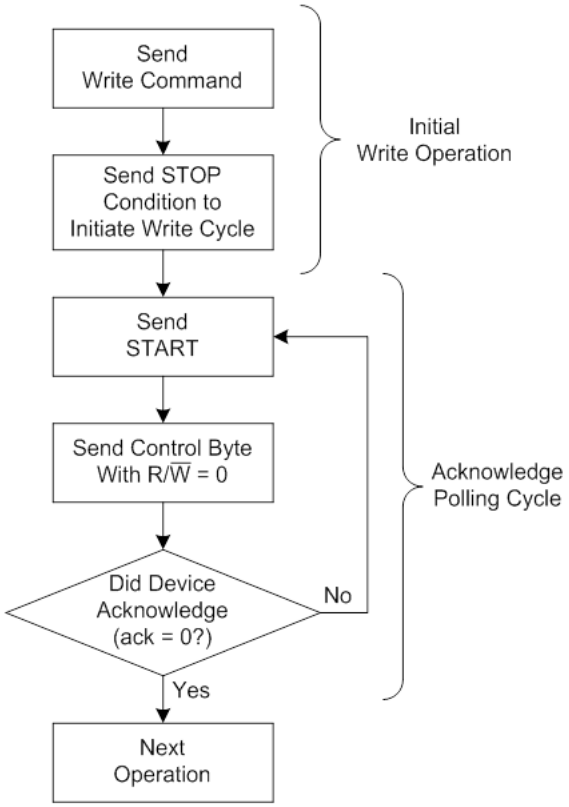
9. Polling

The fact that the device will not acknowledge during a write cycle can be used to determine when the write cycle is complete. By polling the device during the write cycle, bus throughput can be maximized.

Once the STOP command for the write cycle is sent by the master, the device initiates the internally timed write cycle. Acknowledge polling, by the master, can be initiated immediately. Acknowledge polling involves the master sending a START command, followed by the control byte for a write command (R/$\overline{W}$=0). If the device is still busy with the write cycle, no acknowledge is returned. If no acknowledge is returned, the START command and control byte can be re-transmitted. If the write cycle is complete, the device will return an acknowledge. The master can then proceed with the next read or write command. See for a flow diagram.

NOTE: Care must be taken when polling the device. The control byte that was used to initiate the write must match the control byte used for polling.

Figure 9-1. Acknowledge Polling Flow



10. Read Operation

Read operations are initiated in the same way as the write operations, except that the R/$\overline{W}$ bit of the control byte is set to one. There are three types of read operations: Current Address Read, Random Read, and Sequential Read.

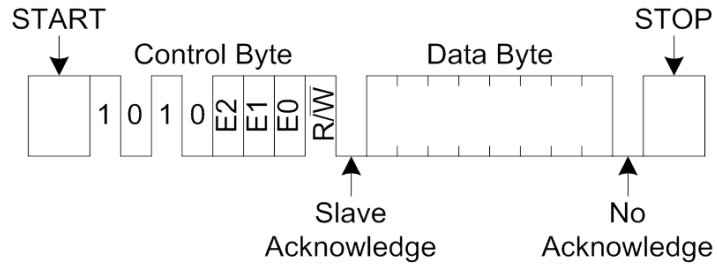
10.1 Current Address Read

The device internal address pointer maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n (any legal address), the next Current Address Read operation would access data from address n+1. After the last memory address, the address counter “rolls-over”, and the device continues to output data from memory address 00h.

If a Current Address Read is performed after a Byte Write or Page Write, care must be taken to understand that during the page/byte write command, the address can wrap around within the same page.

Upon receipt of the control byte with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and transmits the 8-bit data word located at the address of the internal address pointer. The master will not acknowledge the transfer, but does generate a STOP condition and the device discontinues transmission. See Figure 10-1.

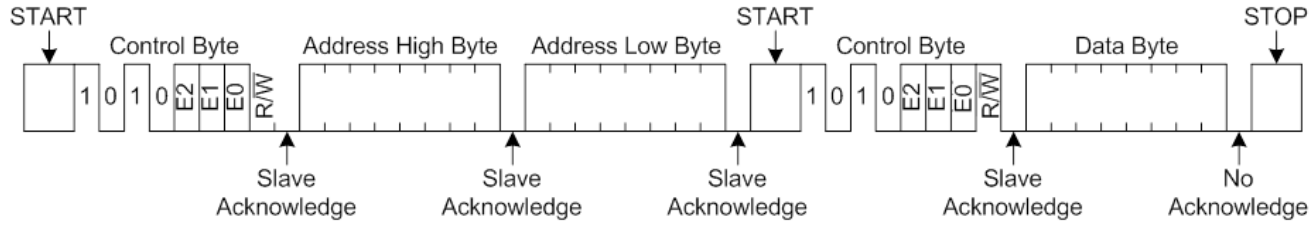
Figure 10-1. Current Address Read



10.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform a Random Read, first the address to be accessed must be set. This is done by sending the address to the device as part of a write operation (R/$\overline{W}$ = 0). After the address is sent and acknowledged by the device, the master generates a START. This terminates the write operation, but the address pointer will be set to the address sent. The master then issues the same control byte as the write operation, but with the R/$\overline{W}$ bit set to 1. The device will acknowledge and transmit the 8-bit data byte located at the address location written. The master will not acknowledge the transfer of the data byte, but will instead generate a STOP condition, which causes the device to discontinue transmission. See Figure 10-2. After the Random Read operation, the internal address counter will increment to the address location following the one that was just read.

Figure 10-2. Random Read

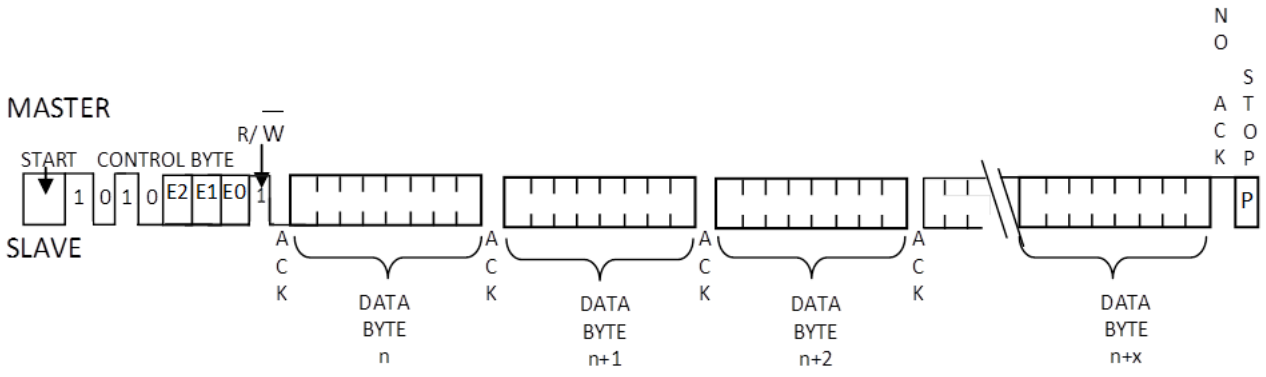


10.3 Sequential Read

Sequential read allows the whole memory contents to be serially read during one operation. Sequential Read is initiated in the same way as a Random Read except that after the device transmits the first data byte, the master issues an acknowledge instead of a STOP condition. This acknowledge from the master directs the device to transmit the next sequentially addressed byte (See Figure 10-3). Following the final byte transmitted to the master, the master will not generate an acknowledge, but will generate a STOP condition which causes the device to discontinue transmission.

To provide the Sequential Read, the device contains an internal address pointer which is incremented by one at each acknowledge received by the master, and by the STOP condition.

Figure 10-3. Sequential Read



11. Electrical Specifications

11.1 Absolute Maximum Ratings

Table 11-1. Absolute Maximum Ratings*

Parameter	Specification
Operating ambient temp range	-40°C to +85°C
Storage temperature range	-65°C to +150°C
Input supply voltage, VCC to GND	- 0.3V to 3.6V
Voltage on any pin with respect to GND	-0.5V to (V_{CC} + 0.5V)
ESD protection on all pins (Human Body Model)	>2kV
Junction temperature	125°C

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these, or any other conditions beyond those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

11.2 DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
		T_A = -40°C to +85° C, V_{CC} = 1.65V to 3.6V				
V_{CC}	Supply Range	1.65V to 3.6V	1.65		3.6	V
V_{VCCI}	V_{CC} Inhibit				1.55	V
		V_{CC}= 3.3V SCL at 1MHz		0.25	0.5	mA
I_{CC2}		V_{CC}= 3.3V		1	3	mA
I_{CC3}	Supply Current, Standby (1)	V_{CC}= 1.65V. SCL=SDA=1.65V	@25°C	1	3	µA
			@85°C	6	11	
		V_{CC}= 3.3V. SCL=SDA=3.3V	@25°C	2.2	3	
			@85°C	11	17	
I_{IL}	Input Leakage	SCL, SDA, WP, E0, E1, E2, V_{IN}=0V or			±1	µA
I_{OL}	Output Leakage	SDA V_{IN}=0V to V_{CC}			±1	µA
V_{IL}	Input Low Voltage	SCL, SDA, WP, E0, E1, E2	-0.3		V_{CC} x	V
V_{IH}	Input High Voltage	SCL, SDA, WP, E0, E1, E2	V_{CC} x 0.7		V_{CC} +	V
V_{OL}	Output Low Voltage	SDA I_{OL} = 3.0mA			0.4	V

1. Values are based on device characterization, not 100% tested in production.

11.3 AC Characteristics

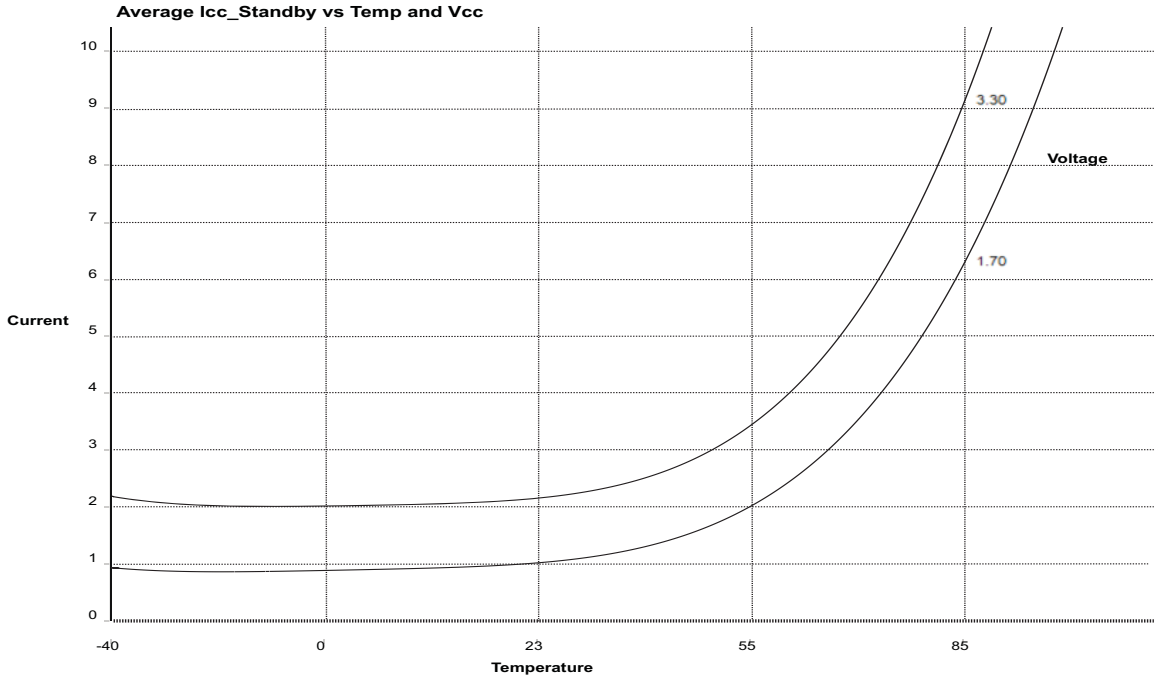
Applicable over recommended operating range:
TA = -40°C to +85° C, V_{CC} = 1.65V to 3.6V, CL = $C_B \leq 100pF$

Symbol	Parameter		Min	Typ	Max	Units
f_{CLK}	SCL clock frequency	$V_{cc} \geq 1.65V$	0		1	MHz
t_{RI}	SCL and SDA input rise time (1)				300	ns
t_{FL}	SCL and SDA input fall time (1)				100	ns
t_{SCLH}	SCL high time		500			ns
t_{SCLL}	SCL low time		500			ns
t_{STH}	START condition hold time		250			ns
t_{STS}	START condition setup time		250			ns
t_{DAH}	Data input hold time(2)		0			ns
t_{DAS}	Data input setup time		100			ns
t_{STPS}	STOP condition hold time		250			ns
t_{WPS}	WP setup time		600			ns
t_{WPH}	WP hold time		1300			ns
t_{OV}	Output valid from clock(2)				400	ns
t_{BFT}	Bus free time: time the bus must be free before a new transmission can start		500			ns
t_{OF}	Output fall time from VIH min to VIL max CB<100pF		10 + 0.1 C_B		250	ns
t_{SP}	Input filter spike suppression SDA and SCL pins				50	ns
t_{BW}	Byte write cycle time (one byte)			60	100	µs
t_{PW}	Page Write Cycle Time, 128 byte page (up to 30K write cycles)			3	5	ms
	Page Write Cycle Time, 128 byte page (up to 100K write cycles)			18		
t_{PUD}	V_{cc} power-up delay(3)				75	µs
Endurance				100,000(4)		Write Cycles
				Unlimited		Read Cycles
Retention				40		Years

Notes:
1. This parameter is ensured by characterization only.
2. As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
3. V_{cc} must be in operating range.
4. Adesto memory products based on CBRAM technology are “Direct-Write” memories. Endurance cycle calculations follow JEDEC specification JESD22-A117B. Endurance data characterized at 2.5V, +85° C. Endurance specification is identical for both byte and page write (unlike current EEPROM technologies where byte write operations result in lower endurance).

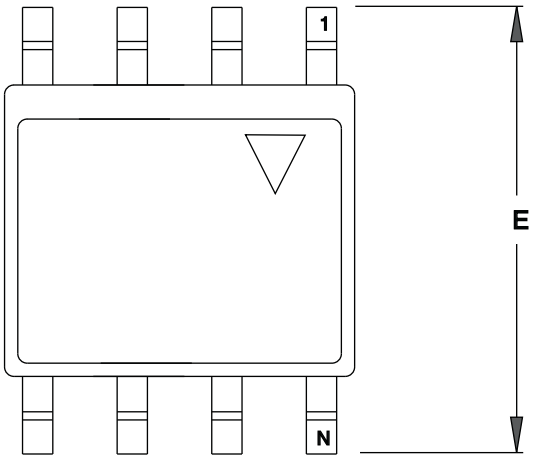
12. Typical Characteristics

Figure 12-1. Icc3, Supply Current, Standby

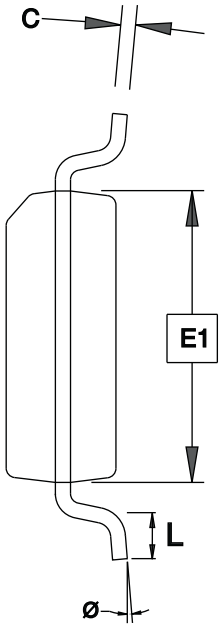


13. Mechanical Dimensions

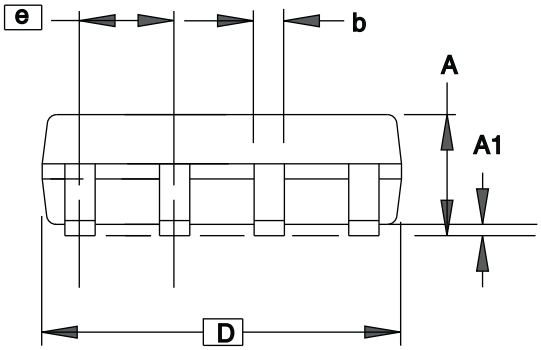
13.1 SN (JEDEC SOIC)



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

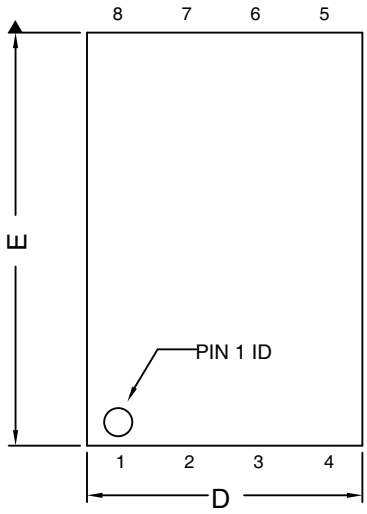
COMMON DIMENSIONS
(Unit of Measure = mm)

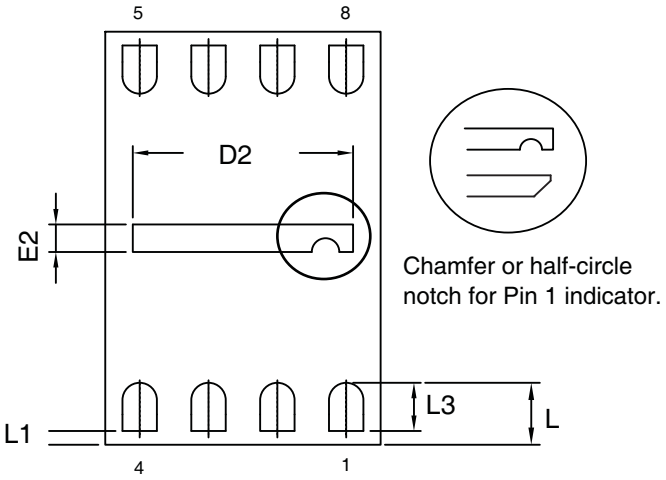
SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
ø	0°	–	8°	

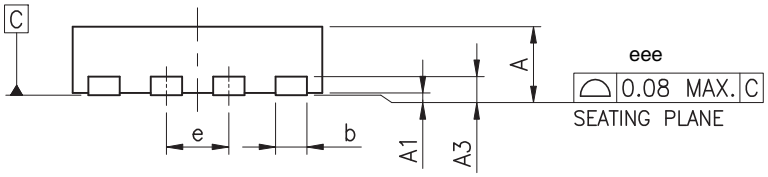
8/20/14

adesto™ TECHNOLOGIES Package Drawing Contact: contact@adestotech.com	TITLE 8S1, 8-lead (0.150"Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	GPC SWB	DRAWING NO. 8S1	REV. G

13.2 MA – 2x3 UDFN







COMMON DIMENSIONS
(Unit of Measure = mm)

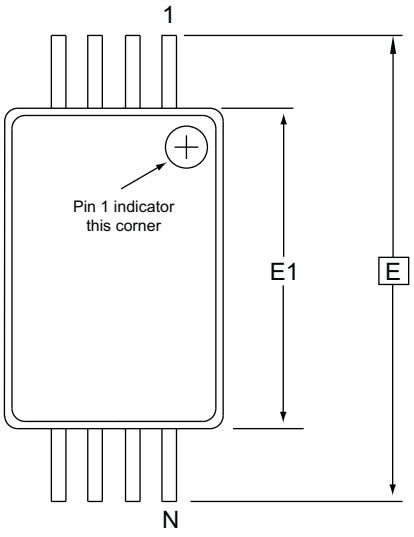
SYMBOL	MIN	NOM	MAX
A	0.45		0.60
A1	0.00		0.05
A3		0.150 REF	
b	0.20		0.30
D		2.00 BSC	
D2	1.50	1.60	1.70
E		3.00 BSC	
E2	0.10	0.20	0.30
e		0.50 BSC	
L	0.40	0.45	0.50
L1	0.00	0.10	
L3	0.30		0.50
eee	–	–	0.08

Notes: 1. All dimensions are in mm. Angles in degrees.
2. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

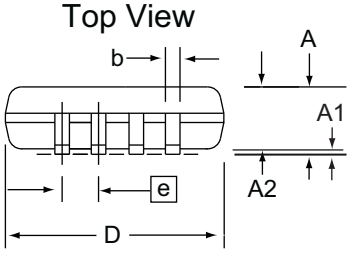
8/26/14

	TITLE	GPC	DRAWING NO.	REV.
adesto TECHNOLOGIES Package Drawing Contact: contact@adestotech.com	8MA3, 8-pad, 2 x 3 x 0.6 mm Body, 0.5 mm Pitch, 1.6 x 0.2 mm Exposed Pad, Saw Singulated Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN/USON)	YCQ	8MA3	GT

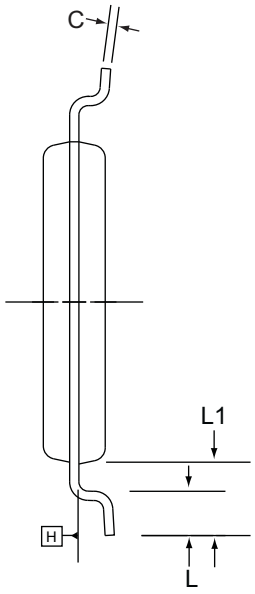
13.3 TA-TSSOP



Top View



Side View



End View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

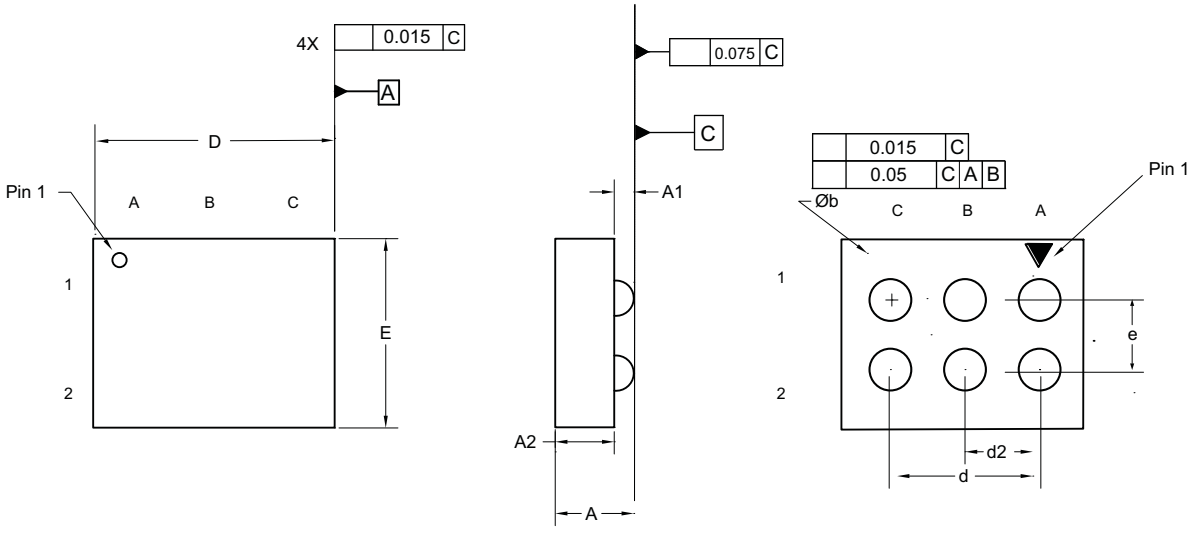
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

12/8/11

adesto® TECHNOLOGIES Package Drawing Contact: contact@adestotech.com	TITLE TA, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	GPC TNR	DRAWING NO. 8X	REV. E

13.4 CS6- 6-Ball WLCSP



TOP VIEW SIDE VIEW BALL SIDE

* Dimensions are NOT to scale.

Pin Assignment Matrix

	A	B	C
1	V_{CC}	GND	GND
2	SCL	SDA	GND

COMMON DIMENSIONS
(Unit of Measure = mm)

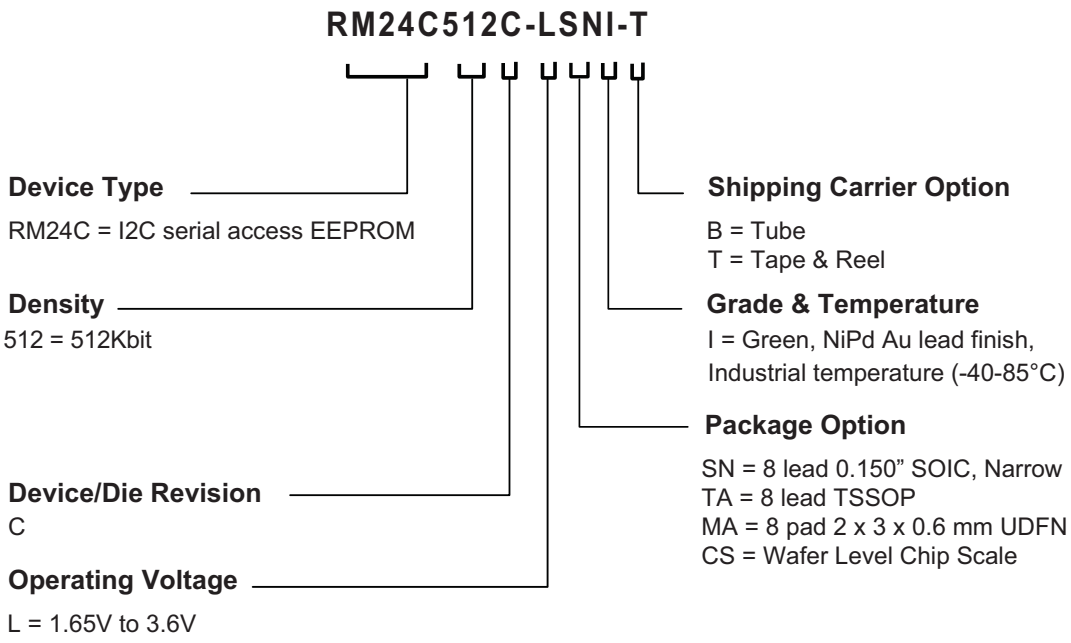
SYMBOL	MIN	TYP	MAX	NOTE
A		0.35		
A1		0.08		
A2		0.27		
E	Contact Adesto for details			
e		0.4		
d		0.8		
d2		0.4		
D	Contact Adesto for details			

7/31/15

adesto TECHNOLOGIES Package Drawing Contact: contact@adestotech.com	TITLE CS-6, 6-ball (3x3 Array) Wafer Level Chip Scale Package, WLCSP	GPC GCL	DRAWING NO. CS6	REV. 0A

14. Ordering Information

14.1 Ordering Detail



14.2 Ordering Codes

Ordering Code	Package	Density	Operating Voltage	Device Grade	Ship Carrier	Qty. Carrier
RM24C512C-LSNI-B	SN	512 Kbit	1.65V to 3.6V	Industrial (-40°C to 85°C)	Tube	100
RM24C512C-LSNI-T					Reel	4000
RM24C512C-LTAI-B	TA				Tube	100
RM24C512C-LTAI-T					Reel	4000
RM24C512C-LMAI-T	MA				Reel	5000
RM24C128C-LCSI-T	CS				Contact Factory	

Package Type	
SN	8-lead 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
TA	8-lead 3 x 4.4 mm, Thin Shrink Small Outline Package
MA	8-pad, 2 x 3 x 0.6 mm, Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)
CS	Wafer Level Chip Scale Package

15. Revision History

Doc. Rev.	Date	Comments
RM24C512C-082A	7/2015	Initial document release.
RM24C512C-L-082B	9/2015	Added WLCSP package option. Updated typical byte and page write specifications. Document status changed to Preliminary. Updated document name to RM24C512C-L.
RM24C512C-L-082C	1/2016	Corrected Temperature Grade to Industrial (-40°C to 85°C).
RM24C512C-L-082D	4/2016	Updated Icc_3 specification. Added Typical Characteristics Figure 12-1.
RM24C512C-L-082E	11/2016	Updated Endurance and Data Retention specifications. Updated T_{PW} and T_{BW} specifications,.

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