

WIZ810MJ Datasheet

(Ver. 1.2)



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Document History Information

Revision	Data	Description
Ver. 1.0	September , 2007	Release with WIZ810MJ Launching
Ver. 1.1	February, 2008	Hardware revision(ver.1.1). Modified the SPI_EN signal description (P.8) Modified the Schematic & Partlist : R10 is mounted as SPI_EN pull-down resistor. (P.15~16)
Ver. 1.2	January, 2009	Added temperature specification

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The screenshot shows the WIZnet website interface. At the top, there is a navigation menu with links for Home, Sitemap, Contact us, and 한국어. Below this is a secondary menu with links for Products, Technology, Technical Q & A, Library, Where to buy, Value Chain, and About us. The main content area features a large banner for the W5100 chip, describing it as a '3 in 1' solution for embedded Internet (TCP/IP Core + MAC + PHY). To the right, there is a 'New Products' section for the WIZ Series with W5100, specifically the Serial-to-Ethernet WIZ100SR. Below the banner, there are three columns of content: 'Application Reference' with a list of projects and dates, 'Solution Provider' with a list of boards and dates, and 'WIZnet News' with a list of news items and dates. A large blue arrow points to a 'Click !!' button, which is highlighted with a red box and labeled 'Technical Support'. At the bottom, there is a footer with the WIZnet logo, copyright information, and logos for NEC, AMEL, and MICROCHIP.

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1. Introduction

WIZ810MJ is the network module that includes W5100 (TCP/IP hardwired chip, include PHY), MAG-JACK (RJ45 with X'FMR) with other glue logics. It can be used as a component and no effort is required to interface W5100 and Transformer. The WIZ810MJ is an ideal option for users who want to develop their Internet enabling systems rapidly.

For the detailed information on implementation of Hardware TCP/IP, refer to the W5100 Datasheet.

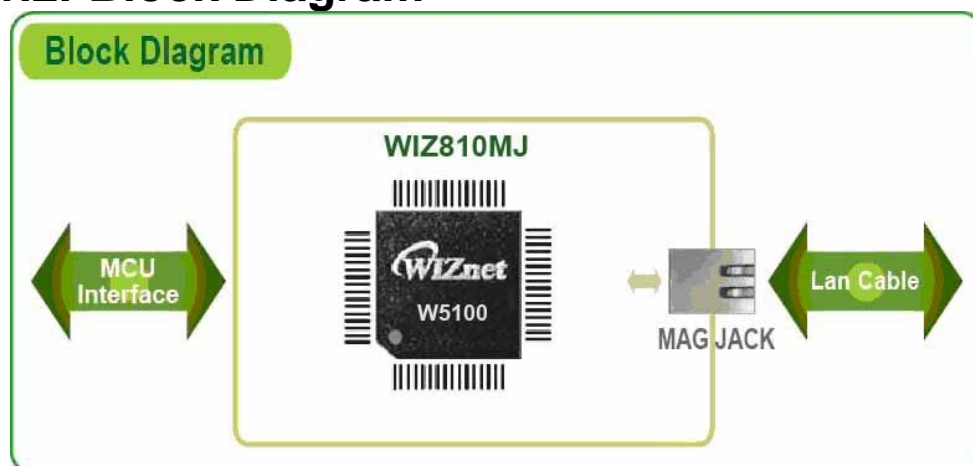
WIZ810MJ consists of W5100 and MAG-JACK.

- TCP/IP, MAC protocol layer: W5100
- Physical layer: Included in W5100
- Connector: MAG-JACK(RJ45 with Transformer)

1.1. Features

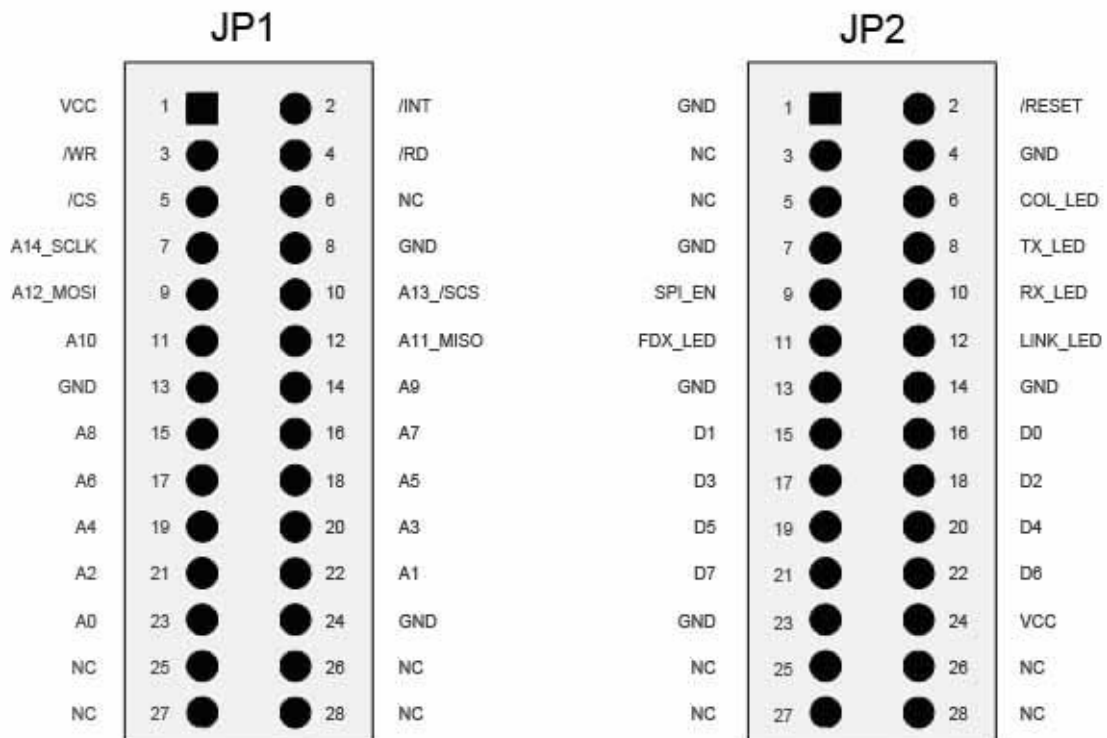
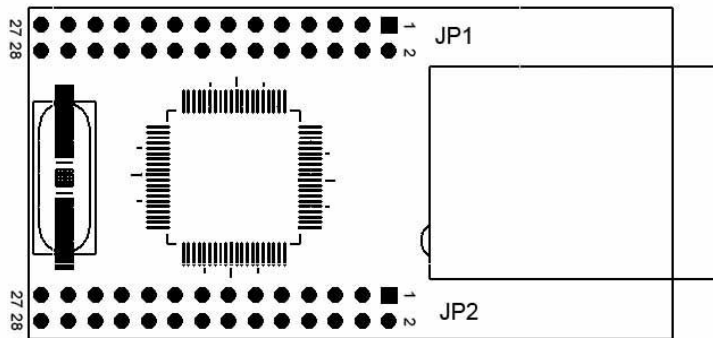
- Supports 10/100 Base TX
- Supports half/full duplex operation
- Supports auto-negotiation and auto crossover detection
- IEEE 802.3/802.3u Complaints
- Operates 3.3V with 5V I/O signal tolerance
- Supports network status indicator LEDs
- Includes Hardware Internet protocols: TCP, IP Ver.4, UDP, ICMP, ARP, PPPoE, IGMP
- Includes Hardware Ethernet protocols: DLC, MAC
- Supports 4 independent connections simultaneously
- Supports MCU bus Interface and SPI Interface
- Supports Direct/Indirect mode bus access
- Supports Socket API for easy application programming
- Interfaces with Two 2.0mm pitch 2 * 14 header pin
- Temperature : 0 ~ 70°C (Operation), -40 ~ 85°C (Storage)

1.2. Block Diagram



2. Pin Assignments & descriptions

2.1. Pin Assignments



I : Input
 I/O : Bi-directional Input and output

O : Output
 P : Power

2.2. Power & Ground

Symbol	Type	Pin No.	Description
VCC	P	JP1:1 , JP2:24	Power : 3.3 V power supply
GND	P	JP1:8, JP1:13, JP1:24, JP2:1, JP2:4, JP2:7 JP2:13, JP2:14, JP2:23	Ground

2.3. MCU Interfaces

Symbol	Type	Pin No.	Description
A14_SCLK	I	JP1:7	ADDRESS PIN OR SCLK(Serial Clock) This pin is used to select a register or memory. When asserting SPI_EN pin high, this pin is used to SPI Clock signal Pin.
A13_/SCS	I	JP1:10	ADDRESS PIN or /SCS (Slave Select) * This pin is used to select a register or memory. When asserting SPI_EN pin high, this pin is used to SPI Slave Select signal Pin. In only SPI Mode, this pin is active low
A12_MOSI	I	JP1:9	ADDRESS PIN or MOSI (Master Out Slave In) * This pin is used to select a register or memory. When asserting SPI_EN pin high, this pin is used to SPI MOSI signal pin.
A11_MISO	I/O	JP1:12	ADDRESS PIN or MISO (Master In Slave Out) * This pin is used to select a register or memory. When asserting SPI_EN pin high, this pin is used to SPI MISO signal pin.
A10~A8	I	JP1:11, JP1:14 JP1:15	Address Used as Address[10-8] pin
A7~A0	I	JP1:16 ~ JP1:23	Address Used as Address[7-0] pin
D7~D0	I/O	JP2:21, JP2:22 JP2:19, JP2:20 JP2:17, JP2:18 JP2:15, JP2:16	Data 8 bit-wide data bus
/CS	I	JP1:5	Module Select : Active low. /CS of W5100
/RD	I	JP1:4	Read Enable : Active low. /RD of W5100
/WR	I	JP1:3	Write Enable : Active low /WR of W5100

/INT	O	JP1:2	Interrupt : Active low After reception or transmission it indicates that the W5100 requires MCU attention. By writing values to the Interrupt Status Register of W5100 the interrupt will be cleared. All interrupts can be masked by writing values to the IMR of W5100 (Interrupt Mask Register). For more details refer to the W5100 Datasheet
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2.4. Network status & LEDs

You can observe the network status using MAG-JACK LEDs. LED interface can be extended to the LED of the main board.

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Symbol	Type	Pin No.	Description
COL_LED	O	JP2:6	Collision LED : Active low when collisions occur.
TX_LED	O	JP2:8	Transmit activity LED : Active low indicates the presence of transmitting activity.
RX_LED	O	JP2:10	Receive activity LED : Active low indicates the presence of receiving activity.
FDX_LED	O	JP2:11	Full Duplex LED : Active low when in full duplex operation. Active high when in half duplex operation.
LINK_LED	O	JP2:12	Link LED : Active low in link state indicates a good status for 10/100M. It is always ON when the link is OK and it flashes while in a TX or RX state.

2.5. Miscellaneous Signals

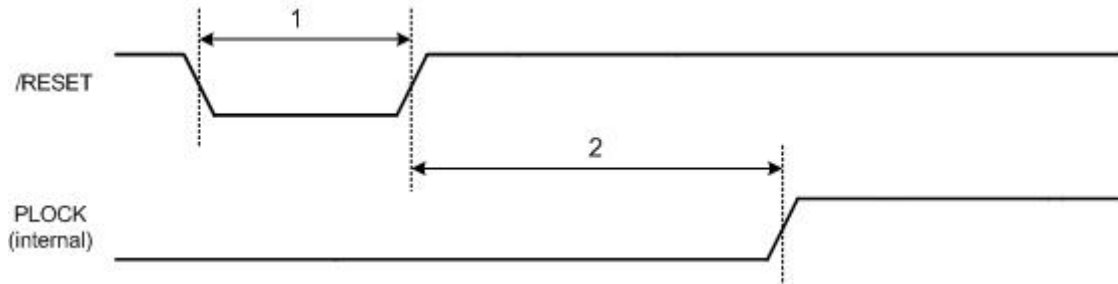
Symbol	Type	Pin No.	Description
/RESET	I	JP2:2	Reset : This pin is active low input to initialize or re-initialize W5100. By asserting this pin low for at least 2us, all internal registers will be re-initialized to their default states.
SPI_EN	I	JP2:9	SPI Enable : This pin selects Enable/Disable W5100 SPI Mode. Low = SPI Mode Disable High = SPI Mode Enable A pull-down resistor(R10) sets to the default of SPI Mode Disable. H/W ver.1.0 : R10 is not mounted H/W ver.1.1 : R10 is mounted
NC	-	JP1 : 6, 25, 26, 27, 28 JP2 : 3, 5, 25, 26, 27, 28	Not Connect

3. Timing Diagrams

WIZ810MJ provides following interfaces of W5100.

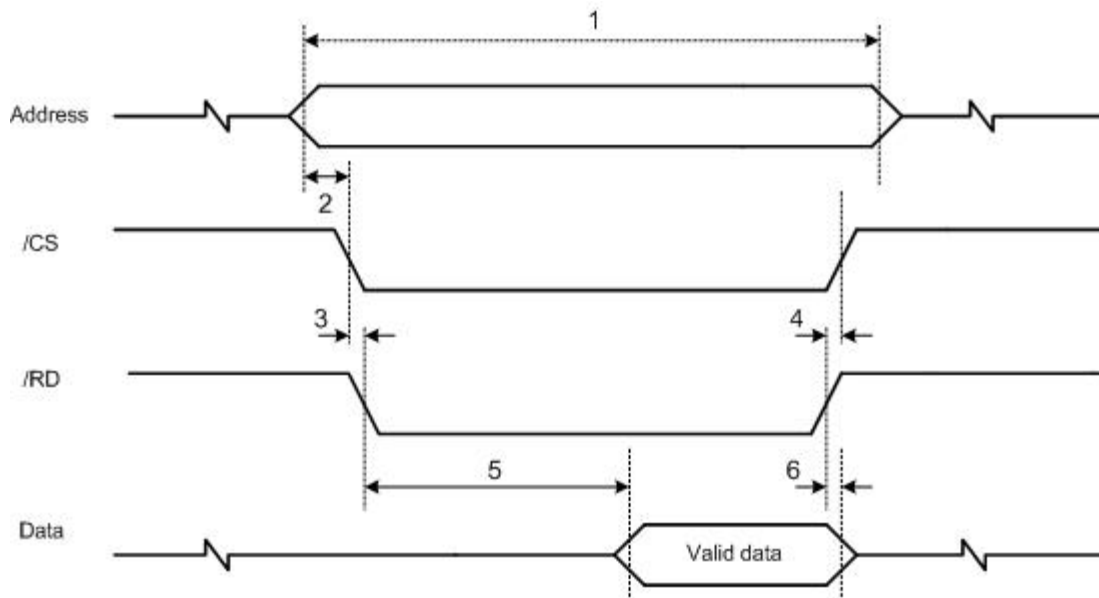
- Direct/Indirect mode bus access
- SPI access

3.1. Reset Timing



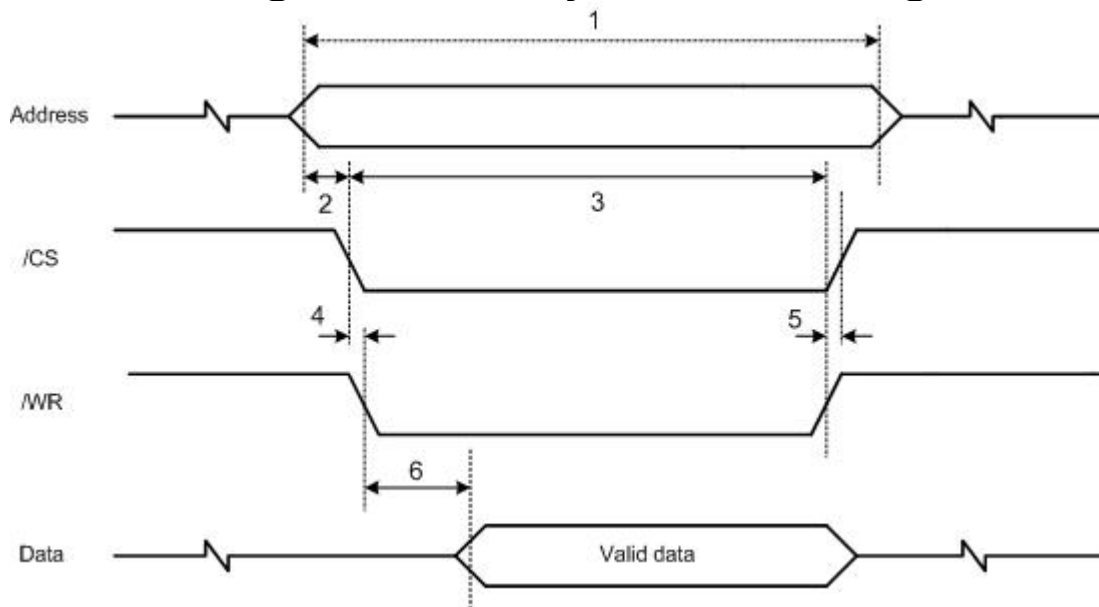
Description		Min	Max
1	Reset Cycle Time	2 us	-
2	/RESET to internal PLOCK	-	10 ms

3.2. Register/Memory READ Timing



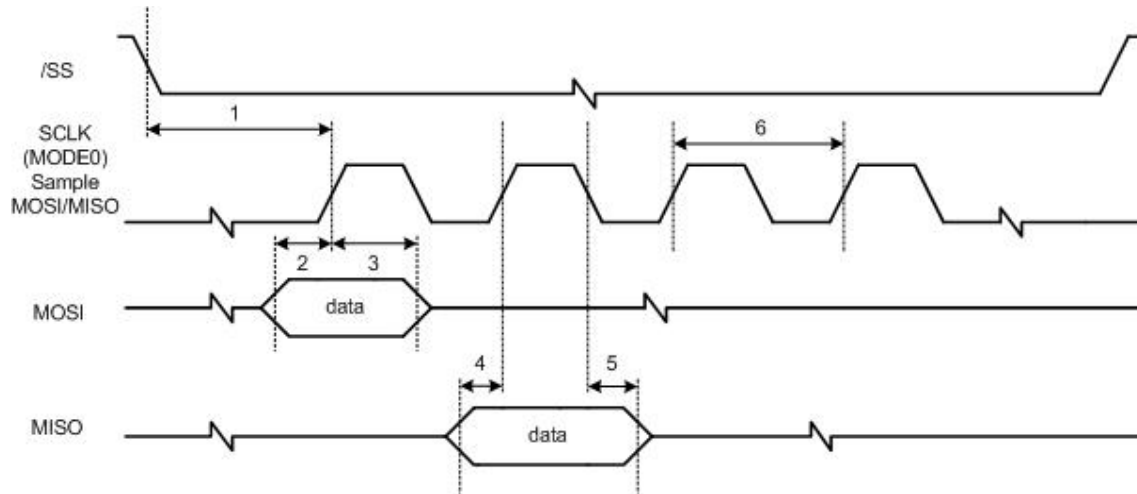
Description		Min	Max
1	Read Cycle Time	80 ns	-
2	Valid Address to /CS low time	8 ns	-
3	/CS low to /RD low time	-	1 ns
4	/RD high to /CS high time	-	1 ns
5	/RD low to Valid Data Output time	-	80 ns
6	/RD high to Data High-Z Output time	-	1 ns

3.3. Register/Memory WRITE Timing



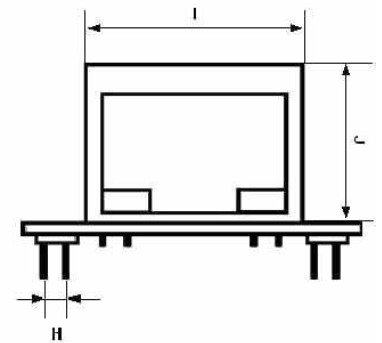
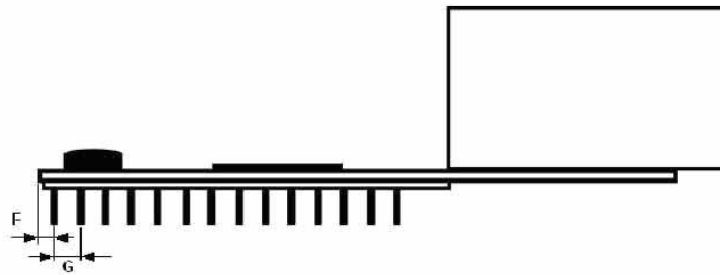
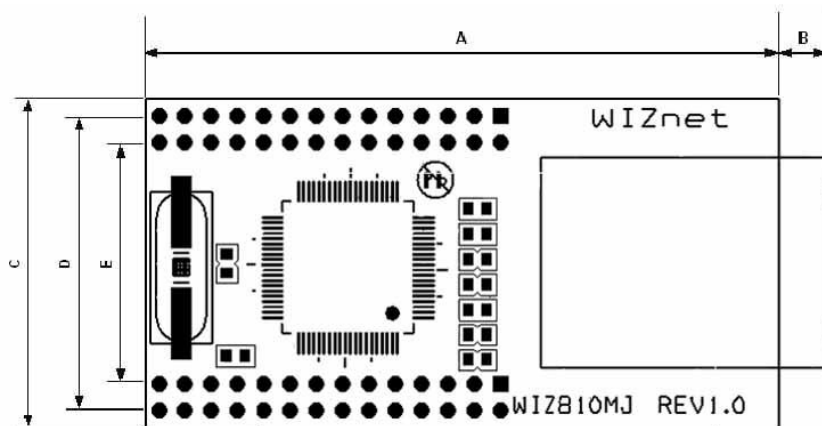
	Description	Min	Max
1	Write Cycle Time	70 ns	-
2	Valid Address to /CS low time	7 ns	-
3	/CS low to /WR high time	70 ns	-
4	/CS low to /WR low time	-	1 ns
5	/WR high to /CS high time	-	1 ns
6	/WR low to Valid Data time	-	14 ns

3.4. SPI Timing



Description	Mode	Min	Max
1 /SS low to SCLK	Slave	21 ns	-
2 Input setup time	Slave	7 ns	-
3 Input hold time	Slave	28 ns	-
4 Output setup time	Slave	7 ns	14 ns
5 Output hold time	Slave	21 ns	-
6 SCLK time	Slave	70 ns	

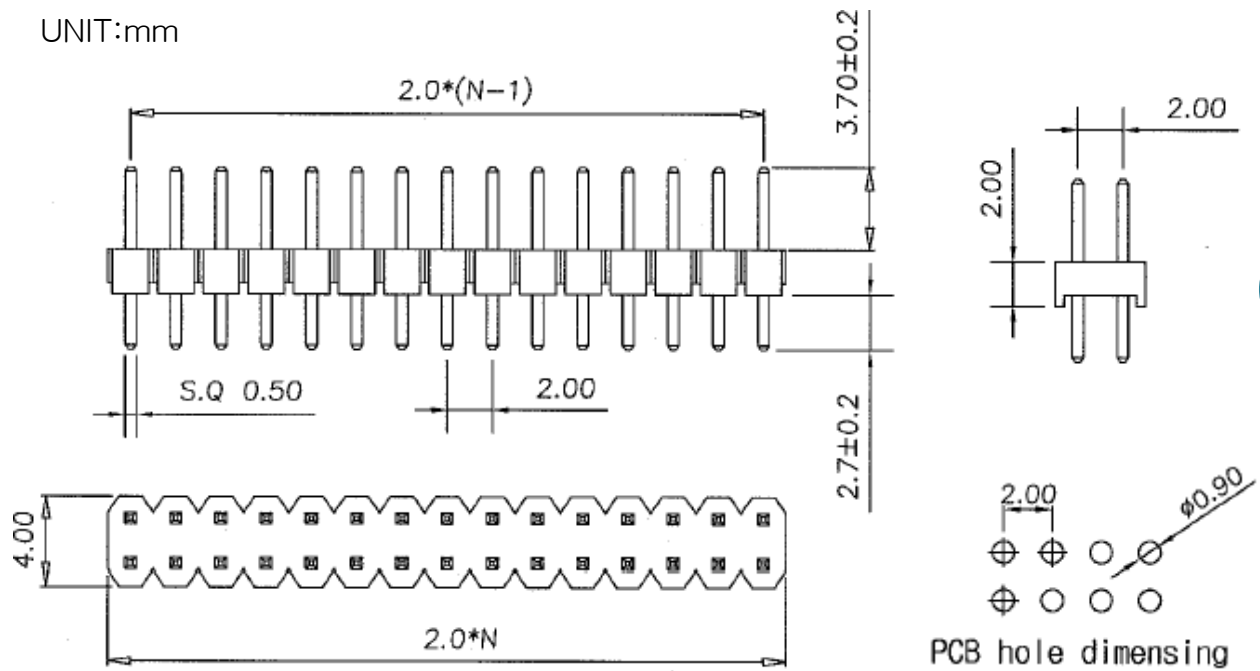
4. Dimensions



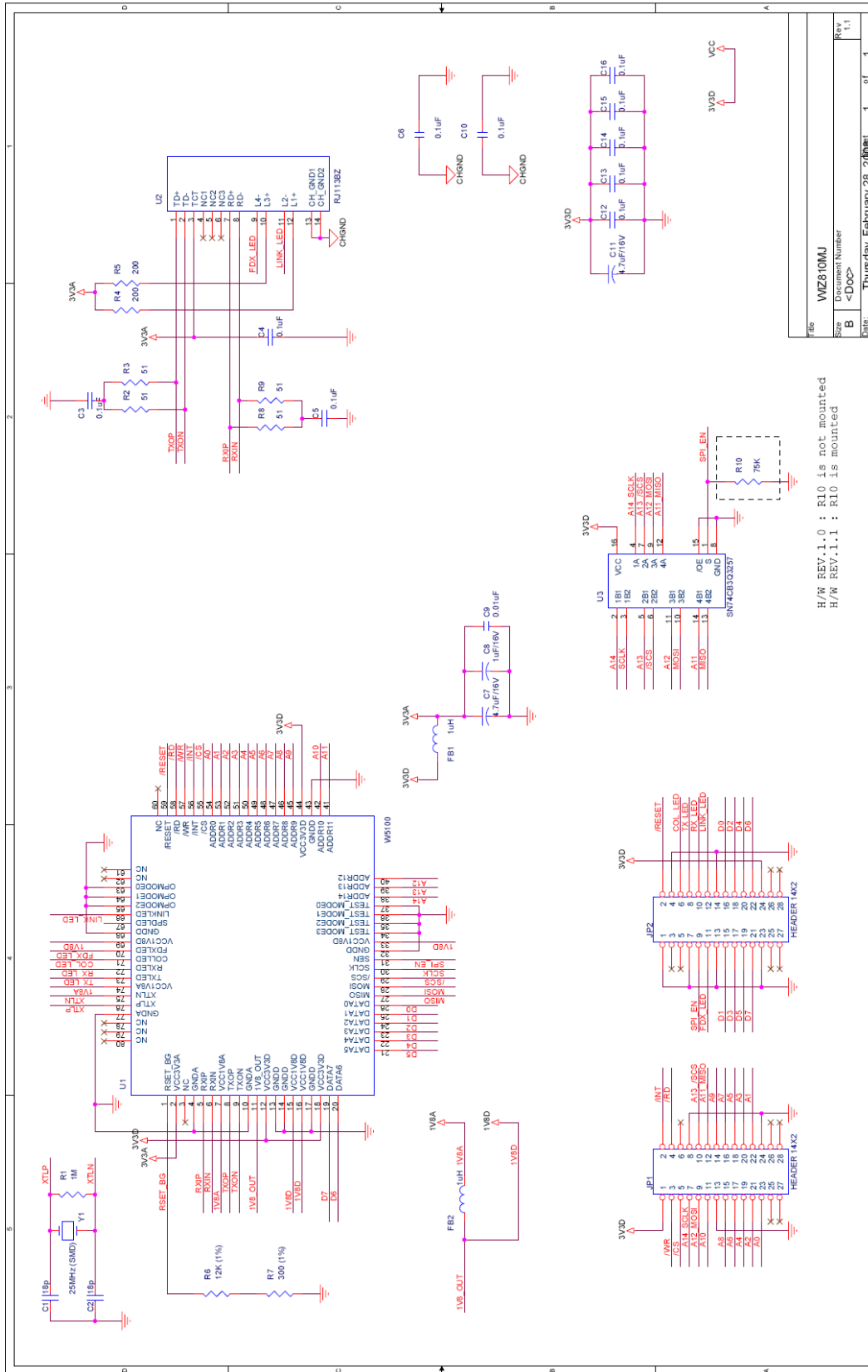
Symbols	Dimensions (mm)
A	48.0
B	3.5
C	25.0
D	22.4
E	18.4
F	1.0
G	2.0
H	2.0
I	16.0
J	13.5

5. Connector Specification

UNIT:mm



6. Schematic



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7. Partlists

Item	Q.ty	Reference	Part	Tech. Characteristics	Package
1	2	C2,C1	18pF	50V-20% Ceramic	CASE 0603
2	10	C3,C4,C5,C6,C10, C12,C13,C14,C15,C16	0.1uF	50V-20% Ceramic	CASE 0603
3	2	C7,C11	4.7uF/16V	16Vmin 10%	EIA/IECQ 3216
4	1	C8	1uF/16V	16Vmin 10%	EIA/IECQ 3216
5	1	C9	0.01uF	50V-20% Ceramic	CASE 0603
6	2	FB2,FB1	1uH Chip Ferrite Inductor	1uH, 50mA	CASE 0805
7	2	JP1,JP2	2X14 28PIN 2mm DIP STRAIGHT Header	2 X 14 2mm pitch	
8	1	R1	1M ohm	1/10W-5% SMD	CASE 0603
9	4	R2,R3,R8,R9	51 ohm 1%	1/10W-1% SMD	CASE 0603
10	2	R5,R4	200 ohm	1/10W-5% SMD	CASE 0603
11	1	R6	12K ohm (1%)	1/10W-1% SMD	CASE 0603
12	1	R7	300 ohm (1%)	1/10W-1% SMD	CASE 0603
13	1	R10	75K ohm	1/10W-5% SMD	CASE 0603
14	1	U1	W5100	WIZnet Hardware TCP/IP	LQFP80
15	1	U2	RJ113BZ	Transformer + RJ45	
16	1	U3	SN74CB3Q3257	Bus Switch(vendor : TI)	TSSOP
17	1	Y1	25MHz (SMD)	SMD Type, CL=18pF	SX-1
18	1		WIZ810MJ REV1.0 1.6T 4LAYER	PRINTED CIRCUIT BOARD	