

Built-in OVP Micro USB Switch with USB2.0, MHL™ and Audio

BD91411GW

●General Description

BD91411GW is USB connector interface IC. It is possible to use it for the application for the mobile device such as smart phones and mobile phones.

●Features

- Complete solution for mini/micro USB connect multiplexing.
- MHL/USB/UART 2paths, AUDIO 1path, Monaural Microphone 1path in 4 to 1 multiplexer.
- Compatible with USB High Speed/Full Speed.
- CECBUS to ID bypass switch.
- Audio switch handle with negative voltage signal.
- Microphone signal paths to VBUS or HDPR are built in.
- ID resistance support to CEA936A, Battery Charging Specification (BCS) ver1.2, MCPC, USB-OTG and MHL specification.
- Power-On Reset.
- USB Charger detection support with BCS ver1.2 specification.
- Over voltage protection (OVP) up to 28V about VB(VBUS) input and VC(cradle) input.
- Power multiplexer OVP input about VB and VC.
- Internal Low Ron FET about OVP(VB and VC).
- OTG power path switch (Output side in this power path support 28V protection) is built in.
- VBUS linked LDO (4.9V or 3.3V are selectable.)
- I²C compatible Interface.

●Key Specifications

- OVP switch ON resistance: 120mΩ (Typ.)
- Over Current Protection(OCP): 2.0A(Min.)
- Regulator output voltage: 3.3V or 4.9V
- MHL/USB switch ON resistance: 5Ω (Typ.)
- MHL/USB switch ON capacitance: 6pF(Typ.)
- VBAT standby current: 6μA (Typ.)
- Operating temperature range: -30°C to +85°C

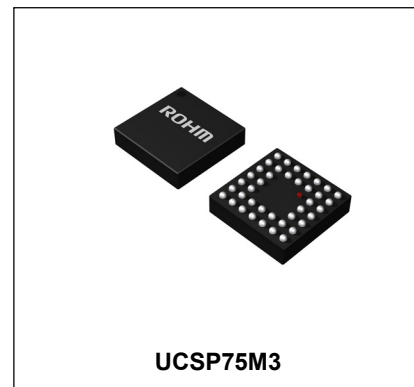
●Applications

- Mobile-Phones · Smart-Phones
- Tablet-PC
- Digital still camera (DSC)

●Package

UCSP75M3

W(Typ.) x D(Typ.) x H(Max.)
3.00mm x 3.00mm x 0.85mm



●Typical Application Circuit

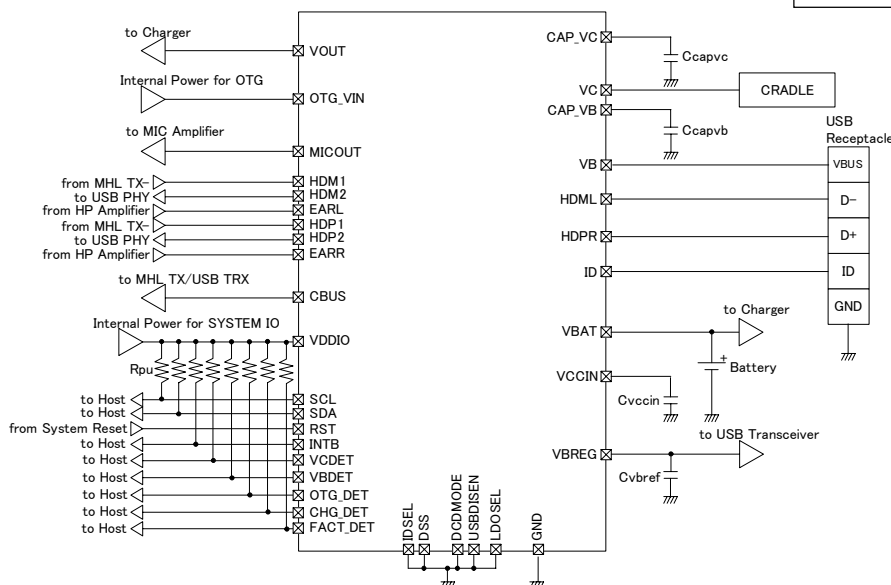


Fig.1 Typical Application Circuit

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1.Pin Configuration

| | | | | | | | |
|---|---------|---------|---------|----------|---------|--------|--------|
| G | TMODE1 | HDM1 | HDP1 | EARL | EARR | ID | TMODE0 |
| F | HDML | HDM2 | HDP2 | FACT_DET | CBUS | VCCIN | VDDIO |
| E | HDPR | MICOUT | DSS | RST | SCL | SDA | VBAT |
| D | GND | LDOSEL | CHG_DET | USBDISEN | DCDMODE | INTB | GND |
| C | VBREG | OTG_DET | (INDEX) | VBDET | VCDET | IDSEL | VC |
| B | OTG_VIN | VB | CAP_VB | VOUT | VOUT | VC | VC |
| A | ATEST0 | VB | VB | VOUT | VOUT | CAP_VC | ATEST1 |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |

Fig.2 Pin configuration (BOTTOM VIEW)

2.Pin Description

| No. | BALL No. | BALL NAME | I/O | Function | pull down | Pins configuration when not in use |
|-----|-------------|-----------|-----|--|-----------|------------------------------------|
| 1 | B6,B7,C7 | VC | I | Power supply about Cradle input | | open or GND |
| 2 | A2,A3,B2 | VB | I | Power supply about USB VBUS input | | open or GND |
| 3 | E7 | VBAT | I | Power supply about Battery Voltage | | open or GND |
| 4 | F7 | VDDIO | I | Power supply for I2C I/F | | open or GND |
| 5 | F6 | VCCIN | O | Power supply for internal circuit | | open |
| 6 | D1,D7 | GND | GND | GND | | GND |
| 7 | A4,A5,B4,B5 | VOUT | O | OVP output | | open |
| 8 | B1 | OTG_VIN | I | OTG Power Input | | open or GND |
| 9 | E3 | DSS | I | MUXSW Initial Value Select Signal. | | GND |
| 10 | A6 | CAP_VC | O | CAP connect pin for SW1 OVP | | open |
| 11 | B3 | CAP_VB | O | CAP connect pin for SW2 OVP | | open |
| 12 | C5 | VCDET | O | VC detecting (UVLO < VC < OVLO) | | open |
| 13 | C4 | VBDET | O | VB detecting (UVLO < VB < OVLO) | | open |
| 14 | C2 | OTG_DET | O | OTG Mode Detection | | open |
| 15 | F4 | FACT_DET | O | Factory Mode Detection | | open |
| 16 | F5 | CBUS | I/O | CBUS Signal Path | | open |
| 17 | C1 | VBREG | O | Regulator with VBUS Output | | open |
| 18 | D2 | LDOSEL | I | Regulator output voltage select. | | GND |
| 19 | E2 | MICOUT | O | MIC signal Output. | | open |
| 20 | G3 | HDP1 | I/O | MHL/USB/UART D+ Signal path1 | | open |
| 21 | G2 | HDM1 | I/O | MHL/USB/UART D- Signal path1 | | open |
| 22 | F3 | HDP2 | I/O | MHL/USB/UART D+ Signal path2 | | open |
| 23 | F2 | HDM2 | I/O | MHL/USB/UART D- Signal path2 | | open |
| 24 | G5 | EARR | I | Headphone Right signal path | 500Ω *1 | open |
| 25 | G4 | EARL | I | Headphone Left signal path | 500Ω *1 | open |
| 26 | E1 | HDPR | I/O | MHL/USB/UART/Earphone/MIC Signal Path | | open |
| 27 | F1 | HDML | I/O | MHL/USB/UART/Earphone Signal Path | | open |
| 28 | D3 | CHG_DET | O | USB Charging port detection | | open |
| 29 | G6 | ID | I/O | ID pull down resistance connecting pin | | open |
| 30 | E5 | SCL | I | I2C Clock signal input | | GND |
| 31 | E6 | SDA | I/O | I2C Data signal input | | GND |
| 32 | D6 | INTB | O | Interrupt signal output | | open |
| 33 | E4 | RST | I | Reset signal input | | GND |
| 34 | D4 | USBDISEN | I | USB Port detection disable. | | GND |
| 35 | G7 | TMODE0 | I | TEST Pin(for Vendor TEST) | 1MΩ | open or GND |
| 36 | G1 | TMODE1 | I | TEST Pin(for Vendor TEST) | 1MΩ | open or GND |
| 37 | A1 | ATEST0 | I/O | TEST Pin(for Vendor TEST) | | Open |
| 38 | A7 | ATEST1 | I/O | TEST Pin(for Vendor TEST) | | Open |
| 39 | D5 | DCDMODE | I | DCD Time out select. | | GND |
| 40 | C6 | IDSEL | I | I2C Device address select | | GND |
| 41 | C3 | INDEX | - | Index mark | | open |

*1 Turn on and turn off can be controlled by Register.

3. Block Diagram

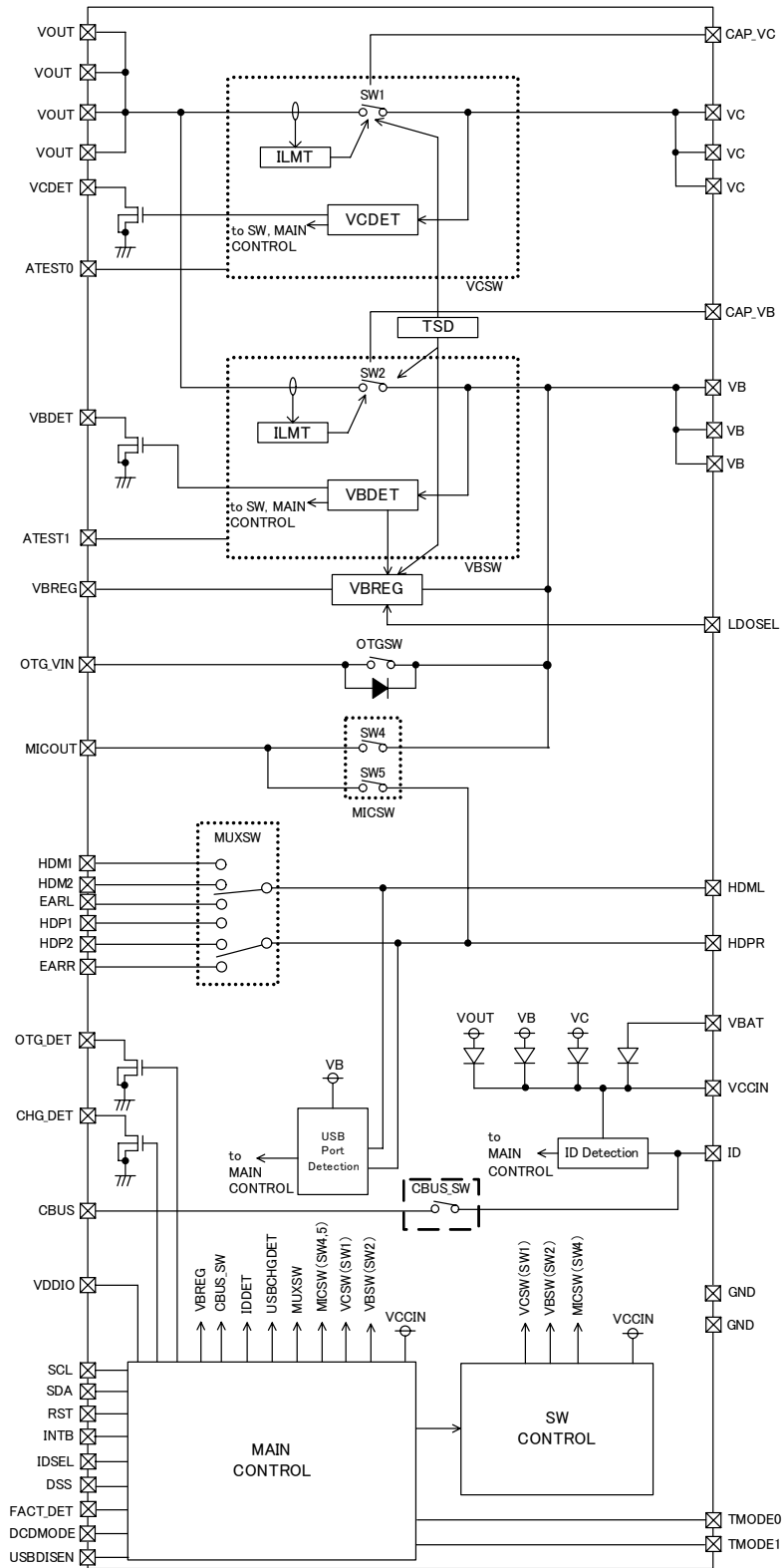


Fig.3 Block Diagram

4. Absolute Maximum Ratings (Ta=25°C)

| Item | Symbol | Rating | Unit |
|--|--------|------------|------|
| Maximum Supply Voltage1 (VB, VC) | VIN1 | -0.3~30 | V |
| Maximum Supply Voltage2 (VBAT) | VIN2 | -0.3~6.0 | V |
| Maximum Supply Voltage3 (VDDIO) | VIN3 | -0.3~4.5 | V |
| Maximum Supply Voltage4 (HDP1, HDM1,) | VIN4 | -1.0~7.0 | V |
| Maximum Supply Voltage5 (HDP2, HDM2) | VIN5 | -1.0~7.0 | V |
| Maximum Supply Voltage6 (EAPR, EARL) | VIN6 | -1.5~7.0 | V |
| Maximum Supply Voltage7 (HDPR, HDML,) | VIN7 | -1.5~7.0 | V |
| Maximum Supply Voltage8 (VOUT, CAP_VB, CAP_VC, OTG_VIN) | VIN8 | -0.3~7.0 | V |
| Maximum Supply Voltage9 (Others pins) | VIN9 | -0.3~6.0 | V |
| Power Dissipation | Pd | 1346 (*1) | mW |
| Operating Temperature Range | Topr | -30 ~ +85 | °C |
| Storage Temperature Range | Tstg | -55 ~ +125 | °C |

*1 This value is the permissible loss using a ROHM specification board (50mm x 58mm board mounting).

At the time of PCB mounting the permissible loss varies with the size and material of board.

When using more than at Ta=25°C, it is reduced 10.77 mW per 1°C. (Caution)

Use in excess of this value may result in damage to the device. Moreover, normal operation is not protected.

5. Recommended Operating Ratings (Ta=25°C)

| Item | Symbol | Range | Unit |
|-----------------|--------|-------------|------|
| VB, VC Voltage | VB | 3.8 ~ 28 | V |
| VBAT Voltage | VBAT | 2.9 ~ 4.6 | V |
| VDDIO Voltage | VDDIO | 1.7 ~ 3.0 | V |
| OTG_VIN Voltage | VOTG | 4.40 ~ 5.25 | V |

6. Electrical Characteristic (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VB=5.0V, VC=5.0V, VDDIO=1.8V, OTG_VIN=0V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|----------|------|------|------|------|---|
| ● Circuit Current | | | | | | |
| VBAT Circuit Current 1 (Standby) | IQVBAT1 | - | 6 | 20 | μA | VBAT=3.6V, VDDIO=1.8V VB=VC=Open, OTG_VIN=0V ID=Open |
| VDDIO Circuit current 1 (Standby) | IQVDDIO1 | - | 0.0 | 1.0 | μA | |
| VBAT Circuit Current 2 (HDSW =ON)) | IQVBAT2 | - | 3 | 10 | μA | VBAT=3.6V, VDDIO=1.8V VB=5V, VC=Open, OTG_VIN=0V ID=Open HDSW=ON |
| VB Circuit Current 2 (HDSW =ON) | IQVB2 | - | 210 | 450 | μA | |
| VBAT Circuit Current 3 (HPSW,MICSW= ON) | IQVBAT3 | - | 55 | 150 | μA | VBAT=3.6V, VDDIO=1.8V, VB=VC=Open, OTG_VIN=0V ID=287kΩ pull down HPSW,MICSW=ON |
| VC Circuit Current 4 (standby) | IQVC4 | - | 150 | 300 | μA | VC=5.0V, VB=0.0V, OTG_VIN=0V, |
| VBAT Circuit Current 5 (OTGSW =ON) | IQVBAT5 | - | 3 | 10 | μA | VBAT=3.6V, VDDIO=1.8V, VB=VC=Open OTG_VIN=5V ID=0kΩ pull down OTGSW=ON |
| OTG_VIN Circuit Current 5 (OTGSW =ON) | IQOTG5 | - | 230 | 450 | μA | |

● Electrical Characteristic (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VB=VC=5.0V, VDDIO=1.8V, OTG_VIN=0V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|--|--------|--------------------|------|--------------------|------|----------------------------|
| ● Digital characteristics(Digital Pins: SCL, SDA, RST, INTB, CHG_DET, OTG_DET, FACT_DET, VCDET and VBDET, IDSEL, LDOSEL, USBDISEN, DCDMODE, DSS) | | | | | | |
| Input "H" level (SCL, SDA, RST) | VIH1 | $0.8 \times VDDIO$ | - | $VDDIO+0.3$ | V | |
| Input "L" level (SCL, SDA, RST) | VIL1 | -0.3 | - | $0.2 \times VDDIO$ | V | |
| Input leak current (SCL, SDA, RST) | IIC1 | -1 | 0 | 1 | μA | Pin voltage: VDDIO |
| Output Voltage "L" (SDA) | VOLSDA | - | - | 0.4 | V | IOL=6mA |
| Output Voltage "L" (INTB, VCDET, VBDET, CHG_DET, OTG_DET, FACT_DET) | VOL1 | - | - | 0.3 | V | Source=1mA |
| OFF Leakage Current (INTB, CHG_DET, OTG_DET, FACT_DET) | IIOFF1 | -3 | - | 3 | μA | VIN=VDDIO |
| OFF Leakage Current (VCDET, VBDET) | IIOFF2 | -3 | - | 3 | μA | VIN=VC(VCDET) or VB(VBDET) |
| Input "H" Level (IDSEL, USBDISEN,DCDMODE, DSS) | VIH2 | $0.8 \times VCCIN$ | - | $VCCIN+0.3$ | V | *1 |
| Input "L" Level (IDSEL, USBDISEN,DCDMODE, DSS) | VIL2 | -0.3 | - | $0.2 \times VCCIN$ | V | *1 |
| Input "H" Level (LDOSEL) | VIH3 | 2.0 | - | $VCCIN+0.3$ | V | *1 |
| Input "L" Level (LDOSEL) | VIL3 | -0.3 | - | 0.6 | V | |
| Input Leakage Current(IDSEL, LDOSEL, USBDISEN, DCDMODE, DSS) | IIC2 | -1 | 0 | 1 | μA | Pin voltage: VCCIN |
| Diode forward Voltage | Vf | - | 0.6 | - | V | |

*1 $VCCIN = (VOUT \text{ or } VBAT \text{ or } VB \text{ or } VC) - V_f$

●Electrical Characteristic (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VB=5.0V, VC=0.0V, VDDIO=1.8V, OTG_VIN=0V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|-------------------------|--------|------|-------|------|-------|------------------|
| ●OVP (VB : SW2) | | | | | | |
| UVLO release voltage | UVLO1H | 3.6 | 3.8 | 4.0 | V | VIN=up |
| UVLO detect voltage | UVLO1L | 3.0 | 3.125 | 3.25 | V | VIN=down |
| OVLO detect voltage | OVLO1 | 6.2 | 6.4 | 6.6 | V | VIN=up |
| OVLO hysteresis voltage | OVLOh1 | - | 120 | - | mV | VIN=down |
| Over current limit | ILM1 | 2.0 | - | - | A | |
| On resistance of SW | RON1 | - | 120 | 250 | mΩ | VB - VOUT SW |
| Start up delay time | Ton1 | - | 5 | 10 | msec | |
| Output turn off time | Toff1 | - | 1 | 5 | μ sec | |
| Reverse Leak Current | Ileak1 | -3 | - | 3 | μ A | VB=0.0V, VC=5.0V |

●Electrical Characteristic (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VB=0.0V, VC=5.0V, VDDIO=1.8V, OTG_VIN=0V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|-------------------------|--------|------|-------|------|-------|------------------|
| ●OVP (VC : SW1) | | | | | | |
| UVLO release voltage | UVLO2H | 3.6 | 3.8 | 4.0 | V | VIN=up |
| UVLO detect voltage | UVLO2L | 3.0 | 3.125 | 3.25 | V | VIN=down |
| OVLO detect voltage | OVLO2 | 6.2 | 6.4 | 6.6 | V | VIN=up |
| OVLO hysteresis voltage | OVLOh2 | - | 120 | - | mV | VIN=down |
| Over current limit | ILM2 | 2.0 | - | - | A | |
| On resistance of SW | RON2 | - | 120 | 250 | mΩ | VC - VOUT SW |
| Start up delay time | Ton2 | - | 5 | 10 | msec | |
| Output turn off time | Toff2 | - | 1 | 5 | μ sec | |
| Reverse Leak Current | Ileak2 | -3 | - | 3 | μ A | VB=5.0V, VC=0.0V |

●Electrical Characteristic (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VB=5.0V, VC=0.0V, VDDIO=1.8V, OTG_VIN=0V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|----------------------------|---------------|------|------|------|------|-----------------------|
| ●VBREG | | | | | | |
| Output Voltage (3.3V Mode) | LDOVOUT 33 | 3.20 | 3.30 | 3.40 | V | LDOSEL=H, Iload = 1mA |
| Output Voltage (4.9V Mode) | LDOVOUT 49 | 4.75 | 4.90 | 5.05 | V | LDOSEL=L, Iload = 1mA |
| Output Current | LDO MAXI | 30 | - | - | mA | |

●Electrical Characteristic (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VB=VC=0V, VDDIO=1.8V, OTG_VIN=5V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|----------------------|--------------|------|------|------|-------|--------------------------|
| ●OTGSW | | | | | | |
| On resistance of SW | RON OTGSW | - | 0.2 | 0.5 | Ω | OTG_VIN=5.0V OTGSW=ON |
| Output turn off time | Toff3 | - | 0.2 | 5 | μ sec | |

●Electrical Characteristic (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VDDIO=1.8V, VB=VC=0V, OTG_VIN=0V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---------------------------|-------------|------|------|------|------|--|
| ●HPSW (EARR,EARL) | | | | | | |
| Analog signal input range | VIN_LR | -1.4 | — | 1.4 | V | |
| ON resistance | RON HPSW | — | 5 | 10 | Ω | EARR = EARL= 0V SINK=10mA |
| Total Harmonic Distortion | THD_HP | — | 0.02 | 0.10 | % | f=1kHz Vin=1.4Vpp RL=16Ω Filter:20kHz LPF |
| Cross talk | CT | — | — | -90 | dB | RL=16Ω, f=1kHz Filter: DIN AUDIO |
| Pull down resistance | RPD HPSW | — | 500 | — | Ω | |
| HPSW start up time | TUPHP | - | - | 2 | ms | HPSW OFF->ON |

●Electrical Characteristic (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VB=5.0V, VDDIO=1.8V, VC=0V, OTG_VIN=0V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|--------------------------------|-------------|------|------|------|------|---------------------------|
| ●HDSW (HDP1, HDM1, HDP2, HDM2) | | | | | | |
| SW resistance when ON | RON HDSW | — | 5 | 10 | Ω | VIN=3.3V or 0V |
| Input current when OFF | IIOFF | -3 | — | 3 | μA | VIN=3.3V or 0V VB=OPEN |
| SW capacitance | CSW | — | (6) | — | pF | HDSW ON |
| HDSW start up time | TUPHD | — | — | 2 | ms | HDSW OFF->ON |

●Electrical Characteristic (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VDDIO=1.8V, VB=VC=0V, OTG_VIN=0V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---------------------------|--------------|------|------|------|------|---|
| ●MICSW (MIC : SW4, SW5) | | | | | | |
| Analog signal input range | VIN_MIC | 0 | — | 2.5 | V | |
| SW resistance when ON | RON MICSW | — | 20 | 40 | Ω | VIN=2.5V or 0V |
| Input current when OFF | IIOFF | -3 | — | 3 | μA | VIN=2.5V or 0V |
| Total Harmonic Distortion | THD_MIC | — | 0.02 | 0.10 | % | f=1kHz Vin=1.0Vpp Vbias=2.0V RL=10kΩ Filter:20kHz LPF |
| MICSW start up time | TUPMIC | - | - | 2 | ms | MICSW OFF-> ON |

●Electrical Characteristic (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VDDIO=1.8V, VB=VC=0V, OTG_VIN=0V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|-----------------------|---------------|------|-------|------|------|----------------|
| ●CBUSSW | | | | | | |
| On resistance of SW | RON CBUSSW | — | 5 | 10 | Ω | VIN=3.3V or 0V |
| Cut off Frequency | FCCBUS | - | (100) | - | MHz | @-3dB |
| Leak current when OFF | IIOFF | -3 | — | 3 | μA | VIN=3.3V or 0V |
| CBUSSW start up time | TUPCBUS | - | - | 2 | ms | CBUSSW OFF->ON |

●Electrical Characteristic (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VB=5.0V, VDDIO=1.8V, VC=0V, OTG_VIN=0V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|----------|------|------|------|------|-------------------|
| ●USBCHG_DET | | | | | | |
| VDP_SRC Voltage (D+ Output Voltage) | VDP_SRC | 0.5 | 0.6 | 0.7 | V | Io=0~200uA |
| VDM_SRC Voltage (D- Output Voltage) | VDM_SRC | 0.5 | 0.6 | 0.7 | V | Io=0~200uA |
| RCD Resistance (D+ pull up resistance) | RCD | 75 | 100 | 125 | kΩ | |
| Not USB port detect (Host D+ pull down resistance) | RHDP | 100 | - | - | kΩ | |
| VDAT_REF voltage (D+/D- detect voltage) | VDAT_REF | 0.3 | 0.35 | 0.4 | V | When HDPR/HDML up |
| VLGC voltage (D+/D- detect voltage) | VLGC | 1.2 | 1.4 | 1.6 | V | When HDPR/HDML up |
| D+ sink current | IDP_SINK | 50 | 85 | 150 | uA | V(HDPR) = 0.6V |
| D- sink current | IDM_SINK | 50 | 85 | 150 | uA | V(HDML) = 0.6V |

●Electrical Characteristic (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VB=5.0V, VDDIO=1.8V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|--------------------------------|---------|------|------|------|---------------|---|
| ●ID | | | | | | |
| Connected resistance detect | RIDopen | 1000 | - | - | kΩ | Open detection |
| | RID1 | - | 797 | - | kΩ | |
| | RID2 | - | 557 | - | kΩ | |
| | RID3 | - | 440 | - | kΩ | |
| | RID4 | - | 390 | - | kΩ | |
| | RID5 | - | 287 | - | kΩ | |
| | RID6 | - | 200 | - | kΩ | |
| | RID7 | - | 180 | - | kΩ | |
| | RID8 | - | 124 | - | kΩ | |
| | RID9 | - | 102 | - | kΩ | |
| | RID10 | - | 68 | - | kΩ | |
| | RID11 | - | 47 | - | kΩ | |
| | RID12 | - | 36.5 | - | kΩ | |
| | RID13 | - | 1 | - | kΩ | |
| RID14 | - | 0 | 50 | Ω | GND detection | |
| COMPH detection voltage | RatioH | 85 | 90 | 95 | % | Ratio = 100 x V (ID) / VCCIN [%] When ID voltage is up. |
| COMPL detection voltage | RatioL | 22 | 26 | 30 | % | Ratio = 100 x V (ID) / VCCIN [%] When ID voltage is down |

7.Features

7-1.Pull down resistance detection in ID pin.

After power-on reset is released by applying a operating voltage to the VB, VC or VBAT pin, the IDRDET block is turned on and becomes ready for insertion detection by the 1.2-M Ω pull-up resistance. Insertion will be detected by connecting the pull-down resistance to the ID pin. Insertion will be detected also when an operating voltage is applied to the VB, VC or VBAT pin with the pull-down resistance connected to the ID pin

When AD conversion will be completed, the interrupt will be triggered.

7-1-1.Priority of MHLSW and ID detection.

When the signal path connecting the ID pin and the CBUS pin is turned on, all functions for detecting the resistance value of the ID pin are disabled.

7-1-2.Application with SEND/END switch detection.

When the detected value of the resistance connected to the ID pin is 797 k Ω , 557 k Ω , 287 k Ω , or 47 k Ω , the comparator COMPL for judging presses on the SEND/END switch will be turned on. By pressing the SEND/END switch of the application, "1" will be written to the register, and at the same time, an interrupt will be triggered at the INTB pin.

7-1-2-1.OTG Application Detection

When the detected value of the resistance connected to the ID pin is below 20 Ω , the OTG_DET pin will be driven to L assuming that a OTG device is detected and "1" will be written to Register.

7-1-2-2.MHL Application Detection

When the detected value of the resistance connected to the ID pin is 1K Ω , a MHL application is detected.

7-1-3.Enable for ID pin pull down resistance detection.

The function of detecting the value of the resistance connected to the ID pin is turned on in the initial state but can be turned on or off by changing the setting in the register.

7-1-4.Retry of ID detection sequence.

During the period from the detection of the value of the ID pin pull-down resistance to detection of removed application, a retry can be made to AD-convert the value of the ID pin pull-down resistance at any desired timing by changing the setting in the register.

7-1-5.Polling mode of ID detection sequence.

The LSI will enter polling mode, in which the resistance value of the ID pin will be repeatedly detected, an interrupt will trigger to the INTB pin only when both ID resistance or register will be updated.

7-1-6.Remove ID pin pull down resistance. (Application detachment)

Pull-out detection will occur if the pull-down resistance is disconnected from the ID pin with the comparator COMPH turned on. After detection of removed application, and an interrupt will be triggered at the INTB pin.

7-2.USB port detection.

When the voltage is normally applied to the VB pin and power-on reset is released, the USB port detection function will be turned on and automatically detect the circuit connected to the HDPR pin and to the HDML pin. The USB port detection function can identify a Standard Downstream Port (SDP), a Dedicated Charging Port (DCP), and a Charging Downstream Port (CDP) that are compliant with BCS Rev. 1.2. Ports, except for some dedicated chargers, are designed to be SDP detected according to BCS Rev. 1.2 in principle if they are incompliant with USB standards or BCS. When USB port detection will be completed, the interrupt will be triggered.

7-2-1.Data Contact Detect/DCD

In data contact detection, contact detection to USB data pin (D+) is performed via HDPR pin. USB data pin contact is completed or timed out, and then this LSI performs Primary detection.

7-2-2.Configuration of DCD time out.

The timeout period can be selected by the DCDMODE external pin.

7-2-3.Primary Detection

In the primary detection, the HDML pin will be compared to identify whether the type of the connection destination host port is a BCS-compliant Charging port or the port defined in USB 2.0.

7-2-4. Secondary Detection

In the secondary detection, to identify whether the type of the connection destination host port is a Dedicated Charging Port compliant with BCS1.2 (BCS-compliant dedicated charger) or a Charging Downstream Port (BCS-complaint charging port through which data can be communicated).

Whichever type of charging port is detected, the result will be stored in the register, and the CHG_DET pin will be driven to inform that a Charging port has been connected.

7-2-5.Shortening of second detection by Enumeration preparation

The second detection after primary is detected has already been shortened while judging the USB port when a portable device equipped with this LSI is possible Enumeration and CDP will be detected compulsorily.

7-2-6.Sequence Retrying.

After the completion of the USB port detection (SDPDET, CDPDET, or DCPDET in the state transition diagram), detection can be retried at any timing. Retries will not be accepted while USB port detection is operating.

7-2-7.Deactivation of USB port detection by External PIN and Internal Register.

The combination of the USBDISEN external pin and the USBDECTRL@02h register makes it possible to freely turn on or off the USB port detection function.

7-3.Signal paths

This LSI is capable of controlling the signal paths between the H DPR/HDML pins and the HDP1/HDM1, HDP2/HDM2,EARR/EARL, and MICOUT pins from the I2C interface. It is capable of controlling the signal path between the VB pin and the MICOUT pin as well.

For MHL transmission/USB transmission, use the path to HDP1/HDM1 or to HDP2/HDM2 enabling high-speed transmission. The signal paths to EARR/EARL and to MICOUT do not support high-speed signal transmission.

7-3-1.H DPR/HDML Signal paths

The H DPR pin has a signal path to each of the HDP1, HDP2, EARR, and MICOUT pins, whereas the HDML pin has a signal path to each of the HDM1, HDM2, and EARL pins.

7-3-2.Configuration of MUXSW initial path by DSS PIN.

The initially selected state of the signal paths can be controlled by the DSS pin. When the state of the DSS pin is "L," the signal path to the HDP1/HDM1 pin will be selected. When the state of the DSS pin is "H," the signal path to the HDP2/HDM2 pin will be selected.

7-3-3.Pull-down resistance in EARR/RARL pin.

A 500Ω pull-down resistance exists in the signal paths to the EARL pin and the EARR pin. The ON/OFF state of these resistances can be controlled independently by the register.

7-3-4.Signal path between ID pin and CBUS pin.

The ID pin has a signal path to the CBUS pin. The signal paths can be selected in the register.

7-4.Interrupt report with INTB pin.

This LSI reports such events as the completion of detection of the resistor connected to the ID pin and the completion of USB port detection to trigger as interrupt signals to the INTB pin. The INTB pin is of an Nch open drain structure, and the logic of an interrupt to be triggered is determined by the register. In the initial state, the INTB pin is set to be driven to L when an interrupt is triggered. The output of the pin is Hi-Z when there is no interrupt.

7-4-1.Active level selector of INTB.

The active level for interrupts can be selected in the register. In the initial state, the value in the register is "0," which drives the INTB pin to "L" at the time of the trigger of an interrupt. By writing "1" into the register, the INTB pin will open (Hi-Z) at the time of the trigger of an interrupt.

7-4-2.Interrupt polarity.

Interrupt polarity can be changed by writing register. In initial state INTB is droved with "L" when interrupt will be triggered.

7-5.Detection of Cradle and VBUS by VBDET pin and VCDET pin.

The application of a voltage from the VBUS or cradle can be detected using the VBDET pin or VCDET pin.

7-6.Detection of Cradle and VBUS by I2C interface reading.

The application of the voltage to the VBUS pin or cradle can be checked through the I2C interface by controlling of registers.

7-7.Detection of Over current state by I2C Interface reading.

This LSI has an independent OCP in each of the VB and VC power supply systems, and its over-current state can be detected by accessing it from the I2C interface.

7-8.Thermal Shut down.

If the junction temperature exceeds the set temperature, the thermal shutdown circuit will become activated and turn off the SW1 and SW2 of the OVP. The TSD detection temperature is 180°C, and the hysteresis temperature for recovery is 10°C.

7-9.VBREG Regulator.

This LSI has a regulator driven by the VBUS voltage. The output from the regulator can be turned on by the VBREG pin in the default state by increasing the voltage of the VB pin to UVLO or a higher level. The VBREG output pin is available for external applications, and two output voltage levels can be selected by LDOSEL pin.

7-10.OTG mode control

To permit power supply from a portable device in the On-The-Go mode of USB2.0, this LSI has an independent power path from the OTG_VIN pin to the VB pin.

7-11.VBUS signal path.

This LSI can select the signal path from the VB pin to the MICOUT pin. By setting "1" in the register with UVLO applied to the VB pin, the VB pin and the MICOUT pin will be connected to each other. These pins will be disconnected by setting "0" in the register.

7-12.Reset systems

This LSI has three reset modes - "power-on reset," "hardware reset," and "software reset." Any resets initialize all functions include all registers.

7-12-1.Power-On Reset

Power-on reset initializes all of the functions of this LSI. When VCCIN is supplied, power-on reset will be automatically released as the UVLO of the VB, VC, or VBAT pin is cleared.

7-12-2.Hardware Reset with RST.

A hardware reset is triggered by external pin RST and can reset all of the functions of this LSI. RST is an H enable pin. It triggers a reset when a voltage within the VIH voltage range is applied to the RST pin, and releases the reset when a voltage within the VIL voltage range is applied to the RST pin.

7-12-3.Software reset from I2C Interface writing.

A software reset can be executed by writing "1" into register from the I2C interface. A software reset can initialize all of the functions of this LSI.

7-13.I²C Interface electrical characteristics.

AC Characteristics on I²C Bus.

| Characteristics | Sign | Min | Max | Unit |
|----------------------------|---------------------|-----|-----|------|
| CLK clock frequency | f _{CLK} | 0 | 400 | kHz |
| CLK clock "low" time | t _{LOW} | 1.3 | - | μs |
| CLK clock "high" time | t _{HIGH} | 0.6 | - | μs |
| Bus free time | t _{BUF} | 1.3 | - | μs |
| Start condition hold time | t _{HD,STA} | 0.6 | - | μs |
| Start condition setup time | t _{SU,STA} | 0.6 | - | μs |
| Data input hold time | t _{HD,DAT} | 0 | 0.9 | μs |
| Data input setup time | t _{SU,DAT} | 100 | - | ns |
| Stop condition setup time | t _{SU,STO} | 0.6 | - | μs |

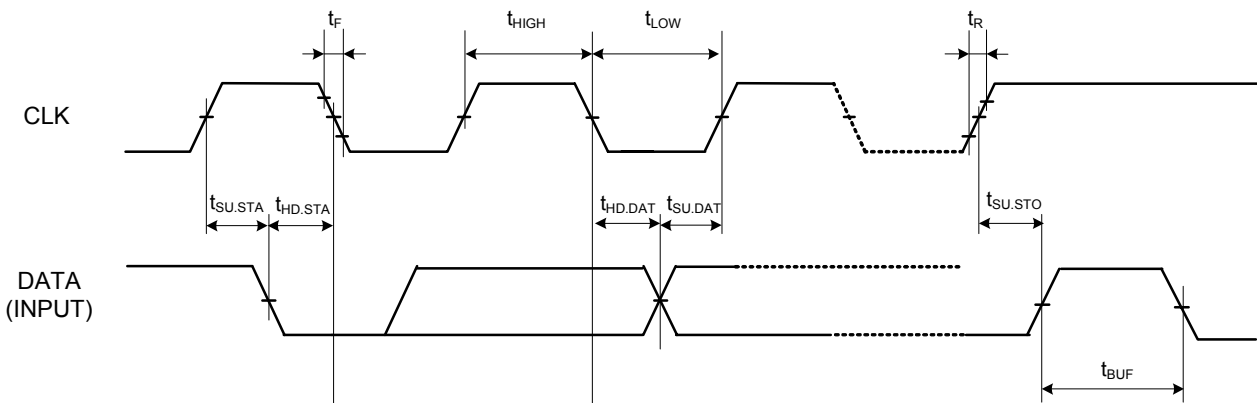


Fig 1. SCL/SDA bus AC Timing 1

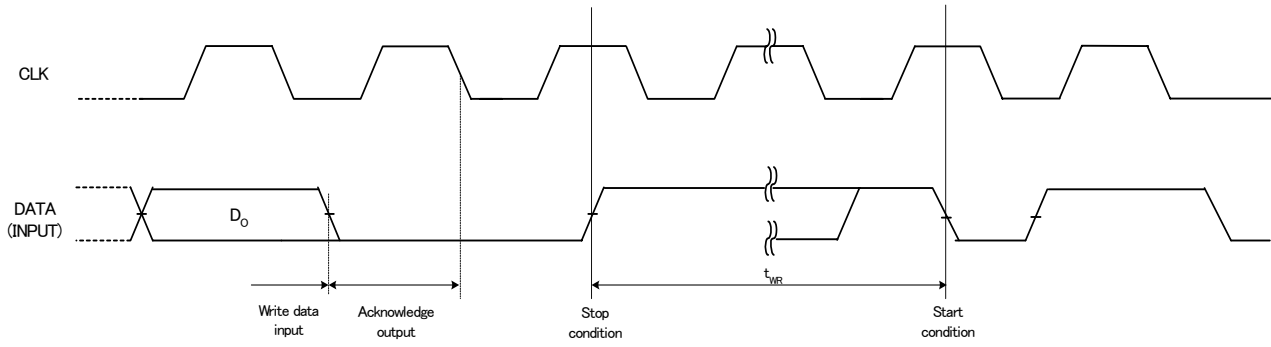


Fig 2. SCL/SDA bus AC Timing 2

7-14. I²C Bus Interface

7-14-1. START and STOP Conditions

When CLK is set at "H" and DATA is changed from "H" and "L," a start condition will be established, and access will begin. By setting changing SDA from "L" to "H" with CLK set at "H," a stop condition will be satisfied, and access will be terminated. All commands begin with a start condition and stop with a stop condition. If a stop condition is generated in the middle of reading, reading will be discontinued, and the application will enter standby mode. If a stop condition is generated in the middle of writing, writing will be suspended until the next start condition, and the application will enter standby mode.

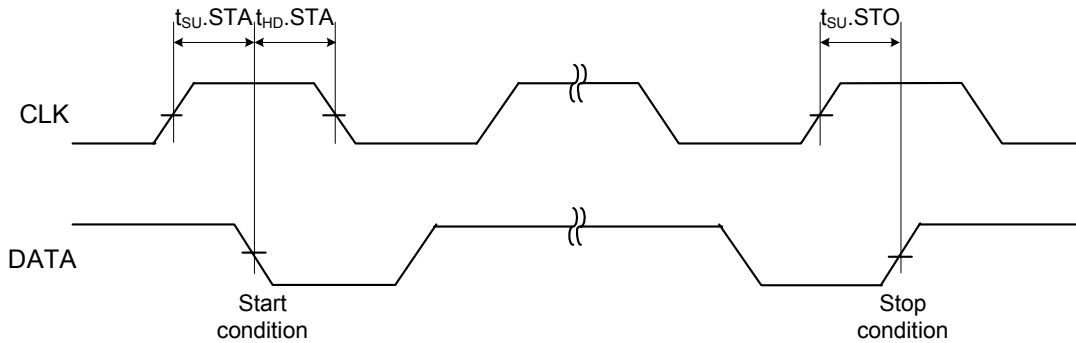


Fig. 3. START and STOP Condition AC Timing.

7-14-2. Modifying Data

One-bit data is transferred while SCL is "H". During bit data transfer, the signal transition of SDA cannot be executed while CL is "H". When SCL is "H" and SDA changes, a start condition or stop condition will be generated and interpreted as a control signal.

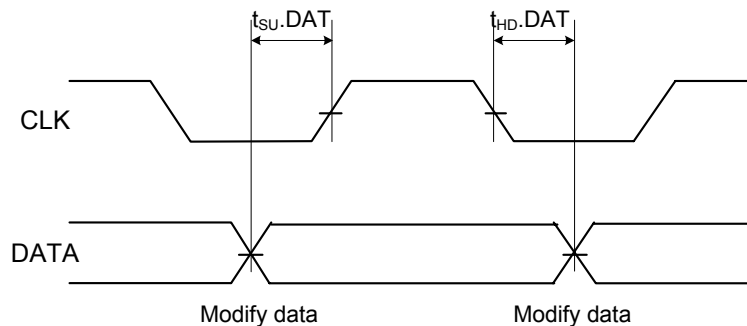


Fig 4. Data transfer AC Timing.

7-14-3.Acknowledge

After a start condition is generated, data will be transferred in eight-bit blocks. After data transfer in eight-bit blocks, the transmitter opens SDA in the ninth cycle, and the receiver returns an acknowledge signal in the ninth cycle by changing SDA to "L." The data is thereby received in a proper manner.

During writing, the receiver returns an acknowledge signal each time it receives eight-bit data, and the transmitter receives the signal.

During reading, the transmitter returns an acknowledge signal after it receives an address following a start condition. The transmitter then receives read data and opens the bus to wait for an acknowledge signal from the receiver. When an acknowledge signal is detected, the receiver outputs the next address data unless a stop condition is generated. Unless acknowledge signal is detected or stop condition is generated, the receiver does not enter standby mode. The bus is kept open until an acknowledge signal or stop condition is detected.

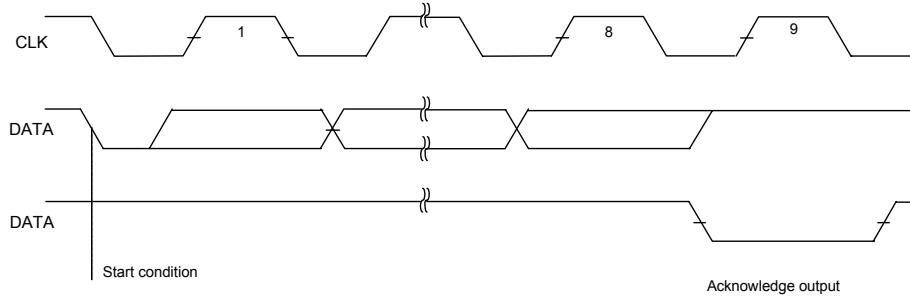
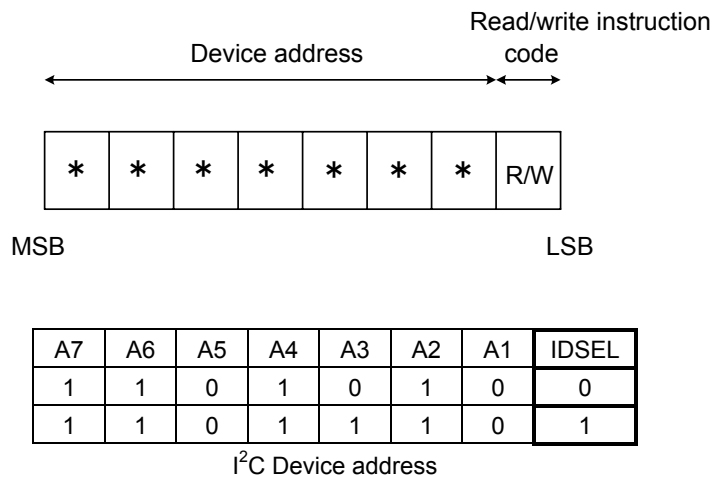


Fig 5. Acknowledge AC Timing.

7-14-4.Device Address

After a start condition is generated, a seven-bit device address and the a one-bit read/write command selection bit will be input. The device address is "1101110" when IDSEL is "H" (VCCIN short), or "1101010" when IDSEL is "L" (GND short). A one-bit (R/E READ/WRITE) signal becomes a read command when it is set at "1," or a write command when it is set at "0." If the device address does not match, the command will not be executed.



7-14-5. Write operation

To write data to the designated address, input the device address, the one-bit signal of "0" (R/W command selection bit), the word address, and the data to be written after the start condition.

The application enters standby mode upon generation of a stop condition.

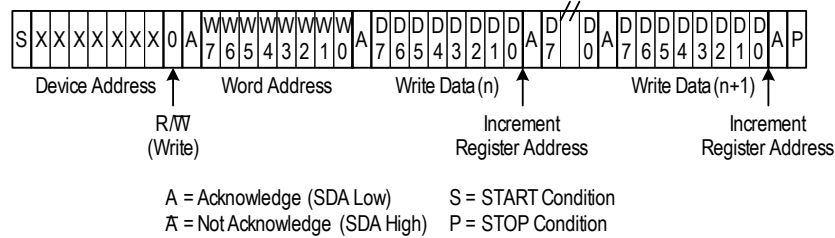


Fig 6. Write protocol sequence.

Write a start condition, a device address, a one-bit signal of "0" (R/W command selection bit), a word address (n), and address (n + 1) data. The acknowledge signal will become "0" or be checked unless a stop condition is generated.

7-14-6. Address roll back specification.

Write, read, and complex read will perform, and the word address will be rolled over by address 00h when the address reaches 07h.

7-14-7. Read back operation.

When reading data from the designated address, the data to be read will be output by writing a device address, a one-bit signal of "0" (R/W command selection bit), and a word address after a start condition and then inputting a start condition, a device address, and a one-bit signal of "1" (R/W command selection bit).

The bus opens with a stop condition.

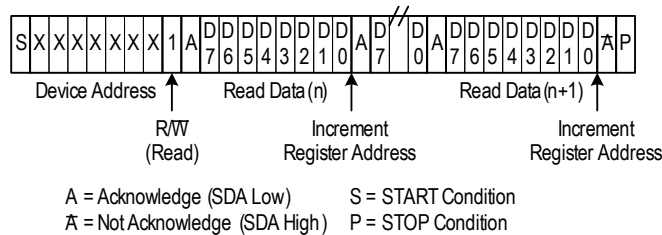


Fig 7 Read back protocol sequence.

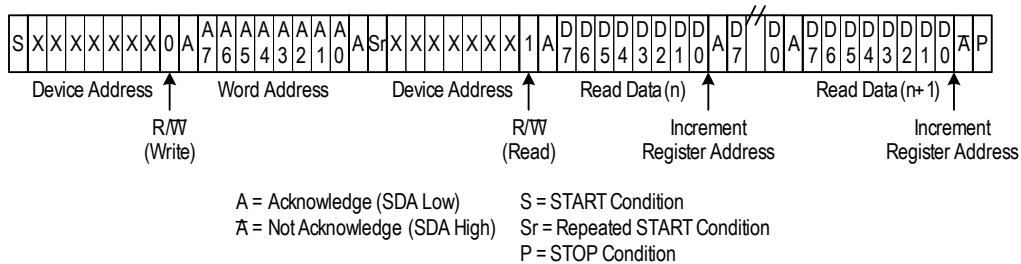


Fig 8. Complex read back protocol sequence.

Complex read back a start condition, a device address, a one-bit signal of "0" (R/W command selection bit), a word address (n), and address (n + 1) data. The acknowledge signal will become "0" or be checked unless a stop condition is generated.

8. Typical Performance Curves

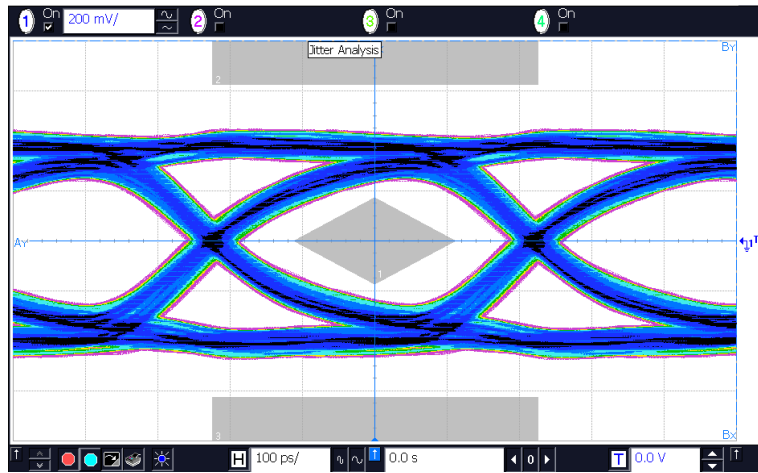


Fig12.MHL Eye-Pattern(720p, 60Hz)

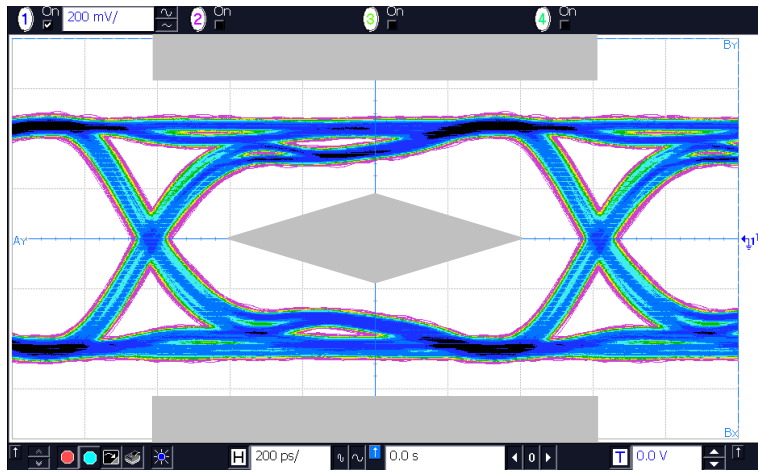


Fig13.MHL Eye-Pattern(480p, 60Hz)

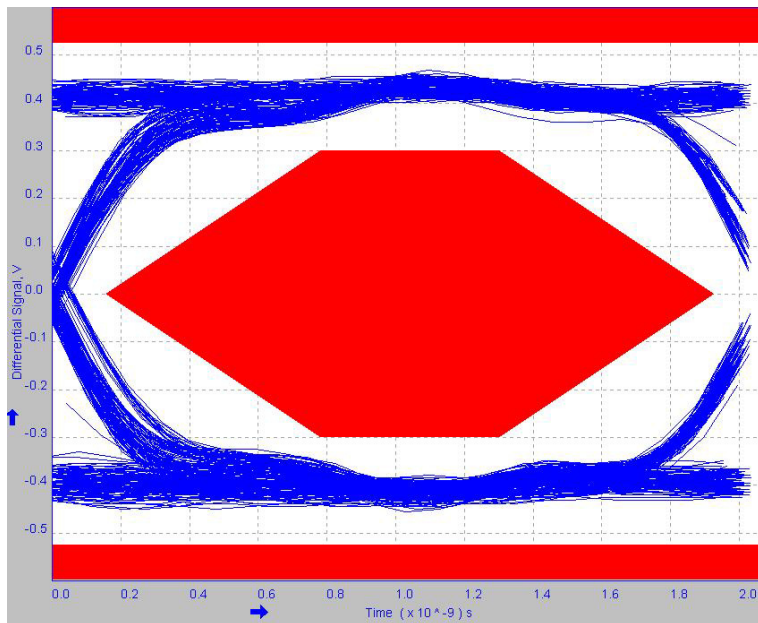


Fig14.USB Eye-Pattern(High-speed)

9.Application Circuit Diagram

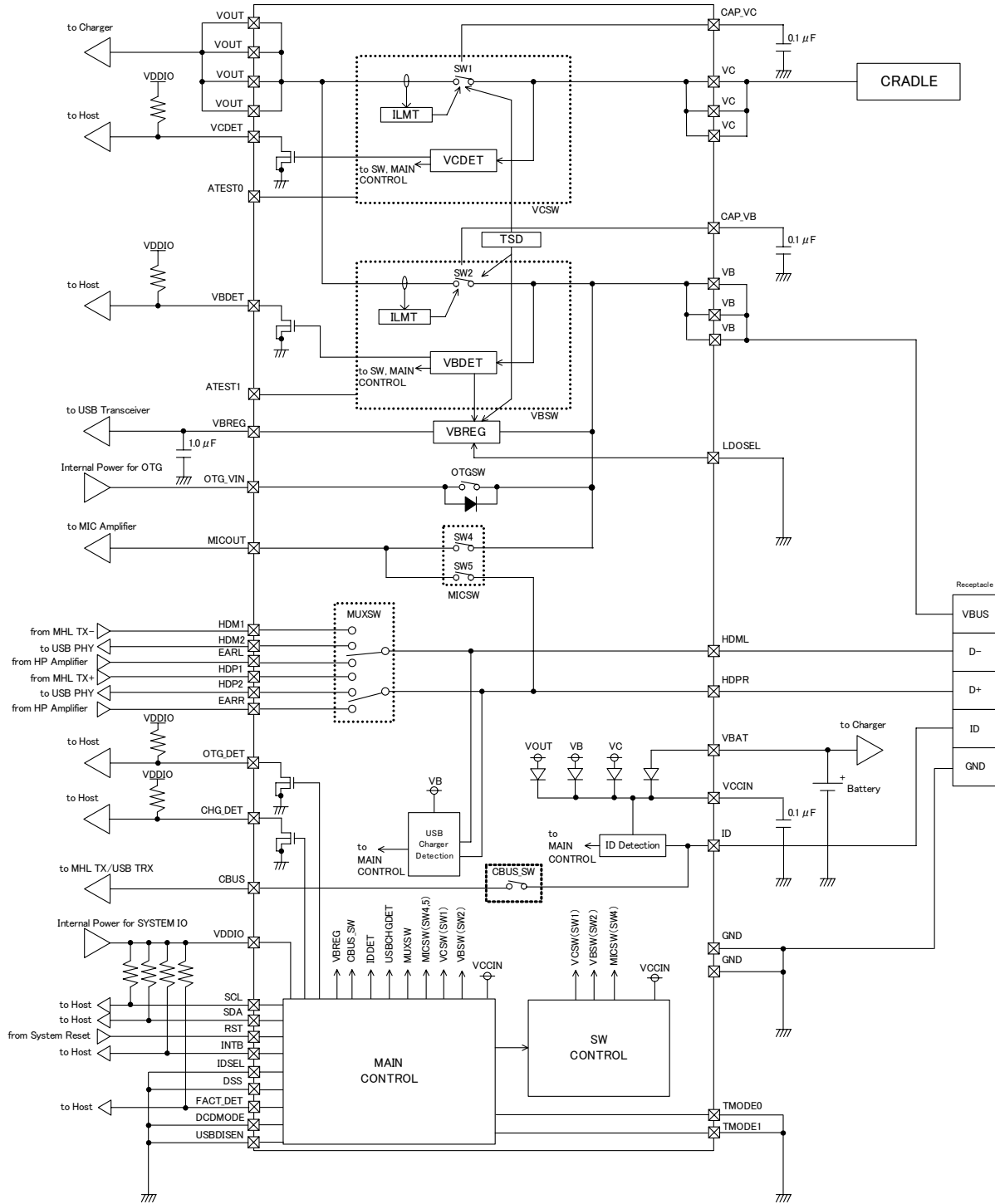
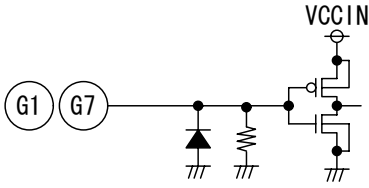
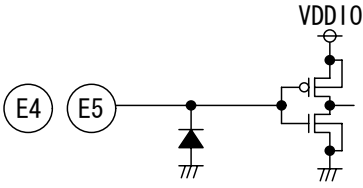
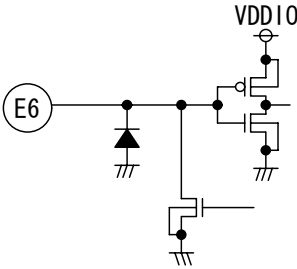
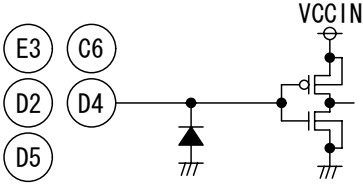
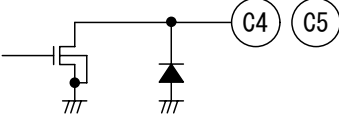


Fig.15 Application Circuit Diagram

10. I/O equivalence circuits

| Ball No. | Ball Name | I/O equivalence circuits |
|----------------------------|--|--|
| G1 G7 | TMODE0 TMODE1 |  |
| E4 E5 | RST SCL |  |
| E6 | SDA |  |
| E3 C6 D2 D4 D5 | DSS IDSEL LDOSEL USB1SEN DCDMODE |  |
| C4 C5 | VCDET VBDET |  |

| Ball No. | Ball Name | I/O equivalence circuits |
|---|--|--------------------------|
| <p>B6 B7 C7 A6 A4 A5 B4 B5 A2 A3 B2 B3 B1</p> | <p>VC VC VC CAP_VC VOUT VOUT VOUT VOUT VB VB VB CAP_VB OTG_VIN</p> | |
| <p>E2</p> | <p>MICOUT</p> | |
| <p>E1 F1</p> | <p>HDPR HDML</p> | |

| Ball No. | Ball Name | I/O equivalence circuits |
|----------|------------------|--------------------------|
| F6 | VCCIN | |
| C1 | VBREG | |
| F5 | CBUS | |
| A7 A1 | ATEST1 ATEST0 | |
| E7 F7 | VBAT VDDIO | |

| Ball No. | Ball Name | I/O equivalence circuits |
|----------------------|--|--------------------------|
| G2 G3 | HDM1 HDP1 | |
| G4 G5 | EARL EARR | |
| F2 F3 | HDM2 HDP2 | |
| D6 F4 D3 C2 | INTB FACT_DET CHG_DET OTG_DET | |
| G6 | ID | |

11. Operational Notes

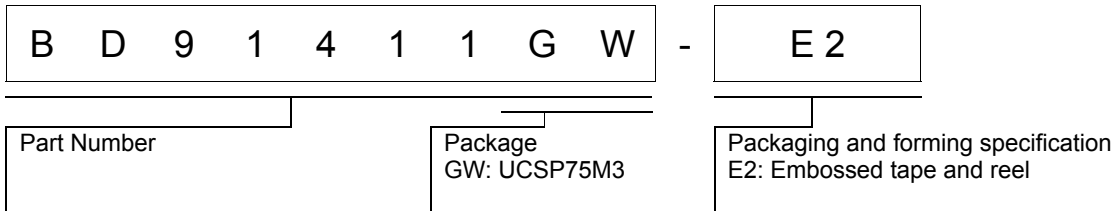
- 1) Absolute maximum ratings
If applied voltage, operating temperature range (Topr), or other absolute maximum ratings are exceeded, there is a risk of damage. Since it is not possible to identify short, open, or other damage modes, if special modes in which absolute maximum ratings are exceeded are assumed, consider applying fuses or other physical safety measures.
- 2) Recommended operating range
This is the range within which it is possible to obtain roughly the expected characteristics. For electrical characteristics, it is those that are guaranteed under the conditions for each parameter. Even when these are within the recommended operating range, voltage and temperature characteristics are indicated.
- 3) Reverse connection of power supply connector.
There is a risk of damaging the LSI by reverse connection of the power supply connector. For protection from reverse connection, take measures such as externally placing a diode between the power supply and the power supply pin of the LSI.
- 4) Power supply lines
In the design of the board pattern, make power supply and GND line wiring low impedance. When doing so, although the digital power supply and analog power supply are the same potential, separate the digital power supply pattern and analog power supply pattern to deter digital noise from entering the analog power supply due to the common impedance of the wiring patterns. Similarly take pattern design into account for GND lines as well. Furthermore, for all power supply pins of the LSI, in conjunction with inserting capacitors between power supply and GND pins, when using electrolytic capacitors, determine constants upon adequately confirming that capacitance loss occurring at low temperatures is not a problem for various characteristics of the capacitors used.
- 5) GND voltage
About the pins except for EARR, EARL, DPRXR and DMTXL, make the potential of a GND pin such that it will be the lowest potential even if operating below that. In addition, confirm that there are no pins for which the potential becomes less than a GND by actually including transition phenomena.
- 6) Shorts between pins and miss assemble
When assemble in the set board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is assembled erroneously, there is a risk of LSI damage. There also is a risk of damage if a foreign substance getting between pins or between a pin and a power supply or GND shorts it.
- 7) Operation in strong magnetic fields
Be careful when using the LSI in a strong magnetic field, since it may malfunction.
- 8) Inspection in set board
When inspecting the LSI in the set board, since there is a risk of stress to the LSI when capacitors are connected to low impedance LSI pins, be sure to discharge for each process. Moreover, when getting it on and off of a jig in the inspection process, always connect it after turning off the power supply, perform the inspection, and remove it after turning off the power supply. Furthermore, as countermeasures against static electricity, use grounding in the assembly process and take appropriate care in transport and storage.
- 9) Input pins
Parasitic elements inevitably are formed on a LSI structure due to potential relationships. Because parasitic elements operate, they give rise to interference with circuit operation and may be the cause of malfunctions as well as damage. Accordingly, take care not to apply a lower voltage than GND to an input pin or use the LSI in other ways such that parasitic elements operate. Moreover, do not apply a voltage to an input pin when the power supply voltage is not being applied to the LSI. Furthermore, when the power supply voltage is being applied, make each input pin a voltage less than the power supply voltage as well as within the guaranteed values of electrical characteristics.
- 10) Ground wiring pattern
When there is a small signal GND and a large current GND, it is recommended that you separate the large current GND pattern and small signal GND pattern and provide single point grounding at the reference point of the set so that voltage variation due to resistance components of the pattern wiring and large currents do not cause the small signal GND voltage to change. Take care that the GND wiring pattern of externally attached components also does not change.
- 11) Externally attached capacitors
When using ceramic capacitors for externally attached capacitors, determine constants upon taking into account a lowering of the rated capacitance due to DC bias and capacitance change due to factors such as temperature.
- 12) Thermal shutdown circuit (TSD)
When junction temperatures become 180°C (typ) or higher, the thermal shutdown circuit operates and turns OVP switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.
- 13) Thermal design
Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

Status of this document

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

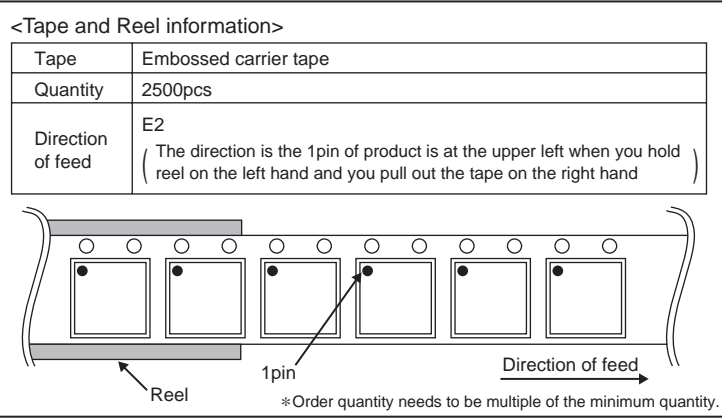
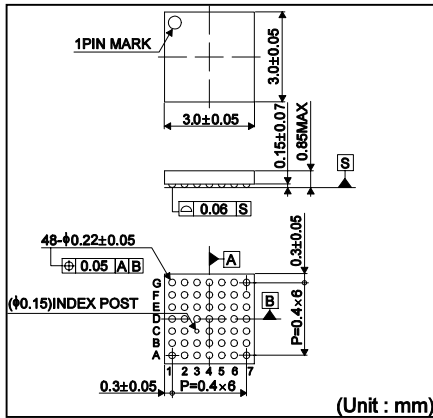
If there are any differences in translation version of this document formal version takes priority

12. Ordering Information



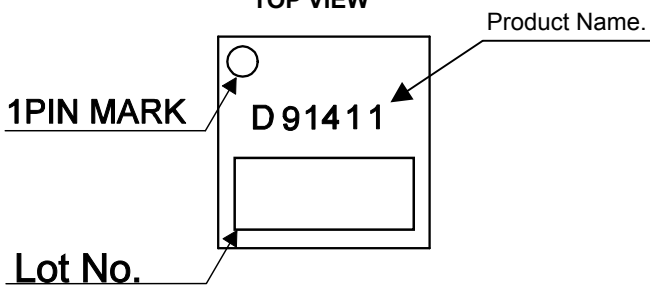
13. Physical Dimension Tape and Reel Information

UCSP75M3(BD91411GW)



14. Marking Diagram

UCSP75M3(BD91411GW)
TOP VIEW



15.Revision History

| Date | Revision | Changes |
|-------------|----------|-------------|
| 13.Jul.2012 | 001 | New Release |

Notice

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 - [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure
- 3) Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc. prior to use, must be necessary:
 - [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
 - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
- 4) The Products are not subject to radiation-proof design.
- 5) Please verify and confirm characteristics of the final or mounted products in using the Products.
- 6) In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse) is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- 7) De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- 8) Confirm that operation temperature is within the specified range described in the product specification.
- 9) ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

● **Precaution for Mounting / Circuit board design**

- 1) When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- 2) In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

● **Precautions Regarding Application Examples and External Circuits**

- 1) If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
- 2) You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

● **Precaution for Electrostatic**

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

● **Precaution for Storage / Transportation**

- 1) Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
- 2) Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
- 3) Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
- 4) Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

● **Precaution for Product Label**

QR code printed on ROHM Products label is for ROHM's internal use only.

● **Precaution for Disposition**

When disposing Products please dispose them properly using an authorized industry waste company.

● **Precaution for Foreign Exchange and Foreign Trade act**

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

● **Precaution Regarding Intellectual Property Rights**

- 1) All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data. ROHM shall not be in any way responsible or liable for infringement of any intellectual property rights or other damages arising from use of such information or data.:
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●Other Precaution

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