OptiMOS® Power-Transistor

Features

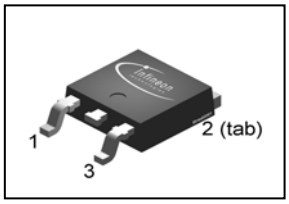
- For fast switching converters and sync. rectification
- N-channel enhancement - logic level
- 175 °C operating temperature
- Avalanche rated
- Pb-free lead plating, RoHS compliant

RoHS

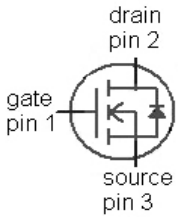
Product Summary

V_{DS}	60	V
$R_{DS(on),max}$	12.7	mΩ
I_D	50	A

PG-TO252-3



Type	IPD127N06L G
	
Package	PG-TO252-3
Marking	127N06L



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C[1)]	50	A
		T_C=100 °C	48	
Pulsed drain current	$I_{D,pulse}$	T_C=25 °C[2)]	200	
Avalanche energy, single pulse	E_{AS}	I_D=50 A, R_{GS}=25 Ω	240	mJ
Reverse diode dv/dt	dv/dt	I_D=50 A, V_{DS}=48 V, di/dt=200 A/µs, $T_{j,max}$=175 °C	6	kV/µs
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	136	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

[1)] Current is limited by bondwire; with an R_{thJC}=1.1 K/W the chip is able to carry 64 A.

[2)] See figure 3

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	1.1	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	75	
		6 cm^2 cooling area[3)]	-	-	50	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	60	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=80 µA	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C	-	0.01	1	µA
		V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C	-	1	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=33 A	-	12.5	16.7	mΩ
		V_{GS}=10 V, I_D=50 A	-	10.0	12.7	
Gate resistance	R_G		-	1.5	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=50 A	35	69	-	S

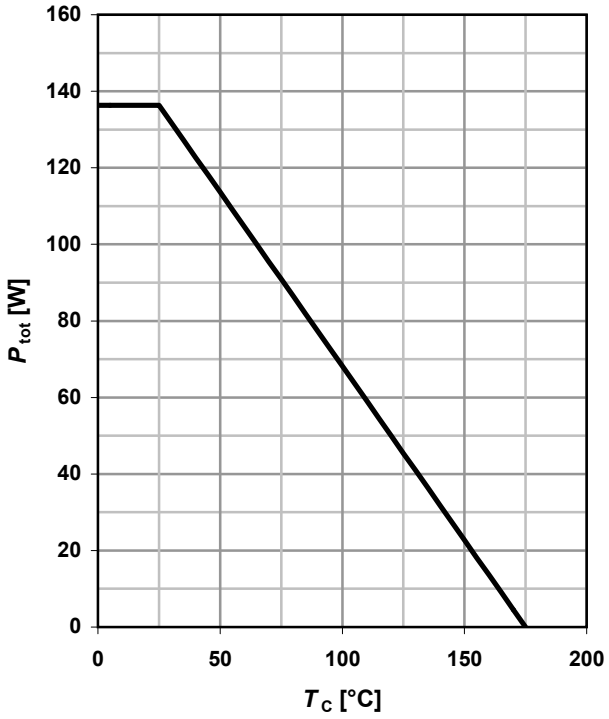
[3)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz	-	1700	2300	pF
Output capacitance	C_{oss}		-	410	550	
Reverse transfer capacitance	C_{rss}		-	110	165	
Turn-on delay time	$t_{d(on)}$	V_{DD}=30 V, V_{GS}=10 V, I_D=50 A, R_G=3.6 Ω	-	9	13	ns
Rise time	t_r		-	14	21	
Turn-off delay time	$t_{d(off)}$		-	39	58	
Fall time	t_f		-	13	21	
Gate Charge Characteristics[4)]						
Gate to source charge	Q_{gs}	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 10 V	-	6	9	nC
Gate charge at threshold	$Q_{g(th)}$		-	3	4	
Gate to drain charge	Q_{gd}		-	17	26	
Switching charge	Q_{sw}		-	21	31	
Gate charge total	Q_g		-	52	69	
Gate plateau voltage	$V_{plateau}$		-	3.7	-	V
Output charge	Q_{oss}	V_{DD}=30 V, V_{GS}=0 V	-	16	21	
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	50	A
Diode pulse current	$I_{S,pulse}$		-	-	200	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=50 A, T_j=25 °C	-	0.93	1.3	V
Reverse recovery time	t_{rr}	V_R=30 V, I_F=I_S, di_F/dt=100 A/µs	-	52	65	ns
Reverse recovery charge	Q_{rr}		-	99	125	nC

[4)] See figure 16 for gate charge parameter definition

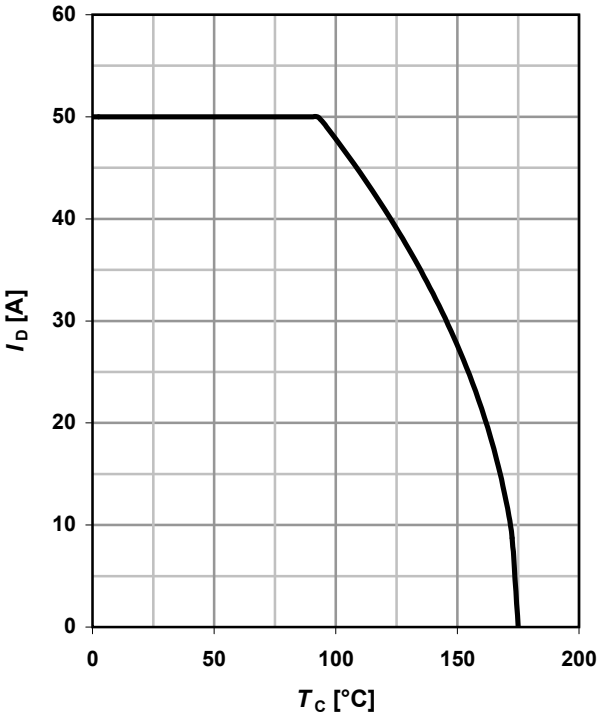
1 Power dissipation

$P_{tot}=f(T_C)$; $V_{GS}\geq 6$ V



2 Drain current

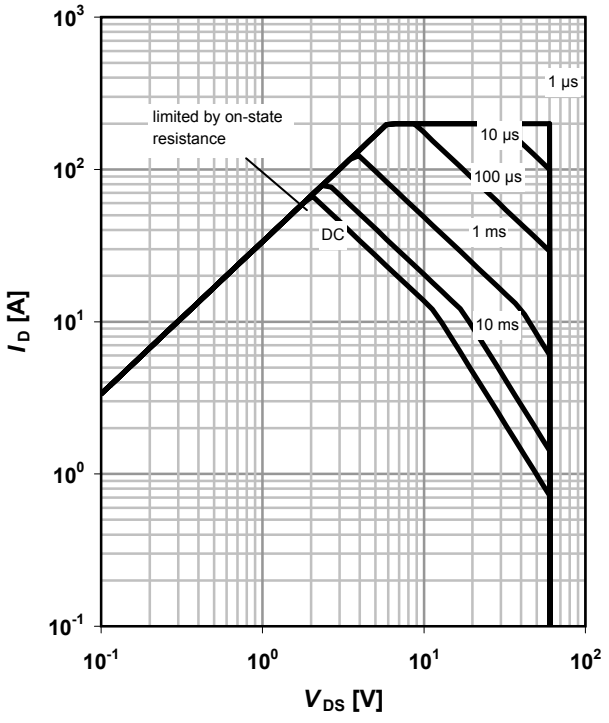
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

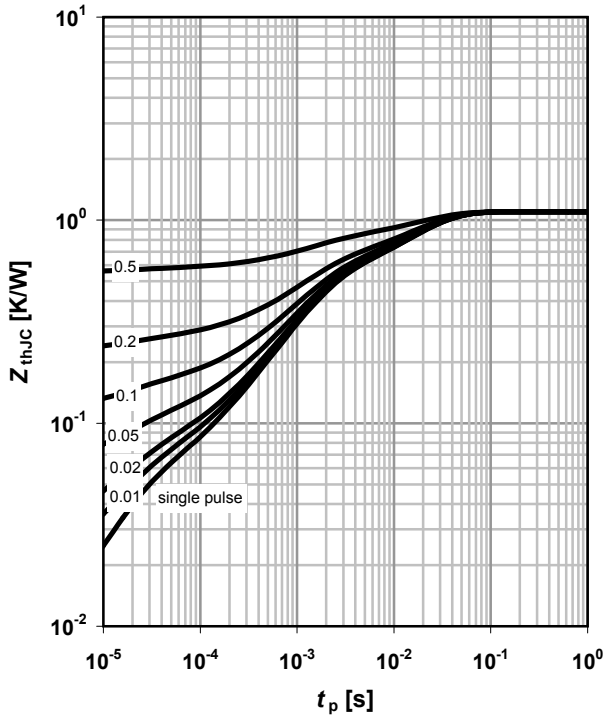
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

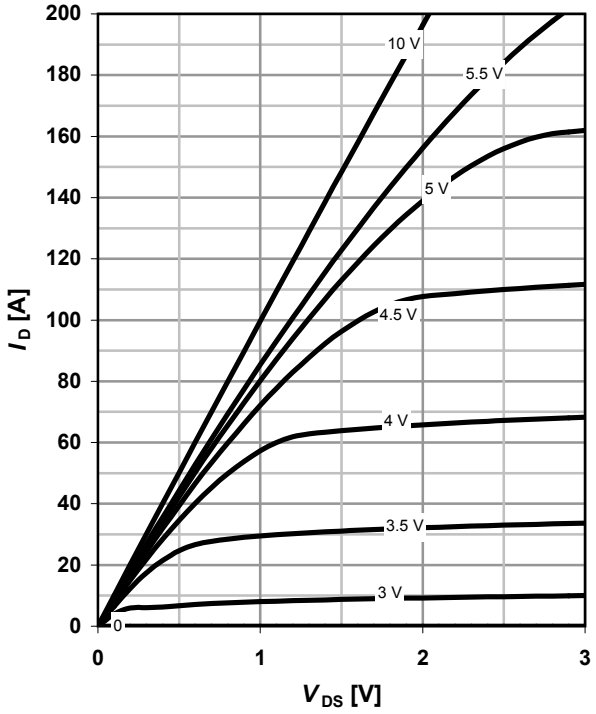
parameter: $D=t_p/T$



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

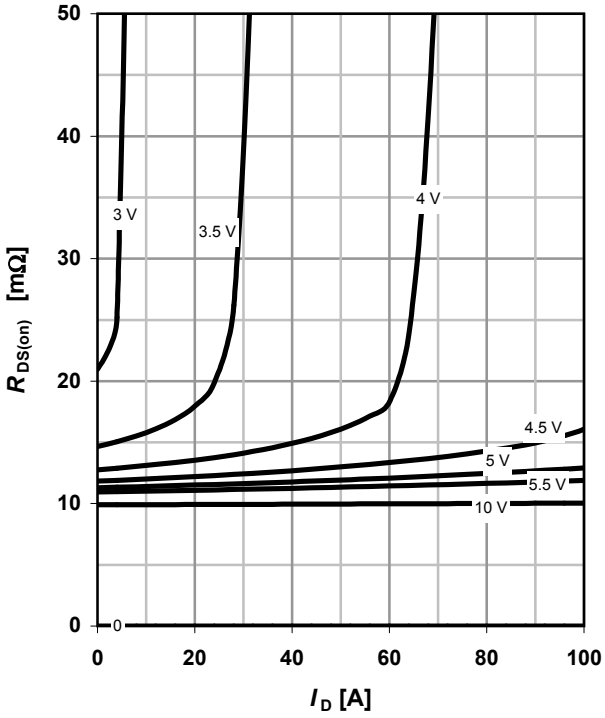
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

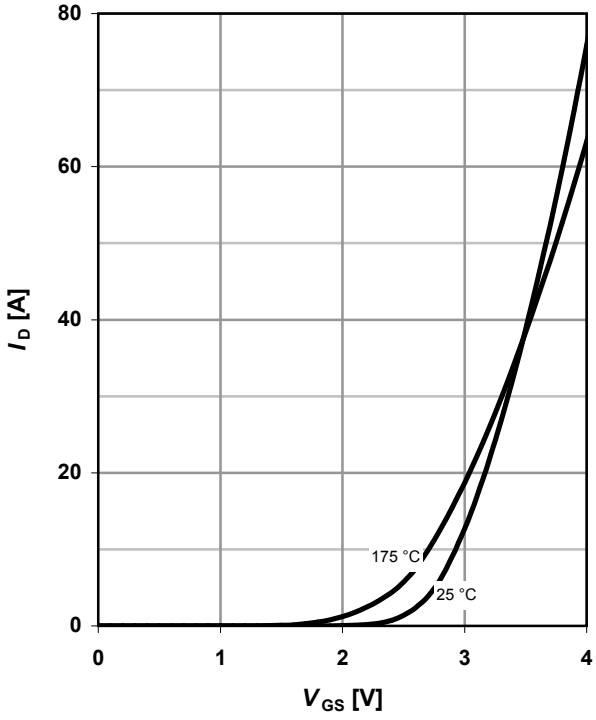
parameter: V_{GS}



7 Typ. transfer characteristics

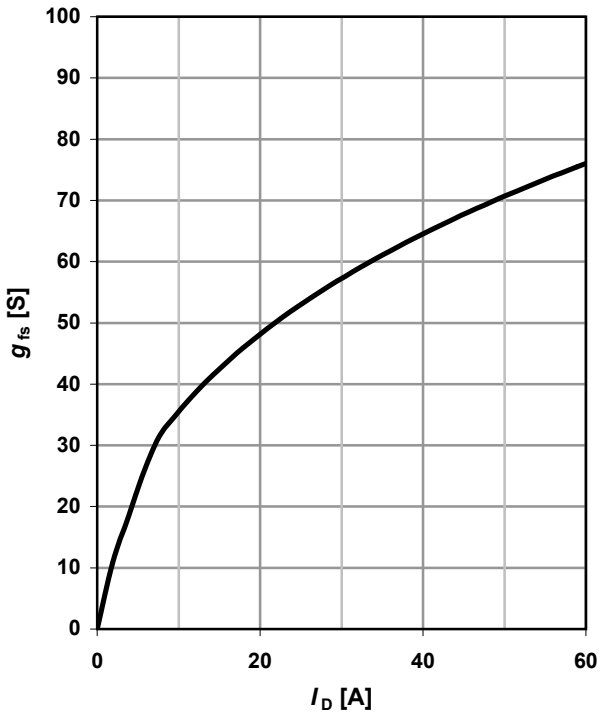
I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



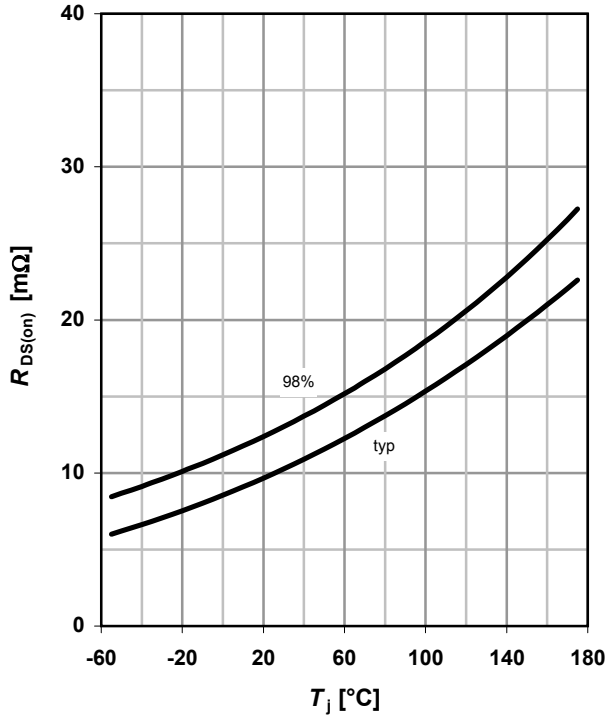
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



9 Drain-source on-state resistance

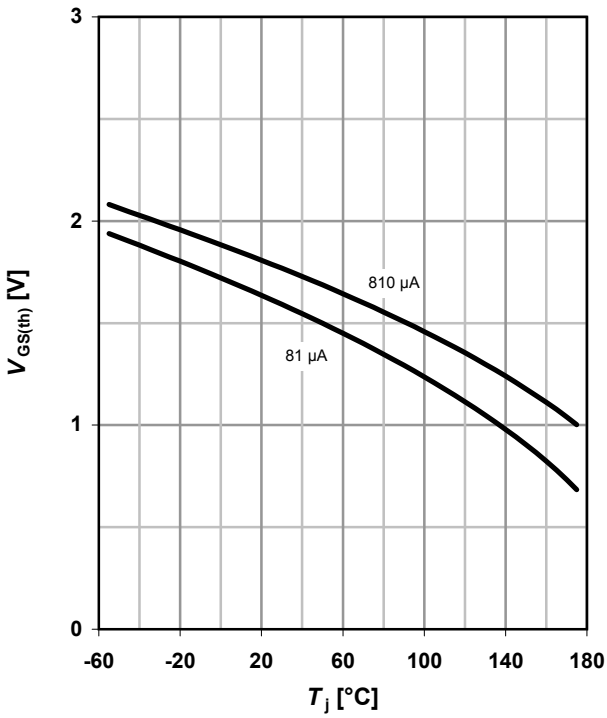
$R_{DS(on)}$=f(T_j); I_D=50 A; V_{GS}=10 V



10 Typ. gate threshold voltage

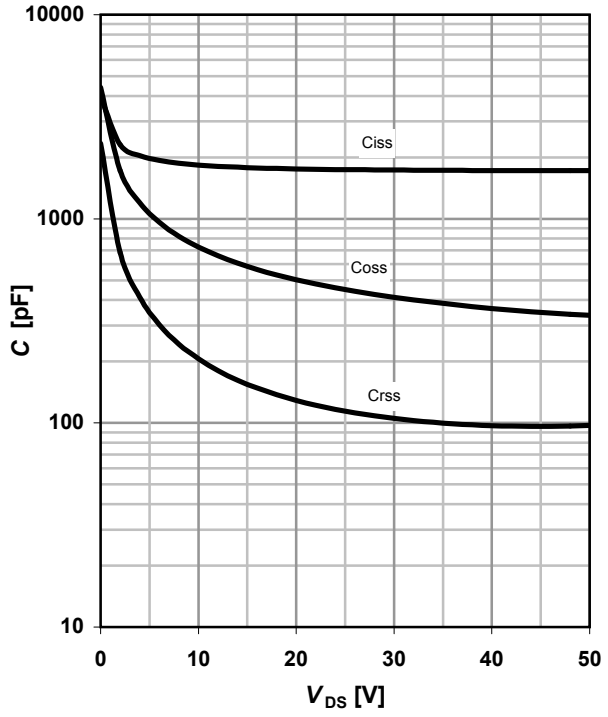
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}

parameter: I_D



11 Typ. capacitances

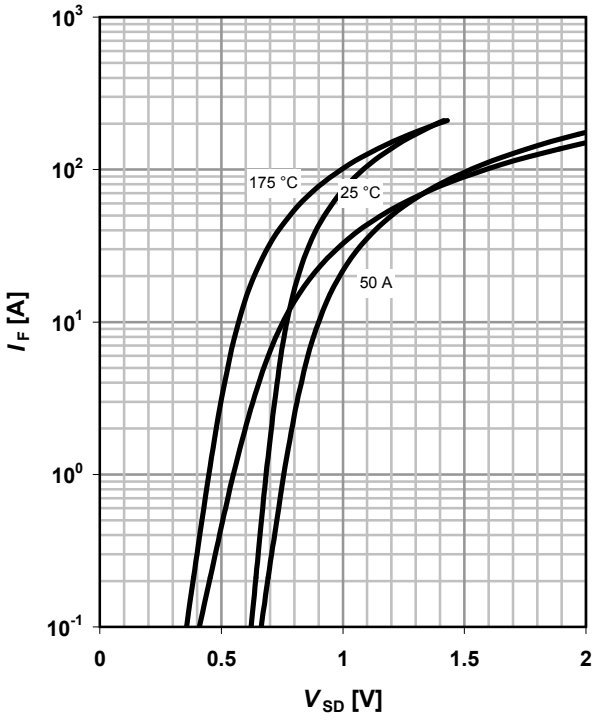
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

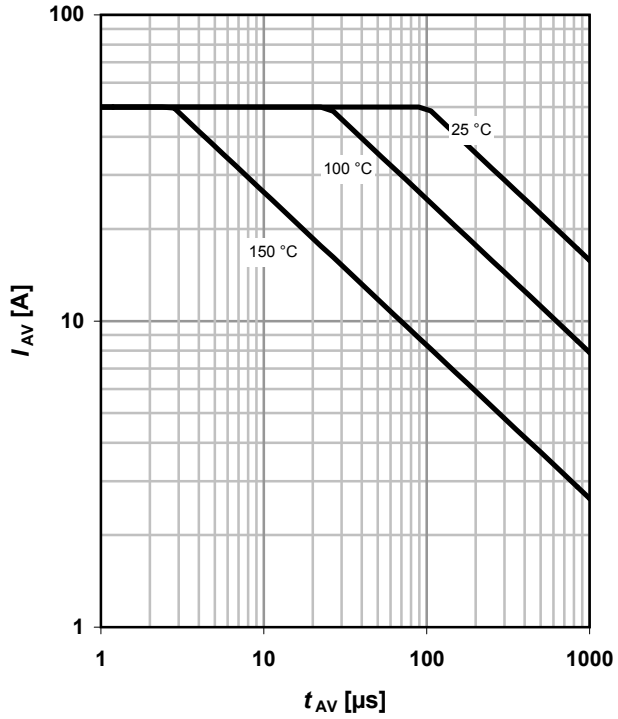
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

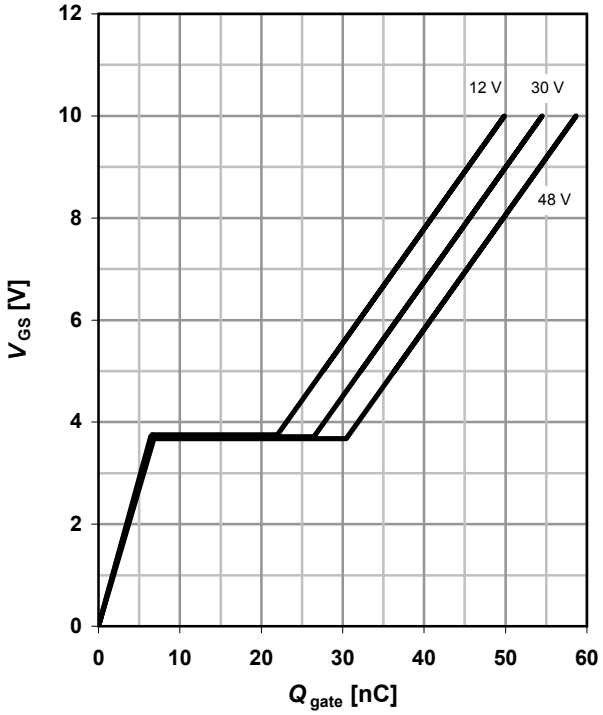
parameter: $T_{j(start)}$



14 Typ. gate charge

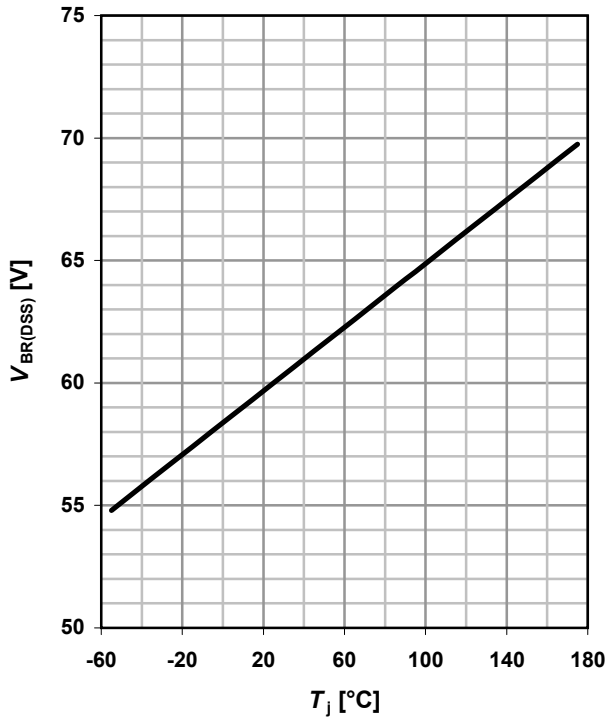
V_{GS}=f(Q_{gate}); I_D=50 A pulsed

parameter: V_{DD}

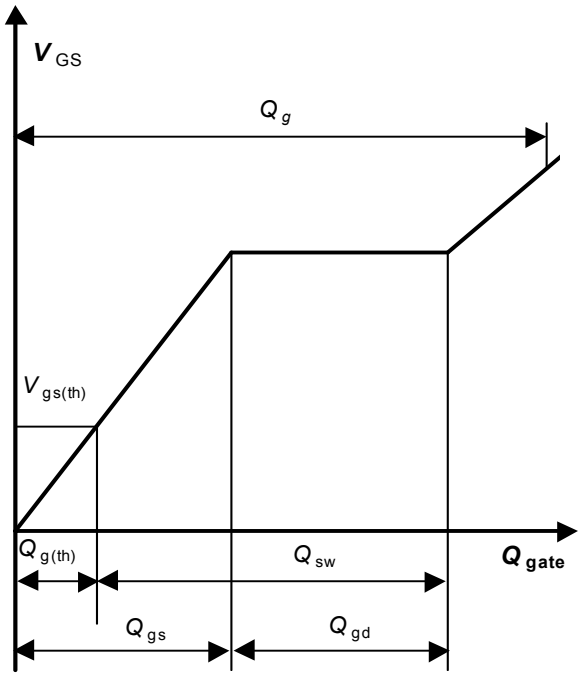


15 Drain-source breakdown voltage

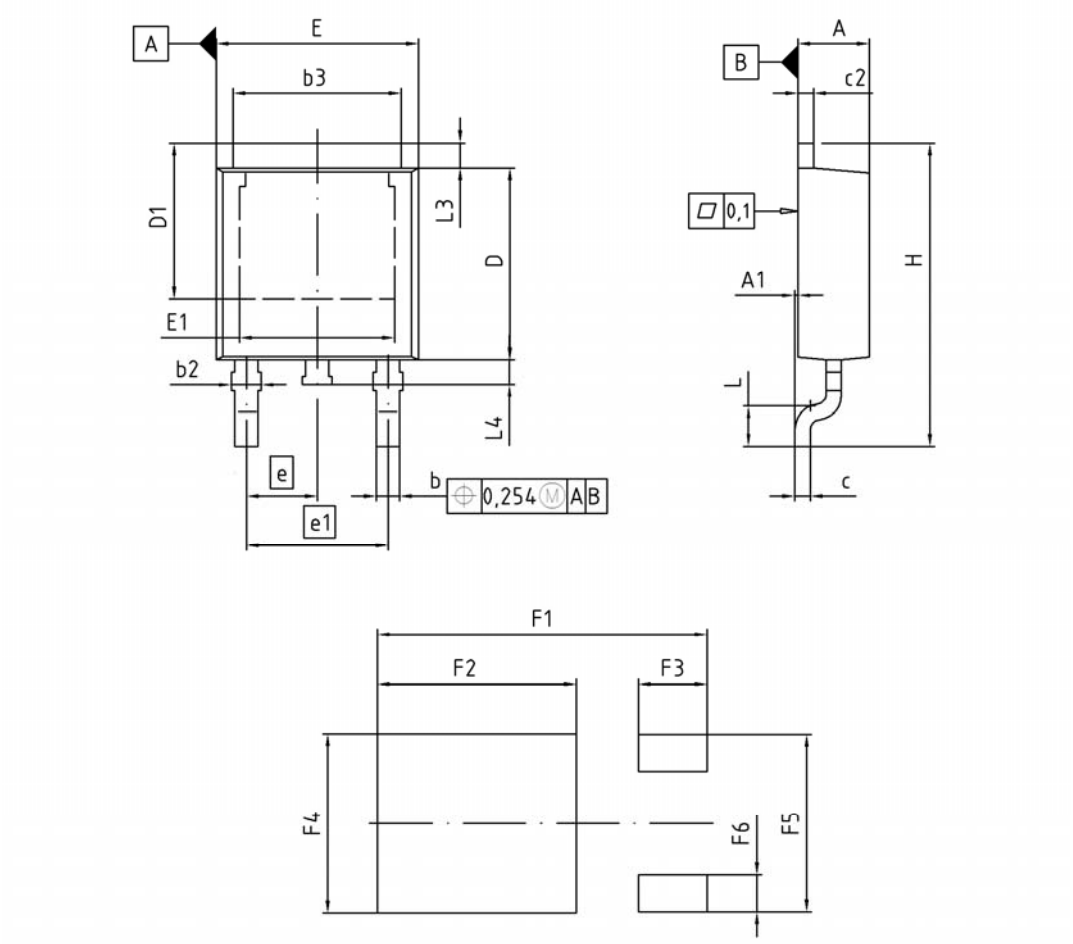
$V_{BR(DSS)}$=f(T_j); I_D=1 mA



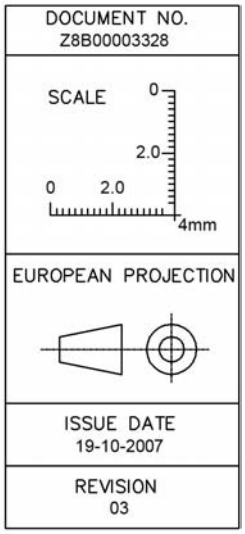
16 Gate charge waveforms



PG-TO252-3: Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.21	0.185	0.205
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.50	10.70	0.413	0.421
F2	6.30	6.50	0.248	0.256
F3	2.10	2.30	0.083	0.091
F4	5.70	5.90	0.224	0.232
F5	5.66	5.86	0.223	0.231
F6	1.10	1.30	0.043	0.051



Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information
For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings
Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.
Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.