SX Family FPGAs RadTolerant and HiRel

Features

RadTolerant SX Family

- Tested Total Ionizing Dose (TID) Survivability Level
- Radiation Performance to 100 Krads (Si) (I_{CC} Standby Parametric)
- Devices Available from Tested Pedigreed Lots
- Up to 160 MHz On-Chip Performance
- Offered as Class B and E-Flow (Actel Space Level Flow)
- QMl Certified Devices

HiRel SX Family

- Fastest HiRel FPGA Family Available
- Up to 240 MHz On-Chip Performance
- Low Cost Prototyping Vehicle for RadTolerant Devices
- Offered as Commercial or Military Temperature Tested and Class B
- Cost Effective QML MIL-Temp Plastic Packaging Options
- Standard Hermetic Packaging Offerings
- QML Certified Devices

High Density Devices

- 16,000 and 32,000 Available Logic Gates
- Up to 225 User I/Os
- Up to 1,080 Dedicated Flip-Flops

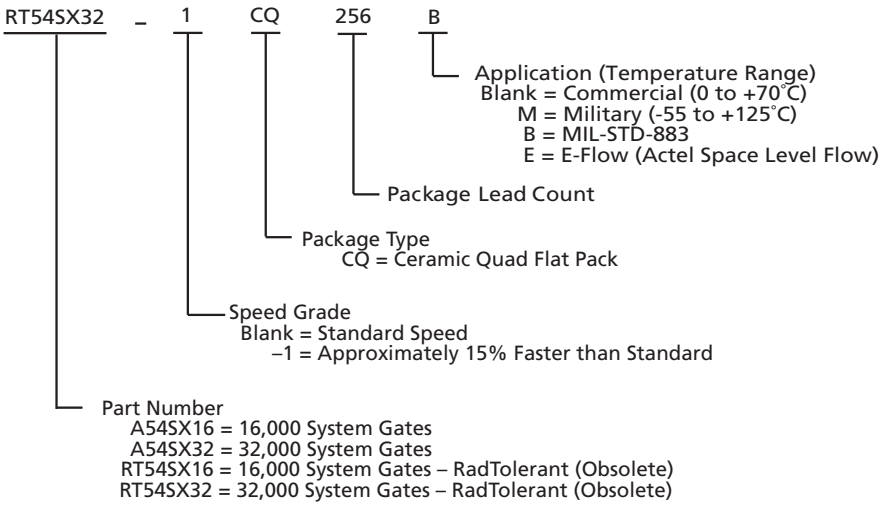
Easy Logic Integration

- Nonvolatile, User Programmable
- Highly Predictable Performance with 100% Automatic Place-and-Route
- 100% Resource Utilization with 100% Pin Locking
- Mixed Voltage Support – 3.3 V Operation with 5.0 V Input Tolerance for Low-Power Operation
- JTAG Boundary Scan Testing in Compliance with IEEE Standard 1149.1
- Secure Programming Technology Prevents Reverse Engineering and Design Theft
- Permanently Programmed for Operation on Power-Up
- Unique In-System Diagnostic and Debug Facility with Silicon Explorer
- Software Design Support with Actel Designer and Libero® Integrated Design Environment (IDE) Tools
- Predictable, Reliable, and Permanent Antifuse Technology Performance

Product Profile

Device	RT54SX16 (Obsolete)	A54SX16	RT54SX32 (Obsolete)	A54SX32
Capacity **System Gates** **Logic Gates**	 24,000 16,000	 24,000 16,000	 48,000 32,000	 48,000 32,000
Logic Modules	1,452	1,452	2,880	2,880
Register Cells	528	528	1,080	1,080
Combinatorial Cells	924	924	1,800	1,800
User I/Os (Maximum)	179	180	227	228
JTAG	Yes	Yes	Yes	Yes
Packages (by pin count) **CQFP**	 208, 256	 208, 256	 208, 256	 208, 256

Ordering Information



Product Plan

	Speed Grade		Application			
	Std	**–1***	**C**	**M**	**B**	**E**
RT54SX16 Devices						
208-Pin Ceramic Quad Flat Pack (CQFP)	Obsolete	Obsolete	Obsolete	Obsolete	Obsolete	Obsolete
256-Pin Ceramic Quad Flat Pack (CQFP)	Obsolete	Obsolete	Obsolete	Obsolete	Obsolete	Obsolete
A54SX16 Devices						
208-Pin Ceramic Quad Flat Pack (CQFP)	✓	✓	✓	✓	✓	–
256-Pin Ceramic Quad Flat Pack (CQFP)	✓	✓	✓	✓	✓	–
RT54SX32 Devices						
208-Pin Ceramic Quad Flat Pack (CQFP)	Obsolete	Obsolete	Obsolete	Obsolete	Obsolete	Obsolete
256-Pin Ceramic Quad Flat Pack (CQFP)	Obsolete	Obsolete	Obsolete	Obsolete	Obsolete	Obsolete
A54SX32 Devices						
208-Pin Ceramic Quad Flat Pack (CQFP)	✓	✓	✓	✓	✓	–
256-Pin Ceramic Quad Flat Pack (CQFP)	✓	✓	✓	✓	✓	–

Applications:
C = Commercial
M = Military
B = MIL-STD-883
E = E-flow (Actel Space Level Flow)

Availability:
✓ = Available
P = Planned
– = Not Planned

**Speed Grade:*
–1 = Approx. 15% faster than Standard

Ceramic Device Resources

	User I/Os	
Device	**CQFP 208-Pin**	**CQFP 256-Pin**
RT54SX16	174	179
A54SX16	175	180
RT54SX32	173	227
A54SX32	174	228

Note: *Contact your Actel sales representative for product availability.*

Table of Contents

SX Family FPGAs RadTolerant and HiRel

General Description

The Actel RadTolerant (RT) and HiRel versions of the SX Family of FPGAs offer many advantages for applications such as commercial and military satellites, deep space probes, and all types of military and high reliability equipment.

The RT and HiRel versions are fully pin-compatible, allowing designs to migrate across different applications that may or may not have radiation requirements. Also, the HiRel devices can be used as a low cost prototyping tool for RT designs.

The programmable architecture of these devices offers high performance, design flexibility, and fast and inexpensive prototyping—all without the expense of test vectors, NRE charges, long lead times, and schedule and cost penalties for design modifications required by ASIC devices.

Device Description

The RT54SX16 and A54SX16 devices have 16,000 available gates and up to 179 I/Os. The RT54SX32 and A54SX32 have 32,000 available gates and up to 228 I/Os. All of these devices support JTAG boundary scan testability.

All of these devices are available in Ceramic Quad Flat Pack (CQFP) packaging, with 208-pin and 256-pin versions. The 256-pin version offers the user the highest I/O capability, while the 208-pin version offers pin compatibility with the commercial Plastic Quad Flat Pack (PQFP-208). This compatibility allows the user to prototype using the very low cost plastic package and then switch to the ceramic package for production. For more information on plastic packages, refer to the *54SX Family FPGAs* datasheet.

The A54SX16 and A54SX32 devices are manufactured using a 0.35 µ technology at the Chartered Semiconductor facility in Singapore. These devices offer the highest speed performance available in FPGAs today.

The RT54SX16 and RT54SX32 devices are manufactured using a 0.6 µ technology at the Matsushita (MEC) facility in Japan. These devices offer levels of radiation survivability far in excess of typical CMOS devices.

Radiation Survivability

Total dose results are summarized in two ways. First, by the maximum total dose level that is reached when the parts fail to meet a device specification but remain functional. For Actel FPGAs, the parameter that exceeds the specification first is I_{CC}, the standby supply current. Second, by the maximum total dose that is reached prior to the functional failure of the device.

The RTSX devices have varying total dose radiation survivability. The ability of these devices to survive radiation effects is both device- and lot-dependent. The customer must evaluate and determine the applicability of these devices to their specific design and environmental requirements.

Actel will provide total dose radiation testing data along with the test data on each pedigreed lot available for sale. These reports are available on the Actel website, or you can contact your local sales representative to receive a copy. A listing of available lots and devices will also be provided. These results are only provided for reference and for customer information.

For a radiation performance summary, see *Radiation Performance of Actel Products*. This summary will also show single event upset (SEU) and single event latch-up (SEL) testing that has been performed on Actel FPGAs.

QML Certification

Actel has achieved full QML certification, demonstrating that quality management, procedures, processes, and controls are in place and comply with MIL-PRF-38535, the performance specification used by the Department of Defense for monolithic integrated circuits. QML certification is a good example of Actel's commitment to supplying the highest quality products for all types of high-reliability, military, and space applications.

Many suppliers of microelectronics components have implemented QML as their primary worldwide business system. Appropriate use of this system not only helps in the implementation of advanced technologies, but also allows for quality, reliable, and cost-effective logistics support throughout the life cycles of QML products.

Disclaimer

All radiation performance information is provided for information purposes only and is not guaranteed. The total dose effects are lot-dependent, and Actel does not guarantee that future devices will continue to exhibit similar radiation characteristics. In addition, actual performance can vary widely due to a variety of factors, including but not limited to, characteristics of the orbit, radiation environment, proximity to satellite exterior, amount of inherent shielding from other sources within the satellite, and actual bare die variations. For these reasons, Actel does not guarantee any level of radiation survivability, and it is solely the responsibility of the customer to determine whether the device will meet the requirements of the specific design.

SX Family Architecture

The SX family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of applications.

Programmable Interconnect Element

Actel's SX family provides much more efficient use of silicon by locating the routing interconnect resources between the Metal 2 (M2) and Metal 3 (M3) layers (Figure 1-1). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements, which are embedded between the M2 and M3 layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible, because it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and there is no configuration bitstream to intercept.

Additionally, the interconnects (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

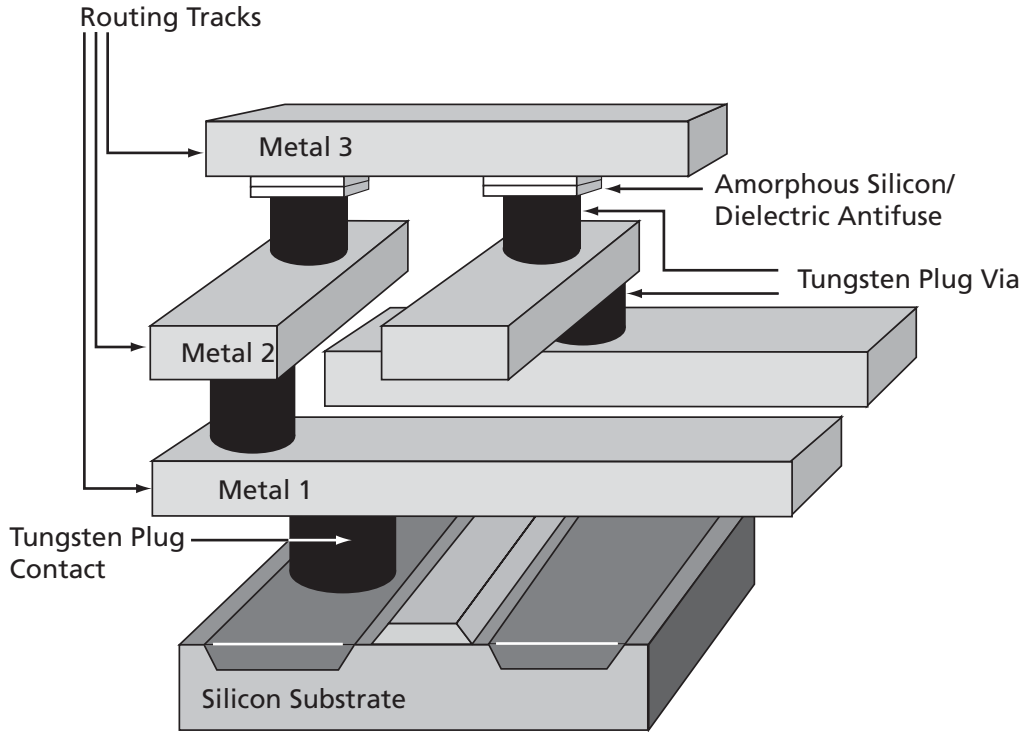


Figure 1-1 • **SX Family Interconnect Elements**

Logic Module Design

The SX family architecture has been called a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing (see Figure 1-2). Actel provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring more control signals than in previous Actel architectures, including asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines). The R-cell registers feature programmable clock polarity, selectable on a register-by-register basis (Figure 1-3 on page 1-4). This provides the designer with additional flexibility while allowing mapping of synthesized functions into the SX FPGA. The clock source for the R-cell can be chosen from the hardwired clock or the routed clock.

The C-cell implements a range of combinatorial functions with up to five inputs (Figure 1-4 on page 1-4). Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a three-input exclusive-OR function into a single C-cell. This facilitates construction of nine-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis-friendly, simplifying the overall design and reducing synthesis time.

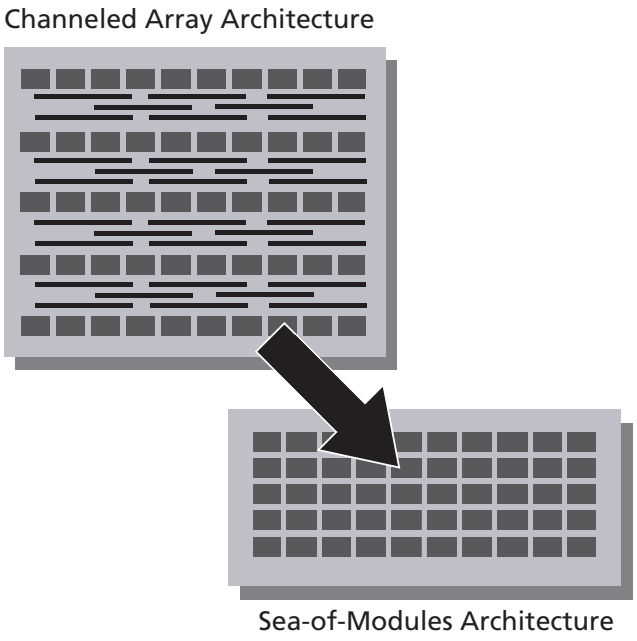


Figure 1-2 • **Channeled Array and Sea-of-Modules Architectures**

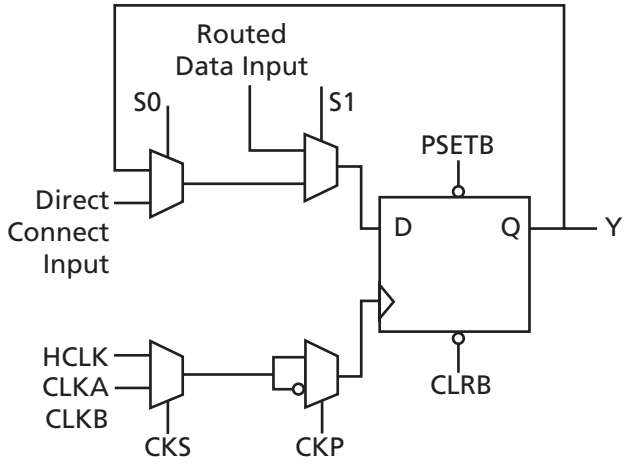


Figure 1-3 • **R-Cell**

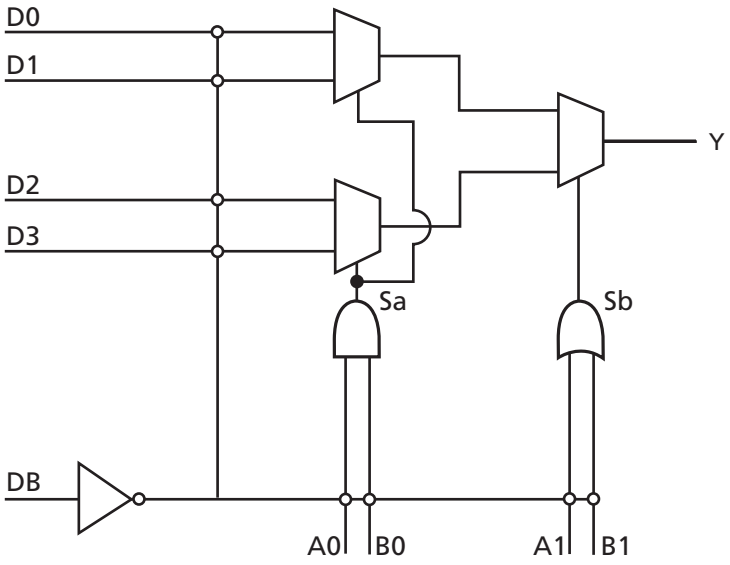


Figure 1-4 • **C-Cell**

Chip Architecture

The SX family's chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

Module Organization

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called Clusters. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, and Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into SuperClusters (see Figure 1-5). SuperCluster 1 is a two-wide grouping of Type 1 Clusters. SuperCluster 2 is a two-wide group containing one Type 1 Cluster and one Type 2 Cluster. SX devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require more combinatorial logic than flip-flops.

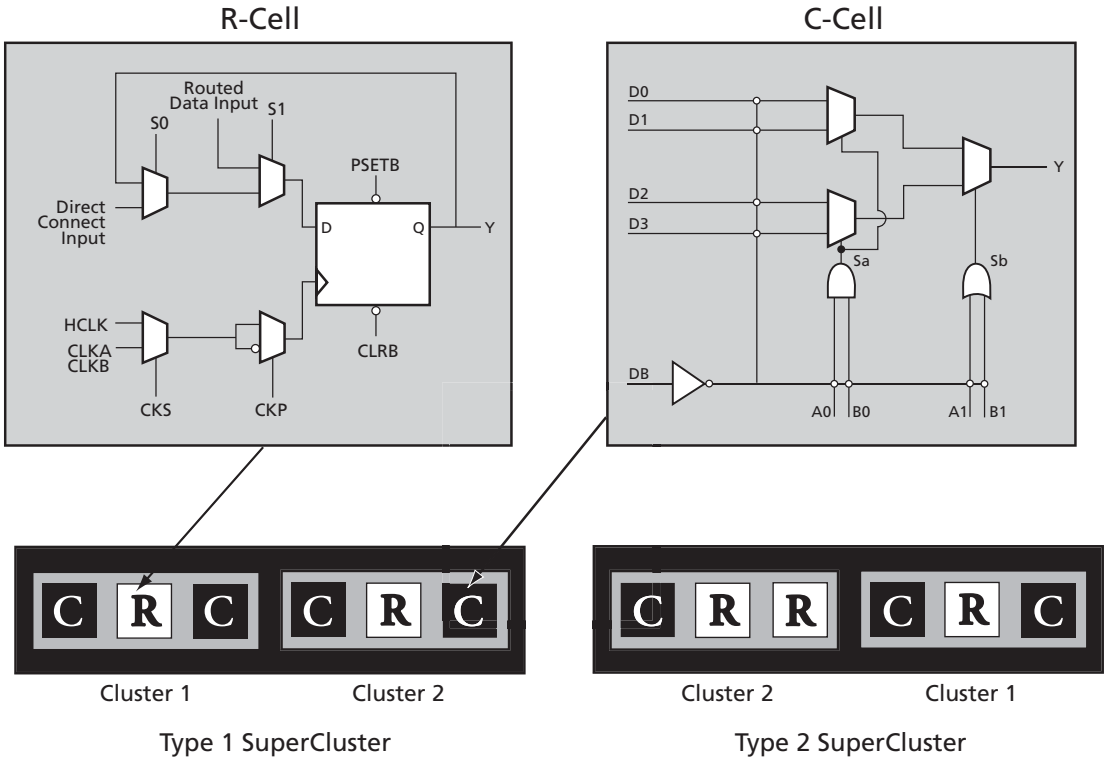


Figure 1-5 • **Cluster Organization**

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect that enable extremely fast and predictable interconnections of modules within Clusters and SuperClusters (see Figure 1-6 and Figure 1-7 on page 1-7). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster, and vertical routing to the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum pin-to-pin propagation of 0.4 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. Actel's segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100% automatic place-and-route software to minimize signal propagation delays.

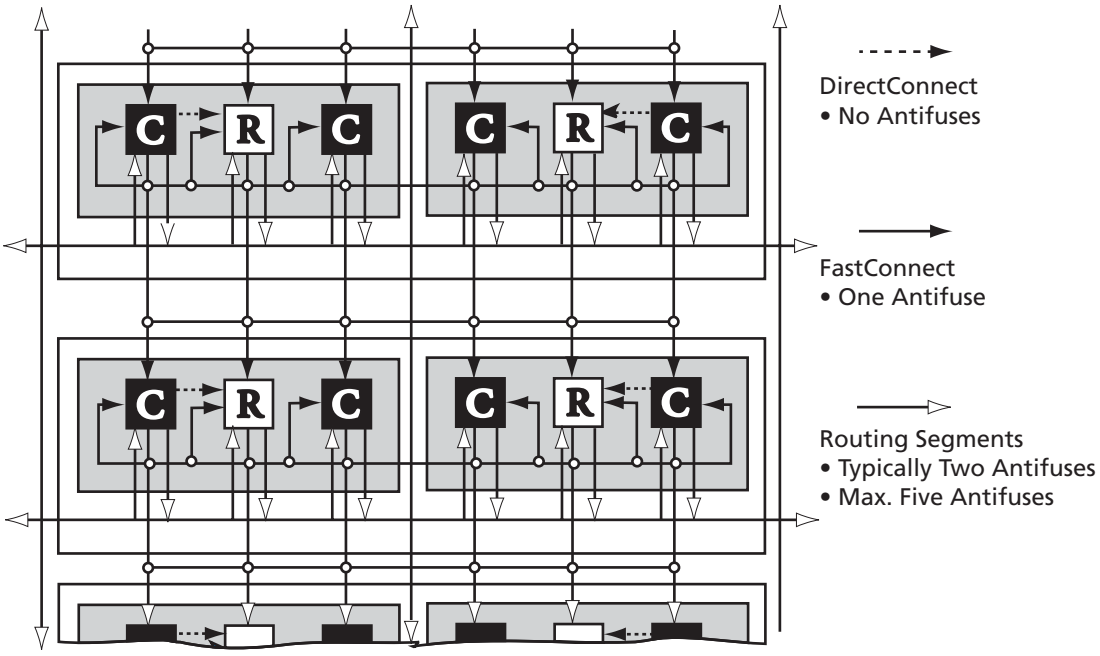


Figure 1-6 • **DirectConnect and FastConnect for Type 1 SuperClusters**

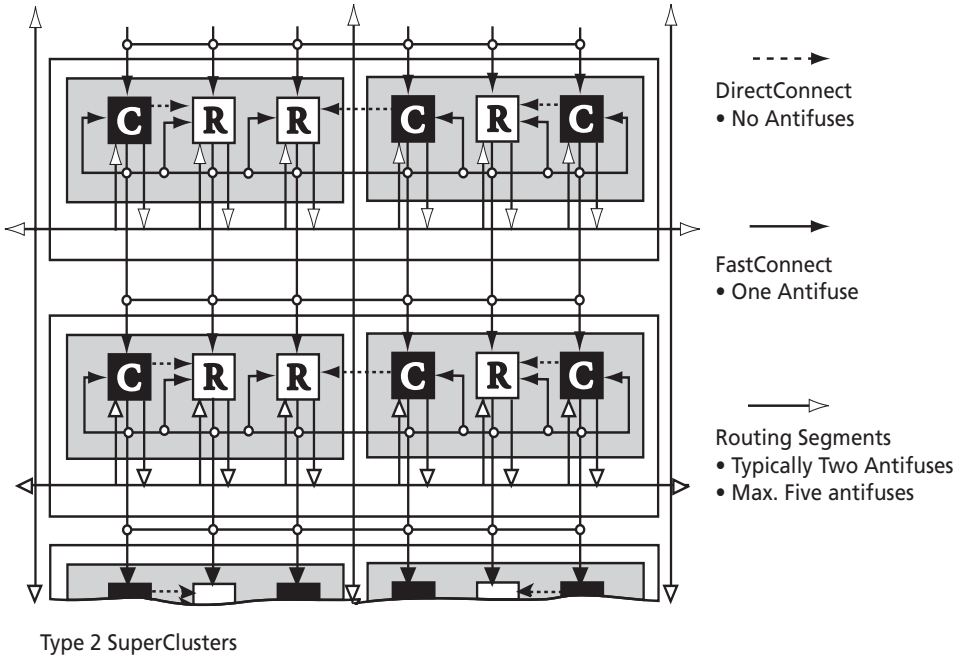


Figure 1-7 • **DirectConnect and FastConnect for Type 2 SuperClusters**

Clock Resources

Actel's high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select MUX in each R-cell. HCLK cannot be connected to combinational logic. This provides a fast propagation path for the clock signal, enabling the 8.9 ns clock-to-out (pad-to-pad) performance of the RTSX devices. The hardwired clock is tuned to provide clock skew is less than 0.5 ns worst case.

The remaining two clocks (CLKA and CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the RTSX device. CLKA and CLKB may be connected to sequential cells or to combinational logic. If CLKA or CLKB is sourced from internal logic signals, then the external clock pin cannot be used for any other input and must be tied low or high. Figure 1-8 describes the clock circuit used for the constant load HCLK. Figure 1-9 describes the CLKA and CLKB circuit used in all RTSX devices with the exception of the RT54SX72S device.

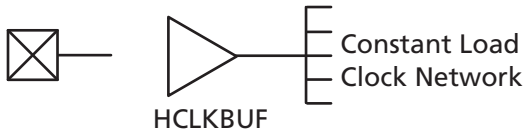


Figure 1-8 • **RTSX Constant Load Clock Pad**

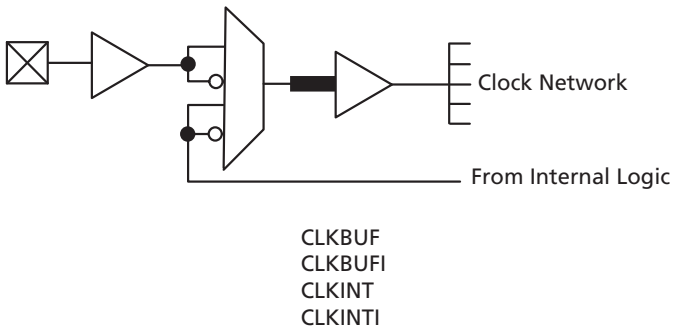


Figure 1-9 • **RTSX Clock Pads**

Other Architecture

Performance

The combination of architectural features described above enables RT54SX devices to operate with internal clock frequencies exceeding 160 MHz, enabling very fast execution of complex logic functions. Thus, the RTSX family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs that previously would have required a gate array to meet performance goals can now be integrated into an RTSX device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance. With RTSX devices, there is no need to use complicated performance-enhancing design techniques such as redundant logic to reduce fanout on critical nets, or the instantiation of macros in HDL code to achieve high performance.

I/O Modules

Each I/O on an RTSX device can be configured as an input, an output, a tristate output, or a bidirectional pin. Even without the inclusion of dedicated registers, these I/Os, in combination with array registers, can achieve clock-to-out (PAD-to-PAD) timing as fast as 5.8 ns. I/O cells including embedded latches and flip-flops require instantiation in HDL code. This is a design complication not encountered in RTSX FPGAs. Fast PAD-to-PAD timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reduces overall design time.

Power Requirements

The RTSX family supports either 3.3 V or 5.0 V I/O voltage operation and is designed to tolerate 5 V inputs in each case (Table 1-1). Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced due to the small number of antifuses in the path, and because of the low resistance properties of the antifuses. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest-power architecture on the market.

Table 1-1 • **Supply Voltages**

	V_{CCA}	V_{CCI}	V_{CCR}	Maximum Input Tolerance	Maximum Output Drive
A54SX16 A54SX32	3.3 V	3.3 V	5.0 V	5.0 V	3.3 V
RTSX16 RTSX32	3.3 V	3.3 V	5.0 V	5.0 V	3.3 V

Boundary Scan Testing (BST)

All RTSX devices are IEEE 1149.1 (JTAG) compliant. They offer superior diagnostic and testing capabilities by providing BST and probing capabilities. These functions are controlled through the special test pins in conjunction with the program fuse. The functionality of each pin is described in Table 1-2. Figure 1-10 on page 1-9 is a block diagram of the RTSX JTAG circuitry.

Table 1-2 • **Boundary Scan Pin Functionality**

Program Fuse Blown (Dedicated Test Mode)	Program Fuse Not Blown (Flexible Mode)
TCK, TDI, TDO are dedicated test pins	TCK, TDI, TDO are flexible and may be used as I/Os
No need for pull-up resistor for TMS	Use a pull-up resistor of 10 kΩ on TMS

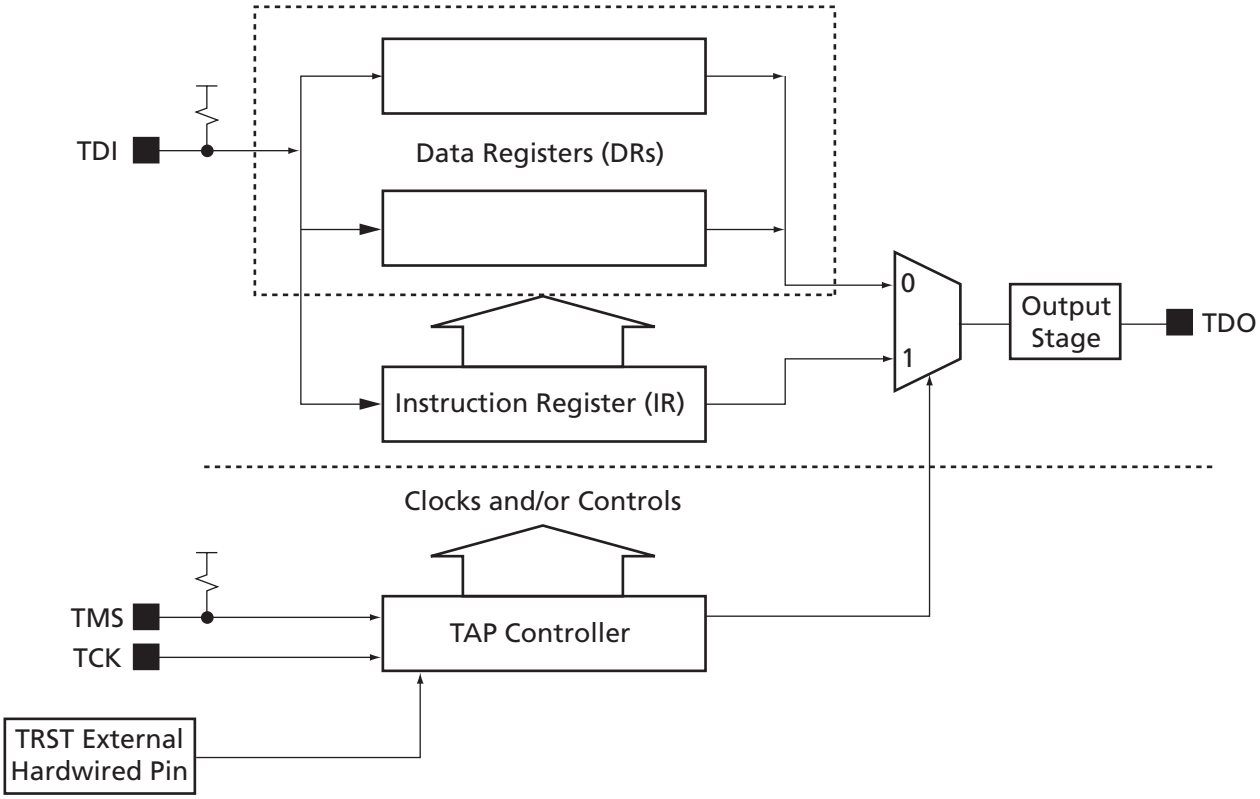


Figure 1-10 • **RTSX JTAG Circuitry**

Configuring Diagnostic Pins

The JTAG and Probe pins (TDI, TCK, TMS, TDO, PRA, and PRB) are placed in the desired mode by selecting the appropriate check boxes in the **Variation** dialog window. This dialog window is accessible through the Design Setup Wizard under the **Tools** menu in the Actel Designer software.

TRST Pin

The TRST pin functions as a Boundary Scan Reset pin. The TRST pin is an asynchronous, active-low input to initialize or reset the BST circuit. An internal pull-up resistor is automatically enabled on the TRST pin.

Dedicated Test Mode

When the **Reserve JTAG** check box is selected in the Designer software, the RTSX is placed in Dedicated Test mode, which configures the TDI, TCK, and TDO pins for BST or in-circuit verification with Silicon Explorer II. An internal pull-up resistor is automatically enabled on both the TMS and TDI pins. In dedicated test mode, TCK, TDI, and TDO are dedicated test pins and become unavailable for pin assignment in the Pin Editor. The TMS pin will function as specified in the IEEE 1149.1 (JTAG) Specification.

Flexible Mode

When the **Reserve JTAG** check box is cleared (the default setting in the Designer software), the RTSX is placed in flexible mode, which allows the TDI, TCK, and TDO pins to function as user I/Os or BST pins. In this mode the internal pull-up resistors on the TMS and TDI pins are disabled. An external 10 kΩ pull-up resistor to V_{CCI} is required on the TMS pin.

The TDI, TCK, and TDO pins are transformed from user I/Os into BST pins when a rising edge is detected on TCK while TMS is at logical low. Once the BST pins are in test mode they will remain in BST mode until the internal BST state machine reaches the "logic reset" state. At this point the BST pins will be released and will function as regular I/O pins. The "logic reset" state is reached five TCK cycles after the TMS pin is set to logical HIGH.

The program fuse determines whether the device is in Dedicated Test or Flexible mode. The default (fuse not programmed) is Flexible mode.

Development Tool Support

The RTSX family of FPGAs is fully supported by both Actel Libero® Integrated Design Environment (IDE) and Designer FPGA Development software. Actel Libero IDE is a design management environment that streamlines the design flow. Libero IDE provides an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw® for Actel from Mentor Graphics®, Model*Sim*™ HDL Simulator from Mentor Graphics, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel. Refer to the *Libero IDE Design Flow* (located on the Actel website) diagram for more information.

Actel Designer software is a place-and-route tool and provides a comprehensive suite of back-end support tools for FPGA development. The Designer software includes timing-driven place-and-route and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can lock his/her design pins before layout while minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, the Actel integrated verification and logic analysis tool. Another tool included in the Designer software is the ACTgen macro builder, which easily creates popular and commonly used logic functions for implementation in your schematic or HDL design. Actel Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

RTSX Probe Circuit Control Pins

The RTSX RadTolerant devices contain internal probing circuitry that provides built-in access to every node in a design, enabling 100-percent real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed using Silicon Explorer II, an easy-to-use integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary scan ports (TDI, TRST, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-11 on page 1-11 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

Design Considerations

For prototyping, the TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Because these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the security fuse should not be programmed during prototyping because doing so disables the probe circuitry.

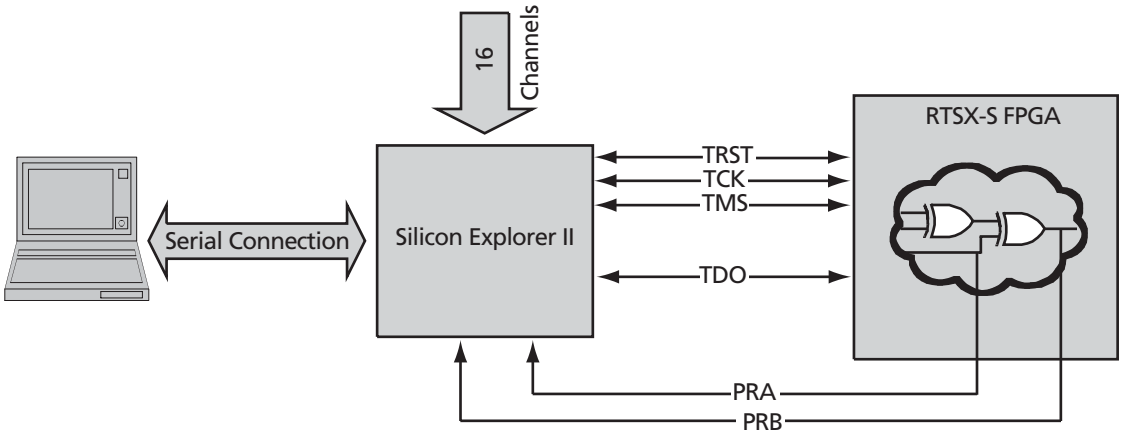


Figure 1-11 • **Probe Setup**

Related Documents

Datasheets

54SX Family FPGAs

http://www.actel.com/documents/A54SXDS.pdf

Application Notes

Power-Up and Power-Down Behavior of 54SX and RT54SX Devices

http://www.actel.com/documents/PowerUpAN.pdf

3.3 V / 5 V Operating Conditions

Recommended Operating Conditions

Table 1-3 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
V_{CCR}	DC Supply Voltage	–0.3 to +6.0	V
V_{CCA}	DC Supply Voltage	–0.3 to +4.0	V
V_{CCI}	DC Supply Voltage	–0.3 to +4.0	V
V_I	Input Voltage	–0.5 to +5.5	V
V_O	Output Voltage	–0.5 to +3.6	V
I_{IO}	I/O Source Sink Current[2]	–30 to +5.0	mA
T_{STG}	Storage Temperature	–40 to +125	°C

Notes:

1. *Stresses beyond those listed in Table 1-3 may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *The I/O source sink numbers refer to tristated inputs and outputs*

Table 1-4 • **Recommended Operating Conditions**

Parameter	Commercial	Military	Units
Temperature Range[1]	0 to +70	–55 to +125	°C
3.3 V Power[2] Supply Tolerance	±10	±10	%V_{CC}
5 V Power Supply [2] Tolerance	±5	±10	%V_{CC}

Notes:

1. *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*
2. *All power supplies must be in the recommended operating range for 250 µs. For more information, refer to the Power-Up and Power-Down Behavior of 54SX and RT54SX Devices application note.*

Electrical Specifications

Table 1-5 • **Electrical Specifications**

Symbol	Parameter	Commercial		Military		
		Min.	Max.	Min.	Max.	Units
V_{OH}	(I_{OH} = –20 µA) (CMOS) (I_{OH} = –8 mA) (TTL) (I_{OH} = –6 mA) (TTL)	(V_{CCI} – 0.1) 2.4	V_{CCI} V_{CCI}	(V_{CCI} – 0.1) 2.4	V_{CCI} V_{CCI}	V
V_{OL}	(I_{OL} = 20 µA) (CMOS) (I_{OL} = 12 mA) (TTL) (I_{OL} = 8 mA) (TTL)		0.10 0.50		 0.50	V
V_{IL}	Low Level Inputs		0.8		0.8	V
V_{IH}	High Level Inputs	2.0		2.0		V
t_R, t_F	Input Transition Time t_R, t_F		50		50	ns
C_{IO}	C_{IO} I/O Capacitance		10		10	pF
I_{CC}	Standby Current, I_{CC}		4.0		25	mA
$I_{CC(D)}$	$I_{CC(D)}$ $I_{Dynamic}$ V_{CC} Supply Current	See the "Power Dissipation" section on page 1-15.				

Power-Up Sequencing

Table 1-6 • **RT54SX16, A54SX16, RT54SX32, A54SX32**

V_{CCA}	V_{CCR}	V_{CCI}	Power-Up Sequence	Comments
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	No possible damage to device
			3.3 V First 5.0 V Second	Possible damage to device

Power-Down Sequencing

Table 1-7 • **RT54SX16, A54SX16, RT54SX32, A54SX32**

V_{CCA}	V_{CCR}	V_{CCI}	Power-Down Sequence	Comments
3.3 V	5.0 V	3.3 V	5.0 V First 3.3 V Second	Possible damage to device
			3.3 V First 5.0 V Second	No possible damage to device

Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc}, and the junction-to-ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for an RT54SX16 in a CQFP 256-pin package at military temperature and still air is shown in EQ 1-1:

$$\text{Absolute Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}\ (°C/W)} = \frac{150°C - 125°C}{23°C/W} = 1.09\ W$$

EQ 1-1

Table 1-8 • **Package Thermal Characteristics**

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	Units
RT54SX16				
Ceramic Quad Flat Pack (CQFP)	208	7.5	29	°C/W
Ceramic Quad Flat Pack (CQFP)	256	4.6	23	°C/W
RT54SX32				
Ceramic Quad Flat Pack (CQFP)	208	6.9	35	°C/W
Ceramic Quad Flat Pack (CQFP)	256	3.5	20	°C/W
A54SX16				
Ceramic Quad Flat Pack (CQFP)	208	7.9	30	°C/W
Ceramic Quad Flat Pack (CQFP)	256	5.6	25	°C/W
A54SX32				
Ceramic Quad Flat Pack (CQFP)	208	7.6	30	°C/W
Ceramic Quad Flat Pack (CQFP)	256	4.8	24	°C/W

Power Dissipation

$$P = (I_{CC}standby + I_{CC}active) * V_{CCA} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CCA} – V_{OH}) * M$$

EQ 1-2

where:

I_{CC}standby is the current flowing when no inputs or outputs are changing.

I_{CC}active is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N is the number of outputs driving TTL loads to V_{OL}.

M is the number of outputs driving TTL loads to V_{OH}.

Accurate values for N and M are difficult to determine because they depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Power consumption due to standby current is typically a small component of the total power consumption. Standby power is shown below for military, worst-case conditions (70°C).

I_{CC}	V_{CC}	Power
20 mA	3.6 V	72 mW

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency-dependent, a function of the logic and the external I/O. Active power dissipation results from charging the internal chip capacitances of the interconnects, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PCB traces and load device inputs. An additional component of the active power dissipation is the totem pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by EQ 1-3:

$$Power\ (\mu W) = C_{EQ} * V_{CCA}^2 * F$$

EQ 1-3

where:

C_{EQ} = Equivalent capacitance in pF

V_{CCA} = Power supply in volts (V)

F = Switching frequency in MHz

Equivalent capacitance is calculated by measuring I_{CC}active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of V_{CCA}. Equivalent capacitance is frequency-independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown in Table 1-9.

Table 1-9 • Equivalent Capacitance Values

		RT54SX16	A54SX16	RT54SX32	A54SX32
Equivalent Capacitance (pF)					
Modules	C_{EQM}	7.0	3.9	7.0	3.9
Input Buffers	C_{EQI}	2.0	1.0	2.0	1.0
Output Buffers	C_{EQO}	10.0	5.0	10.0	5.0
Routed Array Clock Buffer Loads	C_{EQCR}	0.4	0.2	0.6	0.3
Dedicated Clock Buffer Loads	C_{EQCD}	0.25	0.15	0.34	0.23
Fixed Capacitance (pF)					
routed_Clk1	r_1	120	60	210	107
routed_Clk2	r_2	120	60	210	107
Fixed Clock Loads					
Clock Loads on Dedicated Array Clock	s_1	528	528	1,080	1,080

C_{EQ} Values (pF)

To calculate the active power dissipated by the complete design, the switching frequency of each part of the logic must be known. EQ 1-4 shows a piecewise linear summation over all components.

$$\text{Power} = V_{CCA}^2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} + 0.5 * (s_1 * C_{EQCD} * f_{s1})_{dedicated\_CLK}]$$

EQ 1-4

where:

m	=	Number of logic modules switching at f_m
n	=	Number of input buffers switching at f_n
p	=	Number of output buffers switching at f_p
q_1	=	Number of clock loads on the first routed array clock
q_2	=	Number of clock loads on the second routed array clock
r_1	=	Fixed capacitance due to first routed array clock
r_2	=	Fixed capacitance due to second routed array clock
s_1	=	Fixed number of clock loads on the dedicated array clock (528 for A54SX16)
C_{EQM}	=	Equivalent capacitance of logic modules in pF
C_{EQI}	=	Equivalent capacitance of input buffers in pF
C_{EQO}	=	Equivalent capacitance of output buffers in pF
C_{EQCR}	=	Equivalent capacitance of routed array clock in pF
C_{EQCD}	=	Equivalent capacitance of dedicated array clock in pF
C_L	=	Output lead capacitance in pF
f_m	=	Average logic module switching rate in MHz
f_n	=	Average input buffer switching rate in MHz
f_p	=	Average output buffer switching rate in MHz
f_{q1}	=	Average first routed array clock rate in MHz
f_{q2}	=	Average second routed array clock rate in MHz

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so they can be generally used to predict the upper limits of power dissipation.

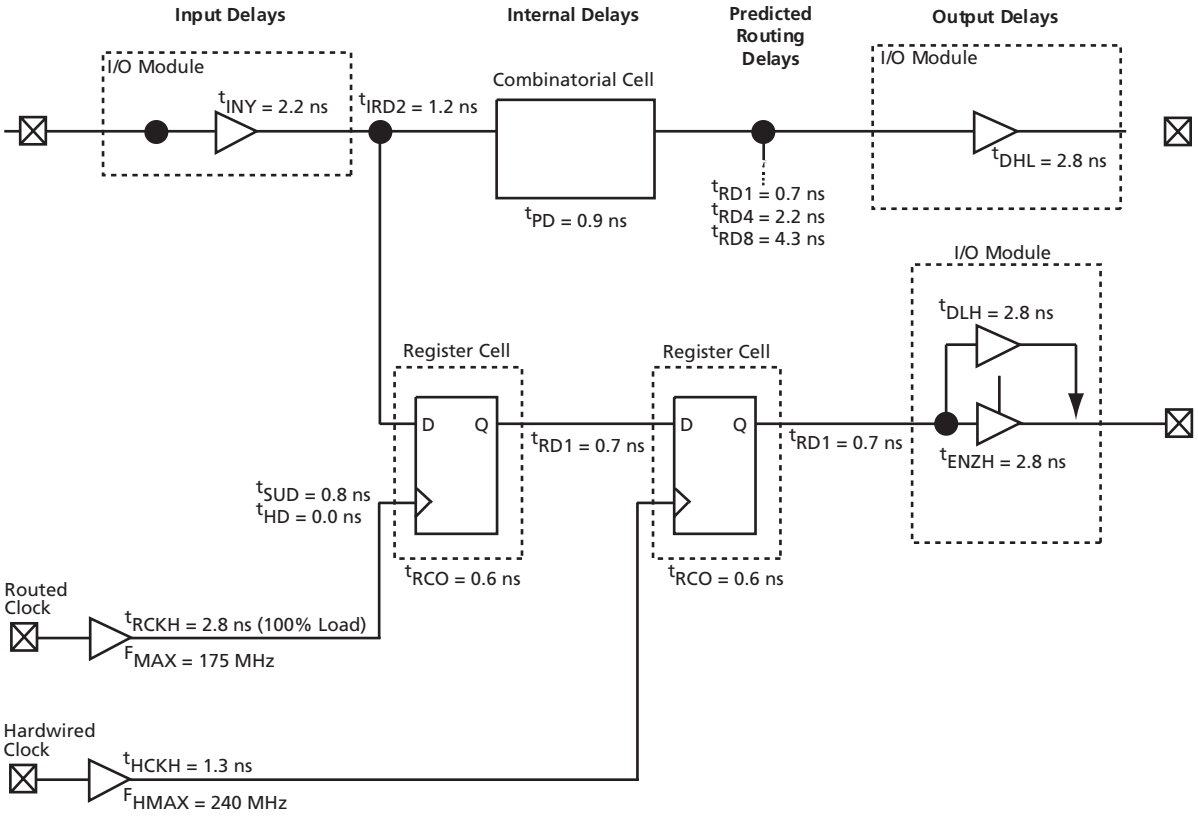
Logic Modules (m)	=	80% of modules
Inputs Switching (n)	=	# inputs/4
Outputs Switching (p)	=	# output/4
First Routed Array Clock Loads (q_1)	=	40% of sequential modules
Second Routed Array Clock Loads (q_2)	=	40% of sequential modules
Load Capacitance (C_L)	=	35 pF
Average Logic Module Switching Rate (f_m)	=	F/10
Average Input Switching Rate (f_n)	=	F/5
Average Output Switching Rate (f_p)	=	F/10
Average First Routed Array Clock Rate (f_{q1})	=	F/2
Average Second Routed Array Clock Rate (f_{q2})	=	F/2
Average Dedicated Array Clock Rate (f_{s1})	=	F

Temperature and Voltage Derating Factors

Table 1-10 • **Temperature and Voltage Derating Factors (Normalized to Worst-Case Commercial, T_J = 70°C, V_{CCA} = 3.0 V)**

	Junction Temperature (T_J)					
V_{CCA}	**–40**	**0**	**25**	**70**	**85**	**125**
3.0	0.78	0.87	0.89	1.00	1.04	1.16
3.3	0.73	0.82	0.83	0.93	0.97	1.08
3.6	0.69	0.77	0.78	0.87	0.92	1.02

SX Timing Model



Note: *Values shown for A54SX16-1 at worst-case commercial conditions.*

Figure 1-12 • **SX Timing Model**

Hardwired Clock

External Setup = $t_{INY} + t_{IRD1} + t_{SUD} – t_{HCKH}$
= 2.2 + 0.7 + 0.8 – 1.7 = 2.0 ns

Clock-to-Out (Pin-to-Pin) = $t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 1.7 + 0.6 + 0.7 + 2.8 = 5.8 ns

Routed Clock

External Setup = $t_{INY} + t_{IRD1} + t_{SUD} – t_{RCKH}$
= 2.2 + 0.7 + 0.8 – 2.4 = 1.3 ns

Clock-to-Out (Pin-to-Pin) = $t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
= 2.4 + 0.6 + 0.7 + 2.8 = 6.5 ns

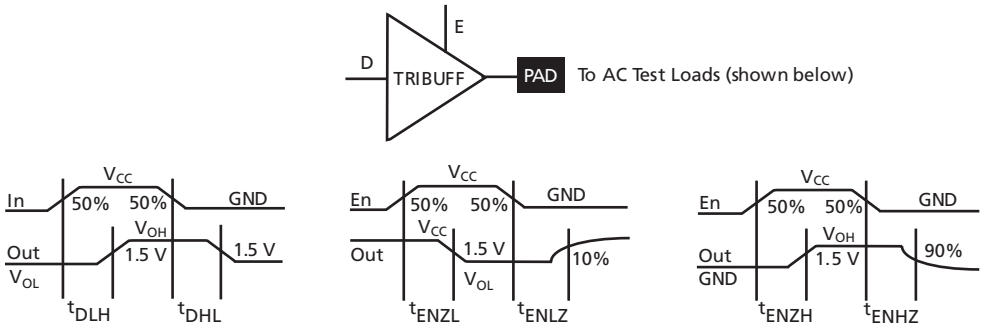


Figure 1-13 • **Output Buffer Delays**

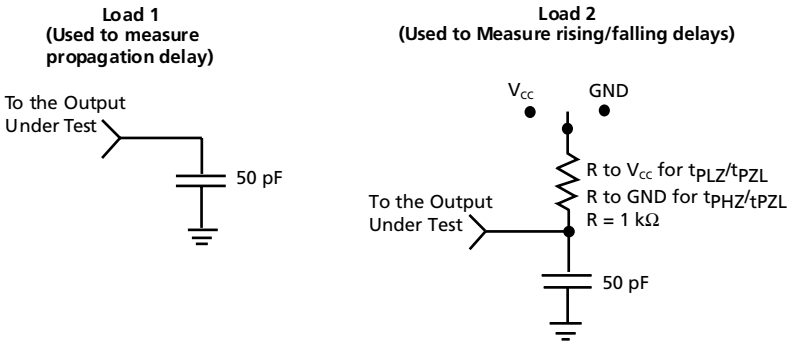


Figure 1-14 • **AC Test Loads**

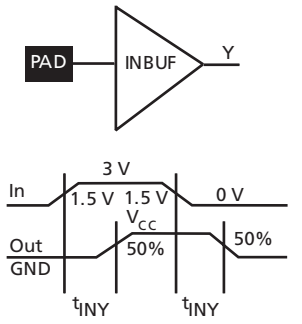


Figure 1-15 • **Input Buffer Delays**

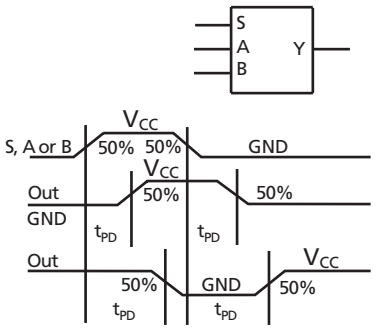


Figure 1-16 • **C-Cell Delays**

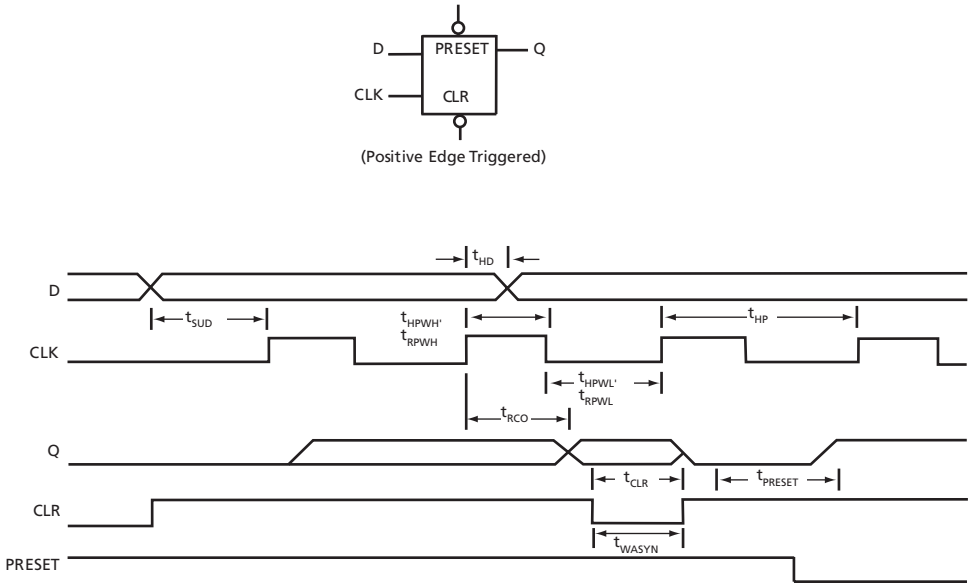


Figure 1-17 • **Register Cell Timing Characteristics – Flip-Flops**

Timing Characteristics

Timing characteristics for SX devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX family members. Internal routing delays are device-dependent. Design dependence means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the Timer tool or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6 percent of the nets in a design may be designated as critical, whereas 90 percent of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout (FO = 24) routing delays in the data sheet specifications section.

Timing Derating

SX devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

A54SX16 Timing Characteristics

Table 1-11 • **A54SX16**
(Worst-Case Military Conditions, V_{CCR} = 4.75 V, V_{CCA}, V_{CCI} = 3.0 V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]						
t_{PD}	Internal Array Module		0.9		1.0	ns
Predicted Routing Delays[2]						
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.6		0.7	ns
t_{RD1}	FO = 1 Routing Delay		0.7		0.8	ns
t_{RD2}	FO = 2 Routing Delay		1.2		1.4	ns
t_{RD3}	FO = 3 Routing Delay		1.7		2.0	ns
t_{RD4}	FO = 4 Routing Delay		2.2		2.6	ns
t_{RD8}	FO = 8 Routing Delay		4.3		5.0	ns
t_{RD12}	FO = 12 Routing Delay		5.6		6.6	ns
t_{RD18}	FO = 18 Routing Delay		9.4		11.0	ns
t_{RD24}	FO = 24 Routing Delay		12.4		14.6	ns
R-Cell Timing						
t_{RCO}	Sequential Clock-to-Q		0.6		0.8	ns
t_{CLR}	Asynchronous Clear-to-Q		0.6		0.8	ns
t_{SUD}	Flip-Flop Data Input Setup	0.8		0.9		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	2.4		2.9		ns
I/O Module Input Propagation Delays						
t_{INYH}	Input Data Pad-to-Y HIGH		2.2		2.6	ns
t_{INYL}	Input Data Pad-to-Y LOW		2.2		2.6	ns
Predicted Input Routing Delays[2]						
t_{IRD1}	FO = 1 Routing Delay		0.7		0.8	ns
t_{IRD2}	FO = 2 Routing Delay		1.2		1.4	ns
t_{IRD3}	FO = 3 Routing Delay		1.7		2.0	ns
t_{IRD4}	FO = 4 Routing Delay		2.2		2.6	ns
t_{IRD8}	FO = 8 Routing Delay		4.3		5.0	ns
t_{IRD12}	FO = 12 Routing Delay		5.6		6.6	ns
t_{IRD18}	FO = 18 Routing Delay		9.4		11.0	ns
t_{IRD24}	FO = 24 Routing Delay		12.4		14.6	ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn}, or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

Table 1-12 • **A54SX16**
(Worst-Case Military Conditions, V_{CCR} = 4.75 V, V_{CCA}, V_{CCI} = 3.0 V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
I/O Module – TTL Output Timing*						
t_{DLH}	Data-to-Pad LOW to HIGH		2.8		3.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.8		3.3	ns
t_{ENZL}	Enable-to-Pad, Z to LOW		2.3		2.8	ns
t_{ENZH}	Enable-to-Pad, Z to HIGH		2.8		3.3	ns
t_{ENLZ}	Enable-to-Pad, LOW to Z		4.5		5.2	ns
t_{ENHZ}	Enable-to-Pad, HIGH to Z		2.2		2.6	ns
d_{TLH}	Delta LOW to HIGH		0.05		0.06	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.08	ns/pF
Dedicated (Hardwired) Array Clock Network						
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.7		2.0	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.9		2.2	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.1		2.4		ns
t_{HPWL}	Minimum Pulse Width LOW	2.1		2.4		ns
t_{HCKSW}	Maximum Skew		0.4		0.4	ns
t_{HP}	Minimum Period	4.2		4.9		ns
f_{HMAX}	Maximum Frequency		240		205	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		2.4		2.9	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.7		3.1	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		2.9		3.3	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.9		3.5	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		2.8		3.3	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.9		3.5	ns
t_{RPWH}	Minimum Pulse Width HIGH	3.1		3.7		ns
t_{RPWL}	Minimum Pulse Width LOW	3.1		3.7		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.6		0.8	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.8		0.9	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.8		0.9	ns

Note: **Delays based on 35 pF loading, except for t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH}, the loading is 5 pF.*

RT54SX16 Timing Characteristics

Table 1-13 • **RT54SX16**
(Worst-Case Military Conditions, V_{CCR} = 4.75 V, V_{CCA}, V_{CCI} = 3.0 V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]						
t_{PD}	Internal Array Module		1.7		1.8	ns
Predicted Routing Delays[2]						
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.2		0.2	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		1.1		1.3	ns
t_{RD1}	FO = 1 Routing Delay		1.3		1.5	ns
t_{RD2}	FO = 2 Routing Delay		2.2		2.6	ns
t_{RD3}	FO = 3 Routing Delay		3.1		3.6	ns
t_{RD4}	FO = 4 Routing Delay		4.0		4.7	ns
t_{RD8}	FO = 8 Routing Delay		7.8		9.0	ns
t_{RD12}	FO = 12 Routing Delay		10.1		11.9	ns
t_{RD18}	FO = 18 Routing Delay		17.0		19.8	ns
t_{RD24}	FO = 24 Routing Delay		22.4		26.3	ns
R-Cell Timing						
t_{RCO}	Sequential Clock-to-Q		1.5		2.0	ns
t_{CLR}	Asynchronous Clear-to-Q		1.5		2.0	ns
t_{SUD}	Flip-Flop Data Input Setup	2.0		2.2		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	4.4		5.3		ns
I/O Module Input Propagation Delays						
t_{INYH}	Input Data Pad-to-Y HIGH		4.0		4.7	ns
t_{INYL}	Input Data Pad-to-Y LOW		4.0		4.7	ns
Predicted Input Routing Delays[2]						
t_{IRD1}	FO = 1 Routing Delay		1.3		1.5	ns
t_{IRD2}	FO = 2 Routing Delay		2.2		2.6	ns
t_{IRD3}	FO = 3 Routing Delay		3.1		3.6	ns
t_{IRD4}	FO = 4 Routing Delay		4.0		4.7	ns
t_{IRD8}	FO = 8 Routing Delay		7.8		9.0	ns
t_{IRD12}	FO = 12 Routing Delay		10.1		11.9	ns
t_{IRD18}	FO = 18 Routing Delay		17.0		19.8	ns
t_{IRD24}	FO = 24 Routing Delay		22.4		26.3	ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

Table 1-14 • **RT54SX16**
(Worst-Case Military Conditions, V_{CCR} = 4.75 V, V_{CCA}, V_{CCI} = 3.0 V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
I/O Module – TTL Output Timing*						
t_{DLH}	Data-to-Pad LOW to HIGH		5.1		6.0	ns
t_{DHL}	Data-to-Pad HIGH to LOW		5.1		6.0	ns
t_{ENZL}	Enable-to-Pad, Z to LOW		4.2		5.1	ns
t_{ENZH}	Enable-to-Pad, Z to HIGH		5.1		6.0	ns
t_{ENLZ}	Enable-to-Pad, LOW to Z		8.1		9.4	ns
t_{ENHZ}	Enable-to-Pad, HIGH to Z		4.0		4.7	ns
d_{TLH}	Delta LOW to HIGH		0.09		0.11	ns/pF
d_{THL}	Delta HIGH to LOW		0.09		0.15	ns/pF
Dedicated (Hardwired) Array Clock Network						
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		3.1		3.6	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		3.5		4.0	ns
t_{HPWH}	Minimum Pulse Width HIGH	3.8		4.4		ns
t_{HPWL}	Minimum Pulse Width LOW	3.8		4.4		ns
t_{HCKSW}	Maximum Skew		0.8		0.8	ns
t_{HP}	Minimum Period	7.6		8.9		ns
f_{HMAX}	Maximum Frequency		130		110	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		4.4		5.3	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		4.9		5.6	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		5.3		6.0	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		5.3		6.3	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		5.1		6.0	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		5.3		6.3	ns
t_{RPWH}	Minimum Pulse Width HIGH	5.6		6.7		ns
t_{RPWL}	Minimum Pulse Width LOW	5.6		6.7		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.1		1.5	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.5		1.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.5		1.7	ns

Note: **Delays based on 35 pF loading, except for t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5 pF.*

A54SX32 Timing Characteristics

Table 1-15 • **A54SX32 Timing Characteristics (Worst-Case Military Conditions, V_{CCR} = 4.75 V, V_{CCA}, V_{CCI} = 3.0 V, T_J = 125°C)**

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]						
t_{PD}	Internal Array Module		0.9		1.0	ns
Predicted Routing Delays[2]						
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.1		0.1	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		0.6		0.7	ns
t_{RD1}	FO = 1 Routing Delay		0.7		0.8	ns
t_{RD2}	FO = 2 Routing Delay		1.2		1.4	ns
t_{RD3}	FO = 3 Routing Delay		1.7		2.0	ns
t_{RD4}	FO = 4 Routing Delay		2.2		2.6	ns
t_{RD8}	FO = 8 Routing Delay		4.3		5.0	ns
t_{RD12}	FO = 12 Routing Delay		5.6		6.6	ns
t_{RD18}	FO = 18 Routing Delay		9.4		11.0	ns
t_{RD24}	FO = 24 Routing Delay		12.4		14.6	ns
R-Cell Timing						
t_{RCO}	Sequential Clock-to-Q		0.6		0.8	ns
t_{CLR}	Asynchronous Clear-to-Q		0.6		0.8	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.8		0.9		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	2.4		2.9		ns
I/O Module Input Propagation Delays						
t_{INYH}	Input Data Pad-to-Y HIGH		2.2		2.6	ns
t_{INYL}	Input Data Pad-to-Y LOW		2.2		2.6	ns
Predicted Input Routing Delays[2]						
t_{IRD1}	FO = 1 Routing Delay		0.7		0.8	ns
t_{IRD2}	FO = 2 Routing Delay		1.2		1.4	ns
t_{IRD3}	FO = 3 Routing Delay		1.7		2.0	ns
t_{IRD4}	FO = 4 Routing Delay		2.2		2.6	ns
t_{IRD8}	FO = 8 Routing Delay		4.3		5.0	ns
t_{IRD12}	FO = 12 Routing Delay		5.6		6.6	ns
t_{IRD18}	FO = 18 Routing Delay		9.4		11.0	ns
t_{IRD24}	FO = 24 Routing Delay		12.4		14.6	ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

Table 1-16 • **A54SX32 Timing Characteristics (Worst-Case Military Conditions, V_{CCR} = 4.75 V, V_{CCA}, V_{CCI} = 3.0 V, T_J = 125°C)**

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
I/O Module – TTL Output Timing*						
t_{DLH}	Data-to-Pad LOW to HIGH		2.8		3.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.8		3.3	ns
t_{ENZL}	Enable-to-Pad, Z to LOW		2.3		2.8	ns
t_{ENZH}	Enable-to-Pad, Z to HIGH		2.8		3.3	ns
t_{ENLZ}	Enable-to-Pad, LOW to Z		4.5		5.2	ns
t_{ENHZ}	Enable-to-Pad, HIGH to Z		2.2		2.6	ns
d_{TLH}	Delta LOW to HIGH		0.05		0.06	ns/pF
d_{THL}	Delta HIGH to LOW		0.05		0.08	ns/pF
Dedicated (Hardwired) Array Clock Network						
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.7		2.0	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.9		2.2	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.1		2.4		ns
t_{HPWL}	Minimum Pulse Width LOW	2.1		2.4		ns
t_{HCKSW}	Maximum Skew		0.4		0.4	ns
t_{HP}	Minimum Period	4.2		4.8		ns
f_{HMAX}	Maximum Frequency		240		205	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		2.4		2.9	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.7		3.1	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		2.9		3.3	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.9		3.5	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		2.8		3.3	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.9		3.5	ns
t_{RPWH}	Minimum Pulse Width HIGH	3.1		3.7		ns
t_{RPWL}	Minimum Pulse Width LOW	3.1		3.7		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.6		0.8	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.8		0.9	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.8		0.9	ns

Note: **Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5 pF.*

RT54SX32 Timing Characteristics

Table 1-17 • **RT54SX32 Timing Characteristics (Worst-Case Military Conditions, V_{CCR} = 4.75 V, V_{CCA}, V_{CCI} = 3.0 V, T_J = 125°C)**

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]						
t_{PD}	Internal Array Module		1.7		1.8	ns
Predicted Routing Delays[2]						
t_{DC}	FO = 1 Routing Delay, Direct Connect		0.2		0.2	ns
t_{FC}	FO = 1 Routing Delay, Fast Connect		1.1		1.3	ns
t_{RD1}	FO = 1 Routing Delay		1.3		1.5	ns
t_{RD2}	FO = 2 Routing Delay		2.2		2.6	ns
t_{RD3}	FO = 3 Routing Delay		3.1		3.6	ns
t_{RD4}	FO = 4 Routing Delay		4.0		4.7	ns
t_{RD8}	FO = 8 Routing Delay		7.8		9.0	ns
t_{RD12}	FO = 12 Routing Delay		10.1		11.9	ns
t_{RD18}	FO = 18 Routing Delay		17.0		19.8	ns
t_{RD24}	FO = 24 Routing Delay		22.4		26.3	ns
R-Cell Timing						
t_{RCO}	Sequential Clock-to-Q		1.5		2.0	ns
t_{CLR}	Asynchronous Clear-to-Q		1.5		2.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	2.0		2.2		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	4.4		5.3		ns
I/O Module Input Propagation Delays						
t_{INYH}	Input Data Pad-to-Y HIGH		4.0		4.7	ns
t_{INYL}	Input Data Pad-to-Y LOW		4.0		4.7	ns
Predicted Input Routing Delays[2]						
t_{IRD1}	FO = 1 Routing Delay		1.3		1.5	ns
t_{IRD2}	FO = 2 Routing Delay		2.2		2.6	ns
t_{IRD3}	FO = 3 Routing Delay		3.1		3.6	ns
t_{IRD4}	FO = 4 Routing Delay		4.0		4.7	ns
t_{IRD8}	FO = 8 Routing Delay		7.8		9.0	ns
t_{IRD12}	FO = 12 Routing Delay		10.1		11.9	ns
t_{IRD18}	FO = 18 Routing Delay		17.0		19.8	ns
t_{IRD24}	FO = 24 Routing Delay		22.4		26.3	ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn}, t_{RCO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD}, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

Table 1-18 • **RT54SX32 Timing Characteristics (Worst-Case Military Conditions, V_{CCR} = 4.75 V, V_{CCA}, V_{CCI} = 3.0 V, T_J = 125°C)**

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
I/O Module – TTL Output Timing*						
t_{DLH}	Data-to-Pad LOW to HIGH		5.1		6.0	ns
t_{DHL}	Data-to-Pad HIGH to LOW		5.1		6.0	ns
t_{ENZL}	Enable-to-Pad, Z to LOW		4.2		5.1	ns
t_{ENZH}	Enable-to-Pad, Z to HIGH		5.1		6.0	ns
t_{ENLZ}	Enable-to-Pad, LOW to Z		8.1		9.4	ns
t_{ENHZ}	Enable-to-Pad, HIGH to Z		4.0		4.7	ns
d_{TLH}	Delta LOW to HIGH		0.09		0.11	ns/pF
d_{THL}	Delta HIGH to LOW		0.09		0.15	ns/pF
Dedicated (Hardwired) Array Clock Network						
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		3.1		3.6	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		3.5		4.0	ns
t_{HPWH}	Minimum Pulse Width HIGH	3.8		4.4		ns
t_{HPWL}	Minimum Pulse Width LOW	3.8		4.4		ns
t_{HCKSW}	Maximum Skew		0.8		0.8	ns
t_{HP}	Minimum Period	7.6		8.9		ns
f_{HMAX}	Maximum Frequency		130		110	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		4.4		5.3	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		4.9		5.6	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		5.3		6.0	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		5.3		6.3	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		5.1		6.0	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		5.3		6.3	ns
t_{RPWH}	Minimum Pulse Width HIGH	5.6		6.7		ns
t_{RPWL}	Minimum Pulse Width LOW	5.6		6.7		ns

Note: **Delays based on 35 pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5 pF.*

Pin Description

CLKA/B **Clock A and B**

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, 3.3 V PCI, or 5.0 V PCI specifications. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating. (For RT54SX72S, these clocks can be configured as user I/O.)

GND **Ground**

LOW supply voltage.

HCLK **Dedicated (Hardwired) Array Clock**

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTL, 3.3 V PCI or 5.0 V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O **Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, 3.3 V PCI, or 5.0 V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

NC **No Connection**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA, I/O, **Probe A/B PRB, I/O**

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O **Test Clock (Input)**

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (see Table 1-2 on page 1-8). This pin functions as an I/O when the JTAG state machine reaches the "logic reset" state.

TDI, I/O **Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 1-2 on page 1-8). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O **Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 1-2 on page 1-8). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TMS **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 boundary scan pins (TCK, TDI, TDO, TRST). In flexible mode, when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-2 on page 1-8). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached five TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O **Boundary Scan Reset Pin**

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active-low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the **Reserve JTAG Reset Pin** check box is cleared in Designer.

V_{CCI} **Supply Voltage**

Supply voltage for I/Os. See Table 1-1 on page 1-8.

V_{CCA} **Supply Voltage**

Supply voltage for Array. See Table 1-1 on page 1-8.

V_{CCR} **Supply Voltage**

Supply voltage for input tolerance (required for internal biasing). See Table 1-1 on page 1-8.

Package Pin Assignments

208-Pin CQFP

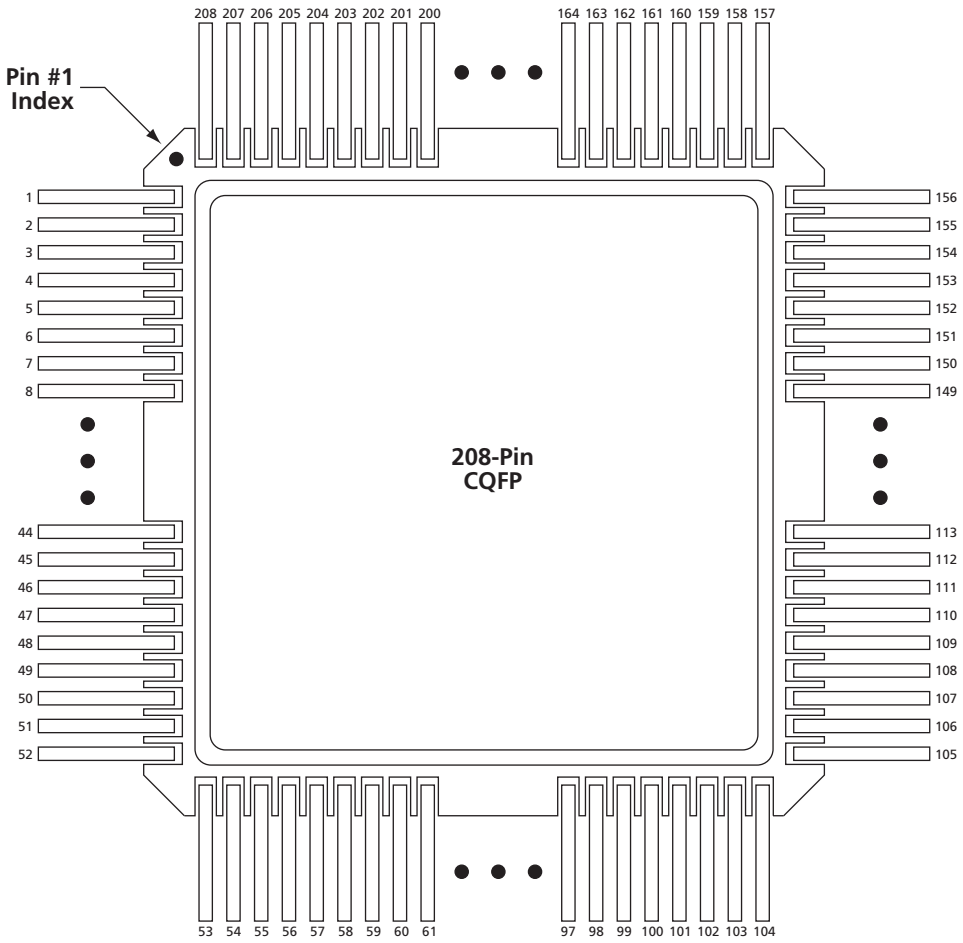


Figure 2-1 • **208-Pin CQFP (Top View)**

208-Pin CQFP				
Pin Number	**A54SX16 Function**	**RT54SX16 Function**	**A54SX32 Function**	**RT54SX32 Function**
1	GND	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O	I/O
4	I/O	I/O	I/O	I/O
5	I/O	I/O	I/O	I/O
6	I/O	I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	I/O	I/O
10	I/O	I/O	I/O	I/O
11	TMS	TMS	TMS	TMS
12	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
13	I/O	I/O	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	I/O	I/O
17	I/O	I/O	I/O	I/O
18	I/O	I/O	I/O	I/O
19	I/O	I/O	I/O	I/O
20	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	I/O	I/O	I/O
23	I/O	I/O	I/O	I/O
24	I/O	I/O	I/O	I/O
25	V_{CCR}	V_{CCR}	V_{CCR}	V_{CCR}
26	GND	GND	GND	GND
27	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
28	GND	GND	GND	GND
29	I/O	I/O	I/O	I/O
30	I/O	TRST	I/O	TRST
31	I/O	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	I/O	I/O	I/O	I/O
34	I/O	I/O	I/O	I/O
35	I/O	I/O	I/O	I/O
36	I/O	I/O	I/O	I/O

208-Pin CQFP				
Pin Number	**A54SX16 Function**	**RT54SX16 Function**	**A54SX32 Function**	**RT54SX32 Function**
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	I/O
39	I/O	I/O	I/O	I/O
40	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
41	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
42	I/O	I/O	I/O	I/O
43	I/O	I/O	I/O	I/O
44	I/O	I/O	I/O	I/O
45	I/O	I/O	I/O	I/O
46	I/O	I/O	I/O	I/O
47	I/O	I/O	I/O	I/O
48	I/O	I/O	I/O	I/O
49	I/O	I/O	I/O	I/O
50	I/O	I/O	I/O	I/O
51	I/O	I/O	I/O	I/O
52	GND	GND	GND	GND
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
61	I/O	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O
63	I/O	I/O	I/O	I/O
64	I/O	I/O	I/O	I/O
65	I/O	I/O	NC	NC
66	I/O	I/O	I/O	I/O
67	I/O	I/O	I/O	I/O
68	I/O	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	I/O	I/O	I/O	I/O
71	I/O	I/O	I/O	I/O
72	I/O	I/O	I/O	I/O

Notes:

1. Pin 30 in RT54SX16 and RT54SX32-CQ208 is a TRST pin.

2. Pin 65 in A54SX32 and RT54SX32-CQ208 is a No Connect.

208-Pin CQFP				
Pin Number	A54SX16 Function	RT54SX16 Function	A54SX32 Function	RT54SX32 Function
73	I/O	I/O	I/O	I/O
74	I/O	I/O	I/O	I/O
75	I/O	I/O	I/O	I/O
76	PRB, I/O	PRB, I/O	PRB, I/O	PRB, I/O
77	GND	GND	GND	GND
78	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
79	GND	GND	GND	GND
80	V_{CCR}	V_{CCR}	V_{CCR}	V_{CCR}
81	I/O	I/O	I/O	I/O
82	HCLK	HCLK	HCLK	HCLK
83	I/O	I/O	I/O	I/O
84	I/O	I/O	I/O	I/O
85	I/O	I/O	I/O	I/O
86	I/O	I/O	I/O	I/O
87	I/O	I/O	I/O	I/O
88	I/O	I/O	I/O	I/O
89	I/O	I/O	I/O	I/O
90	I/O	I/O	I/O	I/O
91	I/O	I/O	I/O	I/O
92	I/O	I/O	I/O	I/O
93	I/O	I/O	I/O	I/O
94	I/O	I/O	I/O	I/O
95	I/O	I/O	I/O	I/O
96	I/O	I/O	I/O	I/O
97	I/O	I/O	I/O	I/O
98	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
99	I/O	I/O	I/O	I/O
100	I/O	I/O	I/O	I/O
101	I/O	I/O	I/O	I/O
102	I/O	I/O	I/O	I/O
103	TDO, I/O	TDO, I/O	TDO, I/O	TDO, I/O
104	I/O	I/O	I/O	I/O
105	GND	GND	GND	GND
106	I/O	I/O	I/O	I/O
107	I/O	I/O	I/O	I/O
108	I/O	I/O	I/O	I/O

208-Pin CQFP				
Pin Number	A54SX16 Function	RT54SX16 Function	A54SX32 Function	RT54SX32 Function
109	I/O	I/O	I/O	I/O
110	I/O	I/O	I/O	I/O
111	I/O	I/O	I/O	I/O
112	I/O	I/O	I/O	I/O
113	I/O	I/O	I/O	I/O
114	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
115	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
116	I/O	I/O	I/O	I/O
117	I/O	I/O	I/O	I/O
118	I/O	I/O	I/O	I/O
119	I/O	I/O	I/O	I/O
120	I/O	I/O	I/O	I/O
121	I/O	I/O	I/O	I/O
122	I/O	I/O	I/O	I/O
123	I/O	I/O	I/O	I/O
124	I/O	I/O	I/O	I/O
125	I/O	I/O	I/O	I/O
126	I/O	I/O	I/O	I/O
127	I/O	I/O	I/O	I/O
128	I/O	I/O	I/O	I/O
129	GND	GND	GND	GND
130	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
131	GND	GND	GND	GND
132	V_{CCR}	V_{CCR}	V_{CCR}	V_{CCR}
133	I/O	I/O	I/O	I/O
134	I/O	I/O	I/O	I/O
135	I/O	I/O	I/O	I/O
136	I/O	I/O	I/O	I/O
137	I/O	I/O	I/O	I/O
138	I/O	I/O	I/O	I/O
139	I/O	I/O	I/O	I/O
140	I/O	I/O	I/O	I/O
141	I/O	I/O	I/O	I/O
142	I/O	I/O	I/O	I/O
143	I/O	I/O	I/O	I/O
144	I/O	I/O	I/O	I/O

Notes:

1. *Pin 30 in RT54SX16 and RT54SX32-CQ208 is a TRST pin.*
2. *Pin 65 in A54SX32 and RT54SX32-CQ208 is a No Connect.*

208-Pin CQFP				
Pin Number	**A54SX16 Function**	**RT54SX16 Function**	**A54SX32 Function**	**RT54SX32 Function**
145	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
146	GND	GND	GND	GND
147	I/O	I/O	I/O	I/O
148	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
149	I/O	I/O	I/O	I/O
150	I/O	I/O	I/O	I/O
151	I/O	I/O	I/O	I/O
152	I/O	I/O	I/O	I/O
153	I/O	I/O	I/O	I/O
154	I/O	I/O	I/O	I/O
155	I/O	I/O	I/O	I/O
156	I/O	I/O	I/O	I/O
157	GND	GND	GND	GND
158	I/O	I/O	I/O	I/O
159	I/O	I/O	I/O	I/O
160	I/O	I/O	I/O	I/O
161	I/O	I/O	I/O	I/O
162	I/O	I/O	I/O	I/O
163	I/O	I/O	I/O	I/O
164	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
165	I/O	I/O	I/O	I/O
166	I/O	I/O	I/O	I/O
167	I/O	I/O	I/O	I/O
168	I/O	I/O	I/O	I/O
169	I/O	I/O	I/O	I/O
170	I/O	I/O	I/O	I/O
171	I/O	I/O	I/O	I/O
172	I/O	I/O	I/O	I/O
173	I/O	I/O	I/O	I/O
174	I/O	I/O	I/O	I/O
175	I/O	I/O	I/O	I/O
176	I/O	I/O	I/O	I/O
177	I/O	I/O	I/O	I/O
178	I/O	I/O	I/O	I/O
179	I/O	I/O	I/O	I/O
180	CLKA	CLKA	CLKA	CLKA
181	CLKB	CLKB	CLKB	CLKB
182	V_{CCR}	V_{CCR}	V_{CCR}	V_{CCR}
183	GND	GND	GND	GND
184	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
185	GND	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O	I/O
188	I/O	I/O	I/O	I/O
189	I/O	I/O	I/O	I/O
190	I/O	I/O	I/O	I/O
191	I/O	I/O	I/O	I/O
192	I/O	I/O	I/O	I/O
193	I/O	I/O	I/O	I/O
194	I/O	I/O	I/O	I/O
195	I/O	I/O	I/O	I/O
196	I/O	I/O	I/O	I/O
197	I/O	I/O	I/O	I/O
198	I/O	I/O	I/O	I/O
199	I/O	I/O	I/O	I/O
200	I/O	I/O	I/O	I/O
201	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
202	I/O	I/O	I/O	I/O
203	I/O	I/O	I/O	I/O
204	I/O	I/O	I/O	I/O
205	I/O	I/O	I/O	I/O
206	I/O	I/O	I/O	I/O
207	I/O	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O	TCK, I/O

Notes:

1. *Pin 30 in RT54SX16 and RT54SX32-CQ208 is a TRST pin.*
2. *Pin 65 in A54SX32 and RT54SX32-CQ208 is a No Connect.*

256-Pin CQFP

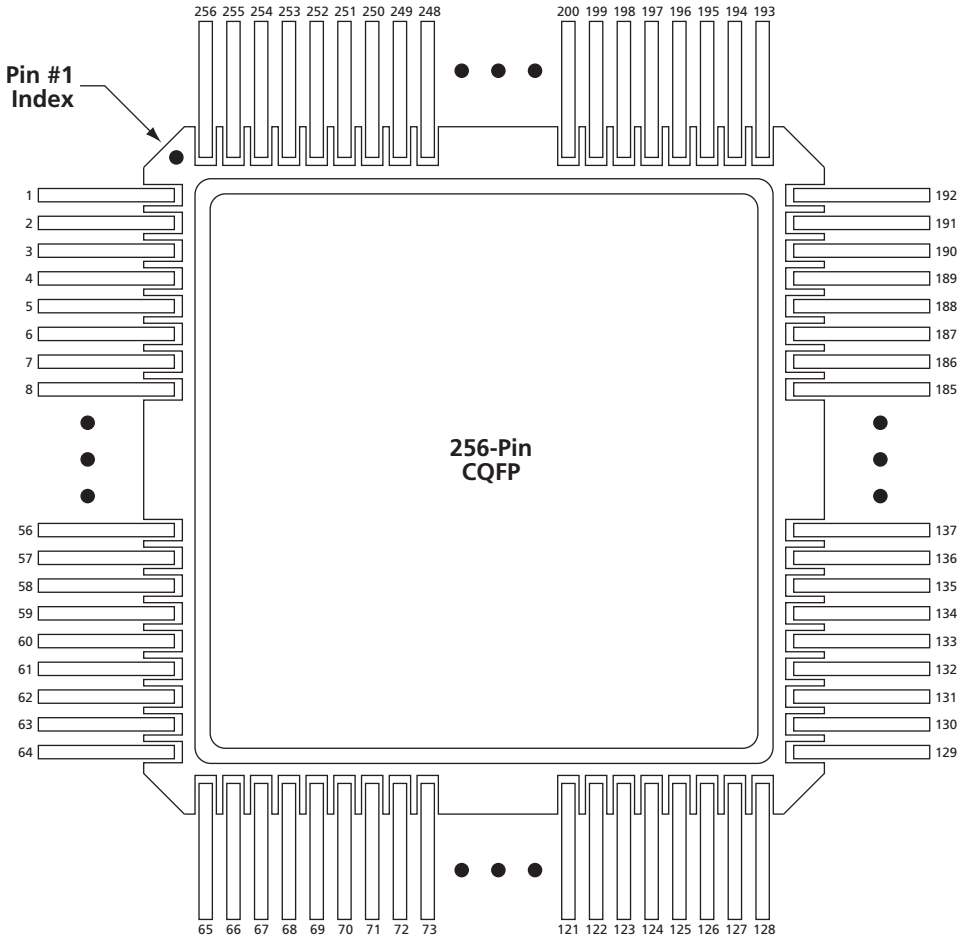


Figure 2-2 • **256-Pin CQFP (Top View)**

256-Pin CQFP				
Pin Number	**A54SX16 Function**	**RT54SX16 Function**	**A54SX32 Function**	**RT54SX32 Function**
1	GND	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O	I/O
4	I/O	I/O	I/O	I/O
5	I/O	I/O	I/O	I/O
6	I/O	I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	I/O	I/O
10	I/O	I/O	I/O	I/O
11	TMS	TMS	TMS	TMS
12	NC	NC	I/O	I/O
13	NC	NC	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	NC	NC	I/O	I/O
17	I/O	I/O	I/O	I/O
18	I/O	I/O	I/O	I/O
19	I/O	I/O	I/O	I/O
20	NC	NC	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	I/O	I/O	I/O
23	I/O	I/O	I/O	I/O
24	I/O	I/O	I/O	I/O
25	I/O	I/O	I/O	I/O
26	I/O	I/O	I/O	I/O
27	I/O	I/O	I/O	I/O
28	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
29	GND	GND	GND	GND
30	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
31	GND	GND	GND	GND
32	NC	NC	I/O	I/O
33	I/O	I/O	I/O	I/O
34	I/O	TRST	I/O	TRST
35	I/O	I/O	I/O	I/O
36	NC	NC	I/O	I/O
37	I/O	I/O	I/O	I/O

256-Pin CQFP				
Pin Number	**A54SX16 Function**	**RT54SX16 Function**	**A54SX32 Function**	**RT54SX32 Function**
38	I/O	I/O	I/O	I/O
39	I/O	I/O	I/O	I/O
40	I/O	I/O	I/O	I/O
41	NC	NC	I/O	I/O
42	I/O	I/O	I/O	I/O
43	I/O	I/O	I/O	I/O
44	I/O	I/O	I/O	I/O
45	I/O	I/O	I/O	I/O
46	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
47	I/O	I/O	I/O	I/O
48	NC	NC	I/O	I/O
49	I/O	I/O	I/O	I/O
50	I/O	I/O	I/O	I/O
51	NC	NC	I/O	I/O
52	I/O	I/O	I/O	I/O
53	I/O	I/O	I/O	I/O
54	NC	NC	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	NC	NC	I/O	I/O
58	I/O	I/O	I/O	I/O
59	GND	GND	GND	GND
60	I/O	I/O	I/O	I/O
61	NC	NC	I/O	I/O
62	I/O	I/O	I/O	I/O
63	NC	NC	I/O	I/O
64	I/O	I/O	I/O	I/O
65	I/O	I/O	I/O	I/O
66	I/O	I/O	I/O	I/O
67	I/O	I/O	I/O	I/O
68	NC	NC	I/O	I/O
69	I/O	I/O	I/O	I/O
70	I/O	I/O	I/O	I/O
71	I/O	I/O	I/O	I/O
72	I/O	I/O	I/O	I/O
73	NC	NC	I/O	I/O
74	I/O	I/O	I/O	I/O

Note: *Pin 34 in RT54SX16 and RT54SX32-CQ256 is a TRST pin.*

256-Pin CQFP				
Pin Number	**A54SX16 Function**	**RT54SX16 Function**	**A54SX32 Function**	**RT54SX32 Function**
75	I/O	I/O	I/O	I/O
76	I/O	I/O	I/O	I/O
77	NC	NC	I/O	I/O
78	I/O	I/O	I/O	I/O
79	I/O	I/O	I/O	I/O
80	I/O	I/O	I/O	I/O
81	I/O	I/O	I/O	I/O
82	I/O	I/O	I/O	I/O
83	I/O	I/O	I/O	I/O
84	I/O	I/O	I/O	I/O
85	I/O	I/O	I/O	I/O
86	I/O	I/O	I/O	I/O
87	I/O	I/O	I/O	I/O
88	I/O	I/O	I/O	I/O
89	I/O	I/O	I/O	I/O
90	PRB, I/O	PRB, I/O	PRB, I/O	PRB, I/O
91	GND	GND	GND	GND
92	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
93	GND	GND	GND	GND
94	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
95	I/O	I/O	I/O	I/O
96	HCLK	HCLK	HCLK	HCLK
97	I/O	I/O	I/O	I/O
98	NC	NC	I/O	I/O
99	I/O	I/O	I/O	I/O
100	I/O	I/O	I/O	I/O
101	I/O	I/O	I/O	I/O
102	NC	NC	I/O	I/O
103	I/O	I/O	I/O	I/O
104	I/O	I/O	I/O	I/O
105	I/O	I/O	I/O	I/O
106	NC	NC	I/O	I/O
107	I/O	I/O	I/O	I/O
108	I/O	I/O	I/O	I/O
109	I/O	I/O	I/O	I/O
110	GND	GND	GND	GND
111	I/O	I/O	I/O	I/O

256-Pin CQFP				
Pin Number	**A54SX16 Function**	**RT54SX16 Function**	**A54SX32 Function**	**RT54SX32 Function**
112	I/O	I/O	I/O	I/O
113	I/O	I/O	I/O	I/O
114	NC	NC	I/O	I/O
115	I/O	I/O	I/O	I/O
116	I/O	I/O	I/O	I/O
117	I/O	I/O	I/O	I/O
118	NC	NC	I/O	I/O
119	I/O	I/O	I/O	I/O
120	I/O	I/O	I/O	I/O
121	I/O	I/O	I/O	I/O
122	NC	NC	I/O	I/O
123	I/O	I/O	I/O	I/O
124	I/O	I/O	I/O	I/O
125	NC	NC	I/O	I/O
126	TDO, I/O	TDO, I/O	TDO, I/O	TDO, I/O
127	NC	NC	I/O	I/O
128	GND	GND	GND	GND
129	I/O	I/O	I/O	I/O
130	I/O	I/O	I/O	I/O
131	I/O	I/O	I/O	I/O
132	I/O	I/O	I/O	I/O
133	I/O	I/O	I/O	I/O
134	I/O	I/O	I/O	I/O
135	I/O	I/O	I/O	I/O
136	I/O	I/O	I/O	I/O
137	I/O	I/O	I/O	I/O
138	NC	NC	I/O	I/O
139	NC	NC	I/O	I/O
140	NC	NC	I/O	I/O
141	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
142	I/O	I/O	I/O	I/O
143	I/O	I/O	I/O	I/O
144	I/O	I/O	I/O	I/O
145	I/O	I/O	I/O	I/O
146	I/O	I/O	I/O	I/O
147	I/O	I/O	I/O	I/O
148	I/O	I/O	I/O	I/O

Note: *Pin 34 in RT54SX16 and RT54SX32-CQ256 is a TRST pin.*

256-Pin CQFP				
Pin Number	A54SX16 Function	RT54SX16 Function	A54SX32 Function	RT54SX32 Function
149	I/O	I/O	I/O	I/O
150	I/O	I/O	I/O	I/O
151	I/O	I/O	I/O	I/O
152	I/O	I/O	I/O	I/O
153	I/O	I/O	I/O	I/O
154	I/O	I/O	I/O	I/O
155	NC	NC	I/O	I/O
156	NC	NC	I/O	I/O
157	NC	NC	I/O	I/O
158	GND	GND	GND	GND
159	V_{CCR}	V_{CCR}	V_{CCR}	V_{CCR}
160	GND	GND	GND	GND
161	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
162	I/O	I/O	I/O	I/O
163	I/O	I/O	I/O	I/O
164	I/O	I/O	I/O	I/O
165	I/O	I/O	I/O	I/O
166	I/O	I/O	I/O	I/O
167	I/O	I/O	I/O	I/O
168	I/O	I/O	I/O	I/O
169	I/O	I/O	I/O	I/O
170	I/O	I/O	I/O	I/O
171	I/O	I/O	I/O	I/O
172	I/O	I/O	I/O	I/O
173	I/O	I/O	I/O	I/O
174	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
175	GND	GND	GND	GND
176	GND	GND	GND	GND
177	I/O	I/O	I/O	I/O
178	NC	NC	I/O	I/O
179	I/O	I/O	I/O	I/O
180	I/O	I/O	I/O	I/O
181	NC	NC	I/O	I/O
182	I/O	I/O	I/O	I/O
183	I/O	I/O	I/O	I/O
184	NC	NC	I/O	I/O
185	I/O	I/O	I/O	I/O

256-Pin CQFP				
Pin Number	A54SX16 Function	RT54SX16 Function	A54SX32 Function	RT54SX32 Function
186	I/O	I/O	I/O	I/O
187	NC	NC	I/O	I/O
188	I/O	I/O	I/O	I/O
189	GND	GND	GND	GND
190	I/O	I/O	I/O	I/O
191	NC	NC	I/O	I/O
192	NC	NC	I/O	I/O
193	I/O	I/O	I/O	I/O
194	I/O	I/O	I/O	I/O
195	NC	NC	I/O	I/O
196	I/O	I/O	I/O	I/O
197	I/O	I/O	I/O	I/O
198	I/O	I/O	I/O	I/O
199	I/O	I/O	I/O	I/O
200	NC	NC	I/O	I/O
201	I/O	I/O	I/O	I/O
202	I/O	I/O	I/O	I/O
203	I/O	I/O	I/O	I/O
204	NC	NC	I/O	I/O
205	I/O	I/O	I/O	I/O
206	I/O	I/O	I/O	I/O
207	I/O	I/O	I/O	I/O
208	NC	NC	I/O	I/O
209	I/O	I/O	I/O	I/O
210	I/O	I/O	I/O	I/O
211	I/O	I/O	I/O	I/O
212	I/O	I/O	I/O	I/O
213	I/O	I/O	I/O	I/O
214	I/O	I/O	I/O	I/O
215	I/O	I/O	I/O	I/O
216	I/O	I/O	I/O	I/O
217	I/O	I/O	I/O	I/O
218	I/O	I/O	I/O	I/O
219	CLKA	CLKA	CLKA	CLKA
220	CLKB	CLKB	CLKB	CLKB
221	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
222	GND	GND	GND	GND

Note: *Pin 34 in RT54SX16 and RT54SX32-CQ256 is a TRST pin.*

256-Pin CQFP				
Pin Number	**A54SX16 Function**	**RT54SX16 Function**	**A54SX32 Function**	**RT54SX32 Function**
223	V_{CCR}	V_{CCR}	V_{CCR}	V_{CCR}
224	GND	GND	GND	GND
225	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O
226	I/O	I/O	I/O	I/O
227	NC	NC	I/O	I/O
228	I/O	I/O	I/O	I/O
229	I/O	I/O	I/O	I/O
230	I/O	I/O	I/O	I/O
231	I/O	I/O	I/O	I/O
232	NC	NC	I/O	I/O
233	I/O	I/O	I/O	I/O
234	I/O	I/O	I/O	I/O
235	I/O	I/O	I/O	I/O
236	NC	NC	I/O	I/O
237	I/O	I/O	I/O	I/O
238	I/O	I/O	I/O	I/O
239	NC	NC	I/O	I/O
240	GND	GND	GND	GND
241	I/O	I/O	I/O	I/O
242	I/O	I/O	I/O	I/O
243	NC	NC	I/O	I/O
244	I/O	I/O	I/O	I/O
245	I/O	I/O	I/O	I/O
246	I/O	I/O	I/O	I/O
247	NC	NC	I/O	I/O
248	I/O	I/O	I/O	I/O
249	I/O	I/O	I/O	I/O
250	NC	NC	I/O	I/O
251	I/O	I/O	I/O	I/O
252	I/O	I/O	I/O	I/O
253	NC	NC	I/O	I/O
254	I/O	I/O	I/O	I/O
255	I/O	I/O	I/O	I/O
256	TCK, I/O	TCK, I/O	TCK, I/O	TCK, I/O

Note: *Pin 34 in RT54SX16 and RT54SX32-CQ256 is a TRST pin.*

Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v2.1)	Page
v2.0	The "Product Profile" was updated.	i
	The "Ordering Information" was updated.	ii
	The "Product Plan" was updated.	ii
	Table 1-1 was updated.	8
Preliminary v1.5	Power-up and -down sequencing information was modified: damage to the device is possible when 3.3 V is powered-up first and when 5.0 V is powered-down first.	13
	The last line of EQ 1-4 was cut off in the previous version. It has been replaced in the existing version.	16
Preliminary v1.5.2	The User I/Os changed.	8
	The following sections are new or were updated: "Clock Resources", "Performance", "I/O Modules", "Power Requirements", "Boundary Scan Testing (BST)","Configuring Diagnostic Pins", "TRST Pin", "Dedicated Test Mode", "Flexible Mode", "Development Tool Support", "RTSX Probe Circuit Control Pins", and "Design Considerations".	7 to 11
	The "Pin Description" has been updated.	28
	Note that the "Package Characteristics and Mechanical Drawings" section has been eliminated from the data sheet. The mechanical drawings are now contained in a separate document, *Package Characteristics and Mechanical Drawings*, available on the Actel web site.	N/A

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

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