DATA SHEET

EM198810

2.4 GHz ISM Band Transceiver/Framer IC

Preliminary Data Sheet

ELAN MICROELECTRONICS CORP.
No.12, Innovation 1st RD., Science-based Industrial Park
Hsin Chu, Taiwan, R.O.C.
TEL: (03) 5639977
FAX: (03) 5782037(SL) 5630118 (SA2)

CONTENTS

2.4 GHz ISM BAND TRANSCEIVER/FRAMER IC

1. FEATURES

The EM198810 is a CMOS integrated circuit that performs all functions from the antenna to the microcontroller for transmission and reception of a 2.4GHz digital data. This transceiver IC integrates most of the functions required for data transmission into a single integrated circuit. Additionally, the programmability implemented reduces significantly external components count, board space requirements and external adjustments.

Key Features:

- Combines 2.4 GHz GFSK RF transceiver with 8-bit data framer function
- Eliminates need for external software or hardware FIFO; offloads MCU for other tasks
- Simple microprocessor interface – 4 wires for SPI, plus 3 wires for RST/buffer control
- Each transmit, receive buffer is 64 bytes deep
- Long packets are possible if buffers are read/written before overflow/underflow occurs
- Always 1Mbps over-the-air symbol rate, regardless of MCU speed or architecture
- Preamble can be 1 to 8 bytes
- Supports 1, 2, 3, or 4 word address (up to 64 bits)
- Various Payload data formats to eliminate DC offset, enhance receive clock recovery and BER
- Programmable data whitening
- Supports Forward Error Correction (FEC): none, 1/3, or 2/3
- Supports 16-bit CRC
- Baseband output clock available
- Power management for minimizing current consumption
- 5x5mm QFN package with minimum RF parasitic
- Lead-free packaging and dice is available on request

Applications

- Wireless devices that need quick time-to-market
- Simple and fast wireless data networks
- Cordless headsets and Cellular Phones
- Wireless streaming audio
- Wireless voice and VOIP
- Wireless Skype earphone
- Home and factory automation
- Wireless security and access control
- Battery Powered wireless devices

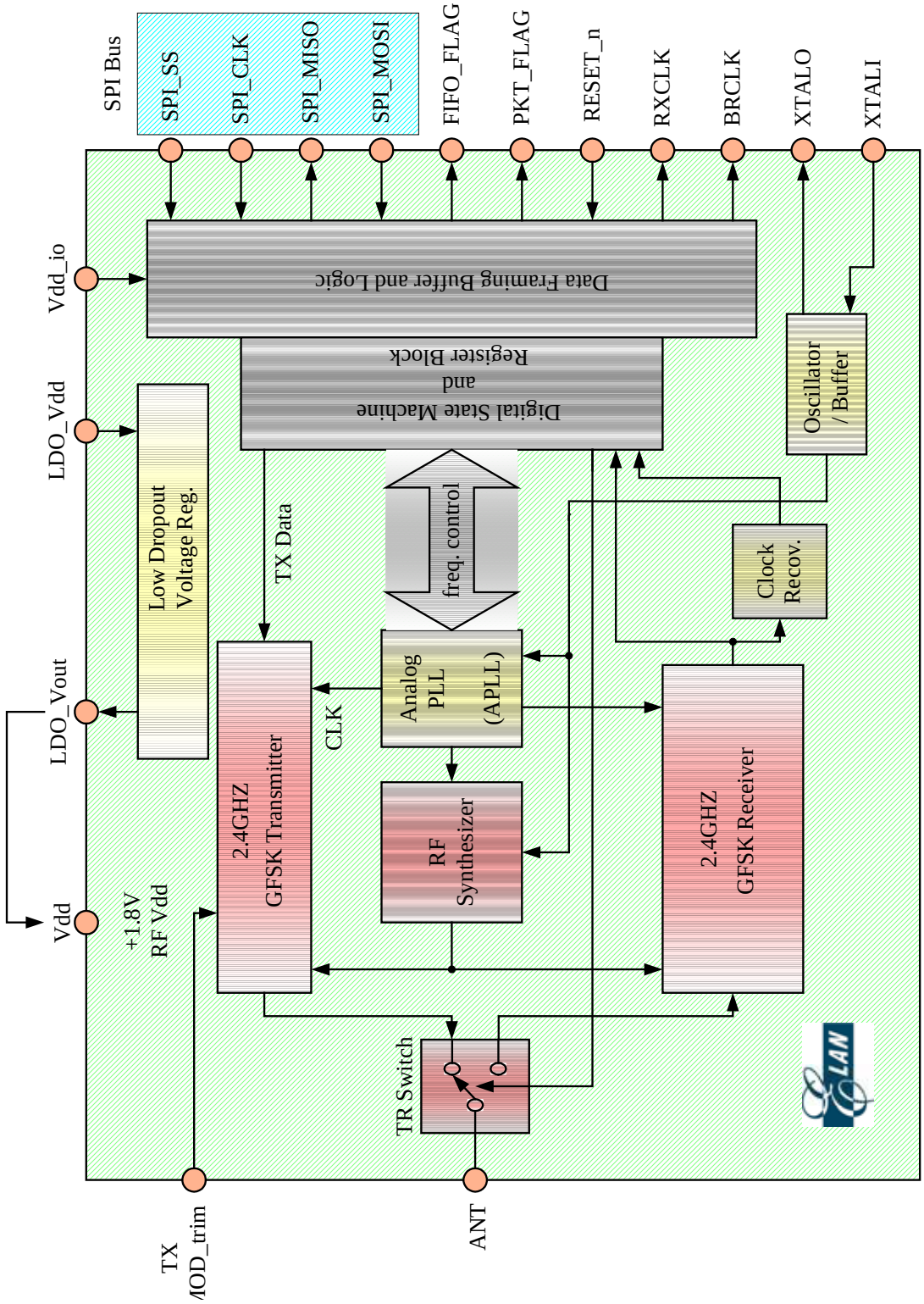
1.1 Description

The Elan EM198810 IC is a low-cost, fully integrated CMOS radio frequency (RF) transceiver block, combined with a 64-byte buffered framer block. The RF transceiver block is a self-contained, fast-hopping GFSK data modem, optimised for use in the widely available 2.4 GHz ISM band. It contains transmit, receive, VCO and PLL functions, including an on-chip channel filter and resonator, thus minimizing the need for external components. The receiver utilizes extensive digital processing for excellent overall performance, even in the presence of interference and transmitter impairments. Transmit power is digitally controlled. The low-IF receiver architecture results in sensitivity to -80dBm or better, with impressive selectivity.
In normal applications, the EM198810 is connected to a low cost microcontroller(ex:EM78P451S).

In normal application The on-chip framer processes and stores the RF data in the background, unloading this critical timing function from the MCU. This lowers MCU speed requirements, expedites product development time, and frees the MCU for implementing additional product features.

The framer register settings determine the over-the-air formatting characteristics. Many configurations are possible, depending on the user's specific needs. Raw transmit data is easily sent over-the-air as a complete frame of data, with preamble, address, payload, and CRC. Receiving data is just the opposite, using the preamble to train the receiver clock recovery, then the address is checked, then the data is reverse formatted for receive, followed by CRC. All of this is done in hardware to ease the programming and overhead requirements of the baseband MCU.
For longer battery life, power consumption is minimized by automatic enabling of the various transmit, receive, PLL, and PA sections, depending on the instantaneous state of the chip. A sleep mode is also provided for ultra low current consumption.
This product is available in 32-lead 5x5 mm JEDEC standard QFN package, featuring an exposed pad on the bottom for best RF characteristics. Lead-free RoHS compliant packaging is available on request.

2. Block diagram



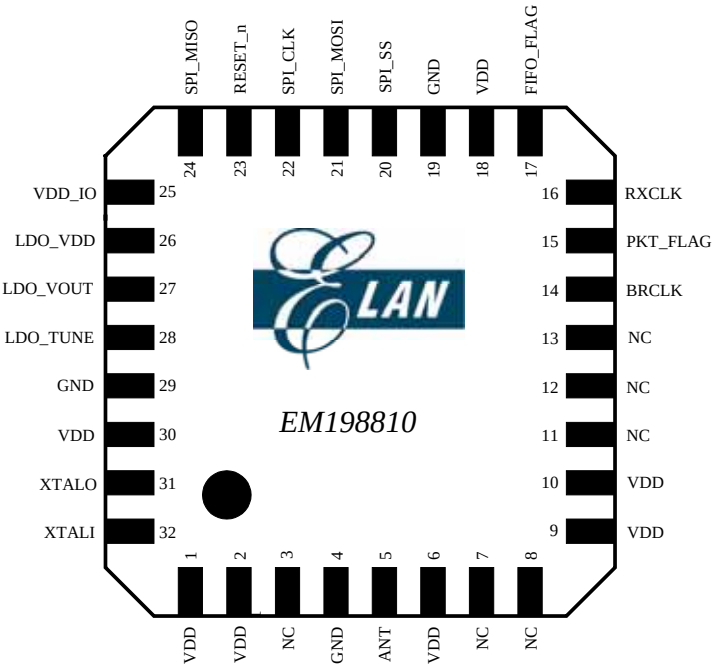
- Fig. 1 –

3. Pins names and pins location

3.1 Pins names

SYMBOL	Type	PIN	DESCRIPTION
VDD	PWR	1	Power supply voltage.
VDD	PWR	2	
NC	--	3	DO NOT CONNECT. Reserved for factory test.
GND	GND	4	Ground connection.
ANT	50ΩRF	5	RF input/output.
VDD	PWR	6	Power supply voltage.
NC	--	7	DO NOT CONNECT. Reserved for factory test.
NC	--	8	
VDD	PWR	9	Power supply voltage.
VDD	PWR	10	
NC	--	11	DO NOT CONNECT. Reserved for factory test.
NC	--	12	
NC	--	13	
BRCLK	O	14	Outputs 1MHz TX symbol clock, 12MHz APLL, or crystal clock. See register definitions for details.
PKT_FLAG	O	15	Transmit/Receive packet process flag.
RXCLK	O	16	Receiver symbol timing clock recovery output. Fixed at 1MHz fundamental rate.
FIFO_FLAG	O	17	FIFO full/empty flag.
VDD	PWR	18	Power supply voltage.
GND	GND	19	Ground connection.
SPI_SS	I	20	Enable line for the SPI bus. Active low.
SPI_MOSI	I	21	Data input for the SPI bus.
SPI_CLK	I	22	Clock line for the SPI bus.
RESET_n	I	23	When RESET_n is low, most of the chip shuts down to conserve power. When raised high, RESET_n is used to turn on the chip,restoring all registers to their default value.
SPI_MISO	O	24	Data output for the SPI bus.
VDD_IO	PWR	25	Vdd for the digital i/o pins. Nominally +3.3 VDC.
LDO_VDD	PWR	26	Unregulated input to the on-chip LDO volt. regulator.
LDO_OUT	PWR	27	+1.8V output of the on-chip LDO voltage regulator.
LOD_TUNE	--	28	Fine-tune for the on-chip LDO voltage regulator.
GND	GND	29	Ground connection.
VDD	PWR	30	Power supply voltage.
XTALO	AO	31	Output of the crystal oscillator gain block.
XTALI	AI	32	Input to the crystal oscillator gain block.
GND	GND	Exposed pad	Ground connection.

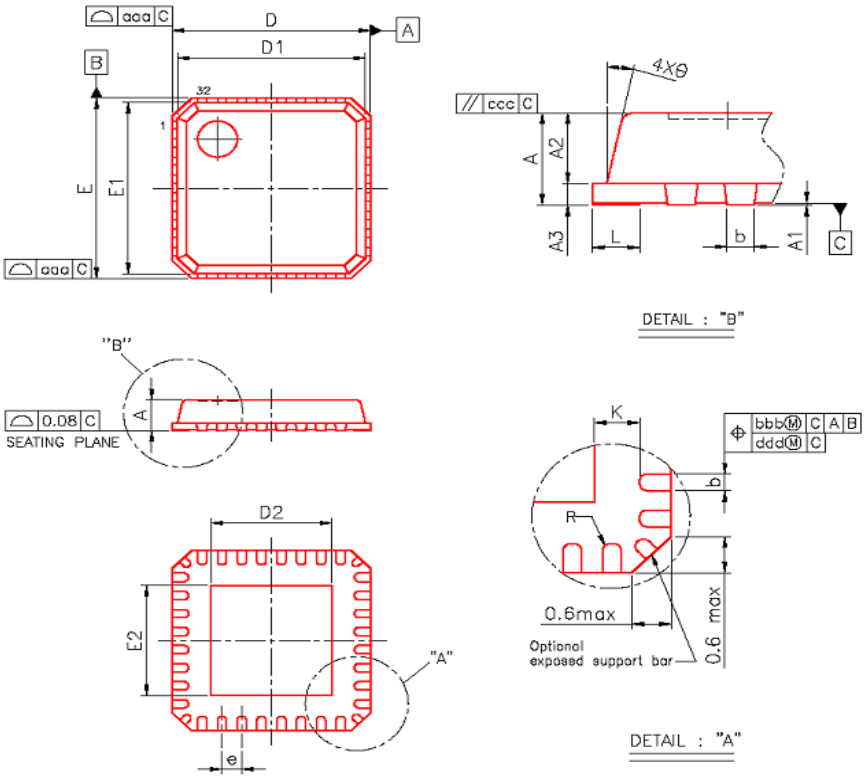
- Table 1 –



- Figure 2 –

3.2 Package Outline

QFN32 Lead Exposed Pad Package, 5x5 mm Pkg. 0.5mm Pitch (JEDEC) MO-220-A



Dim.	Min.	Nom.	Max.	Dim.	Min.	Nom.	Max.
A	0.80	0.85	1.00	L	0.30	0.40	0.50
A1	0.00	0.02	0.05	θ	0°	–	12°
A2	0.60	0.65	0.80	R	0.09	–	–
A3		0.20 REF		K	0.20	–	–
b	0.18	0.25	0.30	aaa	–	–	0.15
D/E		5.00 BSC		bbb	–	–	0.10
D1/E1		4.75 BSC		ccc	–	–	0.10
D2/E2	3.15	3.30	3.45	ddd	–	–	0.05
e		0.50 BSC					

3.3 Pads name and location

SYMBOL	PAD no	Center pad position X;Y in microns
PLL_VDD(A)	1	35.837 ; 1622.464
RF_VSS(A)	2	35.836 ; 1498.956
VCO_GDD(A)	3	35.837 ; 1378.956
nc	4	35.387 ; 1257.956
RF_VSS(A)	5	35.383 ; 1018.956
ANTb(A)	6	35.837 ; 897.956
RF_VSS(A)	7	35.837 ; 778.957
ANT(A)	8	35.789 ; 657.956
RF_VSS(A)	9	35.835 ; 583.952
RF_VDD(A)	10	35.837 ; 418.957
Injp(A)	11	35.837 ; 178.096
Injp(A)	12	222.918 ; 35.006
IF_VDD(A)	13	341.926 ; 35.006
VCO_VDD(A)	14	462.016 ; 35.006
AMS_AVDD(A)	15	581.926 ; 35.006
MONIp(A)	16	702.926 ; 35.006
MONIn(A)	17	1464.189 ; 35.005
TP_BG_IV/TP_VTUNE(A)	18	1584.188 ; 35.006
BRCLK(D)	19	1820.067 ; 34.006
BPKTCTL(D)	20	1940.067 ; 34.006
RXDATA(D)	21	2081.185 ; 219.891
RXCLK(D)	22	2081.185 ; 339.891
testse(D)	23	2081.185 ; 459.891
BXTLEN(D)	24	2081.185 ; 579.891
TEST1(D)	25	2081.185 ; 699.891
VDD_DIG(D)	26	2081.185 ; 821.027
VSS_DIG(D)	27	2081.185 ; 941.027
BnDEN(D)	28	2081.185 ; 1059.839
TEST2(D)	29	2081.185 ; 1179.893
BDDATA(D)	30	2081.185 ; 1299.893
BDCLK(D)	31	2081.185 ; 1420.890
BnPWR(D)	32	2081.185 ; 1539.891
BDATA1(D)	33	2081.185 ; 1659.889
spi_select(D)	34	1885.495 ; 1804.847
VDD_IO(D)	35	1762.415 ; 1804.847
ckpha(D)	36	1641.438 ; 1804.847
LDO_VDD(A)	37	1445.424 ; 1804.847
LDO_OUT_VDD(A)	38	1318.773 ; 1803.847
LDO_TUNE(A)	39	1199.684 ; 1803.847
AMS_DVSS(A)	40	1075.434 ; 1803.847
AMS_DVDD(A)	41	955.348 ; 1803.847
XTALO(A)	42	833.526 ; 1803.946
XTALI(A)	43	671.538 ; 1803.946
VCO_VSS(A)	44	550.438 ; 1803.847

- Table 2 -

3.4 Order information

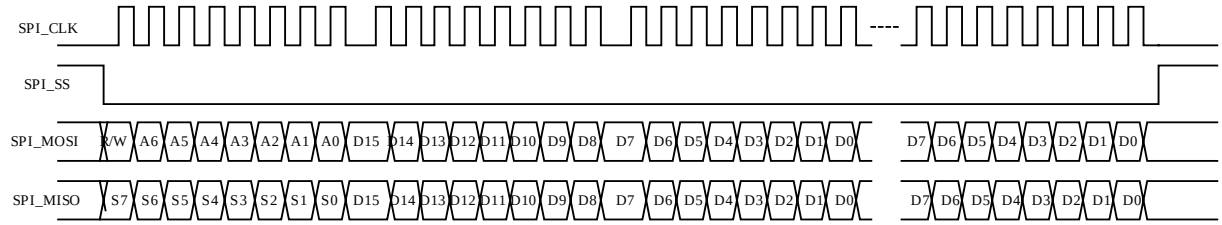
Type number	Package	
	Name	Description
EM198810W	QFN32	Plastic, quad flat package; no leads; 32 terminals; body 5 x 5 x 0.8 mm
EM198810H	Bare die	available

4 Digital Base Band Interface

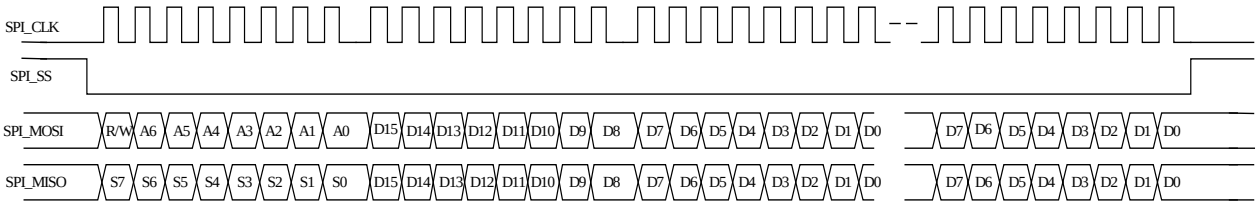
4.1 SPI Command Format

The SPI interface is used to program the IC via the 4 pins SPI_CLK, SPI_SS, SPI_MOSI and SPI_MISO. The SPI_MOSI and SPI_CLK pins are used to load data into an internal shift register. The SPI_MOSI and SPI_CLK pins are use to send data to microcontroller. The data are loaded into the shift register and sent to microcontroller on the rising edge of the clock SPI_CLK and latched on the rising edge of the SPI_SS signal. When the SPI_SS pin is high, the data stored in the shift register is retained even if a SPI_CLK is applied. When the SPI_SS pin is low the data can be rewritten and resent. Inputs timing of the SPI_CLK, SPI_SS, SPI_MOSI and SPI_MISOD are shown in the Fig.2.

Format 1
CKPHA = 0:



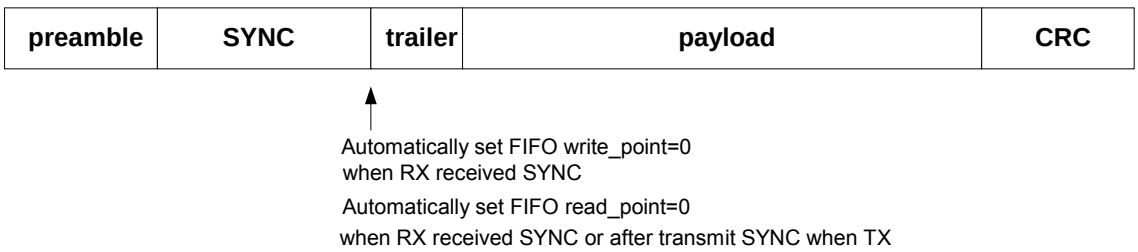
Format 2
CKPHA = 1:



- Fig. 3 –

4.2 Register Information

4.2.1 Package type define and FIFO point set



- Figure 4 –

* Preamble: 1 ~ 8 bytes programmable
* SYNC: 32/48/64 bits programmable as device syncword
* Trailer: 4~16 bits programmable
* Payload: TX/RX data, there are 4 data types: raw data, 8_10 bits, Manchester, interleave with FEC option
* CRC: 16 bit CRC is option

Note: For transmit, it is needed to clear FIFO write point before application write in data via access reg82[15].

4.2.2 Digital Interface

It is very simple interface with application, consisting of SPI interface plus two handshake signals (Table 2).
The EM198810 SPI can only support slave mode.

Pin	Description
SPI_CLK	SPI clock input
SPI_SS	SPI slave select input
SPI_MOSI	SPI data in
SPI_MISO	SPI data out
PKT_FLAG	Packet TX/RX flag
FIFO_FLAG	FIFO full/empty
RESET_n	Reset input, active low

- Table 3 -

4.2.3 Typical Register Values

The following register values (Table 3) are recommended for the Elan Microelectronics details define refer to registers definitions

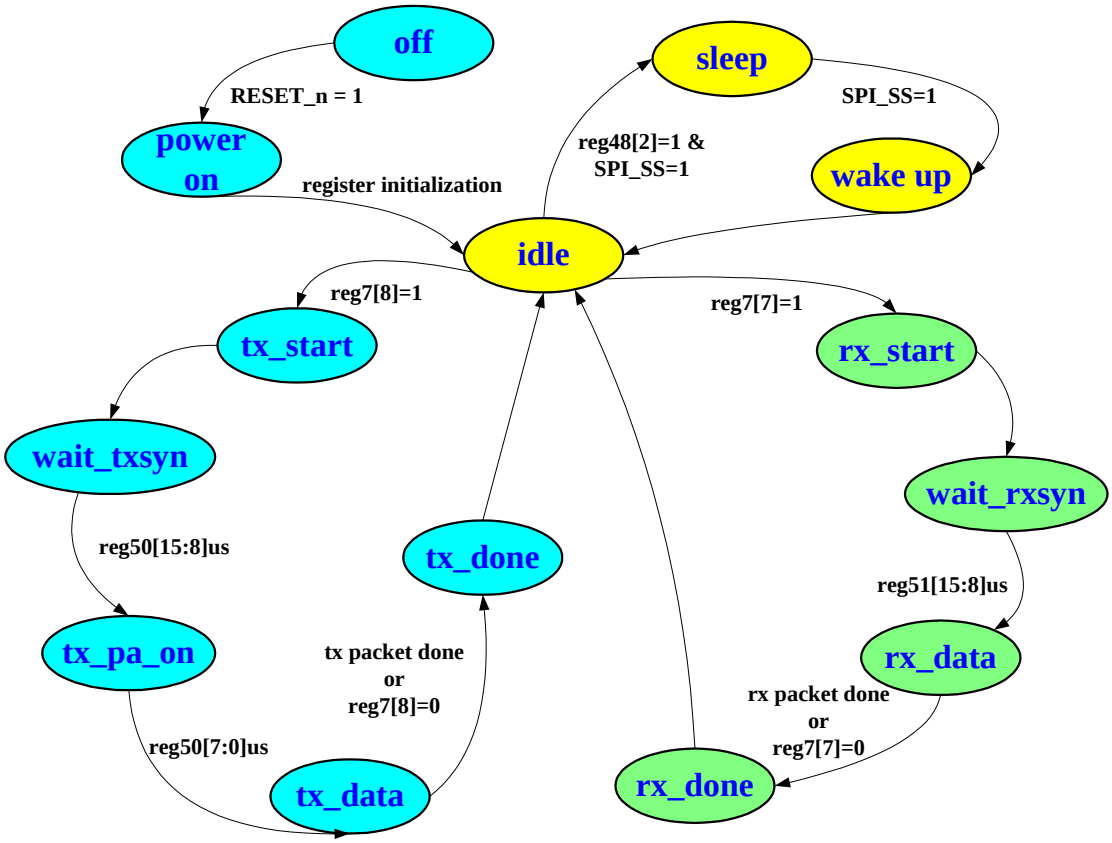
Reg. address	Read/Write	Default value (Hexadecimal)	Recommend value (12MHz crystal frequency) (Hexadecimal)
0	R/W	0000	CD51
2	R/W	00C1	0061
4	R/W	0688	3CD0
5	R/W	0041	00A1
9	R/W	0003	3003
14	R/W	6617	6697
16	R/W	0000	F000
18	R/W	FC00	E000
19	R/W	0014	2114
20	R/W	8103	819C
21	R/W	0962	6962
22	R/W	2602	0402
23	R/W	2602	0802
24	R/W	30C0	B080
25	R/W	3814	7819
26	R/W	5304	6704
48	R/W	1800	5800
51	R/W	4000	A000

- Table 4 -

For more detail description about digital base band interface, please refer to application note AN198810-1.

For the latest register value recommendations, please contact Elan Microelectronics technical group.

4.2.4 State Diagram



- Figure 5 -

5.Electrical Characteristics

5.1 Absolute Maximum Rating

Parameter	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Operating Temp.	T_{OP}	-40		+85	℃
Storage Temp.	$T_{STORAGE}$	-55		+125	℃
V_{DD_IO} Supply Voltage	V_{DDIO_MAX}			+3.7	VDC
V_{DD} Supply Voltage	V_{DD_MAX}			+2.5	VDC
Applied Voltages to Other Pins	V_{OTHER}	-0.3		+3.7	VDC
Input RF Level	P_{IN}			+10	dBm
Output Load mismatch (Z_0=50 ohm)	$VSWR_{OUT}$			10:1	VSWR

- Table 5 -

Note: 1.Absoute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics section below.

2.These devices are electro-static sensitive. Devices should be transported and stored in anti-static containers. Equipment and personnel contacting the devices need to be properly grounded. Cover workbenches with grounded conductive mats.

5.2 Characteristics

The following specifications are guaranteed for T_A=25℃, V_{DD}=1.80±0.18VDC, unless otherwise noted:

Parameter	Symbol	Specification			Unit	Test Condition and Notes
		Min.	Typ.	Max.		
Current Consumption						
Current Consumption - TX	I_{DD_TX}		26		mA	P_{OUT} = nominal output power
Current Consumption - RX	I_{DD_RX}		25		mA	
Current Consumption – DEEP IDLE	$I_{DD\_D\_IDLE}$		1.9		mA	RF Synthesizer and VCO: OFF (see Reg. 21)
Current Consumption – SLEEP	I_{DD_SLP}		3.5		uA	
Digital Inputs						
Logic input high	V_{IH}	0.8V_{DD_io}		V_{DD_io}	V	
Logic input low	V_{IL}	0		0.8	V	
Input Capacitance	$C_{\_IN}$			10	pF	
Input Leakage Current	$I_{\_LEAK\_IN}$			10	uA	
Digital Outputs						
Logic output high	V_{OH}	0.8V_{DD_io}		V_{DD_io}	V	
Logic output low	V_{OL}			0.4	V	
Output Capacitance	$C_{\_OUT}$			10	pF	
Output Leakage Current	$I_{\_LEAK\_OUT}$			10	uA	
Rise/Fall Time	$T_{\_RISE\_OUT}$			5	nS	
Clock Signals						
BRCLK output frequency	F_{BRCLK}		1, 12, or xtal Freq.		MHz	Depends on Register settings. Always either: 1 MHz Tx clock, 12 MHz APLL clock (Tx, Rx, and Idle), or the buffered 12 MHz crystal oscillator frequency.
SPI_CLK rise, fall time	T_{r_spi}			200	nS	Requirement for error-free register reading, writing.
SPI_CLK frequency range	F_{SPI}	0	12		MHz	
Overall Transceiver						
Operating Frequency Range	$F_{\_OP}$	2402		2482	MHz	

Antenna port mismatch (Z_0=50Ω)	$VSWR_I$		<2:1		VSWR	Receive mode. Meas. using 50 ohm balun.
	$VSWR_O$		<2:1		VSWR	Transmit mode. Meas. using 50 ohm balun.

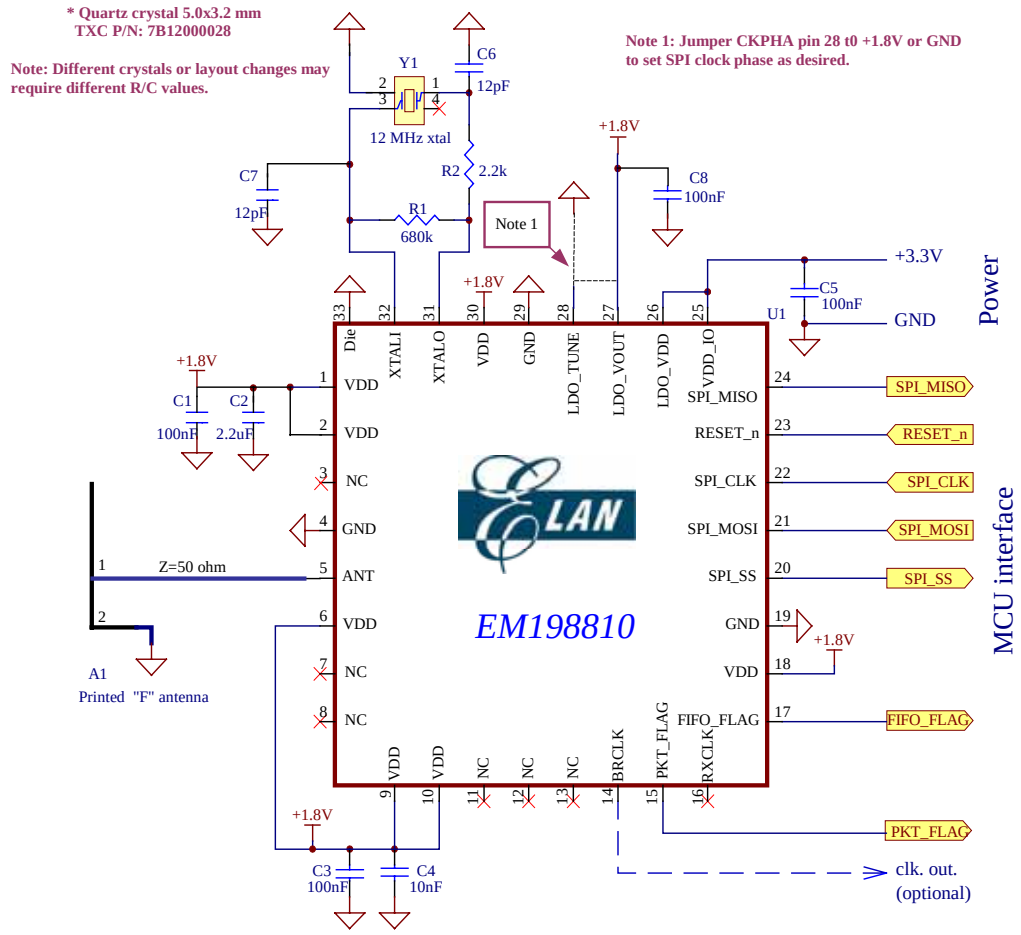
Receive Section: @ BER≦0.1%							
Receiver sensitivity			-85	-80	dBm	Meas. At antenna pin.	
Maximum useable signal		-20			dBm		
Input 3rd order intercept point	IIP_3	-14	-11		dBm		
Data (Symbol) rate	T_S		1		uS		
Min. Carrier/Interference ratio: @ BER≦0.1%							
Co-Channel Interference	$CI_{cochannel}$		9	11	dB	-60 dBm desired signal.	
Adjacent Ch. Interference, 1MHz offset	CI_{1}		-1.5	0	dB	-60 dBm desired signal.	
Adjacent Ch. Interference, 2MHz offset	CI_{2}		-30		dB	-60 dBm desired signal. Interference at 2 MHz below desired signal.	
Adjacent Ch. Interference, ≥ 3MHz offset	CI_{3}		-40		dB	-67 dBm desired signal.	
Image Frequency Interference	CI_{image}		-23	-9	dB	-60 dBm desired signal. Image freq. is always 2 MHz higher than desired signal.	
Adjacent interference to Image (1MHz)	CI_{image_11}		-34	-20	dB	-67 dBm desired signal. Always 3 MHz higher than desired signal.	
Out-of-Band Blocking	OBB_1	-10			dBm	30 MHz to 2000 MHz	Meas. with ACX BF2520 ceramic filter on ant. pin. Desired sig.-70dBm.
	OBB_2	-27			dBm	2000 MHz to 2400 MHz	
	OBB_3	-27			dBm	2500 MHz to 3000 MHz	
	OBB_4	-10			dBm	3000 MHz to 12.75 GHz	
Transmit Section: Reg. 9, bits 15-8 set to 00000000							
RF Output Power	P_{AV}		+2		dBm	Power Level 0	
Modulation Characteristics							
Peak FM Demodulation. 00001111 pattern	$\triangle f1_{avg}$	280	314	350	KHz		
01010101 pattern	$\triangle f2_{max}$	230			KHz	For at least 99.9% of all $\Delta f2_{max}$ meas.	
ISI, % Eye Open	$\triangle f2_{avg}/\triangle f1_{avg}$	80			%	1010 data sequence referenced to 00001111 data sequence	
Zero Crossing Error	ZCERR	-125		+125	nS	+/- 1/8 of Symbol Period	
In-Band Spurious Emission							
+/- 550kHz	IBS_1			-20	dBc		
2MHz offset	IBS_2			-40	dBm		
>3MHz offset	IBS_3			-60	dBm		
Out-of-Band Spurious Emission							
Operation	OBS_O_1		<-60	-36	dBm	30 MHz ~ 1 GHz	
	OBS_O_2		-45	-30	dBm	1 GHz ~ 12.75 GHz, excludes desired signal.	
	OBS_O_3		<-60	-47	dBm	1.8 GHz ~ 1.9 GHz	
	OBS_O_4		<-65	-47	dBm	5.15 GHz ~ 5.3 GHz	
RF VCO and PLL Section							
Typical PLL lock range	F_{LOCK}	2340		2560	MHz		
TX, RX Frequency Tolerance			--		ppm	Same as XTAL pins frequency tolerance	
Channel (Step) Size			1		MHz		
SSB Phase Noise			-95		dBc/Hz	550KHz offset	
			-115		dBc/Hz	2MHz offset	

Crystal oscillator freq. range (Reference Frequency)			12		MHz	Designed for 12 MHz crystal reference freq.	
Crystal oscillator digital trim range, typ.		-12		+12	ppm		
RF PLL Settling Time	T_{HOP}		75	150	uS		
Out-of-Band Spur. Emissions	$OBS_{\_1}$		<-75	-57	dBm	30 MHz ~ 1 GHz	DLE state, Synthesizer and VCO ON.
	$OBS_{\_2}$		-68	-47	dBm	1 GHz ~ 12.75 GHz	
LDO Voltage Regulator Section							
Dropout Voltage	V_{do}			TBD	V	Measured during Receive state	
Quiescent current	I_q			6	uA	No-load current consumed by LDO reg.	
Max. Load Capacitance	Max_C_{out}			1.0	uF	Ensures stability of the high speed LDO V.R.	

- Table 6 -

6. Application Circuit

Typical Application



Simple, low-power (0dBm) 2.4GHz RF Transceiver with Framing and Data buffers

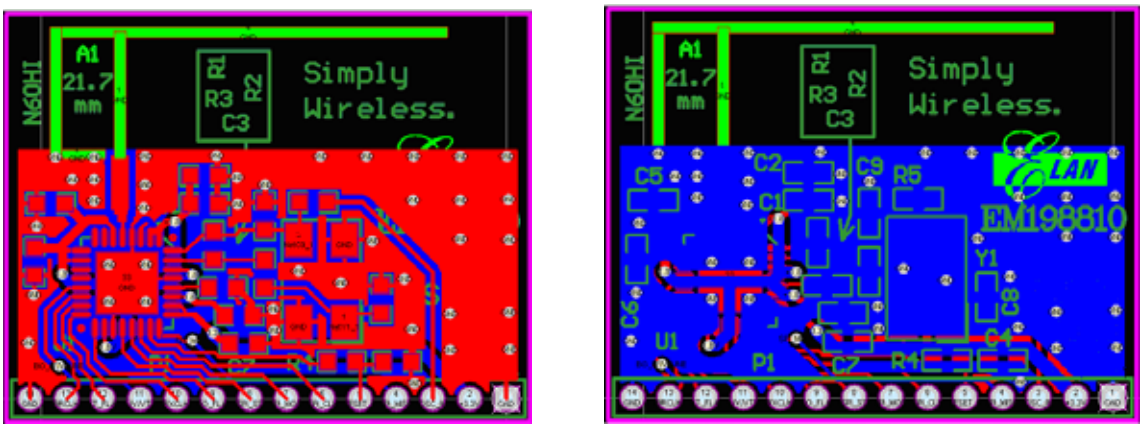
- Figure 6 -

BOM list

Comment	Description	Designator	Quantity	Footprint
10pF	Capacitor	C8	1	SMD-0603
12pF	Capacitor	C9	1	SMD-0603
10nF	Capacitor	C6	1	SMD-0603
100nF	Capacitor	C1 C3 C5 C7	4	SMD-0603
2.2uF	Capacitor	C2	1	SMD-0603
0 ohm	Resistor	R4	1	SMD-0603
2.2k	Resistor	R2	1	SMD-0603
680k	Resistor	R1	1	SMD-0603
12MHz	Crystal	Y1	1	OSC 5x3.2
EM198810	IC	U1	1	QFN 32 5x5
CON1x14	Connector	P1	1	HDR1x14

- Table 7 -

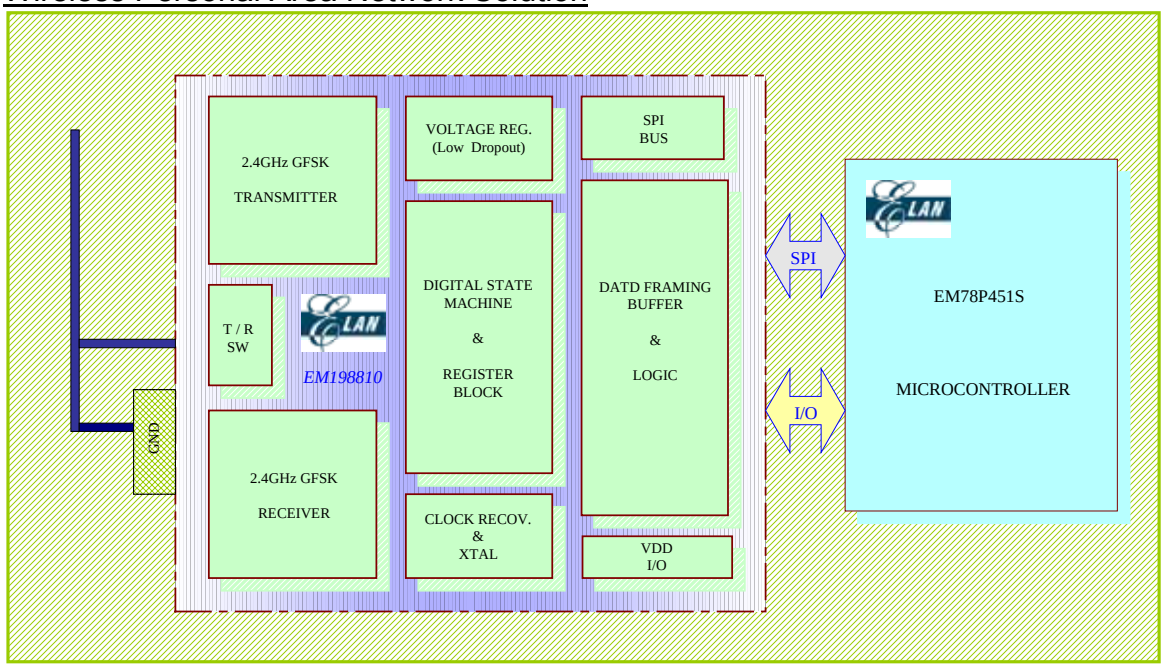
PCB layout



Top layer **Bottom layer**

- Figure 7 -

Wireless Personal Area Network Solution



Elan Wireless personal area network Total Solution

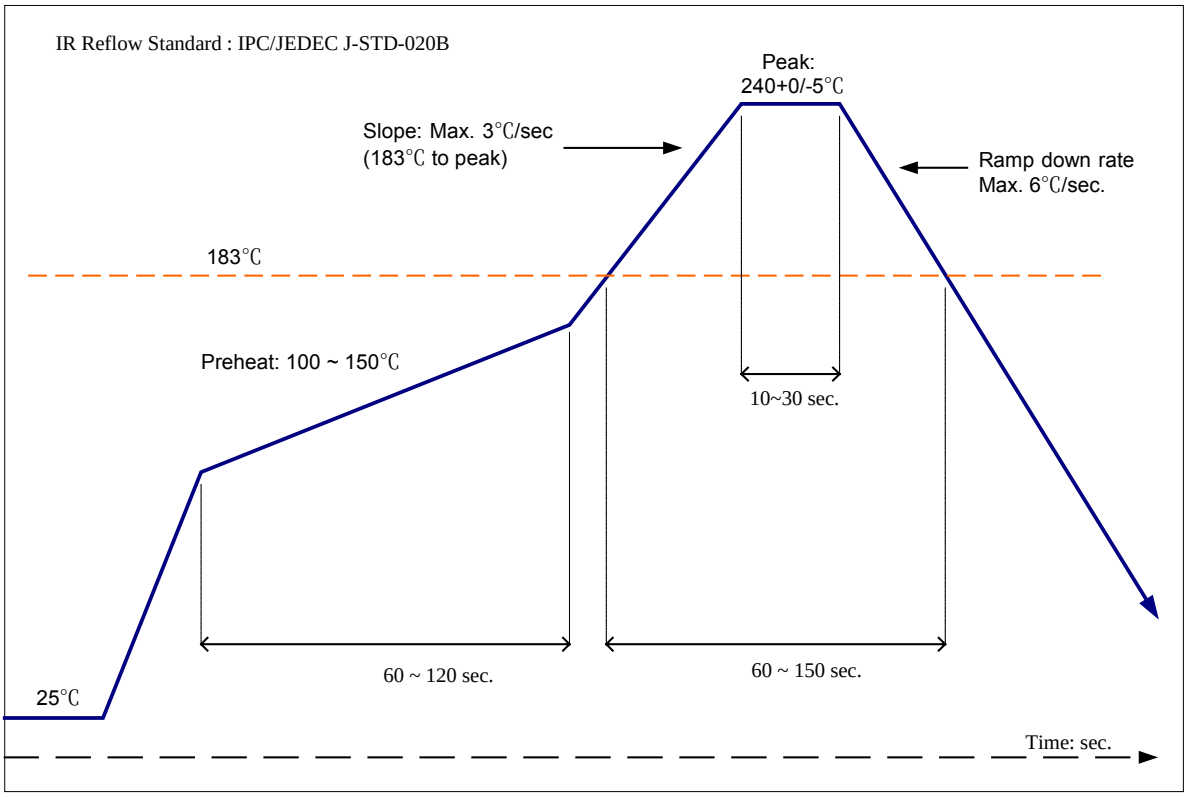
- Fig. 8 –

7. SOLDERING

Reflow soldering requires paste to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Several methods exist for reflowing, throughput times vary between 100 and 300 seconds depending on heating method.

Recommendation: Follow IPC/JEDEC J-STD-020B

Condition: Average ramp-up rate (183℃ to peak): 3℃/sec. max.
Preheat: 100 ~ 150℃ 60 ~ 120 sec.
Temperature maintained above 183℃: 60 ~ 150sec.
Time within 5℃ of actual peak temperature: 10 ~ 30sec.
Peak temperature: 240+0/-5℃
Ramp-down rate: 6℃/sec. max.
Time 25℃ to peak temperature: 6 minutes max.
Cycle interval: 5 minutes



- Fig. 9 -

DATA SHEET STATUS

Data Sheet Status	Product Status	Definitions
Objective specification	Development	This data sheet contains data from the objective specification for product development. Elan Microelectronics reserves the right to change the specification in any manner without notice.
Preliminary specification	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Elan Microelectronics reserves the right to change the specification without notice in order to improve the design and supply the best possible product.
Product specification	Production	This data sheet contains data from the production specification. Elan Microelectronics reserves the right to make changes at any time in order to improve the design, manufacturing and supply.

DISCLAIMERS

Life support policy.—These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Elan Microelectronics customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Elan Microelectronics for any damages resulting from such application.

Right to make changes.—Elan Microelectronics reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Elan Microelectronics assumes no responsibility or liability for these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

ELAN MICROELECTRONICS CORPORATION

Headquarters:

No. 12, Innovation Road 1
Hsinchu Science Park
Hsinchu, TAIWAN 30077
Tel: +886 3 563-9977
Fax: +886 3 563-9966
http://www.emc.com.tw

Hong Kong:

Elan (HK) Microelectronics Corporation, Ltd.
Flat A, 19F., World Tech Centre,
95 How Ming Street, Kwun Tong
Kowloon, HONG KONG
Tel: +852 2723-3376
Fax: +852 2723-7780
elanhk@emc.com.hk

USA:

Elan Information Technology Group (U.S.A.)
1821 Saratoga Ave., Suite 250
Saratoga, CA 95070
USA
Tel: +1 408 366-8225
Fax: +1 408 366-8220

Shenzhen:

Elan Microelectronics Shenzhen, Ltd.
SSMEC Bldg., 3F, Gaoxin S. Ave.
Shenzhen Hi-Tech Industrial Park
Shenzhen, Guandong, CHINA
Tel: +86 755 2601-0565
Fax: +86 755 2601-0500

Shanghai:

Elan Microelectronics Shanghai, Ltd.
23/Bldg. #115 Lane 572, Bibo Road
Zhangjiang Hi-Tech Park
Shanghai, CHINA
Tel: +86 21 5080-3866
Fax: +86 21 5080-4600