QPB9318

Dual-Channel Switch LNA Module

Product Overview

The QPB9318 is a highly integrated front-end module targeted for TDD base stations. The LNA switch module integrates a two-stage LNA and a high power switch in a dual channel configuration. Power down capability for the LNAs can be controlled with shut-down pins for the module.

The QPB9318 can be utilized across the 2.3 – 3.8 GHz range to provide 1.3 dB noise figure for operation in the receive mode and 0.5 dB insertion loss in the transmit mode. The LNAs utilize Qorvo's high performance E-pHEMT process while the pin-diode based switch supports input RF power signals of up to 10W average power assuming 8 dB PAR.

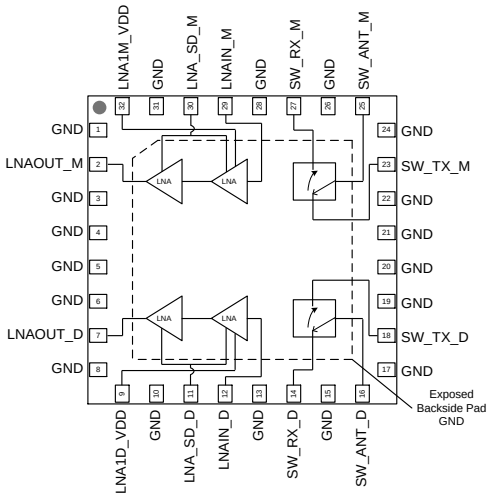
The QPB9318 is packaged in a RoHS-compliant, compact 5 mm x 5 mm surface-mount leadless package. The switch LNA module is targeted for wireless infrastructure applications configured for TDD-based MIMO architectures. The module can be used for next generation 5G or pre-5G solutions or small cell basestation applications.

32 Pad 5 mm x 5 mm leadless SMT Package

Key Features

- 2.3-3.8 GHz Frequency Range
- Integrates dual channels of a two-stage LNA with a high power switch
- Max RF Input power: 10W Pavg (8 dB PAR)
- 1.3 dB Noise Figure (Rx mode)
- 30.5 dB Gain (Rx mode)
- +33.5 dBm OIP3 (Rx mode)
- 0.5 dB Insertion Loss (Tx mode)
- Compact package size, 5x5 mm

Functional Block Diagram



Top View

Applications

- Wireless Infrastructure
- Small cell BTS
- Pre-5G / 5G Massive MIMO systems
- TDD-based architectures
- Bands 38, 41, 42, 43

Ordering Information

Part No.	Description
QPB9318SR	100 pcs on a 7" reel
QPB9318TR13	2500 pcs on a 13" reel
QPB9318PCB401	Evaluation board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150 °C
LNA Supply Voltage (Pins 2, 7, 9, 11, 30, 32)	+7 V
LNA Input Power (Pavg, 8 dB PAR)	+24 dBm
Switch Input Power (Pavg, 8 dB PAR)	+40 dBm
Switch Input Power (Peak)	+48 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
LNA Voltage	+3	+5	+5.25	V
V_{MODE}		+28		V
T_{CASE}	−40		+105	°C
Tj for >10^6 hours MTTF (1)			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

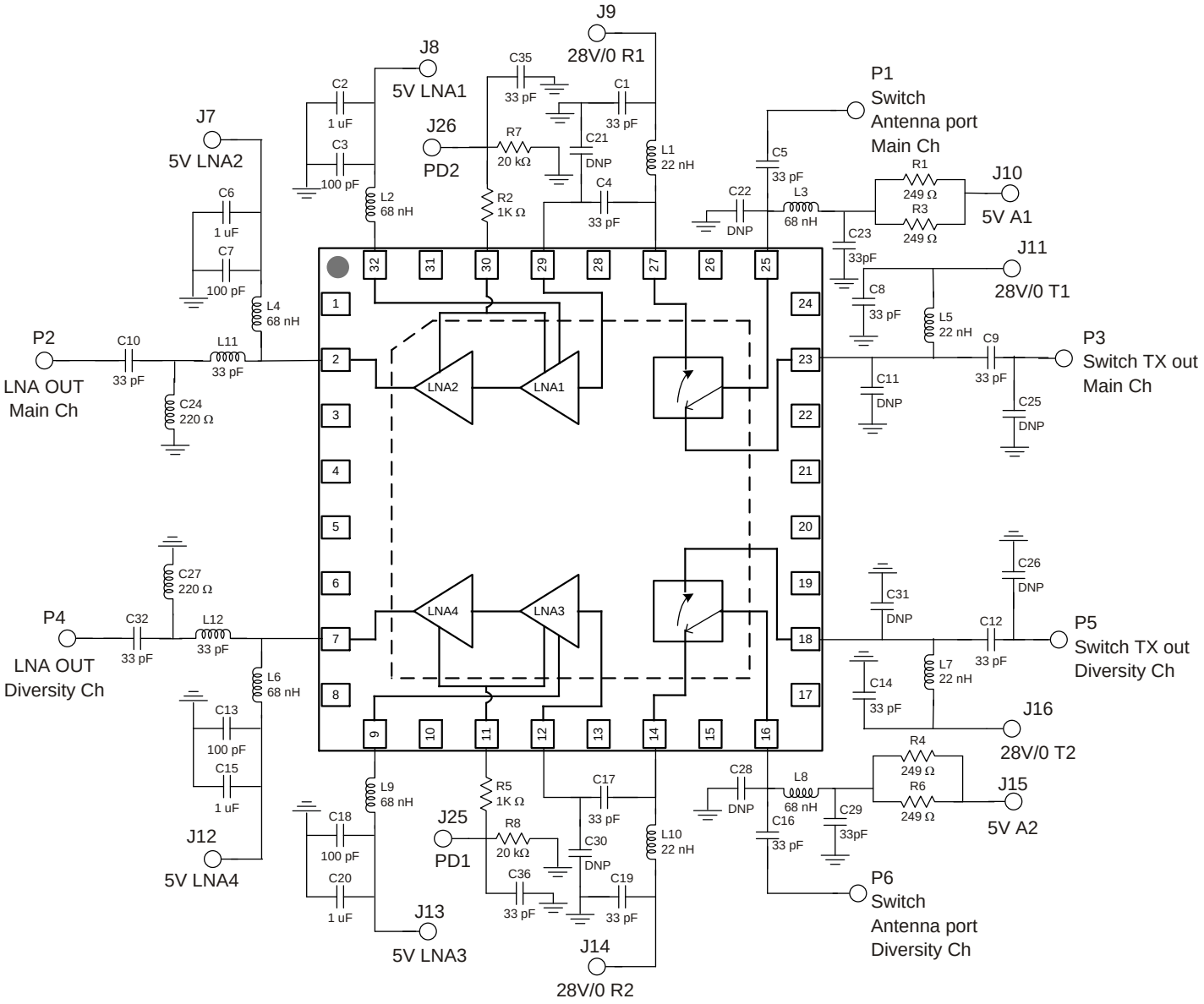
Note 1: Rx Mode

Electrical Specifications

Parameter	Conditions (1)	Min	Typ	Max	Units
Operational Frequency Range		2300		3800	MHz
Test Frequency			2600		MHz
Gain	Rx mode	28	30.5	34	dB
Gain Flatness	Rx mode, 2.545 to 2.665 GHz		0.4		dB
	Rx mode, Any 60 MHz BW within band		0.2		
Noise Figure (2)	Rx mode		1.3	1.7	dB
Output IP3	Rx mode, Pout/tone = +5dBm, Δf = 1MHz	+30	+33.5		dBm
OP1dB	Rx mode		+19.8		dBm
Insertion Loss (2)	Tx mode		0.5	1.0	dB
Input Return Loss (3)	Rx mode		13.5		dB
Output Return Loss (3)	Rx mode		12.4		dB
Channel Isolation (4)	Rx mode		41		dB
Switch Isolation (5)	Tx mode		25		dB
LNA1, LNA2 Supply Voltage			5		V
LNA1 Current	Per channel		45	70	mA
LNA2 Current	Per channel		70	90	mA
LNA Shutdown Current	Per channel		3		mA
LNA Shutdown Control Voltage (Pins 11, 30)	On state	0		+0.5	V
	Off state (Power down)	+1.4	+3.3	V_{DD}	V
Switch Supply Voltage			+28		V
Switch Current (Tx mode) (6)	+28V		10		uA
	+5V		30	40	mA
Switch switching time	50% CTL to 10/90% RF		200		nS
Thermal Resistance	Tx mode		22		°C/W
	Rx mode		23		°C/W

Notes:
1. Test conditions unless otherwise noted: Temp = +25 °C, 50 Ω system.
2. De-embedded to device leads.
3. Requires external matching.
4. Channel Isolation is the difference in desired channel gain to the cross channel gain.
5. Switch Isolation is the insertion loss of the switch in the receive path while in Tx mode.
6. Current into Antenna port, per channel in Tx Mode.

Application Circuit Schematic – QPB9318PCB401

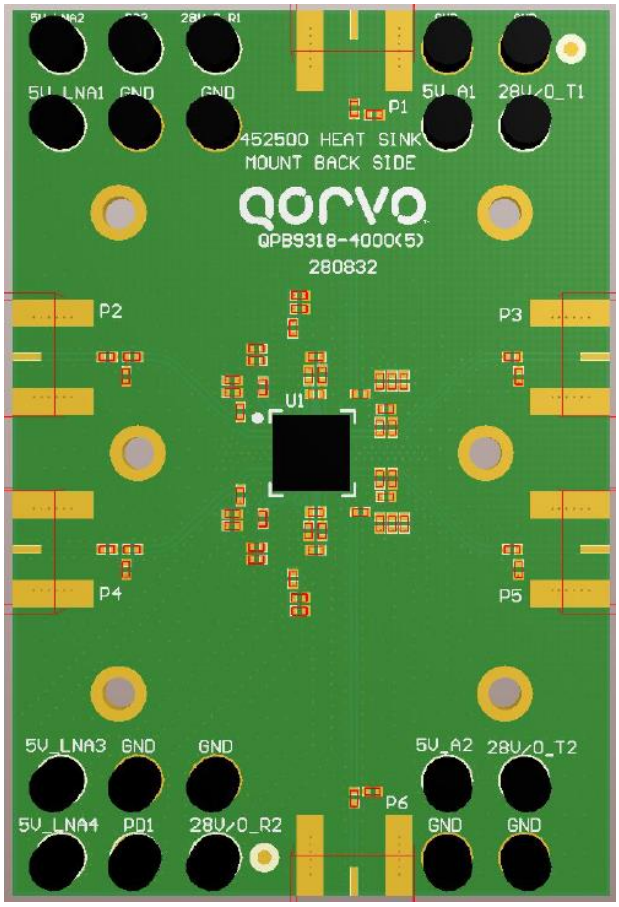


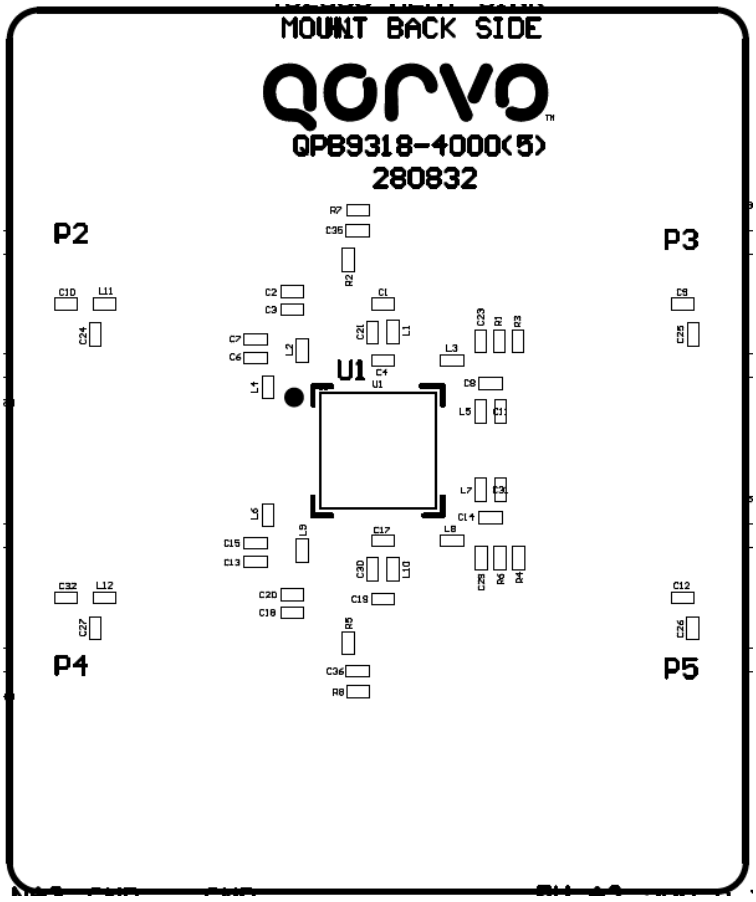
Notes:

For CH1 operation J10 (5V A1) always on +5Vdc and J7 (5V LNA2), J8 (5V LNA1) powered up to +5Vdc.
For CH2 operation J15 (5V A2) always on +5Vdc and J12 (5V LNA4), J13 (5V LNA3) powered up to +5Vdc.

- For CH1 RX operation (similar sequence for CH2):
  1. Set J11 (28V/0 T1) V_{MODE} to high (+28Vdc).
  2. Set J9 (28V/0 R1) V_{MODE} to low (0Vdc).
  3. Enable LNA's J26 (PD2) to 0Vdc.
- For CH1 TX operation (similar sequence for CH2):
  1. Disable LNA's J25 (PD1) to +5Vdc.
  2. Set J9 (28V/0 R1) V_{MODE} to high (+28Vdc).
  3. Set J11 (28V/0 T1) V_{MODE} to low (0Vdc).
- R2, R5, R7 & R8 need to be placed to improve the stability in the first stage LNA. It is recommended that they be placed as close to the pin as possible.

Application Circuit Layout – QPB9318PCB401





Bill of Material – QPB9318PCB401

Ref Des	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board		
U1	n/a	Dual Channel Switch LNA Module	Qorvo	QPB9318
C23, C29	33 pF	CAP, 33pF, 5%, 50V, C0G, 0402	various	
C1, C4, C5, C8, C9, C10, C12, C14, C16, C17, C19, C32, C32, C35, C36, L11, L12	33 pF	CAP, 33pF, 5%, 100V, C0G, 0402	various	
C2, C6, C15, C20	1 uF	CAP, 20%, 6.3V, X5R, 0402	various	
C3, C7, C13, C18	100 pF	CAP, 5%, 50V, C0G, 0402	various	
L1, L5, L7, L10	22 nH	IND, 5%, M/L, 0402	various	
C24, C27	220 Ω	RES, 5%, 1/16W, 0402	various	
L2, L3, L4, L6, L8, L9	68 nH	IND, 5%, M/L, 0402	various	
R1, R3, R4, R6	249 Ω	RES, 1%, 1/16W, 0402	various	
R2, R5	1K Ω	RES, 1%, 1/16W, 0402	various	
R7, R8	20K	RES, 1%, 1/16W, 0402	various	

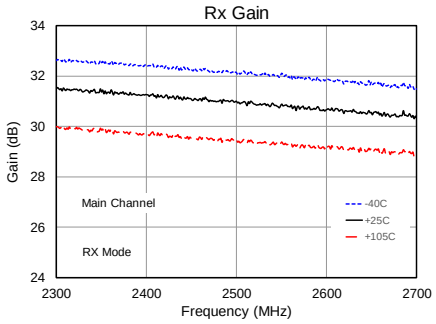
Typical Performance – Rx Mode

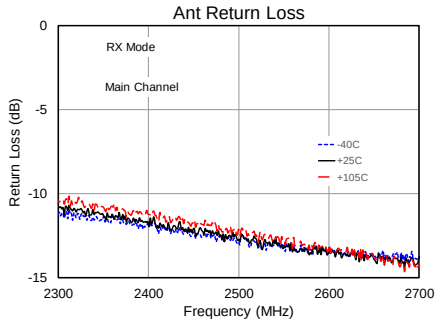
Parameter	Conditions[1]	Typical Value					Units
Frequency		2300	2400	2500	2600	2700	MHz
Gain		31.0	30.8	30.6	30.5	30.0	dB
Input Return Loss		10.9	11.8	12.5	13.5	14.3	dB
Output Return Loss		22.8	19.2	14.9	12.4	9.8	dB
Output P1dB		+20.1	+20.0	+19.8	+19.8	+19.6	dBm
OIP3	Pout= +5 dBm/tone, Δf=1 MHz	+33.9	+33.9	+33.9	+33.5	+33.5	dBm
Noise Figure[2]		1.2	1.2	1.2	1.3	1.3	dB

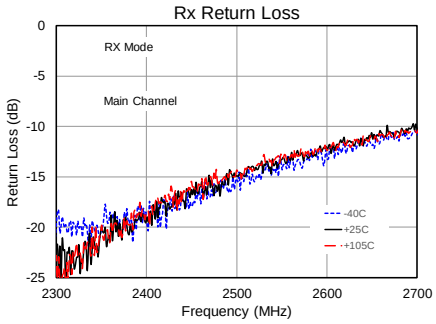
Notes:
1. Test conditions unless otherwise noted: LNA1, 2, 3, 4, A1, A2 = +5V; 28V/0 T1, 2 = +28V; 28V/0 R1, 2, PD1, 2 = 0V; Temp. = +25 °C
2. De-embedded

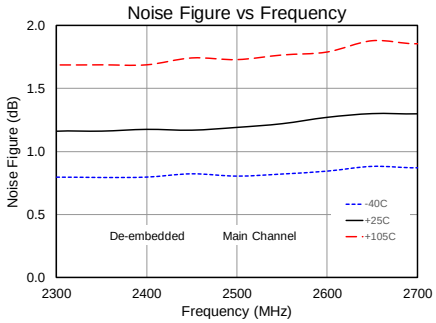
Performance Plots – Rx Mode (Main Channel)

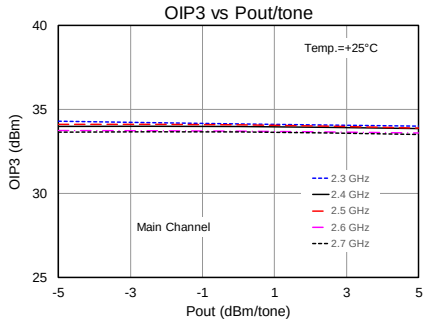
Test conditions unless otherwise noted: LNA1, 2, 3, 4, A1, A2 = +5V; 28V/0 T1, 2 = +28V; 28V/0 R1, 2, PD1, 2 = 0V; Temp.= +25 °C

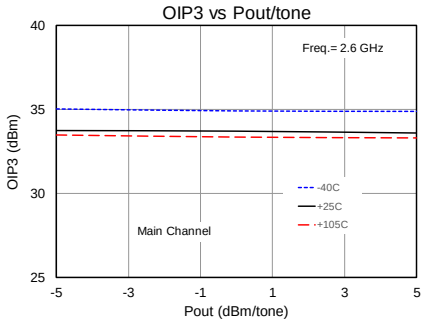


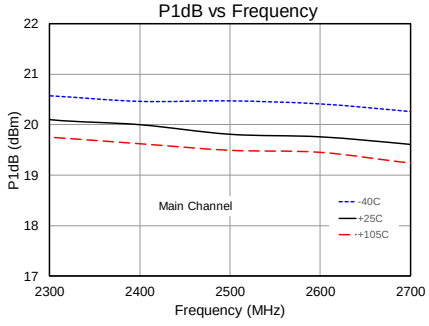


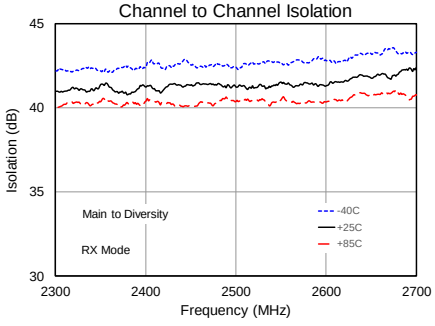






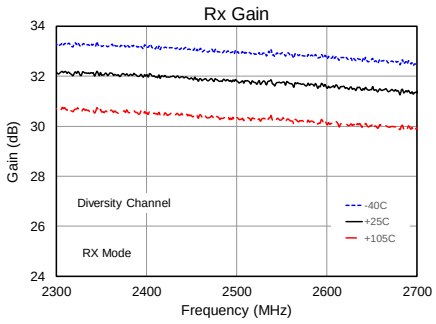


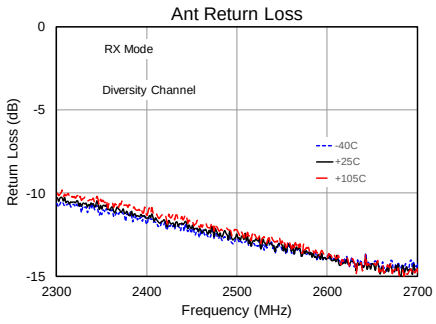


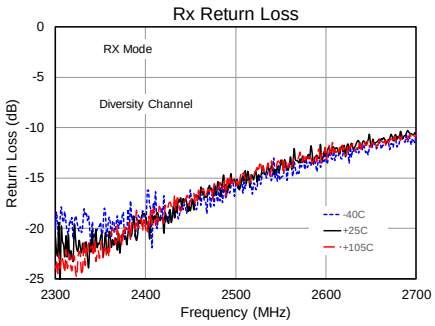


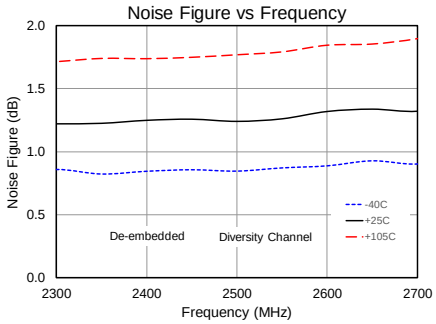
Performance Plots – Rx Mode (Diversity Channel)

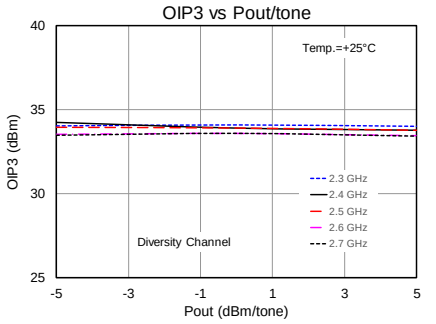
Test conditions unless otherwise noted: LNA1, 2, 3, 4, A1, A2 = +5V; 28V/0 T1, 2 = +28V; 28V/0 R1, 2, PD1, 2 = 0V; Temp.= +25 °C

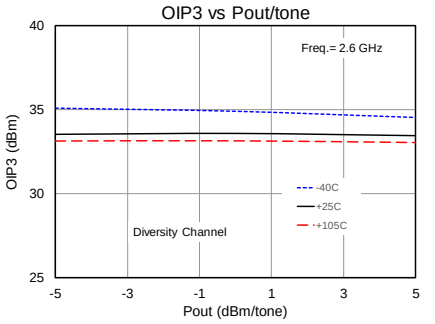


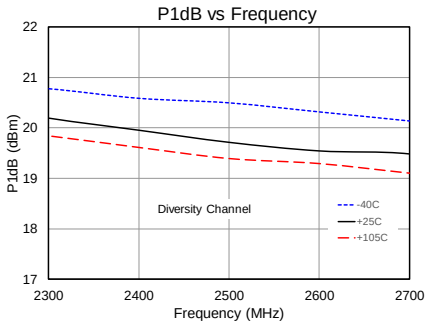


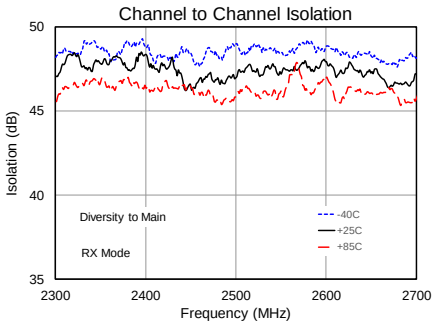












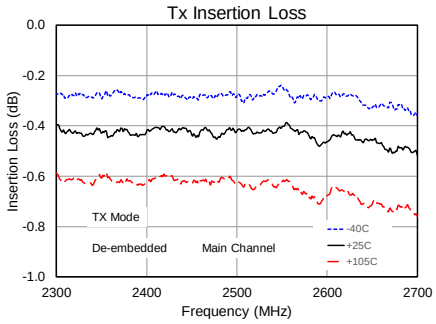
Typical Performance – Tx Mode

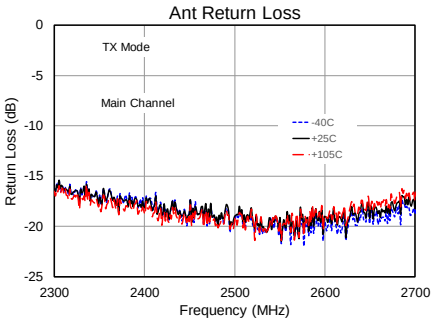
Parameter	Conditions[1]	Typical Value					Units
Frequency		2300	2400	2500	2600	2700	MHz
Insertion Loss[2]		0.4	0.4	0.4	0.5	0.5	dB
Input Return Loss		16.5	17.5	19.4	19.1	17.5	dB
Output Return Loss		16.5	19.3	22.7	25.9	20.8	dB

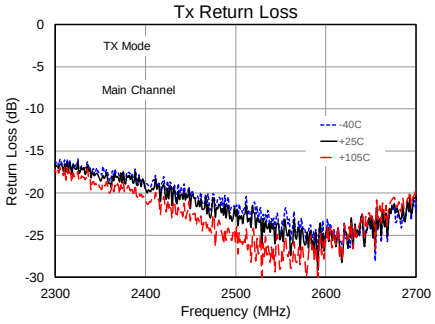
Notes:
1. Test conditions unless otherwise noted: LNA1, 2, 3, 4, A1, A2, PD1, 2 = +5V; 28V/0 R1, 2 = +28V; 28V/0 T1, 2 = 0V; Temp. = +25 °C
2. De-embedded

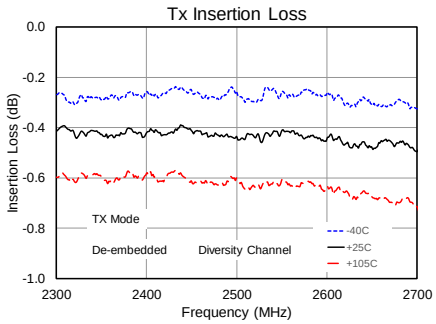
Performance Plots – Tx Mode

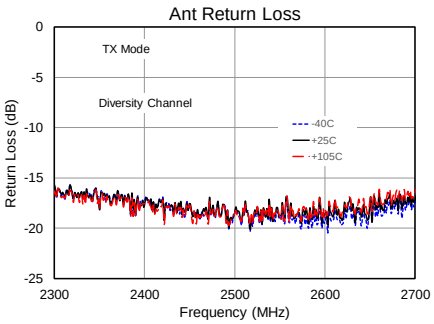
Test conditions unless otherwise noted: LNA1, 2, 3, 4, A1, A2, PD1, 2 = +5V; 28V/0 R1, 2 = +28V; 28V/0 T1, 2 = 0V; Temp.= +25 °C

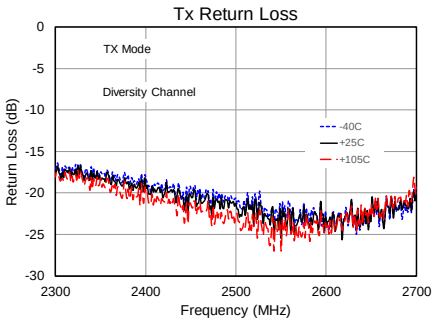




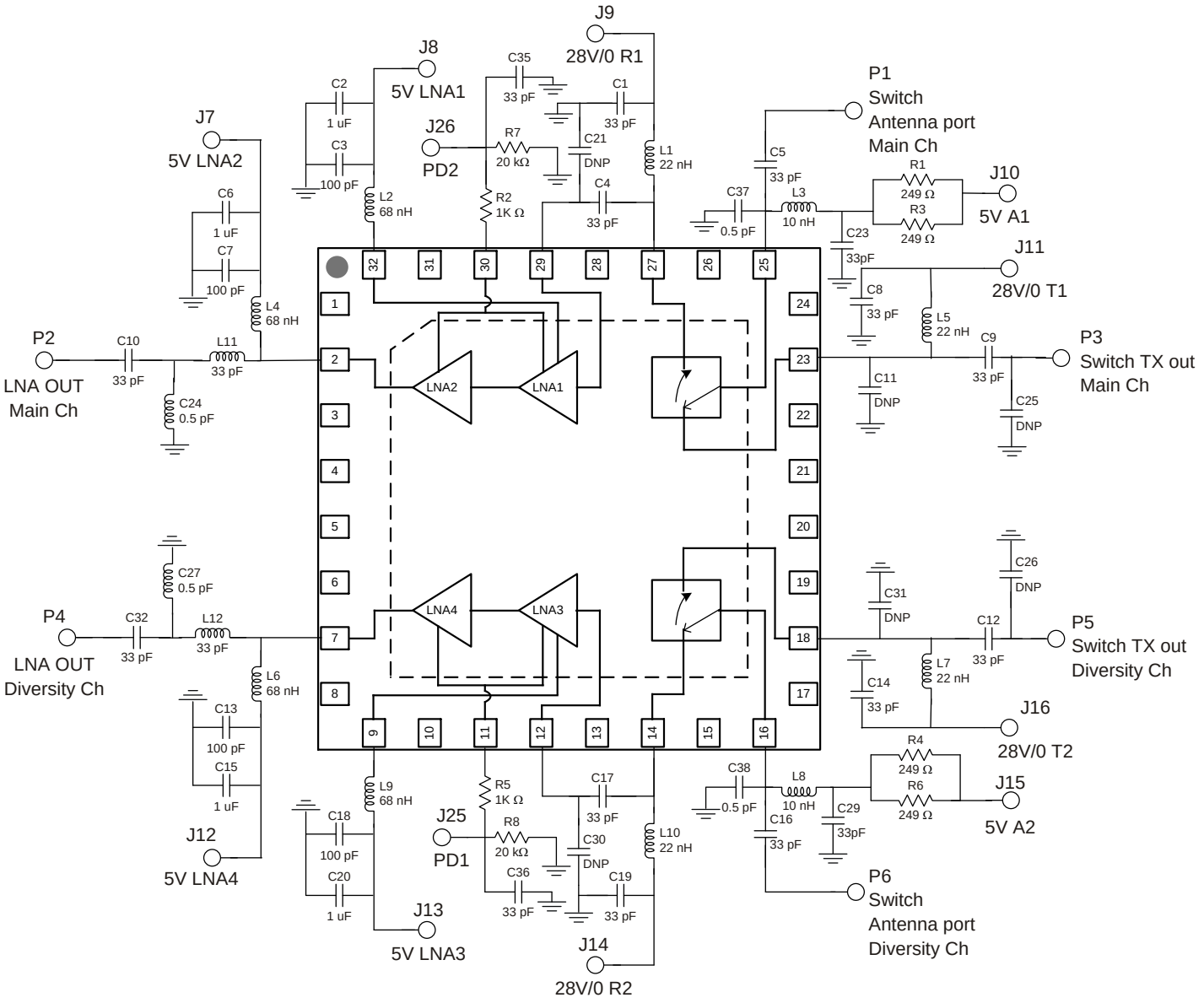








Application Circuit Schematic – 3400 to 3800 MHz

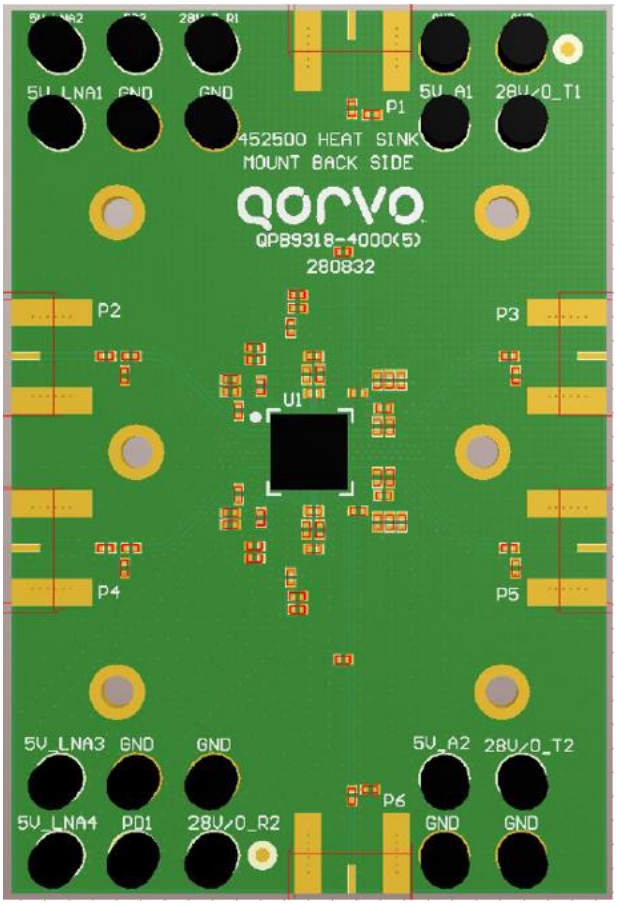


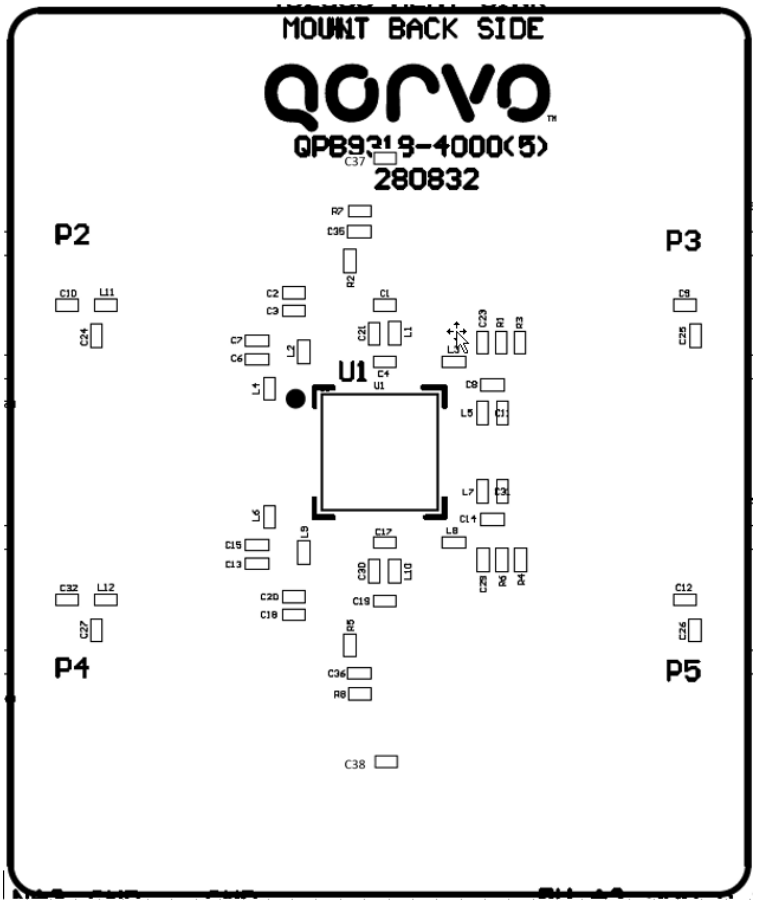
Notes:

For CH1 operation J10 (5V A1) always on +5Vdc and J7 (5V LNA2), J8 (5V LNA1) powered up to +5Vdc.
For CH2 operation J15 (5V A2) always on +5Vdc and J12 (5V LNA4), J13 (5V LNA3) powered up to +5Vdc.

- For CH1 RX operation (similar sequence for CH2):
  4. Set J11 (28V/0 T1) V_{MODE} to high (+28Vdc).
  5. Set J9 (28V/0 R1) V_{MODE} to low (0Vdc).
  6. Enable LNA's J26 (PD2) to 0Vdc.
- For CH1 TX operation (similar sequence for CH2):
  4. Disable LNA's J25 (PD1) to +5Vdc.
  5. Set J9 (28V/0 R1) V_{MODE} to high (+28Vdc).
  6. Set J11 (28V/0 T1) V_{MODE} to low (0Vdc).
- R2, R5, R7 & R8 need to be placed to improve the stability in the first stage LNA. It is recommended that they be placed as close to the pin as possible.

Application Circuit Layout – 3400 to 3800 MHz





Bill of Material – 3400 to 3800 MHz

Ref Des	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board		
U1	n/a	Dual Channel Switch LNA Module	Qorvo	QPB9318
C23, C29	33 pF	CAP, 33pF, 5%, 50V, C0G, 0402	various	
C1, C4, C5, C8, C9, C10, C12, C14, C16, C17, C19, C32, C32, C35, C36, L11, L12	33 pF	CAP, 33pF, 5%, 100V, C0G, 0402	various	
C2, C6, C15, C20	1 uF	CAP, 20%, 6.3V, X5R, 0402	various	
C3, C7, C13, C18	100 pF	CAP, 5%, 50V, C0G, 0402	various	
C24, C27, C37, C38	0.5 pF	CAP, +/-0.1pF, 100V, C0G, 0402	various	
L1, L5, L7, L10	22 nH	IND, 5%, M/L, 0402	various	
L3, L8	10 nH	IND, 5%, M/L, 0402	various	
L2, L4, L6, L9	68 nH	IND, 5%, M/L, 0402	various	
R1, R3, R4, R6	249 Ω	RES, 1%, 1/16W, 0402	various	
R2, R5	1K Ω	RES, 1%, 1/16W, 0402	various	
R7, R8	20K	RES, 1%, 1/16W, 0402	various	

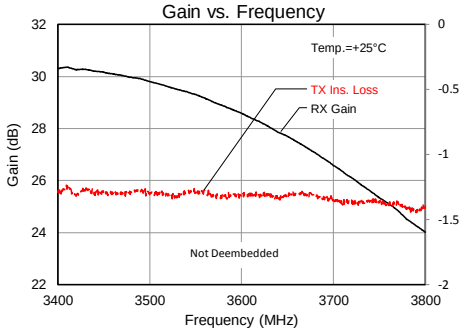
Typical Performance – 3400 to 3800 MHz

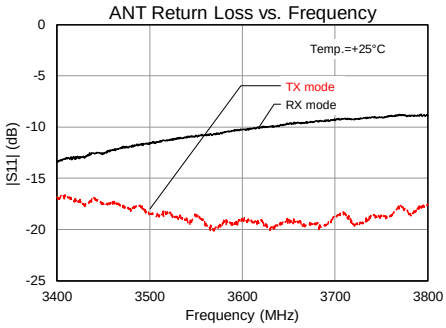
Parameter	Conditions[1]	Typical Value					Units
Frequency		3400	3500	3600	3700	3800	MHz
RX Mode							
Gain		30.3	29.8	28.6	26.6	24.1	dB
Input Return Loss		13.3	11.7	10.3	9.4	8.9	dB
Output Return Loss		12.9	23.7	15.4	9.2	6.3	dB
Output P1dB		+17.9	+17.6	+17.3	+17.3	+16.7	dBm
OIP3	Pout= +5 dBm/tone, Δf=1 MHz	+29.9	+29.4	+28.9	+28.9	+28.4	dBm
Noise Figure[2]		1.4	1.5	1.6	1.7	1.8	dB
TX Mode							
Insertion Loss[2]		0.6	0.6	0.6	0.7	0.7	dB
Input Return Loss		16.9	18.4	19.1	18.8	17.7	dB
Output Return Loss		18.3	20.5	23.6	24.8	23.4	dB

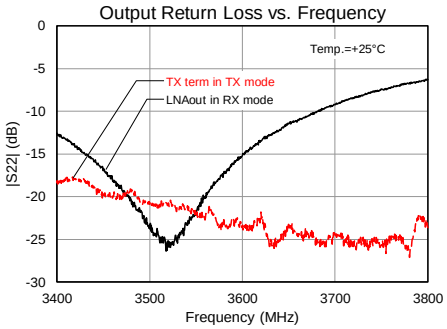
Notes:
1. Test conditions unless otherwise noted: LNA1, 2, 3, 4, A1, A2 = +5V; 28V/0 T1, 2 = +28V; 28V/0 R1, 2, PD1, 2 = 0V; Temp. = +25 °C
2. De-embedded

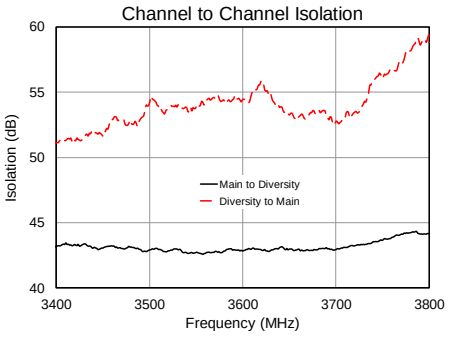
Performance Plots – 3400 to 3800 MHz

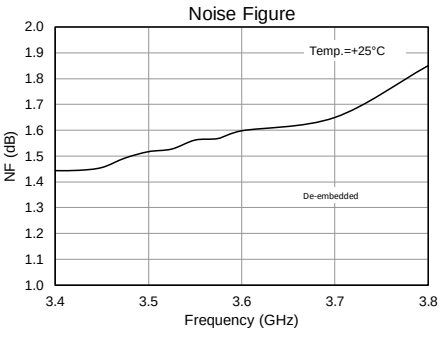
Test conditions unless otherwise noted: LNA1, 2, 3, 4, A1, A2 = +5V; 28V/0 T1, 2 = +28V; 28V/0 R1, 2, PD1, 2 = 0V; Temp.= +25 °C

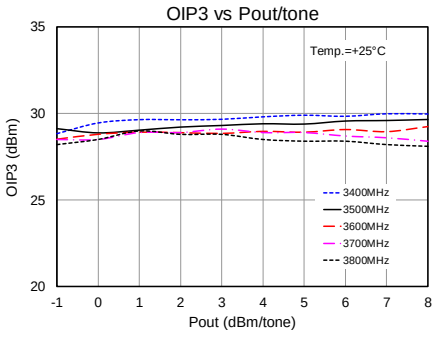




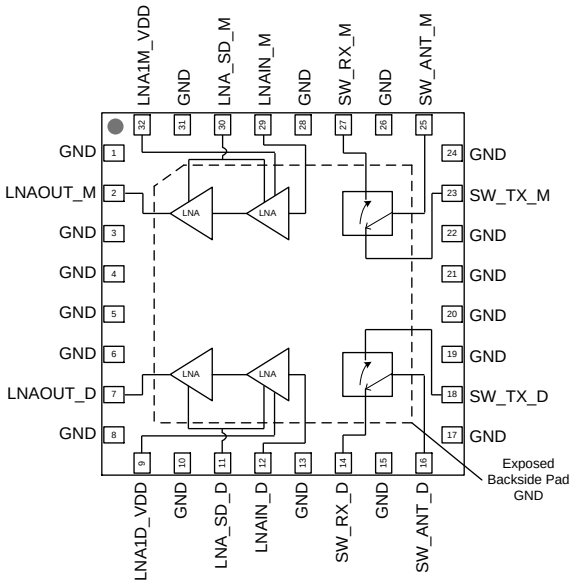








Pin Configuration and Description

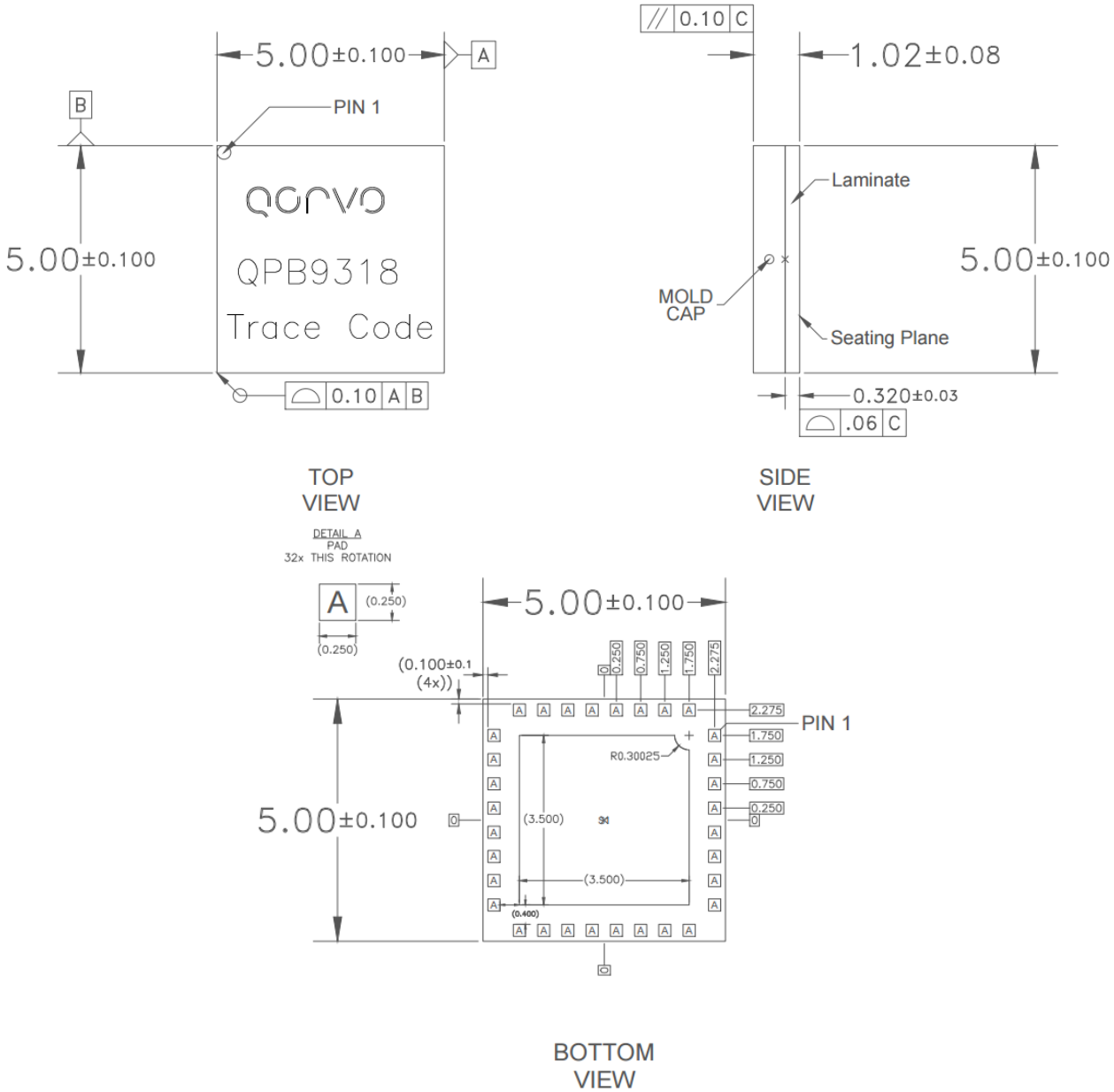


Top View

Pin No.	Label	Description
1, 3, 4, 5, 6, 8, 10, 13, 15, 17, 19, 20, 21, 22, 24, 26, 28, 31	GND	Ground connection. This pin is connected internally and can be left floating or connected to ground.
2	LNAOUT_M	Main channel RX output port. Bias port for LNA2. Needs external DC block.
7	LNAOUT_D	Diversity channel RX output port. Bias port for LNA2. Needs external DC block.
9	LNA1D_VDD	Diversity channel LNA1 bias voltage supply pin. External choke and bypass caps needed.
11	LNA_SD_D	Common shutdown pin for both LNA1 & 2 on diversity channel.
12	LNAIN_D	Diversity channel RF input to LNA chain. External DC block cap needed.
14	SW_RX_D	RX port of switch on diversity channel.
16	SW_ANT_D	Diversity channel antenna port on switch.
18	SW_TX_D	TX port of switch on diversity channel.
23	SW_TX_M	TX port of switch on main channel.
25	SW_ANT_M	Main channel antenna port on switch.
27	SW_RX_M	RX port of switch on diversity channel.
29	LNAIN_M	Main channel RF input to LNA chain. External DC block cap needed.
30	LNA_SD_M	Common shutdown pin for both LNA1 & 2 on main channel.
32	LNA1M_VDD	Main channel LNA1 bias voltage supply pin. External choke and bypass caps needed.
Backside Pad	GND	Ground connection. The back side of the package should be connected to the ground plan though as short of a connection as possible. PCB vias under the device are required.

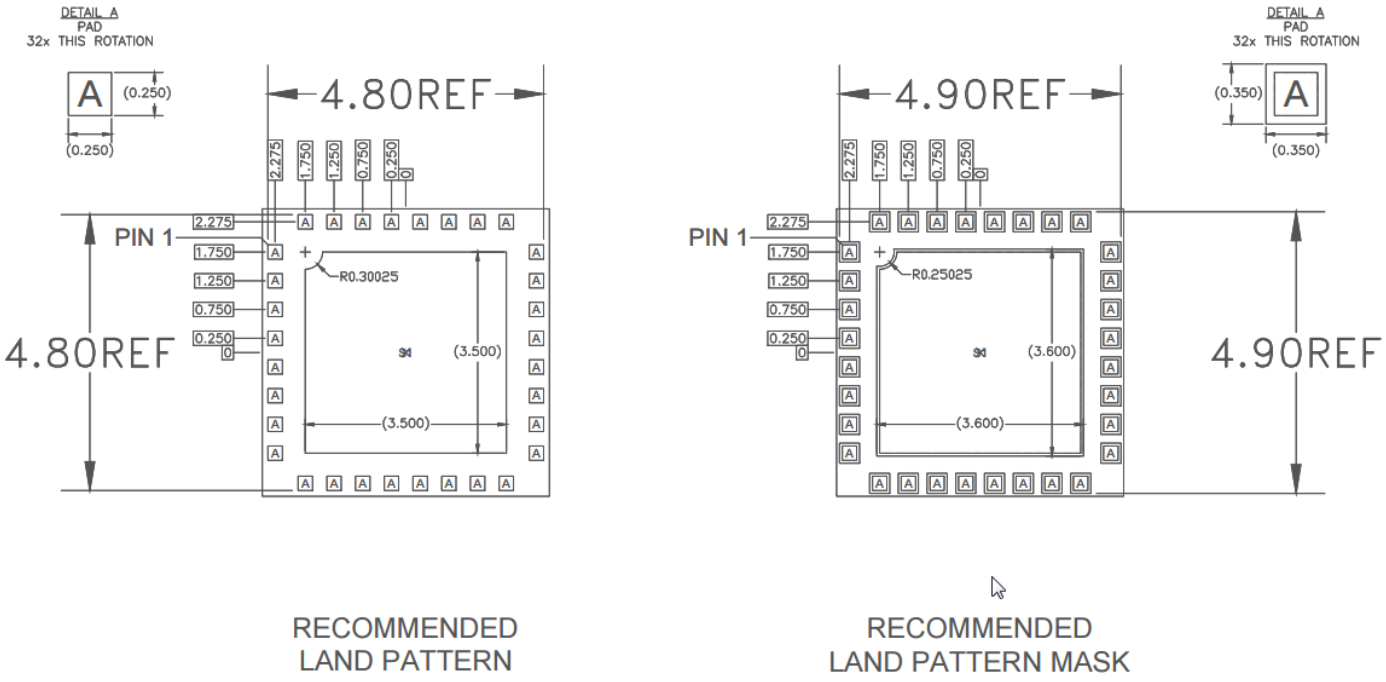
Package Marking and Dimensions

Marking: Part number – QPB9318
Trace Code – XXXX



Notes:
1. All dimensions are in microns. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



Notes:

1. A heat sink underneath the area of the PCB for the mounted device is recommended for proper thermal operation.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Level 1B	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Level C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU. This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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