250 MHz, 10 ns Switching Multiplexers w/Amplifier

AD8170/AD8174

FEATURES

Fully Buffered Inputs and Outputs
Fast Channel Switching: 10 ns
Internal Current Feedback Output Amplifier
High Output Drive: 50 mA
Flexible Gain Setting via External Resistor(s)
High Speed
250 MHz Bandwidth, G = +2
1000 V/μs Slew Rate
Fast Settling Time of 15 ns to 0.1%
Low Power: < 10 mA
Excellent Video Specifications (R_L = 150 Ω, G = +2)
Gain Flatness of 0.1 dB Beyond 80 MHz
0.02% Differential Gain Error
0.05° Differential Phase Error
Low Crosstalk of –78 dB @ 5 MHz
High Disable Isolation of –88 dB @ 5 MHz
High Shutdown Isolation of –92 dB @ 5 MHz
Low Cost
Fast Output Disable Feature for Connecting Multiple Devices (AD8174 Only)
Shutdown Feature Reduces Power to 1.5 mA (AD8174 Only)

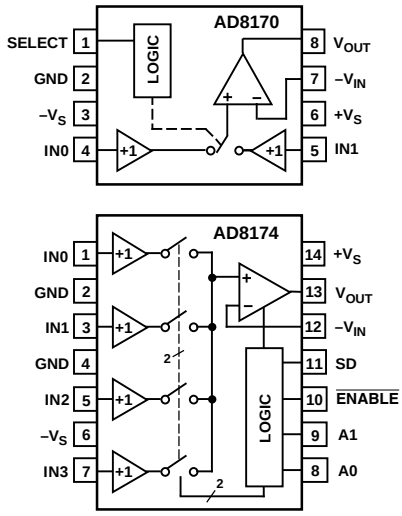
APPLICATIONS

Pixel Switching for "Picture-In-Picture"
LCD and Plasma Displays
Video Routers

PRODUCT DESCRIPTION

The AD8170(2:1) and AD8174(4:1) are very high speed buffered multiplexers. These multiplexers offer an internal current feedback output amplifier whose gain can be programmed via external resistors and is capable of delivering 50 mA of output current. They offer –3 dB signal bandwidth of 250 MHz and slew rate of greater than 1000 V/μs. Additionally, the AD8170 and AD8174 have excellent video specifications with low differential gain and differential phase error of 0.02% and 0.05° and 0.1 dB flatness out to 80 MHz. With a low 78 dB of crosstalk and better than 88 dB isolation, these devices are useful in many high speed applications. These are low power devices consuming only 9.7 mA from a ±5 V supply.

FUNCTIONAL BLOCK DIAGRAM



The AD8174 offers a high speed disable feature allowing the output to be put into a high impedance state for cascading stages so that the off channels do not load the output bus. Additionally, the AD8174 can be shut down (SD) when not in use to minimize power consumption (I_S = 1.5 mA). These products will be offered in 8-lead and 14-lead PDIP and SOIC packages.

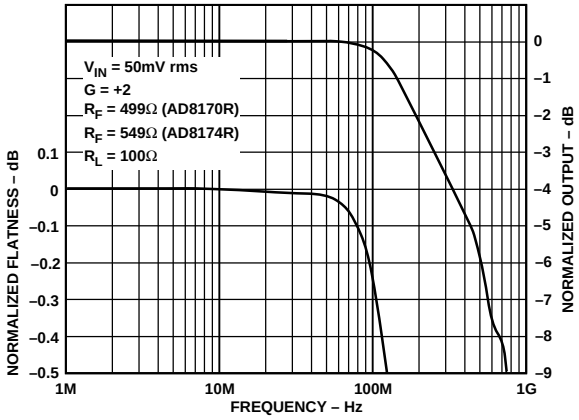


Figure 1. Small Signal Frequency Response

REV. 0

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AD8170/AD8174—SPECIFICATIONS (@ T_A = +25°C, V_S = ±5 V, R_L = 150 Ω, G = +2, R_F = 499 Ω (AD8170R), R_F = 549 Ω (AD8174R) unless otherwise noted)

Parameter		Conditions	AD8170A/AD8174A Min	Typ	Max	Units
SWITCHING CHARACTERISTICS						
Switching Time[1]		Channel-to-Channel				
50% Logic to 10% Output Settling		IN0, IN2 = +0.5 V; IN1, IN3 = –0.5 V		7.5		ns
50% Logic to 90% Output Settling		IN0, IN2 = +0.5 V; IN1, IN3 = –0.5 V		9.1		ns
50% Logic to 99.9% Output Settling		IN0, IN2 = +0.5 V; IN1, IN3 = –0.5 V		25		ns
$\overline{\text{ENABLE}}$ to Channel ON Time[2] (AD8174R)						
50% Logic to 90% Output Settling		IN0, IN2 = +0.5 V; IN1, IN3 = –0.5 V		17		ns
$\overline{\text{ENABLE}}$ to Channel OFF Time[2] (AD8174R)						
50% Logic to 90% Output Settling		IN0, IN2 = +0.5 V; IN1, IN3 = –0.5 V		120		ns
Shutdown to Channel ON Time[3] (AD8174R)						
50% Logic to 90% Output Settling		IN0, IN2 = +0.5 V; IN1, IN3 = –0.5 V		20		ns
Shutdown to Channel OFF Time[3] (AD8174R)						
50% Logic to 90% Output Settling		IN0, IN2 = +0.5 V; IN1, IN3 = –0.5 V		115		ns
Channel Switching Transient (Glitch)[4]		All Inputs Grounded		138 /104		mV p-p
DIGITAL INPUTS						
Logic "1" Voltage		SELECT, A0, A1, $\overline{\text{ENABLE}}$, SD Inputs, T_{MIN}–T_{MAX}	2.0			V
Logic "0" Voltage		SELECT, A0, A1, $\overline{\text{ENABLE}}$, SD Inputs, T_{MIN}–T_{MAX}			0.8	V
Logic "1" Input Current		SELECT, A0, A1 Inputs, T_{MIN}–T_{MAX}		50	300	nA
		$\overline{\text{ENABLE}}$, SD Inputs, T_{MIN}–T_{MAX}		1	5	µA
Logic "0" Input Current		SELECT, A0, A1 Inputs, T_{MIN}–T_{MAX}		3	5	µA
		$\overline{\text{ENABLE}}$, SD Inputs, T_{MIN}–T_{MAX}		30	300	nA
DYNAMIC PERFORMANCE						
–3 dB Bandwidth (Small Signal)[5]		V_O = 50 mV rms, R_L = 100 Ω		250		MHz
–3 dB Bandwidth (Large Signal)[5]		V_O = 1 V rms, R_L = 100 Ω		100		MHz
0.1 dB Bandwidth[5]		V_O = 50 mV rms, R_F = 499 Ω (AD8170R), R_L = 100 Ω				
		V_O = 50 mV rms, R_F = 549 Ω (AD8174R), R_L = 100 Ω		85		MHz
Rise and Fall Time (10% to 90%)		2 V Step		1.6		ns
Slew Rate		2 V Step		1000		V/µs
Settling Time to 0.1%		2 V Step		15		ns
DISTORTION/NOISE PERFORMANCE						
Differential Gain		f = 3.58 MHz		0.02		%
Differential Phase		f = 3.58 MHz		0.05		Degrees
All Hostile Crosstalk[6]	AD8170R	f = 5 MHz, R_L = 100 Ω		–80		dB
		f = 30 MHz, R_L = 100 Ω		–65		dB
	AD8174R	f = 5 MHz, R_L = 100 Ω		–78		dB
		f = 30 MHz, R_L = 100 Ω		–63		dB
Disable Isolation[7]	AD8174R	f = 5 MHz, R_L = 100 Ω		–88		dB
		f = 30 MHz, R_L = 100 Ω		–72		dB
Shutdown Isolation[8]	AD8174R	f = 5 MHz, R_L = 100 Ω		–92		dB
		f = 30 MHz, R_L = 100 Ω		–77		dB
Input Voltage Noise		f = 10 kHz to 30 MHz		10		nV/$\sqrt{\text{Hz}}$
+Input Current Noise		f = 10 kHz to 30 MHz		1.6		pA/$\sqrt{\text{Hz}}$
–Input Current Noise		f = 10 kHz to 30 MHz		8.5		pA/$\sqrt{\text{Hz}}$
Total Harmonic Distortion		f_C = 10 MHz, V_O = 2 V p-p, R_L = 150 Ω		–60		dBc
		f_C = 10 MHz, V_O = 2 V p-p, R_L = 1 kΩ		–72		dBc
DC/TRANSFER CHARACTERISTICS						
Transresistance			400	600		kΩ
Open-Loop Voltage Gain			2000	6000		V/V
Gain Accuracy[9]		G = +1, R_F = 1 kΩ		0.4		%
Gain Matching		Channel-to-Channel		0.05		%
Input Offset Voltage				5	9	mV
		T_{MIN} to T_{MAX}			12	mV
Input Offset Voltage Matching		Channel-to-Channel		1.5	5	mV
Input Offset Voltage Drift				11		µV/°C
Input Bias Current		(+) Switch Input		7	15	µA
		T_{MIN} to T_{MAX}			15	µA
		(–) Buffer Input		3	10	µA
		T_{MIN} to T_{MAX}			14	µA
Input Bias Current Drift		(+) Switch and (–) Buffer Input		20		nA/°C

Parameter		Conditions	AD8170A/AD8174A Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Input Resistance		(+) Switch Input		1.7		MΩ
		(–) Buffer Input		100		Ω
Input Capacitance		Channel Enabled (R Package)		1.1		pF
		Channel Disabled (R Package)		1.1		pF
Input Voltage Range				±3.3		V
Input Common-Mode Rejection Ratio		+CMRR, ΔV_{CM} = 1 V	51	56		dB
		–CMRR, ΔV_{CM} = 1 V	50	52		dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing		R_L = 1 kΩ, T_{MIN}–T_{MAX}	±4.0	±4.26		V
		R_L = 150 Ω, T_{MIN}–T_{MAX}	±3.5	±4.0		V
Output Current		R_L = 10 Ω		50		mA
Short Circuit Current				180		mA
Output Resistance		Enabled		10		mΩ
		Disabled (AD8174)		10		MΩ
Output Capacitance		Disabled (AD8174)		7.5		pF
POWER SUPPLY						
Operating Range			±4		±6	V
Power Supply Rejection Ratio	+PSRR	$+V_S$ = +4.5 V to +5.5 V, $-V_S$ = –5 V	58	66		dB
		T_{MIN}–T_{MAX}	55			dB
	–PSRR	$-V_S$ = –4.5 V to –5.5 V, $+V_S$= +5 V	52	58		dB
		T_{MIN}–T_{MAX}	50			dB
Quiescent Current		All Channels "ON", T_{MIN}–T_{MAX}		8.7/9.7	11/13	mA
		AD8174 Disabled, T_{MIN}–T_{MAX}		4.1	5	mA
		AD8174 Shutdown, T_{MIN}–T_{MAX}		1.5	2.5	mA
OPERATING TEMPERATURE RANGE			–40		+85	°C

NOTES

[1]Shutdown (SD) and $\overline{\text{ENABLE}}$ pins are grounded (AD8174). IN0 (or IN2) = +0.5 V dc, IN1 (or IN3) = –0.5 V dc. SELECT (A0 or A1 for AD8174) input is driven with 0 V to +5 V pulse. Measure transition time from 50% of SELECT (A0 or A1) input value (+2.5 V) and 10% (or 90%) of the total output voltage transition from IN0 (or IN2) channel voltage (+0.5 V) to IN1 (or IN3 = –0.5 V) or vice versa.

[2]AD8174 only. Shutdown (SD) pin is grounded. $\overline{\text{ENABLE}}$ pin is driven with 0 V to +5 V pulse (5 ns rise and fall times). State of A0 and A1 logic inputs determines which channel is activated (i.e., if A0 = Logic 0 and A1 = Logic 1, then IN2 input is selected). Set IN0 (or IN2) = +0.5 V dc, IN1 (or IN3) = –0.5 V dc, and measure transition time from 50% of $\overline{\text{ENABLE}}$ pulse (+2.5 V) to 90% of the total output voltage change. In Figure 5, Δt_{OFF} is the disable time, Δt_{ON} is the enable time.

[3]AD8174 only. $\overline{\text{ENABLE}}$ pin is grounded. Shutdown (SD) pin is driven with 0 V to +5 V pulse (5 ns rise and fall times). State of A0 and A1 logic inputs determines which channel is activated (i.e., if A0 = Logic 1 and A1 = Logic O, then IN1 input is selected). Set IN0 (or IN2) = +0.5 V dc, IN1 (or IN3) = –0.5 V dc, and measure transition time from 50% of SD pulse (+2.5 V) to 90% of the total output voltage change. In Figure 6, Δt_{OFF} is the shutdown assert time, Δt_{ON} is the shutdown release time.

[4]All inputs are grounded. SELECT (A0 or A1 for AD8174) input is driven with 0 V to +5 V pulse. The outputs are monitored. Speeding the edges of the SELECT (A0 or A1) pulse increases the glitch magnitude due to coupling via the ground plane.

[5]Bandwidth of the multiplexer is dependent upon the resistor feedback network. Refer to Table III for recommended feedback component values, which give the best compromise between a wide and a flat frequency response.

[6]Select input(s) that is (are) not being driven (i.e., if SELECT is Logic 1, activated input is IN1; in AD8174, if A0 = Logic 0, A1 = Logic 1, activated input is IN2). Drive all other inputs with V_{IN} = 0.707 V rms, and monitor output at f = 5 MHz and 30 MHz; R_L = 100 Ω (see Figure 13).

[7]AD8174 only. Shutdown (SD) pin is grounded. Mux is disabled, (i.e., $\overline{\text{ENABLE}}$ = Logic 1) and all inputs are driven simultaneously with V_{IN} = 0.354 V rms. Output is monitored at f = 5 MHz and 30 MHz; R_L = 100 Ω. In this mode, the output impedance of the disabled mux is very high (typ 10 MΩ), and the signal couples across the package; the load impedance and the feedback network determine the crosstalk. For instance, in a closed-loop gain of +1, $r_{OUT} \cong$ 10 MΩ, in a gain of +2 ($R_F = R_G$ = 549 Ω), r_{OUT} = 1.1 kΩ (see Figure 14).

[8]AD8174 only. $\overline{\text{ENABLE}}$ pin is grounded. Mux is shutdown (i.e., SD = Logic 1), and all inputs are driven simultaneously with V_{IN} = 0.354 V rms. Output is monitored at f = 5 MHz and 30 MHz; R_L = 100 Ω. (see Figure 14). The mux output impedance in shutdown mode is the same as the disabled mux output impedance.

[9]For Gain Accuracy expression, refer to Equation 4.

Specifications subject to change without notice.

Table I. AD8170 Truth Table

SELECT	V_{OUT}
0	IN0
1	IN1

Table II. AD8174 Truth Table

A0	A1	$\overline{\text{ENABLE}}$	SD	V_{OUT}
0	0	0	0	IN0
1	0	0	0	IN1
0	1	0	0	IN2
1	1	0	0	IN3
X	X	1	0	HIGH Z, I_S = 4.1 mA
X	X	X	1	HIGH Z, I_S = 1.5 mA

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 12.6 V
Internal Power Dissipation[2]
AD8170 8-Lead Plastic (N) . . . . . 1.3 Watts
AD8170 8-Lead Small Outline (R) . . . . . 0.9 Watts
AD8174 14-Lead Plastic (N) . . . . . 1.6 Watts
AD8174 14-Lead Small Outline (R) . . . . . 1.0 Watts
Input Voltage (Common Mode) . . . . . $\pm V_S$
Output Short Circuit Duration . . Observe Power Derating Curves
Storage Temperature Range
N & R Packages . . . . . –65°C to +125°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air: 8-Pin Plastic Package: θ_{JA} = 90°C/Watt; 8-Pin SOIC Package: θ_{JA} = 160°C/Watt; 14-Pin Plastic Package: θ_{JA} = 90°C/Watt 14-Pin SOIC Package: θ_{JA} = 120°C/Watt, where $P_D = (T_J - T_A)/\theta_{JA}$.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8170AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD8170AR	–40°C to +85°C	8-Pin SOIC	SO-8
AD8170AR-REEL	–40°C to +85°C	Reel 8-Pin SOIC	SO-8
AD8174AN	–40°C to +85°C	14-Pin Plastic DIP	N-14
AD8174AR	–40°C to +85°C	14-Pin Narrow SOIC	R-14
AD8174AR-REEL	–40°C to +85°C	Reel 14-Pin SOIC	R-14
AD8170-EB	Evaluation Board	For AD8170R	
AD8174-EB	Evaluation Board	For AD8174R	

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8170 and AD8174 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

While the AD8170 and AD8174 are internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figures 2 and 3.

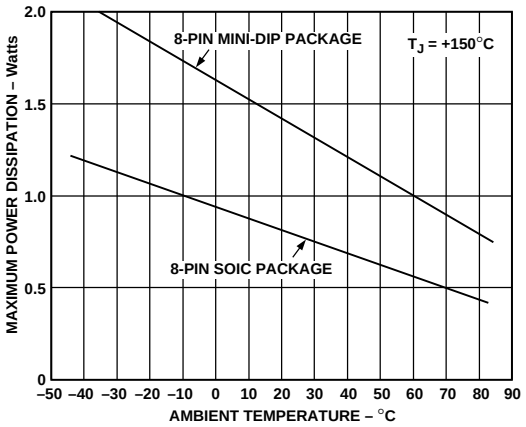


Figure 2. AD8170 Maximum Power Dissipation vs. Temperature

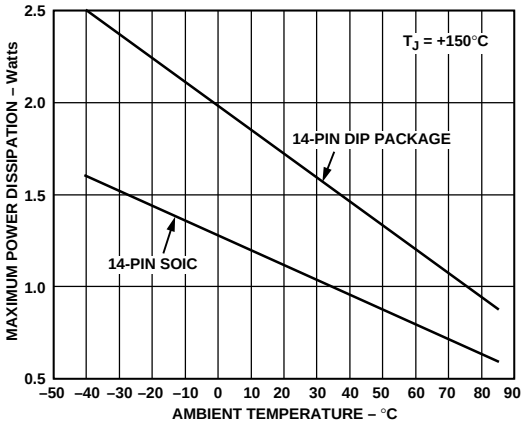


Figure 3. AD8174 Maximum Power Dissipation vs. Temperature

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8170/AD8174 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

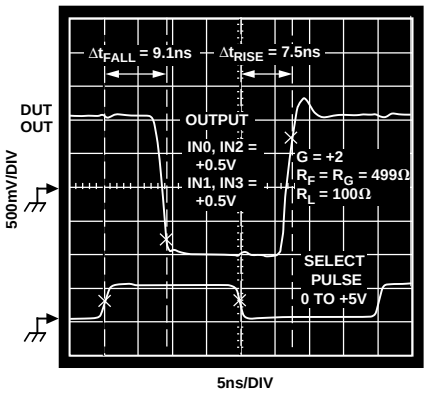


Figure 4. Channel Switching Characteristics

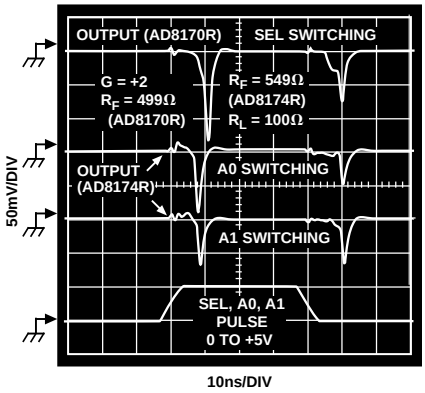


Figure 7. Switching Transient (Glitch) Response

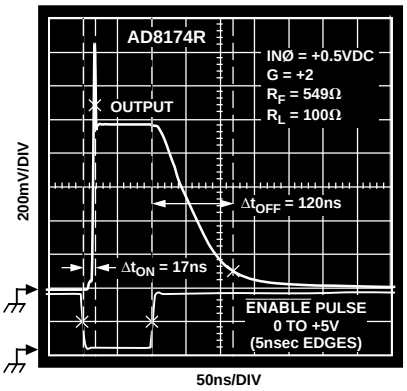


Figure 5. Enable and Disable Switching Characteristics

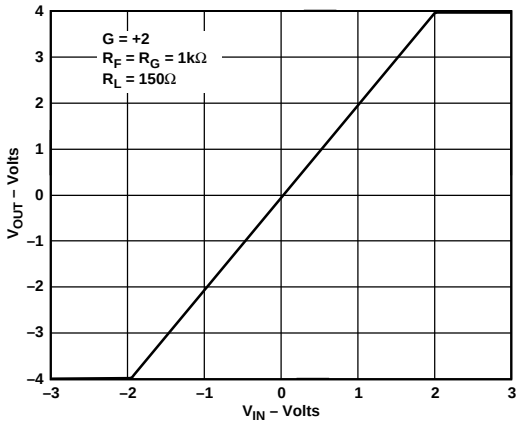


Figure 8. Output Voltage vs. Input Voltage, G = +2

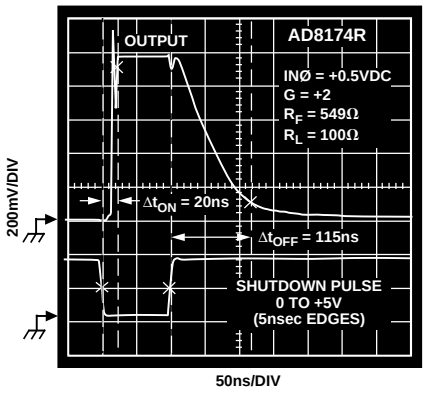


Figure 6. Shutdown Switching Characteristics

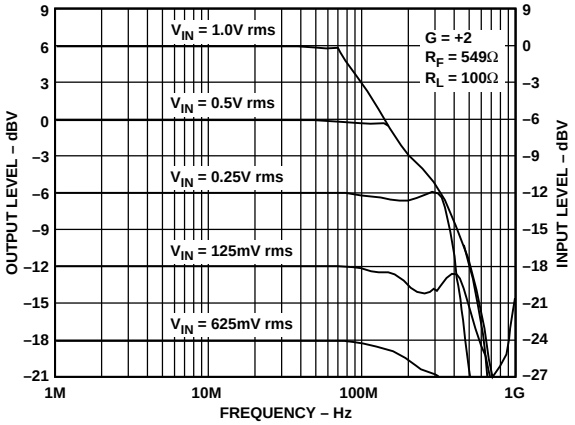


Figure 9. Large Signal Frequency Response

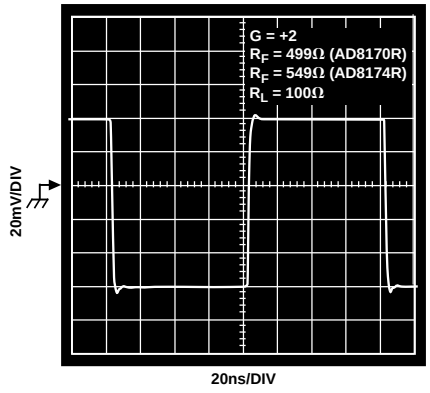


Figure 10. Small Signal Pulse Response

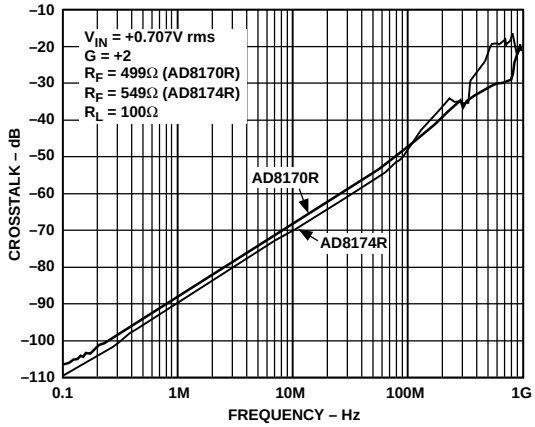


Figure 13. All-Hostile Crosstalk vs. Frequency

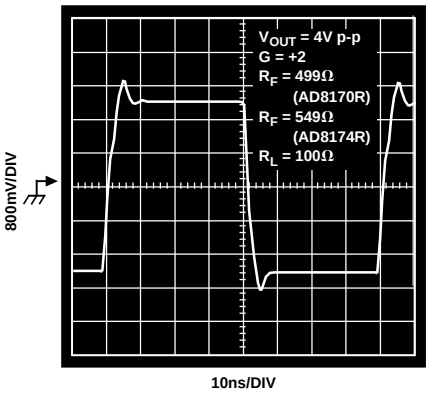


Figure 11. Large Signal Transient Response

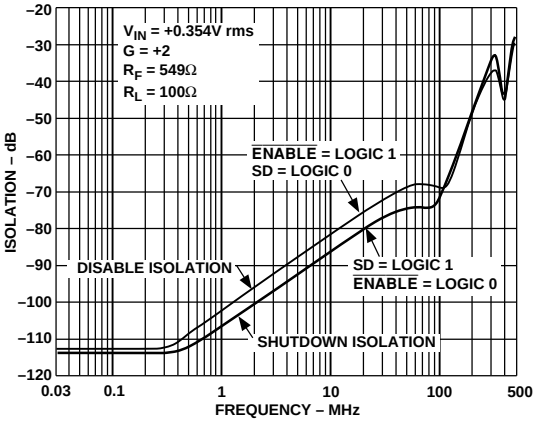


Figure 14. AD8174R Disable and Shutdown Isolation vs. Frequency

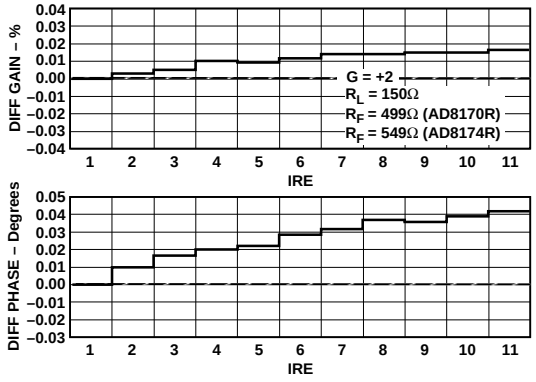


Figure 12. Differential Gain and Phase Error

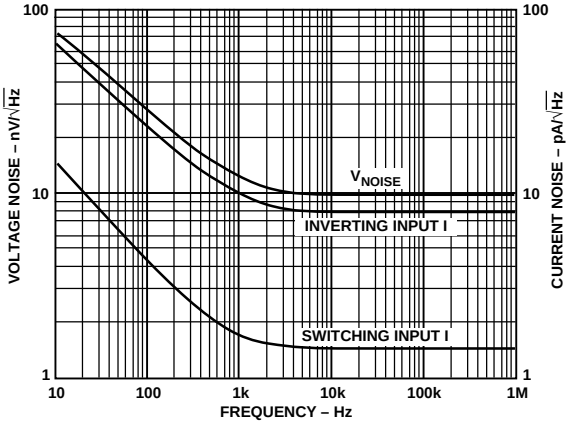


Figure 15. Noise vs. Frequency

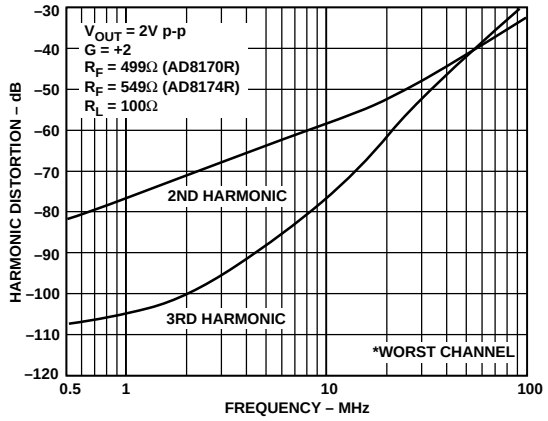


Figure 16. Harmonic Distortion vs. Frequency

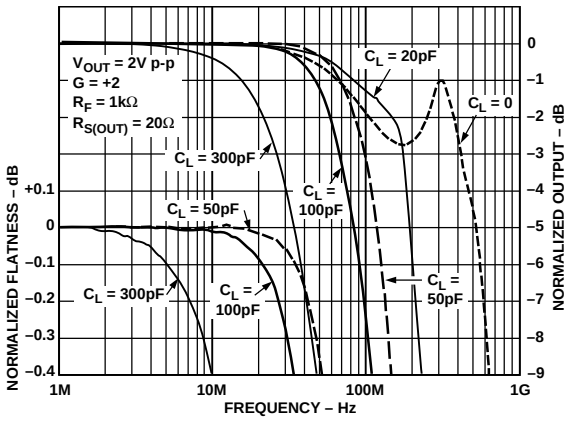


Figure 19. Frequency Response vs. Capacitive Load, G = +2

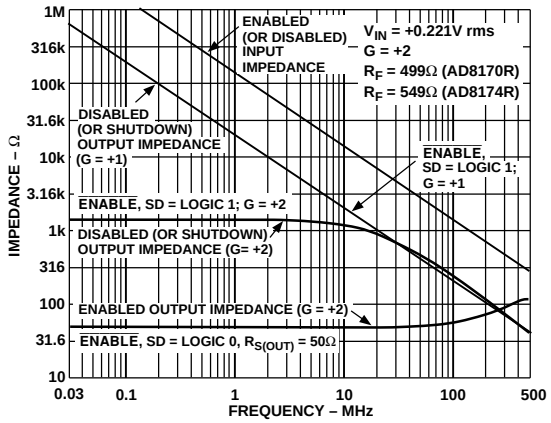


Figure 17. Input & Output Impedance vs. Frequency

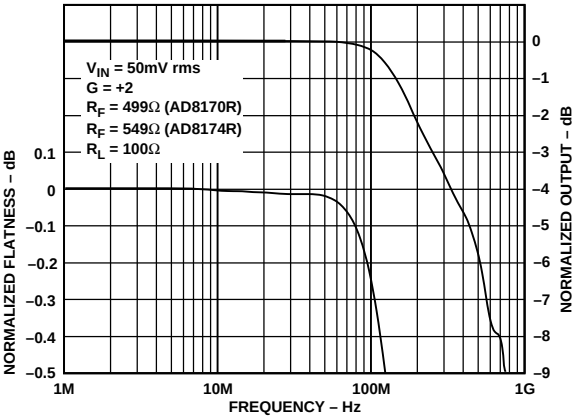


Figure 20. Small Signal Frequency Response

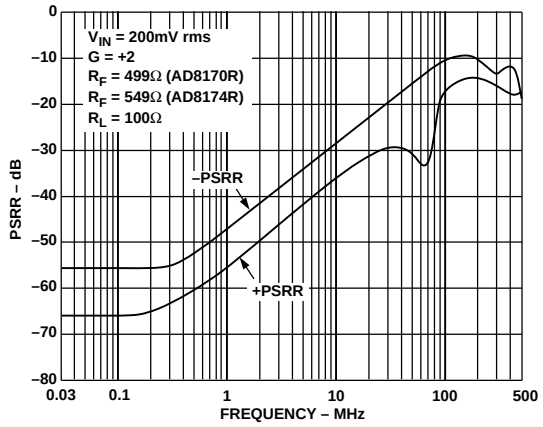


Figure 18. Power Supply Rejection vs. Frequency

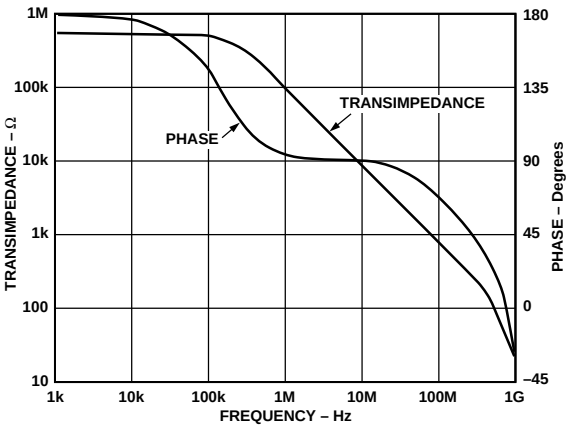


Figure 21. Open-Loop Transresistance and Phase vs. Frequency

THEORY OF OPERATION

General

The AD8170/AD8174 multiplexers integrate wideband analog switches with a high speed current feedback amplifier. The input switches are complementary bipolar follower stages that are turned on and off by using a current steering technique that attains switch times of less than 10 ns and ensures low switching transients. The 250 MHz current feedback amplifier provides up to 50 mA of drive current. Overall gain and frequency response are set by external resistors for maximum versatility.

Figure 22 is a block diagram of the multiplexer signal chain, with a simplified schematic of an input switch. When the channel is on (i.e., V_{ONB} more positive than V_{REFB}, V_{ONT} more negative than V_{REFT}), I2 flows through Q1 and Q2, and I3 flows through Q3 and Q4. This biases up Q5 through Q8 to form the unity gain follower. I1 and I4 (the "off" currents) are steered, either to another switch or to the power supply. When the channel turns off, I2 and I3 are steered away while I1 switches over to pull the base of Q8 up to V_{CLT} + 1 V_{BE} (about 2.7 volts from ground reference) and I4 switches over to pull the base of Q5 down to V_{CLB} – 1 V_{BE} (about –2.7 volts away from ground reference). Clamping the bases of the reverse biased output transistors to a low impedance point greatly improves isolation performance.

The AD8174 has four switches with outputs wired together and driving the positive input of a current feedback amplifier to form a 4:1 multiplexer. It is designed so that only one channel is on at a time. By bringing $\overline{\text{ENABLE}}$ high, the supply current for the amplifier is shut off. This turns the output of the amplifier into a high impedance, allowing the AD8174 to be used in larger arrays. In practice, the disabled output impedance of the mux will be determined by the amplifier's feedback network.

Bringing SD high shuts off the supply current for all the switches, that some of the logic control circuitry and the amplifier, reducing the quiescent current drain to 1.5 mA. If the $\overline{\text{ENABLE}}$ and SD functions are not to be used, those respective pins must be tied to ground for proper operation. Any unused channel input should also be tied to ground.

The AD8170 has two switches driving an amplifier to form a 2:1 multiplexer. No disable or shutdown functions are provided.

DC Performance and Noise Considerations

Figure 23 shows the different contributors to total output offset and noise. Total expected output offset can be calculated using Equation 1 below:

$$V_{OS}(out) = \left[\left(I_{B^+} \times R_S\right) + V_{OS}\right]\left[1 + \frac{R_F}{R_G}\right] + \left(I_{B^-} \times R_F\right) \quad (1)$$

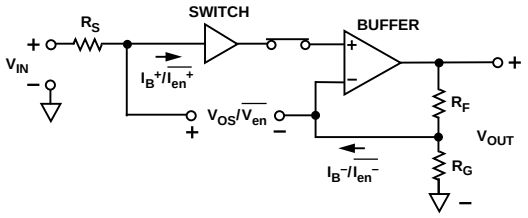


Figure 23. DC Errors for Buffered Multiplexer

Equations 2 and 3 below can be used to predict the output voltage noise of the multiplexer for different choices of gains and external resistors. The different contributions to output noise are root-sum-squared to calculate total output noise spectral density in Equation 2. As there is no peaking in the multiplier's noise characteristic, the total peak-to-peak output noise will be accurately predicted using Equation 3.

$$\overline{V}_{EN_{(OUT)}}\left(nV/\sqrt{Hz}\right) = \sqrt{\left[\left(\overline{I_{EN^+}} \times R_S\right)^2 + \left(\overline{V}_{EN}\right)^2\right]\left[1 + \frac{R_F}{R_G}\right]^2 + \left(\overline{I_{EN^-}} \times R_F\right)^2 + 4KT\left[R_F + R_S\left[1 + \frac{R_F}{R_G}\right]^2 + R_G\left(\frac{R_F}{R_G}\right)^2\right]} \quad (2)$$

$$\overline{V_{EN}}\ p\text{–}p = \overline{V_{EN}} \times \sqrt{f_{-3\,dB}} \times 6.2 \times 1.26 \quad (3)$$

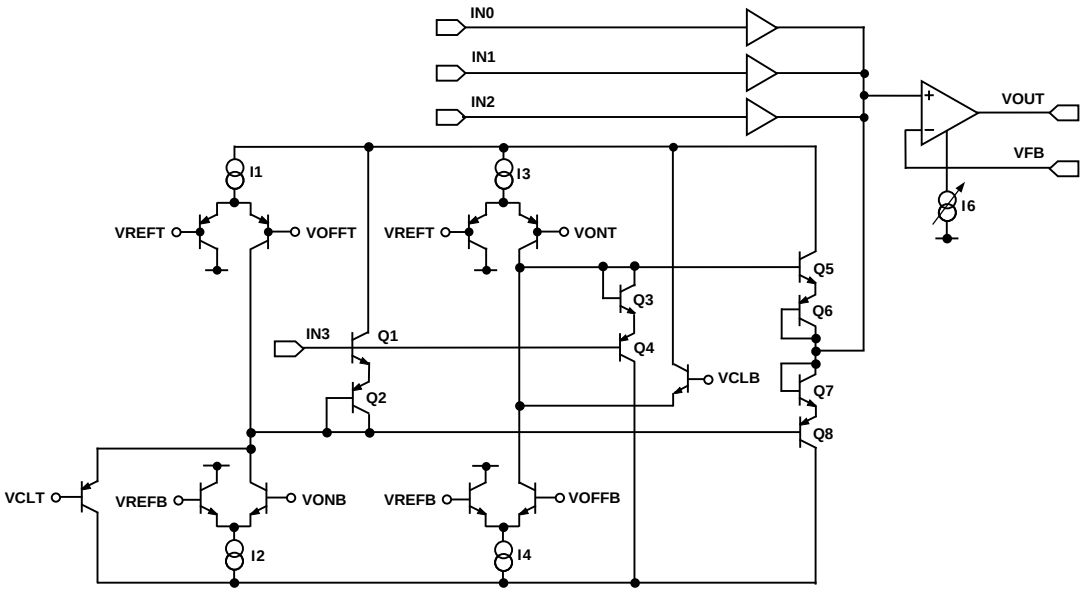


Figure 22. Block Diagram and Simplified Schematic of the AD8170

Equation 4 can be used to calculate expected gain error due to the current feedback amplifier's finite transimpedance and common mode rejection. For low gains and recommended feedback resistors, this will be typically less than 0.4%. For most applications with gain greater than 1, the dominant source of gain error will most likely be the ratio-match of the external resistors. All of the dominant contributors to gain error are associated with the buffer amplifier and external resistors. These do not change as different channels are selected, so channel-to-channel gain match of less than 0.05% is easily attained.

$$G = \left[1+\frac{R_F}{R_G}\right]\frac{R_T}{\left[R_T + R_{IN}\left[1+\frac{R_F}{R_G}\right]+R_F\right]}\left[1-CMRR\right] \quad (4)$$

Ideal Gain ↑ Error Terms ↑

R_T = Amplifier Transresistance = 600 kΩ
R_{IN} = Amplifier Input Resistance ≅ 100 Ω
CMRR = Amplifier Common-Mode Rejection ≅ –52 dB

Choice of External Resistors

The gain and bandwidth of the multiplexer are determined by the closed-loop gain and bandwidth of the onboard current feedback amplifier. These both may be customized by the external resistor feedback network. Table III shows typical bandwidths at some common closed loop gains for given feedback and gain resistors (R_F and R_G, respectively).

The choice of R_F is not critical unless the widest and flattest frequency response must be maintained. The resistors recommended in the table result in the widest 0.1 dB bandwidth with the least peaking. 1% resistors are recommended for applications requiring the best control of bandwidth. Packaging parasitics vary between DIP and SOIC packages, which may result in a slightly different resistor value for optimum frequency performance. Wider bandwidths than those listed in the table can be attained by reducing R_F at the expense of increased peaking.

To estimate the –3 dB bandwidth for feedback resistors not listed in Table III, the following single-pole model for the current feedback amplifier may be used:

$$A_{CL} = \frac{G}{1+sC_T\left(R_F + G_N\ R_{IN}\right)}$$

A_{CL} = Closed Loop Gain
C_T = Transcapacitance ≅ 0.8 pF
R_F = Feedback Resistor
G = Ideal Closed Loop Gain
G_N = (1 + R_F/R_G) = Noise Gain
R_{IN} = Inverting Terminal Input Resistance ≅ 100 Ω

The –3 dB bandwidth is determined from this model as:

$$f_{-3\,dB} \cong \frac{1}{2\pi\, C_T\left(R_F + G_N\ R_{IN}\right)}$$

This model is typically good to within 15%.

Table III. Recommended Component Values

	Gain	R_F (Ω)	R_G (Ω)	Small Signal V_{OUT} = 50 mV rms –3 dB BW (MHz)	Large Signal V_{OUT} = 0.707 V rms –3 dB BW (MHz)
AD8170R	+1	1 k	—	710	270
	+2	499	499	250	290
	+10	499	54.9	50	55
	+20	499	26.3	27	27
AD8174R	+1	1 k	—	780	270
	+2	549	549	235	280
	+10	499	54.9	50	55
	+20	499	26.3	27	27

Capacitive Load

The general rule for current feedback amplifiers is that the higher the load capacitance, the higher the feedback resistor required for stable operation. For the best combination of wide bandwidth and clean pulse response, a small output resistor is also recommended, as shown in Figure 24. Table IV contains values of feedback and series resistors that result in the best pulse response for a given load capacitance.

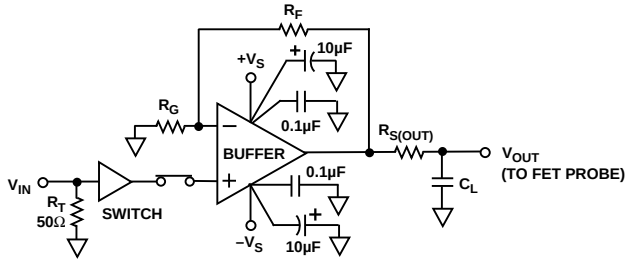


Figure 24. Circuit for Driving a Capacitive Load

Table IV. Recommended Feedback and Series Resistors and Bandwidth vs. Capacitive Load and Gain

	G = +1			G = +2			G = +3			G ⩾ +4	
C_L (pF)	R_F (Ω)	R_{SOUT} (Ω)	V_{OUT} = 2 V p-p –3 dB BW (MHz)	R_F (Ω)	R_{SOUT} (Ω)	V_{OUT} = 2 V p-p –3 dB BW (MHz)	R_F (Ω)	R_{SOUT} (Ω)	V_{OUT} = 2 V p-p –3 dB BW (MHz)	R_F (Ω)	R_{SOUT} (Ω)
20	1 k	50	149	1 k	20	174	499	25	170	499	20
50	1 k	30	104	1 k	15	117	1 k	15	98	499	20
100	2k	20	73	1 k	15	80	1 k	15	71	499	15
300	2k	20	27	1 k	15	34	1 k	15	33	499	15

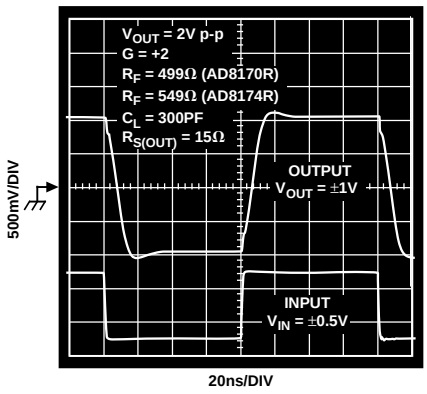


Figure 25. Pulse Response Driving a Large Load Capacitor, C_L = 300 pF

Overload Behavior and Recovery

There are three important overload conditions: input voltage overdrive, output voltage overdrive and current overload at the amplifier's negative feedback input.

At a gain of 1, recovery from driving the input voltages beyond the voltage range of the input switches is very quick, typically less than 30 ns. Recovery from output overdrive is somewhat slower and depends on how much the output is overdriven. Recovery from 15% overdrive is under 60 ns. 50% overdrive produces recovery times of about 85 ns.

Input overdrive in a high gain application can result in a large current flow in the input stage. This current is internally limited to 40 mA. The effect on total power dissipation should be taken into account.

LAYOUT CONSIDERATIONS:

Realizing the high speed performance attainable with the AD8170 and AD8174 requires careful attention to board layout and component selection. Proper RF design techniques and low parasitic component selection are mandatory.

Wire wrap boards, prototype boards, and sockets are not recommended because of their high parasitic inductance and capacitance. Instead, surface-mount components should be soldered directly to a printed circuit board (PCB). The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance ground path. The ground plane should be removed from the area near input and output pins to reduce stray capacitance.

Chip capacitors should be used for supply bypassing. One end of the capacitor should be connected to the ground plane and the other within 1/4 inch of each power pin. An additional large (4.7 μF–10 μF) tantalum capacitor should be connected in parallel with each of the smaller capacitors for low impedance supply bypassing over a broad range of frequencies.

Signal traces should be as short as possible. Stripline or microstrip techniques should be used for long signal traces (longer than about 1 inch). These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end using surface mount components.

Careful layout is imperative to minimize crosstalk. Guards (ground or supply traces) must be run between all signal traces to limit direct capacitive coupling. Input and output signal lines should fan out away from the mux as much as possible. If multiple signal layers are available, a buried stripline structure having ground plane above, below, and between signal traces will have the best crosstalk performance.

Return currents flowing through termination resistors can also increase crosstalk if these currents flow in sections of the finite-impedance ground circuit that is shared between more than one input or output. Minimizing the inductance and resistance of the ground plane can reduce this effect, but further care should be taken in positioning the terminations. Terminating cables directly at the connectors will minimize the return current flowing on the board, but the signal trace between the connector and the mux will look like an open stub and will degrade the frequency response. Moving the termination resistors close to the input pins will improve the frequency response, but the terminations from neighboring inputs should not have a common ground return.

APPLICATIONS

8-to-1 Video Multiplexer

Two AD8174 4-to-1 multiplexers can be combined with a single digital inverter to yield an 8-to-1 multiplexer as shown in Figure 26. The $\overline{\text{ENABLE}}$ control pin allows the two op amp outputs to be connected together directly. Taking the $\overline{\text{ENABLE}}$ pin high shuts off the supply current to the output op amp and places the op amp's output and inverting input (Pin 12, $-V_{IN}$) in high impedance states.

The two least significant bits (LSBs) of the address lines connect directly to the A0 and A1 inputs of both AD8174 devices. The third address line connects directly to the $\overline{\text{ENABLE}}$ input on one device and is inverted before being applied to the $\overline{\text{ENABLE}}$ input on the second device. As a result, when one device is enabled, the second device presents a high impedance. The op amp of the enabled device must however drive both feedback networks ((549 Ω + 549 Ω)/2).

The gain of this multiplexer has been set to +2 in this example. This gives an overall gain of +1 when back terminated lines are used. In applications where switching and settling times are critical, the digital control pins (A0, A1 and $\overline{\text{ENABLE}}$) should also be appropriately terminated (with either 50 Ω or 75 Ω).

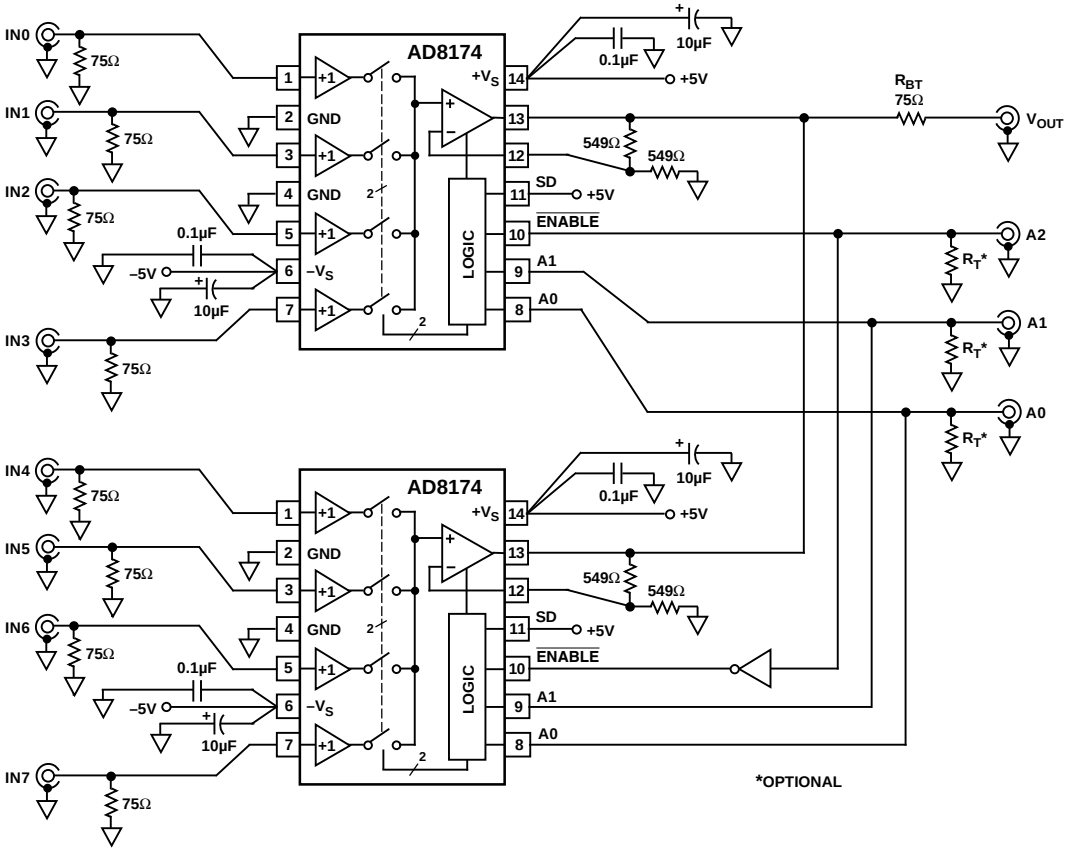


Figure 26. 8-to-1 Multiplexer

Color Document Scanner

Charge Coupled Devices (CCDs) find widespread use in scanner applications. A monochrome CCD delivers a serial stream of voltage levels, each level being proportional to the light shining on that cell. In the case of the color image scanner shown, there are three output streams, representing red, green and blue. Interlaced with the stream of voltage levels is a voltage representing the reset level (or black level) of each cell. A Correlated Double Sampler (CDS) subtracts these two voltages from each other in order to eliminate the relatively large offsets which are common with CCDs.

The next step in the data acquisition process involves digitizing the three signal streams. Assuming that the analog to digital converter chosen has a fast enough sample rate, multiplexing the three streams into a single ADC is generally more economic than using one ADC per channel. In the example shown, the AD8174 is used to multiplex the red, green and blue channels into the AD876, an 8- or 10-bit 20 MSPS ADC. Because of its high bandwidth, the AD8174 is capable of driving the switched capacitor input stage of the AD876 without additional buffering. In addition to the bandwidth, it is necessary to consider the settling time of the multiplexer. In this case, the ADC has a sample rate of 20 MHz which corresponds to a sampling period of 50 ns. Typically, one phase of the sampling clock is used for conversion (i.e., all levels are held steady) and the other phase is used for switching and settling to the next channel. Assuming a 50% duty cycle, the signal chain must settle within 25 ns. With a settling time to 0.1% of 15 ns, the multiplexer easily satisfies this criterion.

In the example shown, the fourth (spare) channel of the AD8174 is used to measure a reference voltage. This voltage would probably be measured less frequently than the R, G and B signals. Multiplexing a reference voltage offers the advantage that any temperature drift effects caused by the multiplexer will equally impact the reference voltage and the to-be-measured signals. If the fourth channel is unused, it is good design practice to tie the input permanently to ground.

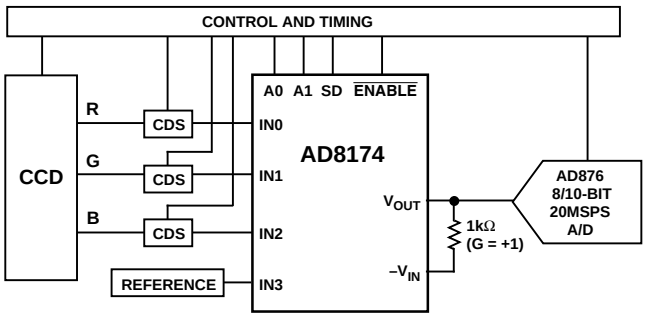


Figure 27. Color Document Scanner

EVALUATION BOARD

Evaluation boards for the AD8170 and AD8174 are available that have been carefully laid out and tested to demonstrate the specified high speed performance of the devices. Figure 28 and Figure 32 show the schematics of the AD8170 and AD8174 evaluation boards respectively. For ordering information, please refer to the Ordering Guide.

Figure 29 shows the silkscreen of the component side of the solder side of the AD8170 evaluation board. Figures 30 and 31 show the layout of the component side and solder side respectively. The silkscreens and layout of the AD8174 evaluation board are shown in Figures 33, 34, 35 and 36.

Both evaluation boards ship with 75 Ω termination resistors on their analog inputs and analog outputs. To use the evaluation board in nonvideo applications where 50 Ω termination is more popular, these resistors can be replaced with 50 Ω values. The digital control pins are terminated with 50 Ω resistors to allow easy connection to laboratory equipment.

The gain of the output current feedback op amp on both boards has been set to +2. For other gains the two gain resistors can be easily replaced. Refer to Table III for appropriate values at gains other than +2.

For connection to external instruments, side-launched SMA type connectors are provided. Space is also provided on the board for the installation of SMB of SMC type connectors.

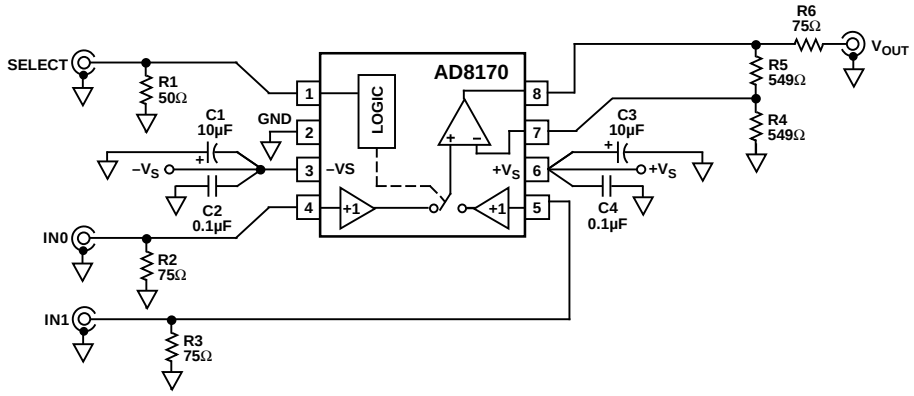


Figure 28. AD8170 Evaluation Board

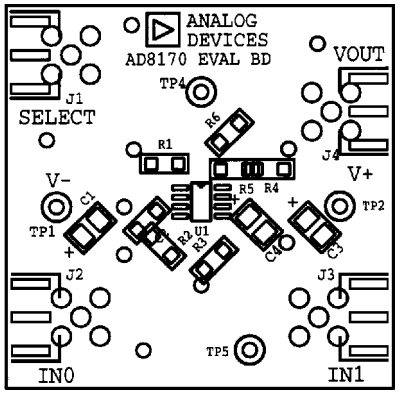


Figure 29. AD8170 Component Side Silkscreen

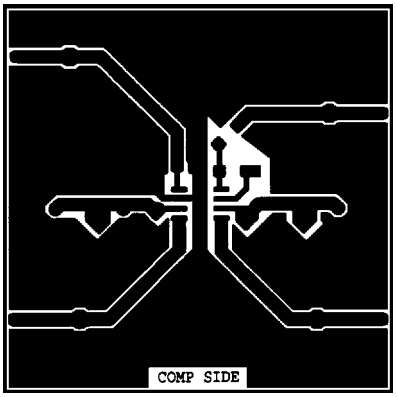


Figure 30. AD8170 Board Layout (Component Side)

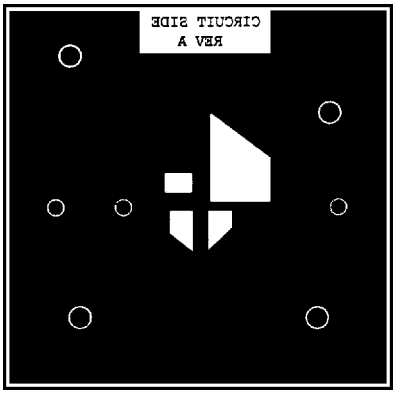


Figure 31. AD8170 Board Layout (Solder Side)

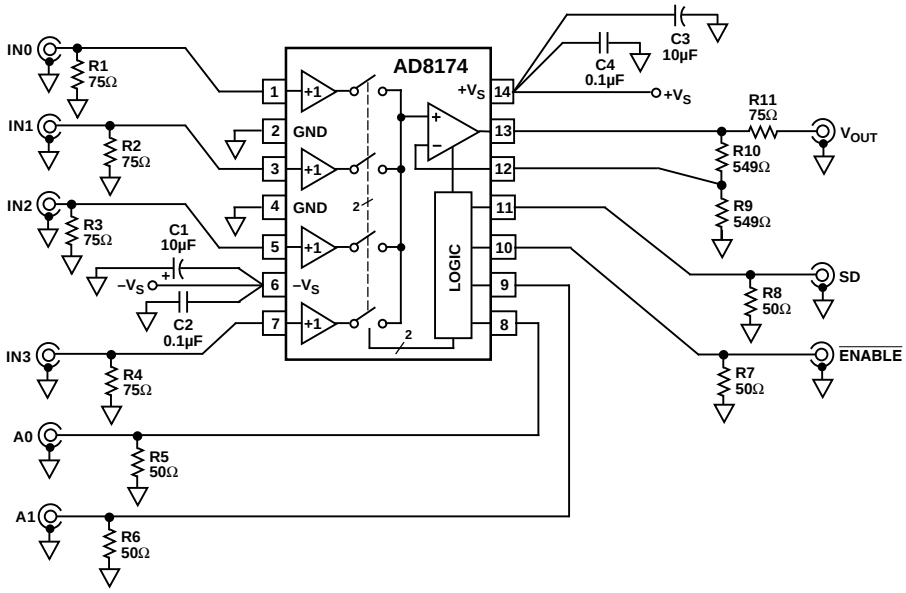


Figure 32. AD8174 Evaluation Board

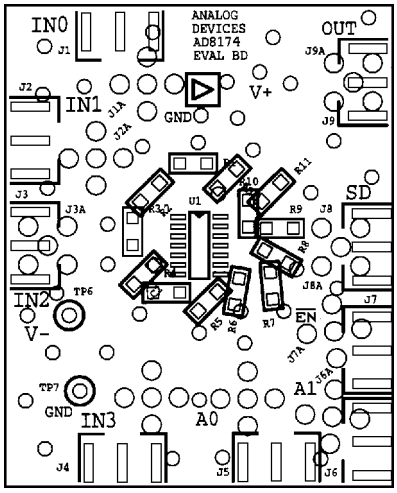


Figure 33. AD8174 Component Side Silkscreen

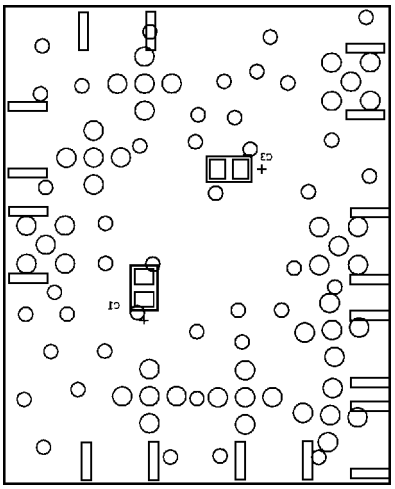


Figure 35. AD8174 Solder Side Silkscreen

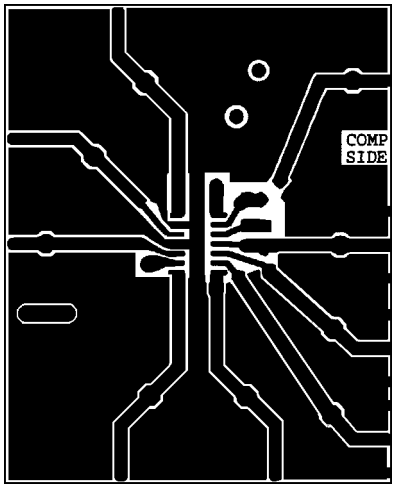


Figure 34. AD8174 Board Layout (Component Side)

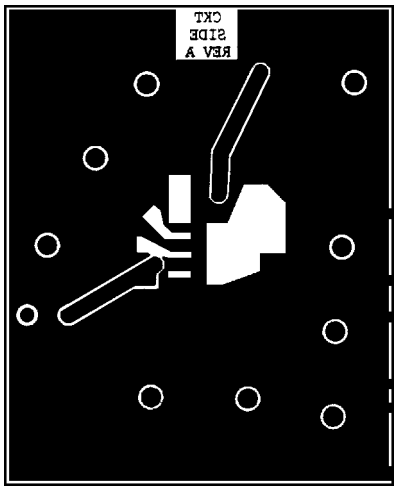


Figure 36. AD8174 Board Layout (Solder Side)

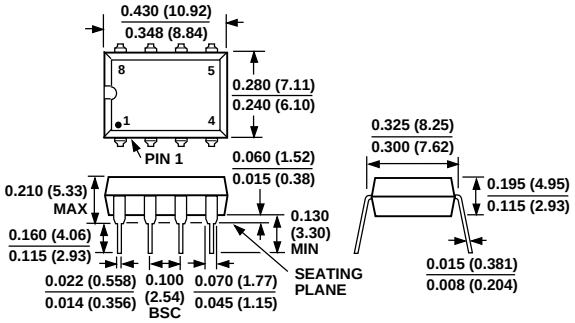
NOTES

1. AD8170R/AD8174R Evaluation Board inputs are configured with 50 Ω impedance striplines. This FR4 board type has the following stripline dimensions: 60-mil width, 12-mil gap between center conductor and outside ground plane "islands," and 62-mil board thickness.
2. Several types of SMA connectors can be mounted on this board: the side-mount type, which can be easily installed at the edges of the board; and the top-mount type, which is placed on top. When using the top-mount SMA connector, it is recommended that the stripline on the outside 1/8" of the board edge be removed with an X-Acto blade as this unused stripline acts as an open stub, which could degrade the small-signal frequency response of the mux.
3. Input termination resistor placement on the evaluation board is critical to reducing crosstalk. Each termination resistor is oriented so that ground return currents flow counterclockwise to a ground plane "island." Although the direction of this ground current flow is arbitrary, it is important that no two input or output termination resistors share a connection to the same ground "island."

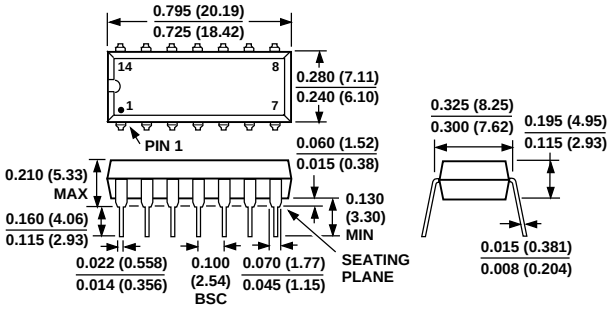
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

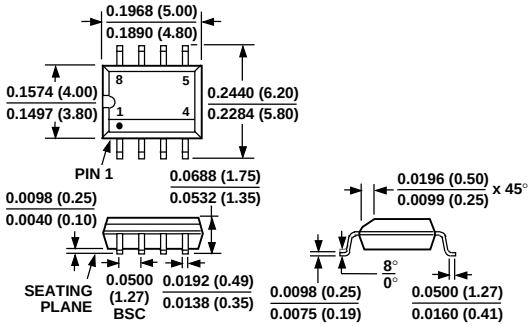
8-Lead Plastic DIP (N-8)



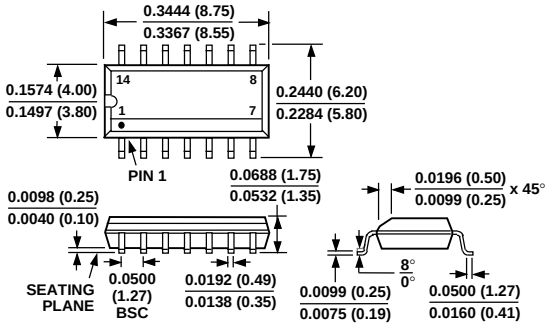
14-Lead Plastic DIP (N-14)



8-Lead Plastic SOIC (SO-8)



14-Lead SOIC (R-14)



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