



# ispMACH™ 4A CPLD Family

## High Performance E<sup>2</sup>CMOS® In-System Programmable Logic



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### FEATURES

- ◆ **High-performance, E<sup>2</sup>CMOS 3.3-V & 5-V CPLD families**
- ◆ **Flexible architecture for rapid logic designs**
  - Excellent First-Time-Fit™ and refit feature
  - SpeedLocking™ performance for guaranteed fixed timing
  - Central, input and output switch matrices for 100% routability and 100% pin-out retention
- ◆ **High speed**
  - 5.0ns t<sub>PD</sub> Commercial and 7.5ns t<sub>PD</sub> Industrial
  - 182MHz f<sub>CNT</sub>
- ◆ **32 to 512 macrocells; 32 to 768 registers**
- ◆ **44 to 388 pins in PLCC, PQFP, TQFP, BGA, fpBGA and caBGA packages**
- ◆ **Flexible architecture for a wide range of design styles**
  - D/T registers and latches
  - Synchronous or asynchronous mode
  - Dedicated input registers
  - Programmable polarity
  - Reset/ preset swapping
- ◆ **Advanced capabilities for easy system integration**
  - 3.3-V & 5-V JEDEC-compliant operations
  - JTAG (IEEE 1149.1) compliant for boundary scan testing
  - 3.3-V & 5-V JTAG in-system programming
  - PCI compliant (-5/-55/-6/-65/-7/-10/-12 speed grades)
  - Safe for mixed supply voltage system designs
  - Programmable pull-up or Bus-Friendly™ inputs and I/Os
  - Hot-socketing
  - Programmable security bit
  - Individual output slew rate control
- ◆ **Advanced E<sup>2</sup>CMOS process provides high-performance, cost-effective solutions**
- ◆ **Lead-free package options**

**Table 1. ispMACH 4A Device Features**

| <b>3.3 V Devices</b> |                |                |                |                 |                 |                 |                 |                 |
|----------------------|----------------|----------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| <b>Feature</b>       | <b>M4A3-32</b> | <b>M4A3-64</b> | <b>M4A3-96</b> | <b>M4A3-128</b> | <b>M4A3-192</b> | <b>M4A3-256</b> | <b>M4A3-384</b> | <b>M4A3-512</b> |
| Macrocells           | 32             | 64             | 96             | 128             | 192             | 256             | 384             | 512             |
| User I/O options     | 32             | 32/64          | 48             | 64              | 96              | 128/160/192     | 160/192         | 160/192/256     |
| $t_{PD}$ (ns)        | 5.0            | 5.5            | 5.5            | 5.5             | 6.0             | 5.5             | 6.5             | 7.5             |
| $f_{CNT}$ (MHz)      | 182            | 167            | 167            | 167             | 160             | 167             | 154             | 125             |
| $t_{COS}$ (ns)       | 4.0            | 4.0            | 4.0            | 4.0             | 4.5             | 4.0             | 4.5             | 5.5             |
| $t_{SS}$ (ns)        | 3.0            | 3.5            | 3.5            | 3.5             | 3.5             | 3.5             | 3.5             | 5.0             |
| Static Power (mA)    | 20             | 25/52          | 40             | 55              | 85              | 110/150         | 149/155         | 179             |
| JTAG Compliant       | Yes            | Yes            | Yes            | Yes             | Yes             | Yes             | Yes             | Yes             |
| PCI Compliant        | Yes            | Yes            | Yes            | Yes             | Yes             | Yes             | Yes             | Yes             |

| <b>5 V Devices</b> |                |                |                |                 |                 |                 |
|--------------------|----------------|----------------|----------------|-----------------|-----------------|-----------------|
| <b>Feature</b>     | <b>M4A5-32</b> | <b>M4A5-64</b> | <b>M4A5-96</b> | <b>M4A5-128</b> | <b>M4A5-192</b> | <b>M4A5-256</b> |
| Macrocells         | 32             | 64             | 96             | 128             | 192             | 256             |
| User I/O options   | 32             | 32             | 48             | 64              | 96              | 128             |
| $t_{PD}$ (ns)      | 5.0            | 5.5            | 5.5            | 5.5             | 6.0             | 6.5             |
| $f_{CNT}$ (MHz)    | 182            | 167            | 167            | 167             | 160             | 154             |
| $t_{COS}$ (ns)     | 4.0            | 4.0            | 4.0            | 4.0             | 4.5             | 5.0             |
| $t_{SS}$ (ns)      | 3.0            | 3.5            | 3.5            | 3.5             | 3.5             | 3.5             |
| Static Power (mA)  | 20             | 25             | 40             | 55              | 74              | 110             |
| JTAG Compliant     | Yes            | Yes            | Yes            | Yes             | Yes             | Yes             |
| PCI Compliant      | Yes            | Yes            | Yes            | Yes             | Yes             | Yes             |

## GENERAL DESCRIPTION

The ispMACH™ 4A family from Lattice offers an exceptionally flexible architecture and delivers a superior Complex Programmable Logic Device (CPLD) solution of easy-to-use silicon products and software tools. The overall benefits for users are a guaranteed and predictable CPLD solution, faster time-to-market, greater flexibility and lower cost. The ispMACH 4A devices offer densities ranging from 32 to 512 macrocells with 100% utilization and 100% pin-out retention. The ispMACH 4A families offer 5-V (M4A5-xxx) and 3.3-V (M4A3-xxx) operation.

ispMACH 4A products are 5-V or 3.3-V in-system programmable through the JTAG (IEEE Std. 1149.1) interface. JTAG boundary scan testing also allows product testability on automated test equipment for device connectivity.

All ispMACH 4A family members deliver First-Time-Fit and easy system integration with pin-out retention after any design change and refit. For both 3.3-V and 5-V operation, ispMACH 4A products can deliver guaranteed fixed timing as fast as 5.0 ns  $t_{PD}$  and 182 MHz  $f_{CNT}$  through the SpeedLocking feature when using up to 20 product terms per output (Table 2).

**Table 2. ispMACH 4A Speed Grades**

| Device                       | Speed Grade |     |    |     |      |      |      |     |
|------------------------------|-------------|-----|----|-----|------|------|------|-----|
|                              | -5          | -55 | -6 | -65 | -7   | -10  | -12  | -14 |
| M4A3-32<br>M4A5-32           | C           |     |    |     | C, I | C, I | I    |     |
| M4A3-64/32<br>M4A5-64/32     |             | C   |    |     | C, I | C, I | I    |     |
| M4A3-64/64                   |             | C   |    |     | C, I | C, I | I    |     |
| M4A3-96<br>M4A5-96           |             | C   |    |     | C, I | C, I | I    |     |
| M4A3-128<br>M4A5-128         |             | C   |    |     | C, I | C, I | I    |     |
| M4A3-192<br>M4A5-192         |             |     | C  |     | C, I | C, I | I    |     |
| M4A3-256/128<br>M4A5-256/128 |             | C   |    | C   | C, I | C, I | I    |     |
| M4A3-256/192<br>M4A3-256/160 |             |     |    |     | C    | C, I | I    |     |
| M4A3-384                     |             |     |    | C   |      | C, I | C, I | I   |
| M4A3-512                     |             |     |    |     | C    | C, I | C, I | I   |

**Note:**

1. C = Commercial, I = Industrial

The ispMACH 4A family offers 20 density-I/O combinations in Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), Plastic Leaded Chip Carrier (PLCC), Ball Grid Array (BGA), fine-pitch BGA (fpBGA), and chip-array BGA (caBGA) packages ranging from 44 to 388 pins (Table 3). It also offers I/O safety features for mixed-voltage designs so that the 3.3-V devices can accept 5-V inputs, and 5-V devices do not overdrive 3.3-V inputs. Additional features include Bus-Friendly inputs and I/Os, a programmable power-down mode for extra power savings and individual output slew rate control for the highest speed transition or for the lowest noise transition.

**Table 3. ispMACH 4A Package and I/O Options (Number of I/Os and dedicated inputs in Table)**

| 3.3 V Devices  |         |         |         |          |          |             |          |          |
|----------------|---------|---------|---------|----------|----------|-------------|----------|----------|
| Package        | M4A3-32 | M4A3-64 | M4A3-96 | M4A3-128 | M4A3-192 | M4A3-256    | M4A3-384 | M4A3-512 |
| 44-pin PLCC    | 32+2    | 32+2    |         |          |          |             |          |          |
| 44-pin TQFP    | 32+2    | 32+2    |         |          |          |             |          |          |
| 48-pin TQFP    | 32+2    | 32+2    |         |          |          |             |          |          |
| 100-pin TQFP   |         | 64+6    | 48+8    | 64+6     |          |             |          |          |
| 100-pin PQFP   |         |         |         | 64+6     |          |             |          |          |
| 100-ball caBGA |         |         |         | 64+6     |          |             |          |          |
| 144-pin TQFP   |         |         |         |          | 96+16    |             |          |          |
| 144-ball fpBGA |         |         |         |          | 96+16    |             |          |          |
| 208-pin PQFP   |         |         |         |          |          | 128+14, 160 | 160      | 160      |
| 256-ball fpBGA |         |         |         |          |          | 128+14, 192 | 192      | 192      |
| 256-ball BGA   |         |         |         |          |          | 128+14      | 192      |          |
| 388-ball fpBGA |         |         |         |          |          |             |          | 256      |

| 5 V Devices  |         |         |         |          |          |          |
|--------------|---------|---------|---------|----------|----------|----------|
| Package      | M4A5-32 | M4A5-64 | M4A5-96 | M4A5-128 | M4A5-192 | M4A5-256 |
| 44-pin PLCC  | 32+2    | 32+2    |         |          |          |          |
| 44-pin TQFP  | 32+2    | 32+2    |         |          |          |          |
| 48-pin TQFP  | 32+2    | 32+2    |         |          |          |          |
| 100-pin TQFP |         |         | 48+8    | 64+6     |          |          |
| 100-pin PQFP |         |         |         | 64+6     |          |          |
| 144-pin TQFP |         |         |         |          | 96+16    |          |
| 208-pin PQFP |         |         |         |          |          | 128+14   |

## FUNCTIONAL DESCRIPTION

The fundamental architecture of ispMACH 4A devices (Figure 1) consists of multiple, optimized PAL<sup>®</sup> blocks interconnected by a central switch matrix. The central switch matrix allows communication between PAL blocks and routes inputs to the PAL blocks. Together, the PAL blocks and central switch matrix allow the logic designer to create large designs in a single device instead of having to use multiple devices.

The key to being able to make effective use of these devices lies in the interconnect schemes. In the ispMACH 4A architecture, the macrocells are flexibly coupled to the product terms through the logic allocator, and the I/O pins are flexibly coupled to the macrocells due to the output switch matrix. In addition, more input routing options are provided by the input switch matrix. These resources provide the flexibility needed to fit designs efficiently.



Figure 1. ispMACH 4A Block Diagram and PAL Block Structure

### Notes:

1. 16 for ispMACH 4A devices with 1:1 macrocell-I/O cell ratio (see next page).
2. Block clocks do not go to I/O cells in M4A(3,5)-32/32.
3. M4A(3,5)-192, M4A(3,5)-256, M4A3-384, and M4A3-512 have dedicated clock pins which cannot be used as inputs and do not connect to the central switch matrix.

**Table 4. Architectural Summary of ispMACH 4A devices**

|                          | ispMACH 4A Devices |  |
|--------------------------|--------------------|--|
|                          |                    | M4A3-64/32, M4A5-64/32<br>M4A3-96/48, M4A5-96/48<br>M4A3-128/64, M4A5-128/64<br>M4A3-192/96, M4A5-192/96<br>M4A3-256/128, M4A5-256/128<br>M4A3-384<br>M4A3-512 |
| Macrocell-I/O Cell Ratio | 2:1                | 1:1  |
| Input Switch Matrix      | Yes                | Yes <sup>1</sup>   |
| Input Registers          | Yes                | No   |
| Central Switch Matrix    | Yes                | Yes  |
| Output Switch Matrix     | Yes                | Yes  |

The Macrocell-I/O cell ratio is defined as the number of macrocells versus the number of I/O cells internally in a PAL block (Table 4).

The central switch matrix takes all dedicated inputs and signals from the input switch matrices and routes them as needed to the PAL blocks. Feedback signals that return to the same PAL block still must go through the central switch matrix. This mechanism ensures that PAL blocks in ispMACH 4A devices communicate with each other with consistent, predictable delays.

The central switch matrix makes a ispMACH 4A device more advanced than simply several PAL devices on a single chip. It allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into PAL blocks through the central switch matrix so that the designer does not have to be concerned with the internal architecture of the device.

Each PAL block consists of:

- ◆ Product-term array
- ◆ Logic allocator
- ◆ Macrocells
- ◆ Output switch matrix
- ◆ I/O cells
- ◆ Input switch matrix
- ◆ Clock generator

**Notes:**

1. M4A3-64/64 internal switch matrix functionality embedded in central switch matrix.

## Product-Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the central switch matrix (Table 5), and are provided in both true and complement forms for efficient logic implementation.

**Table 5. PAL Block Inputs**

| Device                        | Number of Inputs to PAL Block |
|-------------------------------|-------------------------------|
| M4A3-32/32 and M4A5-32/32     | 33                            |
| M4A3-64/32 and M4A5-64/32     | 33                            |
| M4A3-64/64                    | 33                            |
| M4A3-96/48 and M4A5-96/48     | 33                            |
| M4A3-128/64 and M4A5-128/64   | 33                            |
| M4A3-192/96 and M4A5-192/96   | 34                            |
| M4A3-256/128 and M4A5-256/128 | 34                            |
| M4A3-256/160 and M4A3-256/192 | 36                            |
| M4A3-384                      | 36                            |
| M4A3-512                      | 36                            |

## Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in “product term clusters.” The availability and distribution of product term clusters are automatically considered by the software as it fits functions within a PAL block. The size of a product term cluster has been optimized to provide high utilization of product terms, making complex functions using many product terms possible. Yet when few product terms are used, there will be a minimal number of unused—or wasted—product terms left over. The product term clusters available to each macrocell within a PAL block are shown in Tables 6 and 7.

Each product term cluster is associated with a macrocell. The size of a cluster depends on the configuration of the associated macrocell. When the macrocell is used in synchronous mode (Figure 2a), the basic cluster has 4 product terms. When the associated macrocell is used in asynchronous mode (Figure 2b), the cluster has 2 product terms. Note that if the product term cluster is routed to a different macrocell, the allocator configuration is not determined by the mode of the macrocell actually being driven. The configuration is always set by the mode of the macrocell that the cluster will drive if not routed away, regardless of the actual routing.

In addition, there is an extra product term that can either join the basic cluster to give an extended cluster, or drive the second input of an exclusive-OR gate in the signal path. If included with the basic cluster, this provides for up to 20 product terms on a synchronous function that uses four extended 5-product-term clusters. A similar asynchronous function can have up to 18 product terms.

When the extra product term is used to extend the cluster, the value of the second XOR input can be programmed as a 0 or a 1, giving polarity control. The possible configurations of the logic allocator are shown in Figures 3 and 4.

**Table 6. Logic Allocator for All ispMACH 4A Devices (except M4A(3,5)-32/32)**

| Output Macrocell | Available Clusters  | Output Macrocell | Available Clusters  |
|------------------|---|------------------|---|
| M <sub>0</sub>   | C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub>                  | M <sub>8</sub>   | C <sub>7</sub> , C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub>    |
| M <sub>1</sub>   | C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub> | M <sub>9</sub>   | C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub>   |
| M <sub>2</sub>   | C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub> | M <sub>10</sub>  | C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub>  |
| M <sub>3</sub>   | C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> | M <sub>11</sub>  | C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub> |
| M <sub>4</sub>   | C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub> | M <sub>12</sub>  | C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub> |
| M <sub>5</sub>   | C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub> | M <sub>13</sub>  | C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub> |
| M <sub>6</sub>   | C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub> , C <sub>8</sub> | M <sub>14</sub>  | C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>                   |
| M <sub>7</sub>   | C <sub>6</sub> , C <sub>7</sub> , C <sub>8</sub> , C <sub>9</sub> | M <sub>15</sub>  | C <sub>14</sub> , C <sub>15</sub>                                     |

**Table 7. Logic Allocator for M4A(3,5)-32/32**

| Output Macrocell | Available Clusters  | Output Macrocell | Available Clusters  |
|------------------|---|------------------|---|
| M <sub>0</sub>   | C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub>                  | M <sub>8</sub>   | C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub>                     |
| M <sub>1</sub>   | C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub> | M <sub>9</sub>   | C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub>   |
| M <sub>2</sub>   | C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub> | M <sub>10</sub>  | C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub>  |
| M <sub>3</sub>   | C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> | M <sub>11</sub>  | C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub> |
| M <sub>4</sub>   | C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub> | M <sub>12</sub>  | C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub> |
| M <sub>5</sub>   | C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub> | M <sub>13</sub>  | C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub> |
| M <sub>6</sub>   | C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub>                  | M <sub>14</sub>  | C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>                   |
| M <sub>7</sub>   | C <sub>6</sub> , C <sub>7</sub>                                   | M <sub>15</sub>  | C <sub>14</sub> , C <sub>15</sub>                                     |



**a. Synchronous Mode**

17466G-005



**b. Asynchronous Mode**

17466G-006

**Figure 2. Logic Allocator: Configuration of Cluster “n” Set by Mode of Macrocell “n”**





17466G-007

**Figure 3. Logic Allocator Configurations: Synchronous Mode**



17466G-008

**Figure 4. Logic Allocator Configurations: Asynchronous Mode**

Note that the configuration of the logic allocator has absolutely no impact on the speed of the signal. All configurations have the same delay. This means that designers do not have to decide between optimizing resources or speed; both can be optimized.

If not used in the cluster, the extra product term can act in conjunction with the basic cluster to provide XOR logic for such functions as data comparison, or it can work with the D-,T-type flip-flop to provide for J-K, and S-R register operation. In addition, if the basic cluster is routed to another macrocell, the extra product term is still available for logic. In this case, the first XOR input will be a logic 0. This circuit has the flexibility to route product terms elsewhere without giving up the use of the macrocell.

Product term clusters do not “wrap” around a PAL block. This means that the macrocells at the ends of the block have fewer product terms available.

## Macrocell

The macrocell consists of a storage element, routing resources, a clock multiplexer, and initialization control. The macrocell has two fundamental modes: synchronous and asynchronous (Figure 5). The mode chosen only affects clocking and initialization in the macrocell.



**a. Synchronous mode**



**b. Asynchronous mode**

17466G-010

**Figure 5. Macrocell**

In either mode, a combinatorial path can be used. For combinatorial logic, the synchronous mode will generally be used, since it provides more product terms in the allocator.

The flip-flop can be configured as a D-type or T-type latch. J-K or S-R registers can be synthesized. The primary flip-flop configurations are shown in Figure 6, although others are possible. Flip-flop functionality is defined in Table 8. Note that a J-K latch is inadvisable as it will cause oscillation if both J and K inputs are HIGH.



a. D-type with XOR



b. D-type with programmable D polarity



c. Latch with XOR



d. Latch with programmable D polarity



e. T-type with programmable T polarity



f. Combinatorial with XOR



g. Combinatorial with programmable polarity

Figure 6. Primary Macrocell Configurations

17466G-011

**Table 8. Register/Latch Operation**

| Configuration   | Input(s) | CLK/LE <sup>1</sup> | Q+        |
|-----------------|----------|---------------------|-----------|
| D-type Register | D=X      | 0, 1, ↓ (↑)         | Q         |
|                 | D=0      | ↑ (↓)               | 0         |
|                 | D=1      | ↑ (↓)               | 1         |
| T-type Register | T=X      | 0, 1, ↓ (↑)         | Q         |
|                 | T=0      | ↑ (↓)               | Q         |
|                 | T=1      | ↑ (↓)               | $\bar{Q}$ |
| D-type Latch    | D=X      | 1 (0)               | Q         |
|                 | D=0      | 0 (1)               | 0         |
|                 | D=1      | 0 (1)               | 1         |

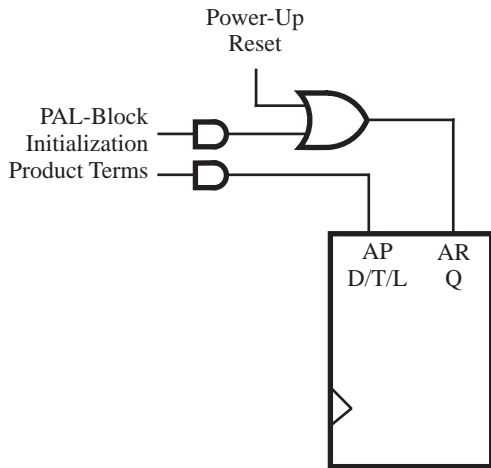
**Note:**

1. Polarity of CLK/LE can be programmed

Although the macrocell shows only one input to the register, the XOR gate in the logic allocator allows the D-, T-type register to emulate J-K, and S-R behavior. In this case, the available product terms are divided between J and K (or S and R). When configured as J-K, S-R, or T-type, the extra product term must be used on the XOR gate input for flip-flop emulation. In any register type, the polarity of the inputs can be programmed.

The clock input to the flip-flop can select any of the four PAL block clocks in synchronous mode, with the additional choice of either polarity of an individual product term clock in the asynchronous mode.

The initialization circuit depends on the mode. In synchronous mode (Figure 7), asynchronous reset and preset are provided, each driven by a product term common to the entire PAL block.



a. Power-up reset

17466G-012



b. Power-up preset

17466G-013

**Figure 7. Synchronous Mode Initialization Configurations**

A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility. In asynchronous mode (Figure 8), a single individual product term is provided for initialization. It can be selected to control reset or preset.



17466G-014

17466G-015

**Figure 8. Asynchronous Mode Initialization Configurations**

Note that the reset/preset swapping selection feature effects power-up reset as well. The initialization functionality of the flip-flops is illustrated in Table 9. The macrocell sends its data to the output switch matrix and the input switch matrix. The output switch matrix can route this data to an output if so desired. The input switch matrix can send the signal back to the central switch matrix as feedback.

**Table 9. Asynchronous Reset/Preset Operation**

| AR | AP | CLK/LE <sup>1</sup> | Q+          |
|----|----|---------------------|-------------|
| 0  | 0  | X                   | See Table 8 |
| 0  | 1  | X                   | 1           |
| 1  | 0  | X                   | 0           |
| 1  | 1  | X                   | 0           |

**Note:**

- Transparent latch is unaffected by AR, AP

## Output Switch Matrix

The output switch matrix allows macrocells to be connected to any of several I/O cells within a PAL block. This provides high flexibility in determining pinout and allows design changes to occur without effecting pinout.

In ispMACH 4A devices with 2:1 Macrocell-I/O cell ratio, each PAL block has twice as many macrocells as I/O cells. The ispMACH 4A output switch matrix allows for half of the macrocells to drive I/O cells within a PAL block, in combinations according to Figure 9. Each I/O cell can choose from eight macrocells; each macrocell has a choice of four I/O cells. The ispMACH 4A devices with 1:1 Macrocell-I/O cell ratio allow each macrocell to drive one of eight I/O cells (Figure 9).



Figure 9. ispMACH 4A Output Switch Matrix

Table 10. Output Switch Matrix Combinations for ispMACH 4A Devices with 2:1 Macrocell-I/O Cell Ratio

| Macrocell | Routeable to I/O Cells |
|-----------|------------------------|
| M0, M1    | I/O0, I/O5, I/O6, I/O7 |
| M2, M3    | I/O0, I/O1, I/O6, I/O7 |
| M4, M5    | I/O0, I/O1, I/O2, I/O7 |
| M6, M7    | I/O0, I/O1, I/O2, I/O3 |
| M8, M9    | I/O1, I/O2, I/O3, I/O4 |
| M10, M11  | I/O2, I/O3, I/O4, I/O5 |

**Table 10. Output Switch Matrix Combinations for ispMACH 4A Devices with 2:1 Macrocell-I/O Cell Ratio**

| Macrocell | Routable to I/O Cells  |
|-----------|------------------------|
| M12, M13  | I/03, I/04, I/05, I/06 |
| M14, M15  | I/04, I/05, I/06, I/07 |

| I/O Cell | Available Macrocells                 |
|----------|--------------------------------------|
| I/00     | M0, M1, M2, M3, M4, M5, M6, M7       |
| I/01     | M2, M3, M4, M5, M6, M7, M8, M9       |
| I/02     | M4, M5, M6, M7, M8, M9, M10, M11     |
| I/03     | M6, M7, M8, M9, M10, M11, M12, M13   |
| I/04     | M8, M9, M10, M11, M12, M13, M14, M15 |
| I/05     | M0, M1, M10, M11, M12, M13, M14, M15 |
| I/06     | M0, M1, M2, M3, M12, M13, M14, M15   |
| I/07     | M0, M1, M2, M3, M4, M5, M14, M15     |

**Table 11. Output Switch Matrix Combinations for M4A3-256/160 and M4A3-256/192**

| Macrocell | Routable to I/O Cells |      |       |       |       |       |       |       |
|-----------|-----------------------|------|-------|-------|-------|-------|-------|-------|
| M0        | I/00                  | I/01 | I/02  | I/03  | I/04  | I/05  | I/06  | I/07  |
| M1        | I/00                  | I/01 | I/02  | I/03  | I/04  | I/05  | I/06  | I/07  |
| M2        | I/00                  | I/01 | I/02  | I/03  | I/04  | I/05  | I/06  | I/07  |
| M3        | I/00                  | I/01 | I/02  | I/03  | I/04  | I/05  | I/06  | I/07  |
| M4        | I/00                  | I/01 | I/02  | I/03  | I/04  | I/05  | I/06  | I/07  |
| M5        | I/00                  | I/01 | I/02  | I/03  | I/04  | I/05  | I/06  | I/07  |
| M6        | I/00                  | I/01 | I/02  | I/03  | I/04  | I/05  | I/06  | I/07  |
| M7        | I/00                  | I/01 | I/02  | I/03  | I/04  | I/05  | I/06  | I/07  |
| M8        | I/08                  | I/09 | I/010 | I/011 | I/012 | I/013 | I/014 | I/015 |
| M9        | I/08                  | I/09 | I/010 | I/011 | I/012 | I/013 | I/014 | I/015 |
| M10       | I/08                  | I/09 | I/010 | I/011 | I/012 | I/013 | I/014 | I/015 |
| M11       | I/08                  | I/09 | I/010 | I/011 | I/012 | I/013 | I/014 | I/015 |
| M12       | I/08                  | I/09 | I/010 | I/011 | I/012 | I/013 | I/014 | I/015 |
| M13       | I/08                  | I/09 | I/010 | I/011 | I/012 | I/013 | I/014 | I/015 |
| M14       | I/08                  | I/09 | I/010 | I/011 | I/012 | I/013 | I/014 | I/015 |
| M15       | I/08                  | I/09 | I/010 | I/011 | I/012 | I/013 | I/014 | I/015 |

| I/O Cell | Available Macrocells |    |    |    |    |    |    |    |
|----------|----------------------|----|----|----|----|----|----|----|
| I/00     | M0                   | M1 | M2 | M3 | M4 | M5 | M6 | M7 |
| I/01     | M0                   | M1 | M2 | M3 | M4 | M5 | M6 | M7 |
| I/02     | M0                   | M1 | M2 | M3 | M4 | M5 | M6 | M7 |
| I/03     | M0                   | M1 | M2 | M3 | M4 | M5 | M6 | M7 |
| I/04     | M0                   | M1 | M2 | M3 | M4 | M5 | M6 | M7 |
| I/05     | M0                   | M1 | M2 | M3 | M4 | M5 | M6 | M7 |
| I/06     | M0                   | M1 | M2 | M3 | M4 | M5 | M6 | M7 |
| I/07     | M0                   | M1 | M2 | M3 | M4 | M5 | M6 | M7 |

**Table 11. Output Switch Matrix Combinations for M4A3-256/160 and M4A3-256/192**

| Macrocell | Routable to I/O Cells |    |     |     |     |     |     |     |
|-----------|-----------------------|----|-----|-----|-----|-----|-----|-----|
| I/O8      | M8                    | M9 | M10 | M11 | M12 | M13 | M14 | M15 |
| I/O9      | M8                    | M9 | M10 | M11 | M12 | M13 | M14 | M15 |
| I/O10     | M8                    | M9 | M10 | M11 | M12 | M13 | M14 | M15 |
| I/O11     | M8                    | M9 | M10 | M11 | M12 | M13 | M14 | M15 |
| I/O12     | M8                    | M9 | M10 | M11 | M12 | M13 | M14 | M15 |
| I/O13     | M8                    | M9 | M10 | M11 | M12 | M13 | M14 | M15 |
| I/O14     | M8                    | M9 | M10 | M11 | M12 | M13 | M14 | M15 |
| I/O15     | M8                    | M9 | M10 | M11 | M12 | M13 | M14 | M15 |

**Table 12. Output Switch Matrix Combinations for M4A(3,5)-32/32**

| Macrocell                            | Routable to I/O Cells                                |
|--------------------------------------|--|
| M0, M1, M2, M3, M4, M5, M6, M7       | I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7       |
| M8, M9, M10, M11, M12, M13, M14, M15 | I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15 |

| I/O Cell   | Available Macrocells                 |
|--|--------------------------------------|
| I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7       | M0, M1, M2, M3, M4, M5, M6, M7       |
| I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15 | M8, M9, M10, M11, M12, M13, M14, M15 |

**Table 13. Output Switch Matrix Combinations for M4A3-64/64**

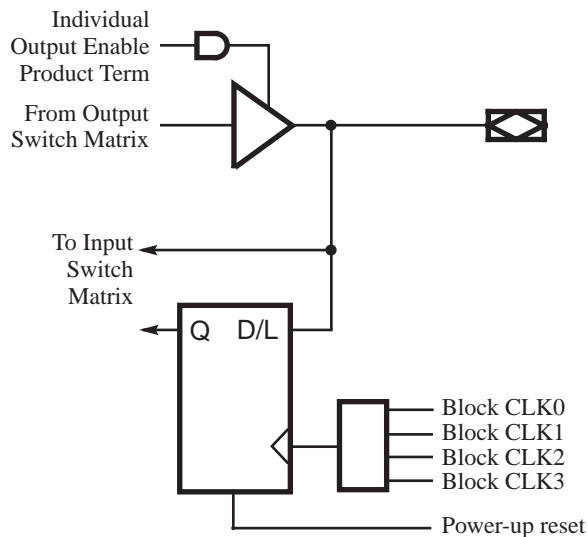
| Macrocell | Routable to I/O Cells                                |
|-----------|--|
| M0, M1    | I/O0, I/O1, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15 |
| M2, M3    | I/O0, I/O1, I/O2, I/O3, I/O12, I/O13, I/O14, I/O15   |
| M4, M5    | I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O14, I/O15     |
| M6, M7    | I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7       |
| M8, M9    | I/O2, I/O3, I/O4, I/O5, I/O6, I/O7, I/O8, I/O9       |
| M10, M11  | I/O4, I/O5, I/O6, I/O7, I/O8, I/O9, I/O10, I/O11     |
| M12, M13  | I/O6, I/O7, I/O8, I/O9, I/O10, I/O11, I/O12, I/O13   |
| M14, M15  | I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15 |

| I/O Cell     | Available Macrocells                 |
|--------------|--------------------------------------|
| I/O0, I/O1   | M0, M1, M2, M3, M4, M5, M6, M7       |
| I/O2, I/O3   | M2, M3, M4, M5, M6, M7, M8, M9       |
| I/O4, I/O5   | M4, M5, M6, M7, M8, M9, M10, M11     |
| I/O6, I/O7   | M6, M7, M8, M9, M10, M11, M12, M13   |
| I/O8, I/O9   | M8, M9, M10, M11, M12, M13, M14, M15 |
| I/O10, I/O11 | M0, M1, M10, M11, M12, M13, M14, M15 |
| I/O12, I/O13 | M0, M1, M2, M3, M12, M13, M14, M15   |
| I/O14, I/O15 | M0, M1, M2, M3, M4, M5, M14, M15     |



## I/O Cell

The I/O cell (Figures 10 and 11) simply consists of a programmable output enable, a feedback path, and flip-flop (except ispMACH 4A devices with 1:1 macrocell-I/O cell ratio). An individual output enable product term is provided for each I/O cell. The feedback signal drives the input switch matrix.



17466G-017

**Figure 10. I/O Cell for ispMACH 4A Devices with 2:1 Macrocell-I/O Cell Ratio**



17466G-018

**Figure 11. I/O Cell for ispMACH 4A Devices with 1:1 Macrocell-I/O Cell Ratio**

The I/O cell (Figure 10) contains a flip-flop, which provides the capability for storing the input in a D-type register or latch. The clock can be any of the PAL block clocks. Both the direct and registered versions of the input are sent to the input switch matrix. This allows for such functions as “time-domain-multiplexed” data comparison, where the first data value is stored, and then the second data value is put on the I/O pin and compared with the previous stored value.

Note that the flip-flop used in the ispMACH 4A I/O cell is independent of the flip-flops in the macrocells. It powers up to a logic low.

### **Zero-Hold-Time Input Register**

The ispMACH 4A devices have a zero-hold-time (ZHT) fuse which controls the time delay associated with loading data into all I/O cell registers and latches. When programmed, the ZHT fuse increases the data path setup delays to input storage elements, matching equivalent delays in the clock path. When the fuse is erased, the setup time to the input storage element is minimized. This feature facilitates doing worst-case designs for which data is loaded from sources which have low (or zero) minimum output propagation delays from clock edges.

## Input Switch Matrix

The input switch matrix (Figures 12 and 13) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.



17466G-002

Figure 12. ispMACH 4A with 2:1 Macrocell-I/O Cell Ratio - Input Switch Matrix



17466G-003

Figure 13. ispMACH 4A with 1:1 Macrocell-I/O Cell Ratio - Input Switch Matrix

## PAL Block Clock Generation

Each ispMACH 4A device has four clock pins that can also be used as inputs. These pins drive a clock generator in each PAL block (Figure 14). The clock generator provides four clock signals that can be used anywhere in the PAL block. These four PAL block clock signals can consist of a large number of combinations of the true and complement edges of the global clock signals. Table 14 lists the possible combinations.



17466G-004

**Figure 14. PAL Block Clock Generator**<sup>1</sup>

1. *M4A(3,5)-32/32 and M4A(3,5)-64/32 have only two clock pins, GCLK0 and GCLK1. GCLK2 is tied to GCLK0, and GCLK3 is tied to GCLK1.*

**Table 14. PAL Block Clock Combinations**<sup>1</sup>

| Block CLK0         | Block CLK1         | Block CLK2                                | Block CLK3                                |
|--------------------|--------------------|---|---|
| GCLK0              | GCLK1              | X   | X   |
| $\overline{GCLK1}$ | GCLK1              | X   | X   |
| GCLK0              | $\overline{GCLK0}$ | X   | X   |
| $\overline{GCLK1}$ | $\overline{GCLK0}$ | X   | X   |
| X                  | X                  | GCLK2 (GCLK0)                             | GCLK3 (GCLK1)                             |
| X                  | X                  | $\overline{GCLK3}$ ( $\overline{GCLK1}$ ) | GCLK3 (GCLK1)                             |
| X                  | X                  | GCLK2 (GCLK0)                             | $\overline{GCLK2}$ ( $\overline{GCLK0}$ ) |
| X                  | X                  | $\overline{GCLK3}$ ( $\overline{GCLK1}$ ) | $\overline{GCLK2}$ ( $\overline{GCLK0}$ ) |

**Note:**

1. *Values in parentheses are for the M4A(3,5)-32/32 and M4A(3,5)-64/32.*

This feature provides high flexibility for partitioning state machines and dual-phase clocks. It also allows latches to be driven with either polarity of latch enable, and in a master-slave configuration.

## ispMACH 4A TIMING MODEL

The primary focus of the ispMACH 4A timing model is to accurately represent the timing in a ispMACH 4A device, and at the same time, be easy to understand. This model accurately describes all combinatorial and registered paths through the device, making a distinction between internal feedback and external feedback. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. The input register specifications are also reported as internal feedback. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback.

The parameter,  $t_{BUF}$ , is defined as the time it takes to go from feedback through the output buffer to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the parameter designator is followed by an “i”. By adding  $t_{BUF}$  to this internal parameter, the external parameter is derived. For example,  $t_{PD} = t_{PDi} + t_{BUF}$ . A diagram representing the modularized ispMACH 4A timing model is shown in Figure 15. Refer to the application note entitled *MACH 4 Timing and High Speed Design* for a more detailed discussion about the timing parameters.



17466G-025

Figure 15. ispMACH 4A Timing Model

## SPEEDLOCKING FOR GUARANTEED FIXED TIMING

The ispMACH 4A architecture allows allocation of up to 20 product terms to an individual macrocell with the assistance of an XOR gate without incurring additional timing delays.

The design of the switch matrix and PAL blocks guarantee a fixed pin-to-pin delay that is independent of the logic required by the design. Other competitive CPLDs incur serious timing delays as product terms expand beyond their typical 4 or 5 product term limits. Speed *and* SpeedLocking combine to give designs easy access to the performance required in today's designs.

## IEEE 1149.1-COMPLIANT BOUNDARY SCAN TESTABILITY

All ispMACH 4A devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

## IEEE 1149.1-COMPLIANT IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All ispMACH 4A devices provide In-System Programming (ISP) capability through their Boundary ScanTest Access Ports. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

ispMACH 4A devices can be programmed across the commercial temperature and voltage range. The PC-based ispVM™ software facilitates in-system programming of ispMACH 4A devices. ispVM takes the JEDEC file output produced by the design implementation software, along with information about the JTAG chain, and creates a set of vectors that are used to drive the JTAG chain. ispVM software can use these vectors to drive a JTAG chain via the parallel port of a PC. Alternatively, ispVM software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispMACH 4A devices during the testing of a circuit board.

## PCI COMPLIANT

ispMACH 4A devices in the -5/-55/-6/-65/-7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above  $V_{CC}$  because of their 5-V input tolerant feature.

## SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS

Both the 3.3-V and 5-V  $V_{CC}$  ispMACH 4A devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V device will accept inputs up to 5.5 V. Both the 5-V and 3.3-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

## PULL UP OR BUS-FRIENDLY INPUTS AND I/Os

All ispMACH 4A devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

All ispMACH 4A devices have a programmable bit that configures all inputs and I/Os with either pull-up or Bus-Friendly characteristics. If the device is configured in pull-up mode, all inputs and I/O pins are

weakly pulled up. For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

## **POWER MANAGEMENT**

Each individual PAL block in ispMACH 4A devices features a programmable low-power mode, which results in power savings of up to 50%. The signal speed paths in the low-power PAL block will be slower than those in the non-low-power PAL block. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in the low-power mode.

## **PROGRAMMABLE SLEW RATE**

Each ispMACH 4A device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

## **POWER-UP RESET/SET**

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the  $V_{CC}$  rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

## **SECURITY BIT**

A programmable security bit is provided on the ispMACH 4A devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

## **HOT SOCKETING**

ispMACH 4A devices are well-suited for those applications that require hot socketing capability. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down MACH devices be minimal on active signals.



**Figure 16. PAL Block for ispMACH 4A with 2:1 Macrocell - I/O Cell Ratio**



17466H-41

Figure 17. PAL Block for ispMACH 4A Devices with 1:1 Macrocell-I/O Cell Ratio (except M4A (3,5)-32/32)





Figure 18. PAL Block for M4A (3,5)-32/32

17466H-042

## BLOCK DIAGRAM – M4A(3,5)-32/32



## BLOCK DIAGRAM – M4A(3,5)-64/32



17466H-020

## BLOCK DIAGRAM – M4A3-64/64



17466H-020A

# BLOCK DIAGRAM – M4A(3,5)-96/48



17466G-021

# BLOCK DIAGRAM – M4A(3,5)-128/64



17466H-022

# BLOCK DIAGRAM – M4A(3,5)-192/96



17466G-067

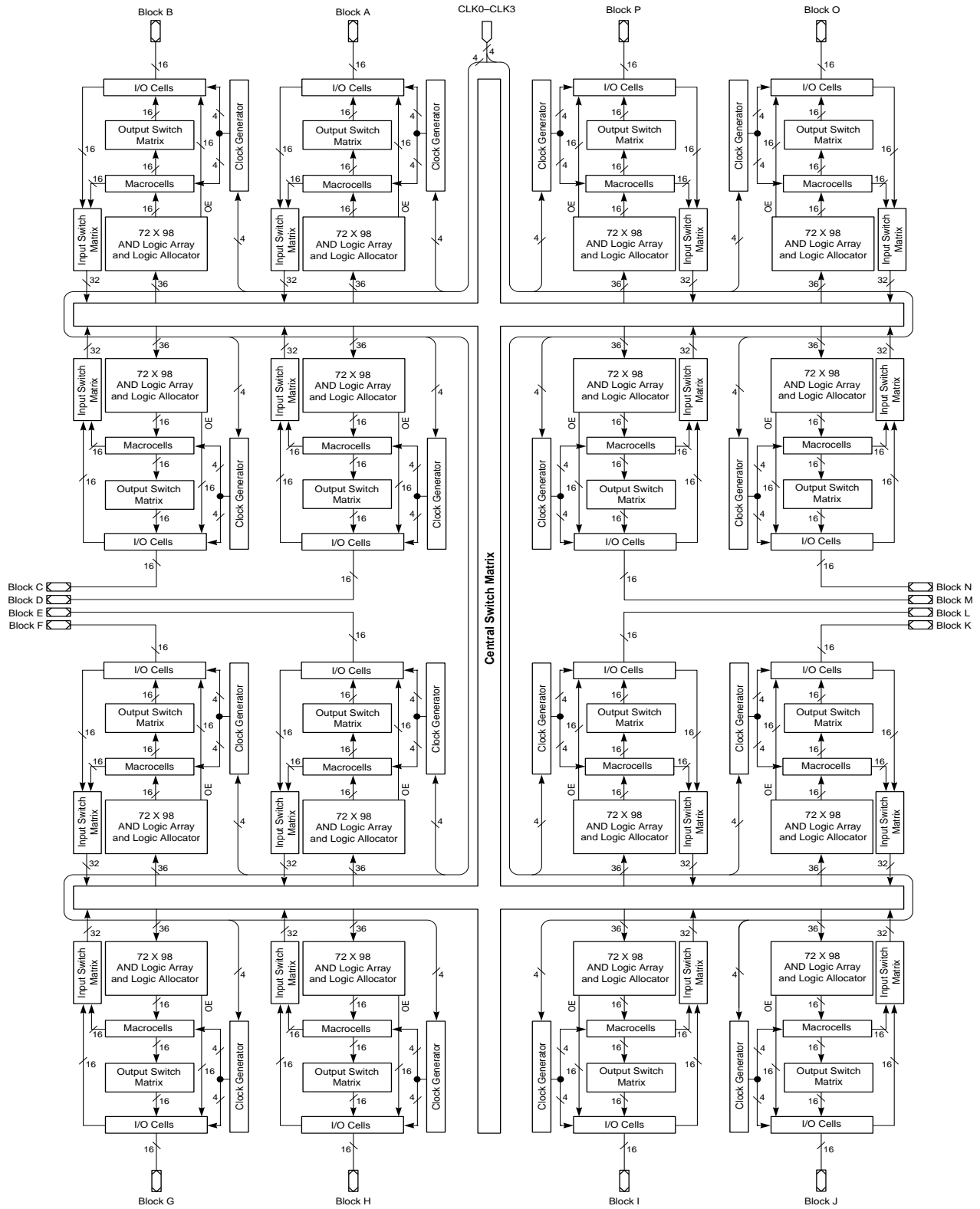
# BLOCK DIAGRAM – M4A(3,5)-256/128



17466G-024



# BLOCK DIAGRAM – M4A3-256/160, M4A3-256/192



17466G-050

# BLOCK DIAGRAM – M4A3-384/160, M4A3-384/192



# BLOCK DIAGRAM - M4A3-512/160, M4A3-512/192, M4A3-512/256



17466G-068

## ABSOLUTE MAXIMUM RATINGS

### M4A5

|  |                            |
|--|----------------------------|
| Storage Temperature  | -65°C to +150°C            |
| Ambient Temperature<br>with Power Applied                            | -55°C to +100°C            |
| Device Junction Temperature  | +130°C                     |
| Supply Voltage<br>with Respect to Ground                             | -0.5 V to +7.0 V           |
| DC Input Voltage   | -0.5 V to $V_{CC} + 0.5$ V |
| Static Discharge Voltage   | 2000 V                     |
| Latchup Current ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ ) | 200 mA                     |

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

## OPERATING RANGES

### Commercial (C) Devices

|  |                    |
|--|--------------------|
| Ambient Temperature ( $T_A$ )<br>Operating in Free Air | 0°C to +70°C       |
| Supply Voltage ( $V_{CC}$ )<br>with Respect to Ground  | +4.75 V to +5.25 V |

### Industrial (I) Devices

|  |                   |
|--|-------------------|
| Ambient Temperature ( $T_A$ )<br>Operating in Free Air | -40°C to +85°C    |
| Supply Voltage ( $V_{CC}$ )<br>with Respect to Ground  | +4.50 V to +5.5 V |

Operating ranges define those limits between which the functionality of the device is guaranteed.

## 5-V DC CHARACTERISTICS OVER OPERATING RANGES

| Parameter Symbol | Parameter Description                 | Test Conditions  | Min | Typ | Max  | Unit    |
|------------------|---------------------------------------|--|-----|-----|------|---------|
| $V_{OH}$         | Output HIGH Voltage                   | $I_{OH} = -3.2$ mA, $V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$          | 2.4 |     |      | V       |
|                  |                                       | $I_{OH} = -100$ $\mu$ A, $V_{CC} = \text{Max}$ , $V_{IN} = V_{IH}$ or $V_{IL}$     |     | 3.3 | 3.6  | V       |
| $V_{OL}$         | Output LOW Voltage                    | $I_{OL} = 24$ mA, $V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 1)   |     |     | 0.5  | V       |
| $V_{IH}$         | Input HIGH Voltage                    | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)                      | 2.0 |     |      | V       |
| $V_{IL}$         | Input LOW Voltage                     | Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)                       |     |     | 0.8  | V       |
| $I_{IH}$         | Input HIGH Leakage Current            | $V_{IN} = 5.25$ V, $V_{CC} = \text{Max}$ (Note 3)                                  |     |     | 10   | $\mu$ A |
| $I_{IL}$         | Input LOW Leakage Current             | $V_{IN} = 0$ V, $V_{CC} = \text{Max}$ (Note 3)                                     |     |     | -10  | $\mu$ A |
| $I_{OZH}$        | Off-State Output Leakage Current HIGH | $V_{OUT} = 5.25$ V, $V_{CC} = \text{Max}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 3) |     |     | 10   | $\mu$ A |
| $I_{OZL}$        | Off-State Output Leakage Current LOW  | $V_{OUT} = 0$ V, $V_{CC} = \text{Max}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 3)    |     |     | -10  | $\mu$ A |
| $I_{SC}$         | Output Short-Circuit Current          | $V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 4)                                  | -30 |     | -160 | mA      |

### Notes:

- Total  $I_{OL}$  for one PAL block should not exceed 64 mA.
- These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
- Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.

## ABSOLUTE MAXIMUM RATINGS

### M4A3

|  |                  |
|--|------------------|
| Storage Temperature  | -65°C to +150°C  |
| Ambient Temperature with Power Applied                               | -55°C to +100°C  |
| Device Junction Temperature  | +130°C           |
| Supply Voltage with Respect to Ground                                | -0.5 V to +4.5 V |
| DC Input Voltage   | -0.5 V to 6.0 V  |
| Static Discharge Voltage   | 2000 V           |
| Latchup Current ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ ) | 200 mA           |

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

## OPERATING RANGES

### Commercial (C) Devices

|  |                       |                  |
|--|-----------------------|------------------|
| Ambient Temperature ( $T_A$ )                      | Operating in Free Air | 0°C to +70°C     |
| Supply Voltage ( $V_{CC}$ ) with Respect to Ground |                       | +3.0 V to +3.6 V |

### Industrial (I) Devices

|  |                       |                  |
|--|-----------------------|------------------|
| Ambient Temperature ( $T_A$ )                      | Operating in Free Air | -40°C to +85°C   |
| Supply Voltage ( $V_{CC}$ ) with Respect to Ground |                       | +3.0 V to +3.6 V |

Operating ranges define those limits between which the functionality of the device is guaranteed.

## 3.3-V DC CHARACTERISTICS OVER OPERATING RANGES

| Parameter Symbol | Parameter Description                 | Test Conditions   | Min                         | Typ            | Max  | Unit          |
|------------------|---------------------------------------|---|-----------------------------|----------------|------|---------------|
| $V_{OH}$         | Output HIGH Voltage                   | $V_{CC} = \text{Min}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$                                      | $I_{OH} = -100 \mu\text{A}$ | $V_{CC} - 0.2$ |      | V             |
|                  |                                       |   | $I_{OH} = -3.2 \text{ mA}$  | 2.4            |      | V             |
| $V_{OL}$         | Output LOW Voltage                    | $V_{CC} = \text{Min}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$<br>(Note 1)                          | $I_{OL} = 100 \mu\text{A}$  |                | 0.2  | V             |
|                  |                                       |   | $I_{OL} = 24 \text{ mA}$    |                | 0.5  | V             |
| $V_{IH}$         | Input HIGH Voltage                    | Guaranteed Input Logical HIGH Voltage for all Inputs  | 2.0                         |                | 5.5  | V             |
| $V_{IL}$         | Input LOW Voltage                     | Guaranteed Input Logical LOW Voltage for all Inputs   | -0.3                        |                | 0.8  | V             |
| $I_{IH}$         | Input HIGH Leakage Current            | $V_{IN} = 3.6 \text{ V}$ , $V_{CC} = \text{Max}$ (Note 2)                                   |                             |                | 5    | $\mu\text{A}$ |
| $I_{IL}$         | Input LOW Leakage Current             | $V_{IN} = 0 \text{ V}$ , $V_{CC} = \text{Max}$ (Note 2)                                     |                             |                | -5   | $\mu\text{A}$ |
| $I_{OZH}$        | Off-State Output Leakage Current HIGH | $V_{OUT} = 3.6 \text{ V}$ , $V_{CC} = \text{Max}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2) |                             |                | 5    | $\mu\text{A}$ |
| $I_{OZL}$        | Off-State Output Leakage Current LOW  | $V_{OUT} = 0 \text{ V}$ , $V_{CC} = \text{Max}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)   |                             |                | -5   | $\mu\text{A}$ |
| $I_{SC}$         | Output Short-Circuit Current          | $V_{OUT} = 0.5 \text{ V}$ , $V_{CC} = \text{Max}$ (Note 3)                                  | -15                         |                | -160 | mA            |

#### Notes:

- Total  $I_{OL}$  for one PAL block should not exceed 64 mA.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
- Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

#### Notes:

- See "MACH Switching Test Circuit" document on the Literature Download page of the Lattice web site.
- This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.

## ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup>

|                               |   | -5  |     | -55 |     | -6  |     | -65 |     | -7  |      | -10 |      | -12 |      | -14  |      | Unit |
|-------------------------------|---|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|-----|------|-----|------|------|------|------|
|                               |   | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max  | Min | Max  | Min | Max  | Min  | Max  |      |
| <b>Combinatorial Delay:</b>   |   |     |     |     |     |     |     |     |     |     |      |     |      |     |      |      |      |      |
| $t_{PDi}$                     | Internal combinatorial propagation delay              |     | 3.5 |     | 4.0 |     | 4.3 |     | 4.5 |     | 5.0  |     | 7.0  |     | 9.0  |      | 11.0 | ns   |
| $t_{PD}$                      | Combinatorial propagation delay                       |     | 5.0 |     | 5.5 |     | 6.0 |     | 6.5 |     | 7.5  |     | 10.0 |     | 12.0 |      | 14.0 | ns   |
| <b>Registered Delays:</b>     |   |     |     |     |     |     |     |     |     |     |      |     |      |     |      |      |      |      |
| $t_{SS}$                      | Synchronous clock setup time, D-type register         | 3.0 |     | 3.5 |     | 3.5 |     | 3.5 |     | 5.0 |      | 5.5 |      | 7.0 |      | 10.0 |      | ns   |
| $t_{SST}$                     | Synchronous clock setup time, T-type register         | 4.0 |     | 4.0 |     | 4.0 |     | 4.0 |     | 6.0 |      | 6.5 |      | 8.0 |      | 11.0 |      | ns   |
| $t_{SA}$                      | Asynchronous clock setup time, D-type register        | 2.5 |     | 2.5 |     | 2.5 |     | 3.0 |     | 3.5 |      | 4.0 |      | 5.0 |      | 8.0  |      | ns   |
| $t_{SAT}$                     | Asynchronous clock setup time, T-type register        | 3.0 |     | 3.0 |     | 3.0 |     | 3.5 |     | 4.5 |      | 5.0 |      | 6.0 |      | 9.0  |      | ns   |
| $t_{HS}$                      | Synchronous clock hold time                           | 0.0 |     | 0.0 |     | 0.0 |     | 0.0 |     | 0.0 |      | 0.0 |      | 0.0 |      | 0.0  |      | ns   |
| $t_{HA}$                      | Asynchronous clock hold time                          | 2.5 |     | 2.5 |     | 2.5 |     | 3.0 |     | 3.5 |      | 4.0 |      | 5.0 |      | 8.0  |      | ns   |
| $t_{COSi}$                    | Synchronous clock to internal output                  |     | 2.5 |     | 2.5 |     | 2.8 |     | 3.0 |     | 3.0  |     | 3.0  |     | 3.5  |      | 3.5  | ns   |
| $t_{COS}$                     | Synchronous clock to output                           |     | 4.0 |     | 4.0 |     | 4.5 |     | 5.0 |     | 5.5  |     | 6.0  |     | 6.5  |      | 6.5  | ns   |
| $t_{COAi}$                    | Asynchronous clock to internal output                 |     | 5.0 |     | 5.0 |     | 5.0 |     | 5.0 |     | 6.0  |     | 8.0  |     | 10.0 |      | 12.0 | ns   |
| $t_{COA}$                     | Asynchronous clock to output                          |     | 6.5 |     | 6.5 |     | 6.8 |     | 7.0 |     | 8.5  |     | 11.0 |     | 13.0 |      | 15.0 | ns   |
| <b>Latched Delays:</b>        |   |     |     |     |     |     |     |     |     |     |      |     |      |     |      |      |      |      |
| $t_{SSL}$                     | Synchronous latch setup time                          | 4.0 |     | 4.0 |     | 4.0 |     | 4.5 |     | 6.0 |      | 7.0 |      | 8.0 |      | 10.0 |      | ns   |
| $t_{SAL}$                     | Asynchronous latch setup time                         | 3.0 |     | 3.0 |     | 3.5 |     | 3.5 |     | 4.0 |      | 4.0 |      | 5.0 |      | 8.0  |      | ns   |
| $t_{HSL}$                     | Synchronous latch hold time                           | 0.0 |     | 0.0 |     | 0.0 |     | 0.0 |     | 0.0 |      | 0.0 |      | 0.0 |      | 0.0  |      | ns   |
| $t_{HAL}$                     | Asynchronous latch hold time                          | 3.0 |     | 3.0 |     | 3.5 |     | 3.5 |     | 4.0 |      | 4.0 |      | 5.0 |      | 8.0  |      | ns   |
| $t_{PDLi}$                    | Transparent latch to internal output                  |     | 5.5 |     | 5.5 |     | 5.8 |     | 6.0 |     | 7.5  |     | 9.0  |     | 11.0 |      | 12.0 | ns   |
| $t_{PDL}$                     | Propagation delay through transparent latch to output |     | 7.0 |     | 7.0 |     | 7.5 |     | 8.0 |     | 10.0 |     | 12.0 |     | 14.0 |      | 15.0 | ns   |
| $t_{GOSi}$                    | Synchronous gate to internal output                   |     | 3.0 |     | 3.0 |     | 3.0 |     | 3.0 |     | 3.5  |     | 4.5  |     | 7.0  |      | 8.0  | ns   |
| $t_{GOS}$                     | Synchronous gate to output                            |     | 4.5 |     | 4.5 |     | 4.8 |     | 5.0 |     | 6.0  |     | 7.5  |     | 10.0 |      | 11.0 | ns   |
| $t_{GOAi}$                    | Asynchronous gate to internal output                  |     | 6.0 |     | 6.0 |     | 6.0 |     | 6.0 |     | 8.5  |     | 10.0 |     | 13.0 |      | 15.0 | ns   |
| $t_{GOA}$                     | Asynchronous gate to output                           |     | 7.5 |     | 7.5 |     | 7.8 |     | 8.0 |     | 11.0 |     | 13.0 |     | 16.0 |      | 18.0 | ns   |
| <b>Input Register Delays:</b> |   |     |     |     |     |     |     |     |     |     |      |     |      |     |      |      |      |      |
| $t_{SIRS}$                    | Input register setup time                             | 1.5 |     | 1.5 |     | 2.0 |     | 2.0 |     | 2.0 |      | 2.0 |      | 2.0 |      | 2.0  |      | ns   |
| $t_{HIRS}$                    | Input register hold time                              | 2.5 |     | 2.5 |     | 3.0 |     | 3.0 |     | 3.0 |      | 3.0 |      | 3.0 |      | 4.0  |      | ns   |
| $t_{ICOSi}$                   | Input register clock to internal feedback             |     | 3.0 |     | 3.0 |     | 3.0 |     | 3.0 |     | 3.5  |     | 4.5  |     | 6.0  |      | 6.0  | ns   |
| <b>Input Latch Delays:</b>    |   |     |     |     |     |     |     |     |     |     |      |     |      |     |      |      |      |      |
| $t_{SIL}$                     | Input latch setup time                                | 1.5 |     | 1.5 |     | 1.5 |     | 2.0 |     | 2.0 |      | 2.0 |      | 2.0 |      | 2.0  |      | ns   |
| $t_{HIL}$                     | Input latch hold time                                 | 2.5 |     | 2.5 |     | 2.5 |     | 3.0 |     | 3.0 |      | 3.0 |      | 3.0 |      | 4.0  |      | ns   |
| $t_{IGOSi}$                   | Input latch gate to internal feedback                 |     | 3.5 |     | 3.5 |     | 3.8 |     | 4.0 |     | 4.0  |     | 4.0  |     | 4.0  |      | 5.0  | ns   |
| $t_{PDILi}$                   | Transparent input latch to internal feedback          |     | 1.5 |     | 1.5 |     | 1.5 |     | 1.5 |     | 2.0  |     | 2.0  |     | 2.0  |      | 2.0  | ns   |

## ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup>

|   |  | -5  |     | -55 |     | -6  |      | -65 |      | -7   |      | -10  |      | -12  |      | -14  |      | Unit |
|---|--|-----|-----|-----|-----|-----|------|-----|------|------|------|------|------|------|------|------|------|------|
|   |  | Min | Max | Min | Max | Min | Max  | Min | Max  | Min  | Max  | Min  | Max  | Min  | Max  | Min  | Max  |      |
| <b>Input Register Delays with ZHT Option:</b> |  |     |     |     |     |     |      |     |      |      |      |      |      |      |      |      |      |      |
| $t_{SIRZ}$                                    | Input register setup time - ZHT  | 6.0 |     | 6.0 |     | 6.0 |      | 6.0 |      | 6.0  |      | 6.0  |      | 6.0  |      | 6.0  |      | ns   |
| $t_{HIRZ}$                                    | Input register hold time - ZHT   | 0.0 |     | 0.0 |     | 0.0 |      | 0.0 |      | 0.0  |      | 0.0  |      | 0.0  |      | 0.0  |      | ns   |
| <b>Input Latch Delays with ZHT Option:</b>    |  |     |     |     |     |     |      |     |      |      |      |      |      |      |      |      |      |      |
| $t_{SILZ}$                                    | Input latch setup time - ZHT   | 6.0 |     | 6.0 |     | 6.0 |      | 6.0 |      | 6.0  |      | 6.0  |      | 6.0  |      | 6.0  |      | ns   |
| $t_{HILZ}$                                    | Input latch hold time - ZHT  | 0.0 |     | 0.0 |     | 0.0 |      | 0.0 |      | 0.0  |      | 0.0  |      | 0.0  |      | 0.0  |      | ns   |
| $t_{PDIL}$<br>$Z_i$                           | Transparent input latch to internal feedback - ZHT                               |     | 6.0 |     | 6.0 |     | 6.0  |     | 6.0  |      | 6.0  |      | 6.0  |      | 6.0  |      | 6.0  | ns   |
| <b>Output Delays:</b>                         |  |     |     |     |     |     |      |     |      |      |      |      |      |      |      |      |      |      |
| $t_{BUF}$                                     | Output buffer delay  |     | 1.5 |     | 1.5 |     | 1.8  |     | 2.0  |      | 2.5  |      | 3.0  |      | 3.0  |      | 3.0  | ns   |
| $t_{SIW}$                                     | Slow slew rate delay adder   |     | 2.5 |     | 2.5 |     | 2.5  |     | 2.5  |      | 2.5  |      | 2.5  |      | 2.5  |      | 2.5  | ns   |
| $t_{EA}$                                      | Output enable time   |     | 7.5 |     | 7.5 |     | 8.5  |     | 8.5  |      | 9.5  |      | 10.0 |      | 12.0 |      | 15.0 | ns   |
| $t_{ER}$                                      | Output disable time  |     | 7.5 |     | 7.5 |     | 8.5  |     | 8.5  |      | 9.5  |      | 10.0 |      | 12.0 |      | 15.0 | ns   |
| <b>Power Delay:</b>                           |  |     |     |     |     |     |      |     |      |      |      |      |      |      |      |      |      |      |
| $t_{PL}$                                      | Power-down mode delay adder  |     | 2.5 |     | 2.5 |     | 2.5  |     | 2.5  |      | 2.5  |      | 2.5  |      | 2.5  |      | 2.5  | ns   |
| <b>Reset and Preset Delays:</b>               |  |     |     |     |     |     |      |     |      |      |      |      |      |      |      |      |      |      |
| $t_{SRi}$                                     | Asynchronous reset or preset to internal register output                         |     | 7.5 |     | 7.7 |     | 8.0  |     | 8.0  |      | 9.5  |      | 11.0 |      | 13.0 |      | 16.0 | ns   |
| $t_{SR}$                                      | Asynchronous reset or preset to register output                                  |     | 9.0 |     | 9.2 |     | 10.0 |     | 10.0 |      | 12.0 |      | 14.0 |      | 16.0 |      | 19.0 | ns   |
| $t_{SRR}$                                     | Asynchronous reset and preset register recovery time                             | 7.0 |     | 7.0 |     | 7.5 |      | 7.5 |      | 8.0  |      | 8.0  |      | 10.0 |      | 15.0 |      | ns   |
| $t_{SRW}$                                     | Asynchronous reset or preset width   | 7.0 |     | 7.0 |     | 8.0 |      | 8.0 |      | 10.0 |      | 10.0 |      | 12.0 |      | 15.0 |      | ns   |
| <b>Clock/LE Width:</b>                        |  |     |     |     |     |     |      |     |      |      |      |      |      |      |      |      |      |      |
| $t_{WLS}$                                     | Global clock width low   | 2.0 |     | 2.0 |     | 2.5 |      | 2.5 |      | 3.0  |      | 4.0  |      | 5.0  |      | 6.0  |      | ns   |
| $t_{WHS}$                                     | Global clock width high  | 2.0 |     | 2.0 |     | 2.5 |      | 2.5 |      | 3.0  |      | 4.0  |      | 5.0  |      | 6.0  |      | ns   |
| $t_{WLA}$                                     | Product term clock width low   | 3.0 |     | 3.0 |     | 3.5 |      | 3.5 |      | 4.0  |      | 5.0  |      | 8.0  |      | 9.0  |      | ns   |
| $t_{WHA}$                                     | Product term clock width high  | 3.0 |     | 3.0 |     | 3.5 |      | 3.5 |      | 4.0  |      | 5.0  |      | 8.0  |      | 9.0  |      | ns   |
| $t_{CWS}$                                     | Global gate width low (for low transparent) or high (for high transparent)       | 4.0 |     | 4.0 |     | 4.5 |      | 4.5 |      | 5.0  |      | 5.0  |      | 6.0  |      | 6.0  |      | ns   |
| $t_{CWA}$                                     | Product term gate width low (for low transparent) or high (for high transparent) | 4.0 |     | 4.0 |     | 4.5 |      | 4.5 |      | 5.0  |      | 5.0  |      | 6.0  |      | 9.0  |      | ns   |
| $t_{WIRL}$                                    | Input register clock width low   | 3.0 |     | 3.0 |     | 3.5 |      | 3.5 |      | 4.0  |      | 5.0  |      | 6.0  |      | 6.0  |      | ns   |
| $t_{WIRH}$                                    | Input register clock width high  | 3.0 |     | 3.0 |     | 3.5 |      | 3.5 |      | 4.0  |      | 5.0  |      | 6.0  |      | 6.0  |      | ns   |
| $t_{WIL}$                                     | Input latch gate width   | 4.0 |     | 4.0 |     | 4.5 |      | 4.5 |      | 5.0  |      | 5.0  |      | 6.0  |      | 6.0  |      | ns   |

## ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup>

|                   |   | -5  |     | -55 |     | -6  |     | -65  |     | -7   |     | -10  |     | -12  |     | -14  |     | Unit |
|-------------------|---|-----|-----|-----|-----|-----|-----|------|-----|------|-----|------|-----|------|-----|------|-----|------|
|                   |   | Min | Max | Min | Max | Min | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max |      |
| <b>Frequency:</b> |   |     |     |     |     |     |     |      |     |      |     |      |     |      |     |      |     |      |
| $f_{MAXS}$        | External feedback, D-type, Min of $1/(t_{WIS} + t_{WHS})$ or $1/(t_{SS} + t_{COS})$                         | 143 |     | 133 |     | 125 |     | 118  |     | 95.2 |     | 87.0 |     | 74.1 |     | 60.6 |     | MHz  |
|                   | External feedback, T-type, Min of $1/(t_{WIS} + t_{WHS})$ or $1/(t_{SST} + t_{COS})$                        | 125 |     | 125 |     | 118 |     | 111  |     | 87.0 |     | 80.0 |     | 69.0 |     | 57.1 |     | MHz  |
|                   | Internal feedback ( $f_{CNT}$ ), D-type, Min of $1/(t_{WIS} + t_{WHS})$ or $1/(t_{SS} + t_{COSi})$          | 182 |     | 167 |     | 160 |     | 154  |     | 125  |     | 118  |     | 95.0 |     | 74.1 |     | MHz  |
|                   | Internal feedback ( $f_{CNT}$ ), T-type, Min of $1/(t_{WIS} + t_{WHS})$ or $1/(t_{SST} + t_{COSi})$         | 154 |     | 154 |     | 148 |     | 143  |     | 111  |     | 105  |     | 87.0 |     | 69.0 |     | MHz  |
|                   | No feedback <sup>2</sup> , Min of $1/(t_{WIS} + t_{WHS})$ , $1/(t_{SS} + t_{HS})$ or $1/(t_{SST} + t_{HS})$ | 250 |     | 250 |     | 200 |     | 200  |     | 154  |     | 125  |     | 100  |     | 83.3 |     | MHz  |
| $f_{MAXA}$        | External feedback, D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COA})$                         | 111 |     | 111 |     | 108 |     | 100  |     | 83.3 |     | 66.7 |     | 55.6 |     | 43.5 |     | MHz  |
|                   | External feedback, T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COA})$                        | 105 |     | 105 |     | 102 |     | 95.2 |     | 76.9 |     | 62.5 |     | 52.6 |     | 41.7 |     | MHz  |
|                   | Internal feedback ( $f_{CNTA}$ ), D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COAi})$         | 133 |     | 133 |     | 125 |     | 125  |     | 105  |     | 83.3 |     | 66.7 |     | 50.0 |     | MHz  |
|                   | Internal feedback ( $f_{CNTA}$ ), T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COAi})$        | 125 |     | 125 |     | 125 |     | 118  |     | 95.2 |     | 76.9 |     | 62.5 |     | 47.6 |     | MHz  |
|                   | No feedback <sup>2</sup> , Min of $1/(t_{WLA} + t_{WHA})$ , $1/(t_{SA} + t_{HA})$ or $1/(t_{SAT} + t_{HA})$ | 167 |     | 167 |     | 143 |     | 143  |     | 125  |     | 100  |     | 62.5 |     | 55.6 |     | MHz  |
| $f_{MAXI}$        | Maximum input register frequency, Min of $1/(t_{WIRH} + t_{WIRL})$ or $1/(t_{SIRS} + t_{HIRS})$             | 167 |     | 167 |     | 143 |     | 143  |     | 125  |     | 100  |     | 83.3 |     | 83.3 |     | MHz  |

### Notes:

1. See "Switching Test Circuit" document on the Literature Download page of the Lattice web site.
2. This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.

## CAPACITANCE<sup>1</sup>

| Parameter Symbol | Parameter Description | Test Conditions |                           | Typ | Unit |
|------------------|-----------------------|-----------------|---------------------------|-----|------|
| $C_{IN}$         | Input capacitance     | $V_{IN}=2.0$ V  | 3.3 V or 5 V, 25°C, 1 MHz | 6   | pF   |
| $C_{I/O}$        | Output capacitance    | $V_{OUT}=2.0$ V | 3.3 V or 5 V, 25°C, 1 MHz | 8   | pF   |

### Note:

1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where this parameter may be affected.



## I<sub>CC</sub> vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected “typical” pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power.



Figure 19. ispMACH 4A I<sub>CC</sub> Curves at High Speed Mode



Figure 20. ispMACH 4A I<sub>CC</sub> Curves at Low Power Mode

## 44-PIN PLCC CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

### Top View



## PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V<sub>CC</sub> = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

## 44-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

### Top View



### PIN DESIGNATIONS

- CLK/I = Clock or Input
- GND = Ground
- I/O = Input/Output
- V<sub>CC</sub> = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

# 48-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

## Top View

48-Pin TQFP (1.4mm Thickness)



17466G-028

## PIN DESIGNATIONS

- CLK/I = Clock or Input
- GND = Ground
- I/O = Input/Output
- V<sub>CC</sub> = Supply Voltage
- NC = No Connect
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

## 100-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-96/48)

### Top View



17466G-029

## PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V<sub>CC</sub> = Supply Voltage

NC = No Connect

TDI = Test Data In

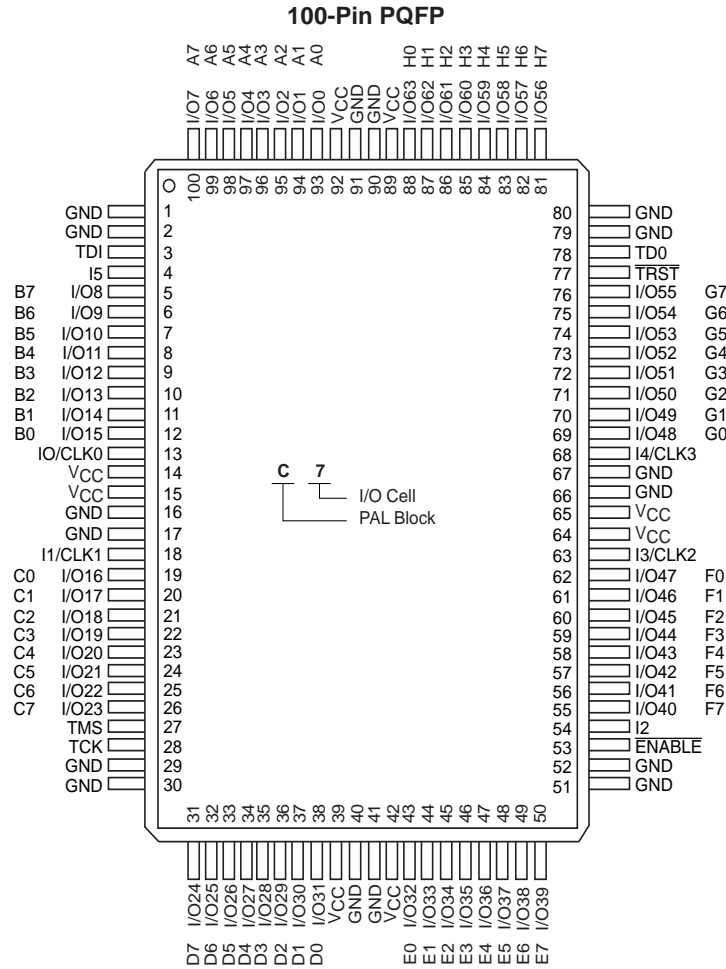
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

## 100-PIN PQFP CONNECTION DIAGRAM (M4A(3,5)-128/64)

### Top View



### PIN DESIGNATIONS

I/CLK = Input or Clock

GND = Ground

I = Input

I/O = Input/Output

V<sub>CC</sub> = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

TRST = Test Reset

ENABLE = Program

# 100-PIN TQFP CONNECTION DIAGRAM (M4A3-64/64 AND M4A(3,5)-128/64)

## Top View



## PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

VCC = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

TRST = Test Reset

ENABLE = Program

# 100-BALL caBGA CONNECTION DIAGRAM (M4A3-128/64)

## Bottom View

### 100-Ball caBGA

|   | 10                       | 9                          | 8           | 7           | 6           | 5           | 4           | 3           | 2           | 1           |   |
|---|--------------------------|----------------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---|
| A | GND                      | I/O63<br>H7                | I/O60<br>H4 | I/O57<br>H1 | GND         | GND         | I/O1<br>A1  | I/O4<br>A4  | I/O7<br>A7  | GND         | A |
| B | $\overline{\text{TRST}}$ | GND                        | I/O61<br>H5 | I5          | VCC         | I/O0<br>A0  | I/O6<br>A6  | GND         | TDI         | I/O15<br>B7 | B |
| C | I/O53<br>G5              | TDO                        | I/O62<br>H6 | I/O58<br>H2 | I/O56<br>H0 | I/O2<br>A2  | GND         | I/O14<br>B6 | I/O13<br>B5 | I/O12<br>B4 | C |
| D | I/O50<br>G2              | I/O55<br>G7                | GND         | I/O59<br>H3 | I/O3<br>A3  | I/O5<br>A5  | I/O11<br>B3 | I/O10<br>B2 | CLK0/I0     | I/O9<br>B1  | D |
| E | CLK3/I4                  | I/O49<br>G1                | I/O51<br>G3 | I/O54<br>G6 | VCC         | I/O16<br>C0 | I/O20<br>C4 | I/O8<br>B0  | VCC         | GND         | E |
| F | GND                      | VCC                        | I/O40<br>F0 | I/O52<br>G4 | I/O48<br>G0 | VCC         | I/O22<br>C6 | I/O19<br>C3 | I/O17<br>C1 | CLK1/I1     | F |
| G | I/O41<br>F1              | CLK2/I3                    | I/O42<br>F2 | I/O43<br>F3 | I/O37<br>E5 | I/O35<br>E3 | I/O27<br>D3 | GND         | I/O23<br>C7 | I/O18<br>C2 | G |
| H | I/O44<br>F4              | I/O45<br>F5                | I/O46<br>F6 | GND         | I/O34<br>E2 | I/O24<br>D0 | I/O26<br>D2 | I/O30<br>D6 | TCK         | I/O21<br>C5 | H |
| J | I/O47<br>F7              | $\overline{\text{ENABLE}}$ | GND         | I/O38<br>E6 | I/O32<br>E0 | VCC         | I2          | I/O29<br>D5 | GND         | TMS         | J |
| K | GND                      | I/O39<br>E7                | I/O36<br>E4 | I/O33<br>E1 | GND         | GND         | I/O25<br>D1 | I/O28<br>D4 | I/O31<br>D7 | GND         | K |

#### PIN DESIGNATIONS

CLK = Clock  
 GND = Ground  
 I = Input  
 I/O = Input/Output  
 N/C = No Connect  
 VCC = Supply Voltage  
 TDI = Test Data In  
 TCK = Test Clock  
 TMS = Test Mode Select  
 TDO = Test Data Out  
 $\overline{\text{TRST}}$  = Test Reset  
 ENABLE = Program



17466G-100cabga



# 144-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-192/96)

## Top View



17466G-033

## PIN DESIGNATIONS

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- V<sub>CC</sub> = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

# 144-BALL FPBGA CONNECTION DIAGRAM (M4A3-192/96)

## Bottom View

144-Ball fpBGA

|   | 12          | 11          | 10          | 9           | 8           | 7           | 6           | 5           | 4           | 3           | 2           | 1           |   |
|---|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---|
| A | GND         | I/O72<br>L7 | I/O76<br>L3 | I13         | GBCLK3      | I0          | I/O82<br>A2 | I/O86<br>A6 | I/O88<br>B0 | I/O93<br>B5 | I/O95<br>B7 | GND         | A |
| B | GND         | I/O73<br>L6 | I/O77<br>L2 | I/O79<br>L0 | VCC         | I1          | I/O83<br>A3 | I/O87<br>A7 | I/O90<br>B2 | I/O94<br>B6 | I/O0<br>D7  | TDI         | B |
| C | GND         | TD0         | I/O74<br>L5 | I14         | GND         | I/O80<br>A0 | I/O84<br>A4 | GND         | I/O92<br>B4 | I/O1<br>D6  | I/O4<br>D3  | I/O3<br>D4  | C |
| D | I/O67<br>K4 | I/O69<br>K2 | I/O71<br>K0 | I/O75<br>L4 | GBCLK0      | I/O81<br>A1 | VCC         | I/O91<br>B3 | I/O2<br>D5  | I2          | I/O6<br>D1  | I/O7<br>D0  | D |
| E | I12         | I/O64<br>K7 | I/O66<br>K5 | I/O70<br>K1 | I/O78<br>L1 | I/O85<br>A5 | I/O89<br>B1 | I/O5<br>D2  | I/O8<br>C7  | I4          | GND         | VCC         | E |
| F | I10         | I11         | GND         | I/O65<br>K6 | I/O68<br>K3 | I15         | I3          | GND         | I/O12<br>C3 | I/O11<br>C4 | I/O10<br>C5 | I/O9<br>C6  | F |
| G | I/O60<br>J3 | I/O61<br>J2 | I/O62<br>J1 | I/O63<br>J0 | VCC         | GND         | I7          | I/O20<br>E3 | I/O17<br>E6 | I/O15<br>C0 | I/O14<br>C1 | I/O13<br>C2 | G |
| H | I/O56<br>J7 | I/O57<br>J6 | I/O58<br>J5 | I/O59<br>J4 | I/O53<br>I2 | I/O41<br>H1 | I/O37<br>G5 | I/O30<br>F1 | I/O22<br>E1 | I/O18<br>E5 | I/O16<br>E7 | VCC         | H |
| J | I/O55<br>I0 | I/O54<br>I1 | VCC         | I/O50<br>I5 | I/O43<br>H3 | VCC         | I/O33<br>G1 | GBCLK2      | I/O27<br>F4 | I/O23<br>E0 | I/O21<br>E2 | I/O19<br>E4 | J |
| K | I/O51<br>I4 | I/O52<br>I3 | I/O49<br>I6 | I/O44<br>H4 | GND         | I/O36<br>G4 | I/O32<br>G0 | VCC         | I6          | I/O26<br>F5 | TCK         | TMS         | K |
| L | GND         | I/O48<br>I7 | I/O46<br>H6 | I/O42<br>H2 | I/O39<br>G7 | I/O35<br>G3 | I9          | GND         | I/O31<br>F0 | I/O29<br>F2 | I/O25<br>F6 | GND         | L |
| M | GND         | I/O47<br>H7 | I/O45<br>H5 | I/O40<br>H0 | I/O38<br>G6 | I/O34<br>G2 | I8          | GBCLK1      | I5          | I/O28<br>F3 | I/O24<br>F7 | GND         | M |
|   | 12          | 11          | 10          | 9           | 8           | 7           | 6           | 5           | 4           | 3           | 2           | 1           |   |

### PIN DESIGNATIONS

CLK = Clock  
 GND = Ground  
 I = Input  
 I/O = Input/Output  
 N/C = No Connect  
 VCC = Supply Voltage  
 TDI = Test Data In  
 TCK = Test Clock  
 TMS = Test Mode Select  
 TD0 = Test Data Out



# 208-PIN PQFP CONNECTION DIAGRAM (M4A(3,5)-256/128 AND M4A3-256/160)

Top View

208-Pin PQFP



17466G-044

# 208-PIN PQFP CONNECTION DIAGRAM (M4A3-384/160 AND M4A3-512/160)

Top View

## 208-Pin PQFP



17466Ga-044

# 256-BALL BGA CONNECTION DIAGRAM (M4A3-256/128)

## Bottom View

### 256-Ball BGA

|   | 20        | 19        | 18        | 17        | 16   | 15        | 14        | 13        | 12       | 11  | 10  | 9        | 8        | 7        | 6        | 5        | 4        | 3        | 2        | 1        |   |
|---|-----------|-----------|-----------|-----------|--|-----------|-----------|-----------|----------|-----|-----|----------|----------|----------|----------|----------|----------|----------|----------|----------|---|
| A | GND       | N/C       | GND       | I/O108 N4 | I/O105 N1  | GND       | I/O100 M4 | I/O96 M0  | GND      | GND | GND | GND      | I/O95 L0 | I/O91 L4 | GND      | I/O87 K0 | N/C      | GND      | GND      | GND      | A |
| B | GND       | I/O113 O6 | N/C       | I/O109 N5 | I/O106 N2  | I/O103 M7 | I/O102 M6 | I/O98 M2  | N/C      | I11 | N/C | N/C      | I/O93 L2 | I/O89 L6 | I/O88 L7 | I/O85 K2 | I/O83 K4 | I/O82 K5 | N/C      | GND      | B |
| C | I/O116 O3 | N/C       | VCC       | TRST      | I/O111 N7  | I/O107 N3 | I/O104 N0 | I/O101 M5 | I/O97 M1 | N/C | I10 | I/O94 L1 | I/O90 L5 | I/O86 K1 | I/O84 K3 | I/O80 K7 | ENABLE   | VCC      | I/O78 J6 | I/O74 J2 | C |
| D | I/O120 P7 | I/O117 O2 | I/O112 O7 | VCC       | VCC  | I/O110 N6 | VCC       | N/C       | I/O99 M3 | N/C | I9  | I/O92 L3 | N/C      | VCC      | I/O81 K6 | VCC      | VCC      | I/O79 J7 | I/O75 J3 | I/O71 I7 | D |
| E | I/O123 P4 | I/O119 O0 | I/O114 O5 | TDI       | <p style="text-align: center;"><b>PIN DESIGNATIONS</b></p> <p>           CLK = Clock<br/>           GND = Ground<br/>           I = Input<br/>           I/O = Input/Output<br/>           N/C = No Connect<br/>           VCC = Supply Voltage<br/>           TDI = Test Data In<br/>           TCK = Test Clock<br/>           TMS = Test Mode Select<br/>           TDO = Test Data Out<br/>           TRST = Test Reset<br/>           ENABLE = Program         </p> |           |           |           |          |     |     |          |          |          |          |          | TDO      | I/O77 J5 | I/O72 J0 | I/O68 I4 | E |
| F | GND       | I/O122 P5 | I/O118 O1 | I/O115 O4 |  |           |           |           |          |     |     |          |          |          |          |          | I/O76 J4 | I/O73 J1 | I/O69 I5 | GND      | F |
| G | I12       | I/O125 P2 | I/O121 P6 | VCC       |  |           |           |           |          |     |     |          |          |          |          |          | VCC      | I/O70 I6 | I/O65 I1 | I8       | G |
| H | GND       | I/O127 P0 | I/O126 P1 | I/O124 P3 |  |           |           |           |          |     |     |          |          |          |          |          | I/O67 I3 | I/O66 I2 | I/O64 I0 | GND      | H |
| J | N/C       | N/C       | N/C       | I13       |  |           |           |           |          |     |     |          |          |          |          |          | I7       | N/C      | N/C      | N/C      | J |
| K | GND       | CLK3      | N/C       | N/C       |  |           |           |           |          |     |     |          |          |          |          |          | N/C      | N/C      | CLK2     | N/C      | K |
| L | N/C       | CLK0      | N/C       | N/C       |  |           |           |           |          |     |     |          |          |          |          |          | N/C      | N/C      | CLK1     | GND      | L |
| M | N/C       | N/C       | N/C       | I0        |  |           |           |           |          |     |     |          |          |          |          |          | I6       | N/C      | I/O63 H0 | I/O62 H1 | M |
| N | GND       | I/O0 A0   | I/O2 A2   | I/O3 A3   |  |           |           |           |          |     |     |          |          |          |          |          | I/O60 H3 | I/O61 H2 | I/O59 H4 | GND      | N |
| P | I1        | I/O1 A1   | I/O6 A6   | VCC       |  |           |           |           |          |     |     |          |          |          |          |          | VCC      | I/O57 H6 | I/O58 H5 | I5       | P |
| R | GND       | I/O5 A5   | I/O9 B1   | N/C       | I/O51 G4   | I/O54 G1  | I/O56 H7  | GND       | R        |     |     |          |          |          |          |          |          |          |          |          |   |
| T | I/O4 A4   | I/O8 B0   | I/O12 B4  | TCK       | TMS  | I/O50 G5  | I/O55 G0  | N/C       | T        |     |     |          |          |          |          |          |          |          |          |          |   |
| U | I/O7 A7   | I/O11 B3  | I/O15 B7  | VCC       | VCC  | I/O18 C5  | VCC       | I/O24 D7  | I/O29 D2 | I2  | N/C | I/O35 E3 | N/C      | VCC      | N/C      | VCC      | VCC      | I/O48 G7 | I/O53 G2 | N/C      | U |
| V | I/O10 B2  | I/O13 B5  | VCC       | I/O16 C7  | I/O17 C6   | I/O21 C2  | I/O23 C0  | I/O27 D4  | I/O31 D0 | I3  | N/C | I/O33 E1 | I/O37 E5 | I/O41 F1 | I/O43 F3 | I/O46 F6 | I/O47 F7 | VCC      | I/O52 G3 | N/C      | V |
| W | GND       | I/O14 B6  | N/C       | N/C       | I/O19 C4   | I/O22 C1  | I/O25 D6  | I/O28 D3  | N/C      | N/C | I4  | N/C      | I/O34 E2 | I/O38 E6 | I/O39 E7 | I/O42 F2 | I/O45 F5 | N/C      | I/O49 G6 | GND      | W |
| Y | GND       | GND       | GND       | N/C       | I/O20 C3   | GND       | I/O26 D5  | I/O30 D1  | GND      | GND | GND | GND      | I/O32 E0 | I/O36 E4 | GND      | I/O40 F0 | I/O44 F4 | GND      | N/C      | GND      | Y |
|   | 20        | 19        | 18        | 17        | 16   | 15        | 14        | 13        | 12       | 11  | 10  | 9        | 8        | 7        | 6        | 5        | 4        | 3        | 2        | 1        |   |

17466G-045

## 256-BALL fpBGA CONNECTION DIAGRAM (M4A3-256/192)

### Bottom View

#### 256-Ball fpBGA

|   | 16            | 15            | 14            | 13            | 12            | 11            | 10            | 9             | 8            | 7            | 6            | 5            | 4            | 3            | 2            | 1            |   |
|---|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|---|
| A | I/O167<br>N15 | I/O181<br>O13 | I/O180<br>O12 | I/O177<br>O9  | I/O174<br>O6  | I/O172<br>O4  | I/O191<br>P14 | I/O186<br>P4  | I/O1<br>A2   | I/O3<br>A6   | GCLK0        | I/O9<br>B1   | I/O13<br>B5  | I/O15<br>B7  | I/O18<br>B10 | I/O20<br>B12 | A |
| B | I/O165<br>N13 | I/O166<br>N14 | I/O182<br>O14 | I/O179<br>O11 | I/O175<br>O7  | I/O173<br>O5  | I/O168<br>O0  | I/O187<br>P6  | I/O0<br>A0   | I/O5<br>A10  | I/O7<br>A14  | I/O10<br>B2  | I/O16<br>B8  | I/O19<br>B11 | I/O21<br>B13 | NC           | B |
| C | I/O163<br>N11 | I/O164<br>N12 | NC            | I/O183<br>O15 | I/O178<br>O10 | I/O170<br>O2  | I/O171<br>O3  | I/O189<br>P10 | I/O184<br>P0 | I/O6<br>A12  | I/O12<br>B4  | I/O14<br>B6  | I/O23<br>B15 | I/O22<br>B14 | TDI          | I/O39<br>C15 | C |
| D | I/O158<br>N6  | I/O159<br>N7  | TDO           | GND           | GND           | VCC           | GND           | VCC           | GND          | GND          | VCC          | GND          | VCC          | I/O17<br>B9  | I/O38<br>C14 | I/O37<br>C13 | D |
| E | I/O156<br>N4  | NC            | I/O162<br>N10 | VCC           | I/O160<br>N8  | I/O161<br>N9  | I/O190<br>P12 | GCLK3         | I/O188<br>P8 | I/O2<br>A4   | I/O8<br>B0   | NC           | GND          | I/O36<br>C12 | I/O35<br>C11 | I/O31<br>C7  | E |
| F | I/O152<br>N0  | I/O157<br>N5  | I/O155<br>N3  | GND           | I/O154<br>N2  | I/O153<br>N1  | I/O176<br>O8  | I/O169<br>O1  | I/O185<br>P2 | I/O4<br>A8   | I/O11<br>B3  | I/O34<br>C10 | VCC          | I/O32<br>C8  | I/O30<br>C6  | I/O29<br>C5  | F |
| G | I/O147<br>M6  | I/O150<br>M12 | I/O149<br>M10 | VCC           | I/O148<br>M8  | I/O151<br>M14 | VCC           | GND           | GND          | VCC          | I/O33<br>C9  | I/O28<br>C4  | GND          | I/O26<br>C2  | I/O25<br>C1  | I/O47<br>D14 | G |
| H | I/O144<br>M0  | I/O146<br>M4  | I/O145<br>OM2 | GND           | I/O136<br>L0  | I/O137<br>L2  | GND           | VCC           | VCC          | GND          | I/O27<br>C3  | I/O24<br>C0  | VCC          | I/O44<br>D8  | I/O43<br>D6  | I/O42<br>D4  | H |
| J | I/O138<br>L4  | I/O139<br>L6  | I/O140<br>L8  | GND           | I/O142<br>L12 | I/O141<br>L10 | GND           | VCC           | VCC          | GND          | I/O46<br>D12 | I/O45<br>D10 | GND          | I/O49<br>E2  | I/O48<br>E0  | I/O50<br>E4  | J |
| K | I/O143<br>L14 | I/O120<br>K0  | I/O121<br>K1  | VCC           | I/O123<br>K3  | I/O122<br>K2  | VCC           | GND           | GND          | VCC          | I/O41<br>D2  | I/O40<br>D0  | VCC          | I/O55<br>E14 | I/O54<br>E12 | I/O56<br>F0  | K |
| L | I/O124<br>K4  | I/O125<br>K5  | I/O127<br>K7  | GND           | I/O130<br>K10 | I/O126<br>K6  | I/O98<br>I4   | I/O91<br>H6   | I/O75<br>G3  | I/O77<br>G5  | I/O52<br>E8  | I/O51<br>E6  | GND          | I/O59<br>F3  | I/O60<br>F4  | I/O57<br>F1  | L |
| M | I/O128<br>K8  | I/O129<br>K9  | I/O131<br>K11 | GND           | I/O107<br>J3  | I/O105<br>J1  | I/O100<br>I8  | I/O90<br>H4   | I/O74<br>G2  | I/O80<br>G8  | I/O83<br>G11 | I/O53<br>E10 | VCC          | I/O68<br>F12 | I/O63<br>F7  | I/O58<br>F2  | M |
| N | I/O132<br>K12 | I/O133<br>K13 | I/O135<br>K15 | VCC           | GND           | VCC           | GND           | VCC           | GND          | GND          | VCC          | GND          | GND          | TCK          | I/O64<br>F8  | I/O61<br>F5  | N |
| P | I/O134<br>K14 | I/O117<br>J13 | I/O118<br>J14 | I/O119<br>J15 | I/O108<br>J4  | I/O106<br>J2  | I/O101<br>I10 | I/O89<br>H2   | I/O93<br>H10 | I/O94<br>H12 | I/O79<br>G7  | I/O84<br>G12 | I/O87<br>G15 | TMS          | I/O65<br>F9  | I/O62<br>F6  | P |
| R | I/O116<br>J12 | I/O115<br>J11 | I/O112<br>J8  | I/O111<br>J7  | I/O104<br>J0  | I/O102<br>I12 | I/O99<br>I6   | I/O96<br>I0   | I/O92<br>H8  | I/O72<br>G0  | I/O76<br>G4  | I/O81<br>G9  | I/O85<br>G13 | I/O71<br>F15 | I/O67<br>F11 | I/O66<br>F10 | R |
| T | I/O114<br>J10 | I/O113<br>J9  | I/O110<br>J6  | I/O109<br>J5  | I/O103<br>I14 | GCLK2         | I/O97<br>I2   | I/O88<br>H0   | GCLK1        | I/O95<br>H14 | I/O73<br>G1  | I/O78<br>G6  | I/O82<br>G10 | I/O86<br>G14 | I/O70<br>F14 | I/O69<br>F13 | T |

#### PIN DESIGNATIONS

CLK = Clock  
 GND = Ground  
 I = Input  
 I/O = Input/Output  
 N/C = No Connect  
 VCC = Supply Voltage  
 TDI = Test Data In  
 TCK = Test Clock  
 TMS = Test Mode Select  
 TDO = Test Data Out



17466G-047

# 256-BALL BGA CONNECTION DIAGRAM - (M4A3-384/192)

## Bottom View

### 256-Ball BGA

|   | 20       | 19        | 18        | 17        | 16  | 15        | 14        | 13        | 12        | 11        | 10        | 9          | 8          | 7          | 6          | 5          | 4         | 3         | 2         | 1         |           |   |  |  |  |  |  |  |           |           |           |           |   |
|---|----------|-----------|-----------|-----------|---|-----------|-----------|-----------|-----------|-----------|-----------|------------|------------|------------|------------|------------|-----------|-----------|-----------|-----------|-----------|---|--|--|--|--|--|--|-----------|-----------|-----------|-----------|---|
| A | GND      | I/O11 FX7 | GND       | I/O44 FX6 | I/O58 CX6   | GND       | I/O70 CX2 | I/O76 DX6 | GND       | GND       | GND       | GND        | I/O108 AX5 | I/O116 BX0 | GND        | I/O128 BX7 | I/O134 O3 | GND       | GND       | GND       | A         |   |  |  |  |  |  |  |           |           |           |           |   |
| B | GND      | I/O12 GX7 | I/O28 FX5 | I/O45 FX3 | I/O59 CX7   | I/O64 CX5 | I/O71 CX3 | I/O77 DX7 | I/O84 DX5 | I/O90 DX2 | I/O96 AX0 | I/O102 AX3 | I/O109 AX6 | I/O117 BX1 | I/O122 BX4 | I/O129 BX6 | I/O135 O4 | I/O148 O6 | I/O164 O7 | GND       | B         |   |  |  |  |  |  |  |           |           |           |           |   |
| C | I/O0 GX6 | I/O13 GX5 | VCC       | I/O46 FX4 | I/O60 FX2   | I/O65 FX1 | I/O72 CX4 | I/O78 CX0 | I/O85 DX4 | I/O91 DX1 | I/O97 AX1 | I/O103 AX4 | I/O110 BX2 | I/O118 BX5 | I/O123 O0  | I/O130 O1  | I/O136 O5 | VCC       | I/O165 N7 | I/O181 N6 | C         |   |  |  |  |  |  |  |           |           |           |           |   |
| D | I/O1 EX7 | I/O14 GX3 | I/O29 GX4 | VCC       | VCC   | I/O66 FX0 | VCC       | I/O79 CX1 | I/O86 DX3 | I/O92 DX0 | I/O98 AX2 | I/O104 AX7 | I/O111 BX3 | VCC        | I/O124 O2  | VCC        | VCC       | VCC       | I/O149 N4 | I/O166 N5 | I/O182 P7 | D |  |  |  |  |  |  |           |           |           |           |   |
| E | I/O2 EX0 | I/O15 GX0 | I/O30 GX1 | TDI       | <p style="text-align: center;"><b>PIN DESIGNATIONS</b></p> <p>           CLK = Clock<br/>           GND = Ground<br/>           I = Input<br/>           I/O = Input/Output<br/>           N/C = No Connect<br/>           VCC = Supply Voltage<br/>           TDI = Test Data In<br/>           TCK = Test Clock<br/>           TMS = Test Mode Select<br/>           TDO = Test Data Out         </p> |           |           |           |           |           |           |            |            |            |            |            | TDO       | I/O150 N2 | I/O167 N3 | I/O183 P6 | E         |   |  |  |  |  |  |  |           |           |           |           |   |
| F | GND      | I/O16 EX1 | I/O31 EX6 | I/O47 GX2 |   |           |           |           |           |           |           |            |            |            |            |            |           |           |           |           |           |   |  |  |  |  |  |  | I/O137 N1 | I/O151 N0 | I/O168 P5 | GND       | F |
| G | I/O3 HX6 | I/O17 EX4 | I/O32 EX5 | VCC       |   |           |           |           |           |           |           |            |            |            |            |            |           |           |           |           |           |   |  |  |  |  |  |  | VCC       | I/O152 P4 | I/O169 P3 | I/O184 M7 | G |
| H | GND      | I/O18 HX5 | I/O33 EX2 | I/O48 EX3 |   |           |           |           |           |           |           |            |            |            |            |            |           |           |           |           |           |   |  |  |  |  |  |  | I/O138 P2 | I/O153 P1 | I/O170 P0 | GND       | H |
| J | I/O4 HX0 | I/O19 HX1 | I/O34 HX4 | I/O49 HX7 |   |           |           |           |           |           |           |            |            |            |            |            |           |           |           |           |           |   |  |  |  |  |  |  | I/O139 M6 | I/O154 M5 | I/O171 M4 | I/O185 M3 | J |
| K | GND      | CLK3      | I/O35 HX2 | I/O50 HX3 |   |           |           |           |           |           |           |            |            |            |            |            |           |           |           |           |           |   |  |  |  |  |  |  | I/O140 M0 | I/O155 M1 | CLK2      | I/O186 M2 | K |
| L | I/O5 A2  | CLK0      | I/O36 A0  | I/O51 A1  |   |           |           |           |           |           |           |            |            |            |            |            |           |           |           |           |           |   |  |  |  |  |  |  | I/O141 L3 | I/O156 L4 | CLK1      | GND       | L |
| M | I/O6 A4  | I/O20 A3  | I/O37 A5  | I/O52 A6  |   |           |           |           |           |           |           |            |            |            |            |            |           |           |           |           |           |   |  |  |  |  |  |  | I/O142 L6 | I/O157 L5 | I/O172 L0 | I/O187 L1 | M |
| N | GND      | I/O21 A7  | I/O38 D0  | I/O53 D1  |   |           |           |           |           |           |           |            |            |            |            |            |           |           |           |           |           |   |  |  |  |  |  |  | I/O143 I5 | I/O158 I0 | I/O173 L7 | GND       | N |
| P | I/O7 D2  | I/O22 D3  | I/O39 D4  | VCC       |   |           |           |           |           |           |           |            |            |            |            |            |           |           |           |           |           |   |  |  |  |  |  |  | VCC       | I/O159 I4 | I/O174 I1 | I/O188 L2 | P |
| R | GND      | I/O23 D5  | I/O40 D6  | I/O54 D7  |   |           |           |           |           |           |           |            |            |            |            |            | I/O144 K5 | I/O160 K0 | I/O175 I3 | GND       | R         |   |  |  |  |  |  |  |           |           |           |           |   |
| T | I/O8 B3  | I/O24 B0  | I/O41 B7  | TCK       |   |           |           |           |           |           |           |            |            |            |            |            | TMS       | I/O161 K4 | I/O176 K1 | I/O189 I2 | T         |   |  |  |  |  |  |  |           |           |           |           |   |
| U | I/O9 B4  | I/O25 B1  | I/O42 B6  | VCC       | VCC   | I/O67 C0  | VCC       | I/O80 F0  | I/O87 E5  | I/O93 E2  | I/O99 H2  | I/O105 H5  | I/O112 G0  | VCC        | I/O125 J1  | VCC        | VCC       | I/O162 K7 | I/O177 K2 | I/O190 I6 | U         |   |  |  |  |  |  |  |           |           |           |           |   |
| V | I/O10 B5 | I/O26 B2  | VCC       | I/O55 C5  | I/O61 C2  | I/O68 C1  | I/O73 F4  | I/O81 F1  | I/O88 E4  | I/O94 E1  | I/O100 H1 | I/O106 H4  | I/O113 G1  | I/O119 G4  | I/O126 J0  | I/O131 J2  | I/O145 J5 | VCC       | I/O178 K3 | I/O191 I7 | V         |   |  |  |  |  |  |  |           |           |           |           |   |
| W | GND      | I/O27 C7  | I/O43 C6  | I/O56 C3  | I/O62 F7  | I/O69 F5  | I/O74 F3  | I/O82 E7  | I/O89 E3  | I/O95 E0  | I/O101 H0 | I/O107 H3  | I/O114 H7  | I/O120 G3  | I/O127 G5  | I/O132 G7  | I/O146 J4 | I/O163 J6 | I/O179 J7 | GND       | W         |   |  |  |  |  |  |  |           |           |           |           |   |
| Y | GND      | GND       | GND       | I/O57 C4  | I/O63 F6  | GND       | I/O75 F2  | I/O83 E6  | GND       | GND       | GND       | GND        | I/O115 H6  | I/O121 G2  | GND        | I/O133 G6  | I/O147 J3 | GND       | I/O180 K6 | GND       | Y         |   |  |  |  |  |  |  |           |           |           |           |   |
|   | 20       | 19        | 18        | 17        | 16  | 15        | 14        | 13        | 12        | 11        | 10        | 9          | 8          | 7          | 6          | 5          | 4         | 3         | 2         | 1         |           |   |  |  |  |  |  |  |           |           |           |           |   |

17466G-046

# 256-BALL fpBGA CONNECTION DIAGRAM (M4A3-256/128)

## Bottom View

### 256-Ball fpBGA

|   | 16        | 15        | 14        | 13        | 12        | 11        | 10        | 9         | 8        | 7        | 6        | 5        | 4        | 3        | 2        | 1        |   |
|---|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|----------|----------|----------|----------|----------|----------|----------|----------|---|
| A | TRST      | I/O117 O5 | I/O116 O4 | I/O113 O1 | I/O126 P6 | I/O124 P4 | I12       | NC        | NC       | NC       | CLK0     | I/O1 A1  | I/O5 A5  | I/O7 A7  | I/O10 B2 | I/O12 B4 | A |
| B | I/O110 N6 | I/O111 N7 | I/O118 O6 | I/O115 O3 | I/O127 P7 | I/O125 P5 | I/O120 P0 | NC        | NC       | NC       | I1       | I/O2 A2  | I/O8 B0  | I/O11 B3 | I/O13 B5 | NC       | B |
| C | I/O108 N4 | I/O109 N5 | NC        | I/O119 O7 | I/O114 O2 | I/O122 P2 | I/O123 P3 | NC        | NC       | I0       | I/O4 A4  | I/O6 A6  | I/O15 B7 | I/O14 B6 | TDI      | I/O23 C7 | C |
| D | NC        | I/O104 N0 | TDO       | GND       | GND       | VCC       | GND       | VCC       | GND      | GND      | VCC      | GND      | VCC      | I/O9 B1  | I/O22 C6 | I/O21 C5 | D |
| E | I/O102 M6 | NC        | I/O107 N3 | VCC       | I/O105 N1 | I/O106 N2 | I13       | CLK3      | NC       | NC       | I/O0 A0  | NC       | GND      | I/O20 C4 | I/O19 C3 | I/O31 D7 | E |
| F | I/O98 M2  | I/O103 M7 | I/O101 M5 | GND       | I/O100 M4 | I/O99 M3  | I/O112 O0 | I/O121 P1 | NC       | NC       | I/O3 A3  | I/O18 C2 | VCC      | I/O16 C0 | I/O30 D6 | I/O29 D5 | F |
| G | NC        | I/O96 M0  | I11       | VCC       | NC        | I/O97 M1  | VCC       | GND       | GND      | VCC      | I/O17 C1 | I/O28 D4 | GND      | I/O26 D2 | I/O25 D1 | I2       | G |
| H | I/O88 L0  | I10       | I9        | GND       | I/O89 L1  | I/O90 L2  | GND       | VCC       | VCC      | GND      | I/O27 D3 | I/O24 D0 | VCC      | NC       | NC       | NC       | H |
| J | I/O91 L3  | I/O92 L4  | I/O93 L5  | GND       | I/O95 L7  | I/O94 L6  | GND       | VCC       | VCC      | GND      | I3       | NC       | GND      | NC       | NC       | NC       | J |
| K | NC        | NC        | NC        | VCC       | NC        | NC        | VCC       | GND       | GND      | VCC      | NC       | NC       | VCC      | I4       | NC       | I/O32 E0 | K |
| L | NC        | NC        | I/O80 K0  | GND       | I/O83 K3  | NC        | NC        | NC        | I/O59 H3 | I/O61 H5 | NC       | NC       | GND      | I/O35 E3 | I/O36 E4 | I/O33 E1 | L |
| M | I/O81 K1  | I/O82 K2  | I/O84 K4  | GND       | I/O67 I3  | I/O65 I1  | NC        | NC        | I/O58 H2 | I/O48 G0 | I/O51 G3 | NC       | VCC      | I/O44 F4 | I/O39 E7 | I/O34 E2 | M |
| N | I/O85 K5  | I/O86 K6  | ENABLE    | VCC       | GND       | VCC       | GND       | VCC       | GND      | GND      | VCC      | GND      | GND      | TCK      | I/O40 F0 | I/O37 E5 | N |
| P | I/O87 K7  | I/O77 J5  | I/O78 J6  | I/O79 J7  | I/O68 I4  | I/O66 I2  | NC        | NC        | NC       | I6       | I/O63 H7 | I/O52 G4 | I/O55 G7 | TMS      | I/O41 F1 | I/O38 E6 | P |
| R | I/O76 J4  | I/O75 J3  | I/O72 J0  | I/O71 I7  | I/O64 I0  | I7        | NC        | NC        | NC       | I/O56 H0 | I/O60 H4 | I/O49 G1 | I/O53 G5 | I/O47 F7 | I/O43 F3 | I/O42 F2 | R |
| T | I/O74 J2  | I/O73 J1  | I/O70 I6  | I/O69 I5  | I8        | CLK2      | NC        | NC        | CLK1     | I5       | I/O57 H1 | I/O62 H6 | I/O50 G2 | I/O54 G6 | I/O46 F6 | I/O45 F5 | T |

#### PIN DESIGNATIONS

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- N/C = No Connect
- VCC = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out
- TRST = Test Reset
- ENABLE = Program



m4a3.256.128\_256bga



## 256-BALL fpBGA CONNECTION DIAGRAM (M4A3-384/192)

### Bottom View

#### 256-Ball fpBGA

|   | 16            | 15            | 14            | 13            | 12            | 11            | 10            | 9             | 8             | 7           | 6           | 5           | 4           | 3           | 2           | 1           |   |
|---|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---|
| A | I/O175<br>FX7 | I/O181<br>GX5 | I/O180<br>GX4 | I/O177<br>GX1 | I/O166<br>EX6 | I/O164<br>EX4 | I/O191<br>HX7 | I/O186<br>HX2 | I/O1<br>A1    | I/O3<br>A3  | CLK0        | I/O25<br>D1 | I/O29<br>D5 | I/O31<br>D7 | I/O10<br>B2 | I/O12<br>B4 | A |
| B | I/O173<br>FX5 | I/O174<br>FX6 | I/O182<br>GX6 | I/O179<br>GX3 | I/O167<br>EX7 | I/O165<br>EX5 | I/O160<br>EX0 | I/O187<br>HX3 | I/O0<br>A0    | I/O5<br>A5  | I/O7<br>A7  | I/O26<br>D2 | I/O8<br>B0  | I/O11<br>B3 | I/O13<br>B5 | N/C         | B |
| C | I/O171<br>FX3 | I/O172<br>FX4 | N/C           | I/O183<br>GX7 | I/O178<br>GX2 | I/O162<br>EX2 | I/O163<br>EX3 | I/O189<br>HX5 | I/O184<br>HX0 | I/O6<br>A6  | I/O28<br>D4 | I/O30<br>D6 | I/O15<br>B7 | I/O14<br>B6 | TDI         | I/O23<br>C7 | C |
| D | I/O150<br>CX6 | I/O151<br>CX7 | TDO           | GND           | GND           | VCC           | GND           | VCC           | GND           | GND         | VCC         | GND         | VCC         | I/O9<br>B1  | I/O22<br>C6 | I/O21<br>C5 | D |
| E | I/O148<br>CX4 | N/C           | I/O170<br>FX2 | VCC           | I/O168<br>FX0 | 169<br>FX1    | I/O190<br>HX6 | CLK3          | I/O188<br>HX4 | I/O2<br>A2  | I/O24<br>D0 | N/C         | GND         | I/O20<br>C4 | I/O19<br>C3 | I/O47<br>F7 | E |
| F | I/O144<br>CX0 | I/O149<br>CX5 | I/O147<br>CX3 | GND           | I/O146<br>CX2 | I/O145<br>CX1 | I/O176<br>GX0 | I/O161<br>EX1 | I/O185<br>HX1 | I/O4<br>A4  | I/O27<br>D3 | I/O18<br>C2 | VCC         | I/O16<br>C0 | I/O46<br>F6 | I/O45<br>F5 | F |
| G | I/O155<br>DX3 | I/O158<br>DX6 | I/O157<br>DX5 | VCC           | I/O156<br>DX4 | I/O159<br>DX7 | VCC           | GND           | GND           | VCC         | I/O17<br>C1 | I/O44<br>F4 | GND         | I/O42<br>F2 | I/O41<br>F1 | I/O39<br>E7 | G |
| H | I/O152<br>DX0 | I/O154<br>DX2 | I/O153<br>DX1 | GND           | I/O128<br>AX0 | I/O129<br>AX1 | GND           | VCC           | VCC           | GND         | I/O43<br>F3 | I/O40<br>F0 | VCC         | I/O36<br>E4 | I/O35<br>E3 | I/O34<br>E2 | H |
| J | I/O130<br>AX2 | I/O131<br>AX3 | I/O132<br>AX4 | GND           | I/O134<br>AX6 | I/O133<br>AX5 | GND           | VCC           | VCC           | GND         | I/O38<br>E6 | I/O37<br>E5 | GND         | I/O57<br>H1 | I/O56<br>H0 | I/O58<br>H2 | J |
| K | I/O135<br>AX7 | I/O136<br>BX0 | I/O137<br>BX1 | VCC           | I/O139<br>BX3 | I/O138<br>BX2 | VCC           | GND           | GND           | VCC         | I/O33<br>E1 | I/O32<br>E0 | VCC         | I/O63<br>H7 | I/O62<br>H6 | I/O48<br>G0 | K |
| L | I/O140<br>BX4 | I/O141<br>BX5 | I/O143<br>BX7 | GND           | I/O114<br>O2  | I/O142<br>BX6 | I/O98<br>M2   | I/O91<br>L3   | I/O67<br>I3   | I/O69<br>I5 | I/O60<br>H4 | I/O59<br>H3 | GND         | I/O51<br>G3 | I/O52<br>G4 | I/O49<br>G1 | L |
| M | I/O112<br>O0  | I/O113<br>O1  | I/O115<br>O3  | GND           | I/O123<br>P3  | I/O121<br>P1  | I/O100<br>M4  | I/O90<br>L2   | I/O66<br>I2   | I/O80<br>K0 | I/O83<br>K3 | I/O61<br>H5 | VCC         | I/O76<br>J4 | I/O55<br>G7 | I/O50<br>G2 | M |
| N | I/O116<br>O4  | I/O117<br>O5  | I/O119<br>O7  | VCC           | GND           | VCC           | GND           | VCC           | GND           | GND         | VCC         | GND         | GND         | TCK         | I/O72<br>J0 | I/O53<br>G5 | N |
| P | I/O118<br>O6  | I/O109<br>N5  | I/O110<br>N6  | I/O111<br>N7  | I/O124<br>P4  | I/O122<br>P2  | I/O101<br>M5  | I/O89<br>L1   | I/O93<br>L5   | I/O94<br>L6 | I/O71<br>I7 | I/O84<br>K4 | I/O87<br>K7 | TMS         | I/O73<br>J1 | I/O54<br>G6 | P |
| R | I/O108<br>N4  | I/O107<br>N3  | I/O104<br>N0  | I/O127<br>P7  | I/O120<br>P0  | I/O102<br>M6  | I/O99<br>M3   | I/O96<br>M0   | I/O92<br>L4   | I/O64<br>I0 | I/O68<br>I4 | I/O81<br>K1 | I/O85<br>K5 | I/O79<br>J7 | I/O75<br>J3 | I/O74<br>J2 | R |
| T | I/O106<br>N2  | I/O105<br>N1  | I/O126<br>P6  | I/O125<br>P5  | I/O103<br>M7  | CLK2          | I/O97<br>M1   | I/O88<br>L0   | CLK1          | I/O95<br>L7 | I/O65<br>I1 | I/O70<br>I6 | I/O82<br>K2 | I/O86<br>K6 | I/O78<br>J6 | I/O77<br>J5 | T |

#### PIN DESIGNATIONS

CLK = Clock  
 GND = Ground  
 I = Input  
 I/O = Input/Output  
 N/C = No Connect  
 VCC = Supply Voltage  
 TDI = Test Data In  
 TCK = Test Clock  
 TMS = Test Mode Select  
 TDO = Test Data Out



# 256-BALL fpBGA CONNECTION DIAGRAM (M4A3-512/192)

## Bottom View

### 256-Ball fpBGA

|   | 16            | 15            | 14            | 13            | 12            | 11            | 10            | 9             | 8             | 7           | 6           | 5           | 4           | 3           | 2           | 1           |   |
|---|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---|
| A | I/O159<br>KX7 | I/O181<br>OX5 | I/O180<br>OX4 | I/O177<br>OX1 | I/O174<br>NX6 | I/O172<br>NX4 | I/O191<br>PX7 | I/O186<br>PX2 | I/O1<br>A1    | I/O3<br>A3  | CLK0        | I/O17<br>C1 | I/O21<br>C5 | I/O23<br>C7 | I/O10<br>B2 | I/O12<br>B4 | A |
| B | I/O157<br>KX5 | I/O158<br>KX6 | I/O182<br>OX6 | I/O179<br>OX3 | I/O175<br>NX7 | I/O173<br>NX5 | I/O168<br>NX0 | I/O187<br>PX3 | I/O0<br>A0    | I/O5<br>A5  | I/O7<br>A7  | I/O18<br>C2 | I/O8<br>B0  | I/O11<br>B3 | I/O13<br>B5 | N/C         | B |
| C | I/O155<br>KX3 | I/O156<br>KX4 | N/C           | I/O183<br>OX7 | I/O178<br>OX2 | I/O170<br>NX2 | I/O171<br>NX3 | I/O189<br>PX5 | I/O184<br>PX0 | I/O6<br>A6  | I/O20<br>C4 | I/O22<br>C6 | I/O15<br>B7 | I/O14<br>B6 | TDI         | I/O39<br>F7 | C |
| D | I/O150<br>JX6 | I/O151<br>JX7 | TDO           | GND           | GND           | VCC           | GND           | VCC           | GND           | GND         | VCC         | GND         | VCC         | I/O9<br>B1  | I/O38<br>F6 | I/O37<br>F5 | D |
| E | I/O148<br>JX4 | N/C           | I/O154<br>KX2 | VCC           | I/O152<br>KX0 | I/O153<br>KX1 | I/O190<br>PX6 | CLK3          | I/O188<br>PX4 | I/O2<br>A2  | I/O16<br>C0 | N/C         | GND         | I/O36<br>F4 | I/O35<br>F3 | I/O47<br>G7 | E |
| F | I/O144<br>JX0 | I/O149<br>JX5 | I/O147<br>JX3 | GND           | I/O146<br>JX2 | I/O145<br>JX1 | I/O176<br>OX0 | I/O169<br>NX1 | I/O185<br>PX1 | I/O4<br>A4  | I/O19<br>C3 | I/O34<br>F2 | VCC         | I/O32<br>F0 | I/O46<br>G6 | I/O45<br>G5 | F |
| G | I/O163<br>LX3 | I/O166<br>LX6 | I/O165<br>LX5 | VCC           | I/O164<br>LX4 | I/O167<br>LX7 | VCC           | GND           | GND           | VCC         | I/O33<br>F1 | I/O44<br>G4 | GND         | I/O42<br>G2 | I/O41<br>G1 | I/O31<br>E7 | G |
| H | I/O160<br>LX0 | I/O162<br>LX2 | I/O161<br>LX1 | GND           | I/O120<br>EX0 | I/O121<br>EX1 | GND           | VCC           | VCC           | GND         | I/O43<br>G3 | I/O40<br>G0 | VCC         | I/O28<br>E4 | I/O27<br>E3 | I/O26<br>E2 | H |
| J | I/O122<br>EX2 | I/O123<br>EX3 | I/O124<br>EX4 | GND           | I/O126<br>EX6 | I/O125<br>EX5 | GND           | VCC           | VCC           | GND         | I/O30<br>E6 | I/O29<br>E5 | GND         | I/O65<br>L1 | I/O64<br>L0 | I/O66<br>L2 | J |
| K | I/O127<br>EX7 | I/O136<br>GX0 | I/O137<br>GX1 | VCC           | I/O139<br>GX3 | I/O138<br>GX2 | VCC           | GND           | GND           | VCC         | I/O25<br>E1 | I/O24<br>E0 | VCC         | I/O71<br>L7 | I/O70<br>L6 | I/O48<br>J0 | K |
| L | I/O140<br>GX4 | I/O141<br>GX5 | I/O143<br>GX7 | GND           | I/O130<br>FX2 | I/O142<br>GX6 | I/O98<br>AX2  | I/O91<br>P3   | I/O75<br>N3   | I/O77<br>N5 | I/O68<br>L4 | I/O67<br>L3 | GND         | I/O51<br>J3 | I/O52<br>J4 | I/O49<br>J1 | L |
| M | I/O128<br>FX0 | I/O129<br>FX1 | I/O131<br>FX3 | GND           | I/O115<br>CX3 | I/O113<br>CX1 | I/O100<br>AX4 | I/O90<br>P2   | I/O74<br>N2   | I/O80<br>O0 | I/O83<br>O3 | I/O69<br>L5 | VCC         | I/O60<br>K4 | I/O55<br>J7 | I/O50<br>J2 | M |
| N | I/O132<br>FX4 | I/O133<br>FX5 | I/O135<br>FX7 | VCC           | GND           | VCC           | GND           | VCC           | GND           | GND         | VCC         | GND         | GND         | TCK         | I/O56<br>K0 | I/O53<br>J5 | N |
| P | I/O134<br>FX6 | I/O109<br>BX5 | I/O110<br>BX6 | I/O111<br>BX7 | I/O116<br>CX4 | I/O114<br>CX2 | I/O101<br>AX5 | I/O89<br>P1   | I/O93<br>P5   | I/O94<br>P6 | I/O79<br>N7 | I/O84<br>O4 | I/O87<br>O7 | TMS         | I/O57<br>K1 | I/O54<br>J6 | P |
| R | I/O108<br>BX4 | I/O107<br>BX3 | I/O104<br>BX0 | I/O119<br>CX7 | I/O112<br>CX0 | I/O102<br>AX6 | I/O99<br>AX3  | I/O96<br>AX0  | I/O92<br>P4   | I/O72<br>N0 | I/O76<br>N4 | I/O81<br>O1 | I/O85<br>O5 | I/O63<br>K7 | I/O59<br>K3 | I/O58<br>K2 | R |
| T | I/O106<br>BX2 | I/O105<br>BX1 | I/O118<br>CX6 | I/O117<br>CX5 | I/O103<br>AX7 | CLK2          | I/O97<br>AX1  | I/O88<br>P0   | CLK1          | I/O95<br>P7 | I/O73<br>N1 | I/O78<br>N6 | I/O82<br>O2 | I/O86<br>O6 | I/O62<br>K6 | I/O61<br>K5 | T |

#### PIN DESIGNATIONS

- CLK = Clock
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- I/O = Input/Output
- N/C = No Connect
- VCC = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out



# 388-BALL fpBGA CONNECTION DIAGRAM (M4A3-512/256)

## Bottom View

### 388-Ball fpBGA

|    | 22         | 21         | 20         | 19         | 18         | 17         | 16         | 15         | 14         | 13         | 12         | 11         | 10        | 9         | 8         | 7         | 6         | 5         | 4         | 3         | 2         | 1        |          |          |   |
|----|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|----------|----------|----------|---|
| A  | GND        | I/O243 OX3 | I/O240 OX0 | I/O241 OX1 | I/O236 NX4 | I/O231 MX7 | I/O228 MX4 | I/O226 MX2 | I/O255 PX7 | I/O251 PX3 | I/O248 PX0 | I/O0 A0    | I/O5 A5   | I/O6 A6   | I/O27 D3  | I/O30 D6  | I/O17 C1  | I/O22 C6  | I/O8 B0   | I/O10 B2  | N/C       | GND      | A        |          |   |
| B  | N/C        | GND        | I/O245 OX5 | I/O242 OX2 | I/O238 NX6 | I/O234 NX2 | I/O232 NX0 | I/O229 MX5 | I/O224 MX0 | I/O253 PX5 | I/O249 PX1 | I/O2 A2    | CLK0      | I/O26 D2  | I/O29 D5  | I/O31 D7  | I/O20 C4  | I/O9 B1   | I/O12 B4  | I/O13 B5  | GND       | TDI      | B        |          |   |
| C  | I/O213 KX5 | TDO        | GND        | I/O247 OX7 | I/O244 OX4 | I/O239 NX7 | I/O235 NX3 | I/O230 MX6 | I/O227 MX3 | CLK3       | I/O250 PX2 | I/O1 A1    | I/O7 A7   | I/O25 D1  | I/O16 C0  | I/O18 C2  | I/O23 C7  | I/O11 B3  | I/O15 B7  | GND       | I/O47 F7  | I/O44 F4 | C        |          |   |
| D  | I/O210 KX2 | I/O212 KX4 | I/O215 KX7 | GND        | I/O246 OX6 | VCC        | I/O237 NX5 | I/O233 NX1 | VCC        | I/O254 PX6 | VCC        | I/O3 A3    | I/O24 D0  | VCC       | I/O19 C3  | I/O21 C5  | VCC       | I/O14 B6  | GND       | I/O46 F6  | I/O43 F3  | I/O41 F1 | D        |          |   |
| E  | I/O207 JX7 | I/O209 KX1 | I/O211 KX3 | I/O214 KX6 |            |            |            |            |            |            |            |            |           |           |           |           |           |           | I/O45 F5  | I/O42 F2  | I/O40 F0  | I/O54 G6 | E        |          |   |
| F  | I/O203 JX3 | I/O205 JX5 | I/O208 KX0 | VCC        |            |            |            |            |            |            |            |            |           |           |           |           |           |           | VCC       | I/O55 G7  | I/O52 G4  | I/O50 G2 | F        |          |   |
| G  | I/O200 JX0 | I/O202 JX2 | I/O204 JX4 | I/O206 JX6 |            |            | VCC        | VCC        | N/C        | I/O225 MX1 | I/O252 PX4 | I/O4 A4    | I/O28 D4  | N/C       | VCC       | VCC       |           |           | I/O53 G5  | I/O51 G3  | I/O49 G1  | I/O39 E7 | G        |          |   |
| H  | I/O221 LX5 | I/O222 LX6 | I/O223 LX7 | I/O201 JX1 |            |            | VCC        | N/C        | GND        | GND        | GND        | GND        | GND       | GND       | N/C       | VCC       |           |           | I/O48 G0  | I/O38 E6  | I/O37 E5  | I/O36 E4 | H        |          |   |
| J  | I/O218 LX2 | I/O219 LX3 | I/O220 LX4 | VCC        |            |            | N/C        | GND        | GND        | GND        | GND        | GND        | GND       | GND       | GND       | N/C       |           |           | VCC       | I/O35 E3  | I/O34 E2  | I/O32 E0 | J        |          |   |
| K  | I/O197 IX5 | I/O198 IX6 | I/O199 IX7 | I/O216 LX0 |            |            | I/O217 LX1 | GND        | GND        | GND        | GND        | GND        | GND       | GND       | GND       | GND       | I/O33 E1  |           |           | I/O63 H7  | I/O62 H6  | I/O61 H5 | I/O60 H4 | K        |   |
| L  | I/O192 IX0 | I/O194 IX2 | I/O195 IX3 | I/O196 IX4 |            |            | I/O193 IX1 | GND        | GND        | GND        | GND        | GND        | GND       | GND       | GND       | GND       | I/O58 H2  |           |           | VCC       | I/O59 H3  | I/O57 H1 | I/O56 H0 | L        |   |
| M  | I/O184 HX0 | I/O185 HX1 | I/O187 HX3 | VCC        |            |            | I/O186 HX2 | GND        | GND        | GND        | GND        | GND        | GND       | GND       | GND       | GND       | I/O69 I5  |           |           | I/O67 I3  | I/O65 I1  | I/O66 I2 | I/O64 I0 | M        |   |
| N  | I/O188 HX4 | I/O189 HX5 | I/O191 HX7 | I/O190 HX6 |            |            | I/O182 EX2 | GND        | GND        | GND        | GND        | GND        | GND       | GND       | GND       | GND       | I/O89 L1  |           |           | I/O88 L0  | I/O71 I7  | I/O70 I6 | I/O68 I4 | N        |   |
| P  | I/O160 EX0 | I/O161 EX1 | I/O163 EX3 | VCC        |            |            | N/C        | GND        | GND        | GND        | GND        | GND        | GND       | GND       | GND       | GND       | N/C       |           |           | VCC       | I/O92 L4  | I/O91 L3 | I/O90 L2 | P        |   |
| R  | I/O164 EX4 | I/O165 EX5 | I/O166 EX6 | I/O177 GX1 |            |            | VCC        | N/C        | GND        | GND        | GND        | GND        | GND       | GND       | N/C       | VCC       |           |           |           | I/O74 J2  | I/O95 L7  | I/O94 L6 | I/O93 L5 | R        |   |
| T  | I/O167 EX7 | I/O176 GX0 | I/O179 GX3 | I/O181 GX5 |            |            | VCC        | VCC        | N/C        | I/O152 DX0 | I/O131 AX3 | I/O122 P2  | I/O98 M2  | N/C       | VCC       | VCC       |           |           |           | I/O78 J6  | I/O76 J4  | I/O73 J1 | I/O72 J0 | T        |   |
| U  | I/O178 GX2 | I/O180 GX4 | I/O183 GX7 | VCC        |            |            |            |            |            |            |            |            |           |           |           |           |           |           |           | VCC       | I/O80 K0  | I/O77 J5 | I/O75 J3 | U        |   |
| V  | I/O182 GX6 | N/C        | I/O169 FX1 | I/O172 FX4 |            |            |            |            |            |            |            |            |           |           |           |           |           |           |           |           | I/O86 K6  | I/O83 K3 | I/O81 K1 | I/O79 J7 | V |
| W  | I/O168 FX0 | I/O170 FX2 | I/O173 FX5 | GND        | I/O143 BX7 | VCC        | I/O150 CX6 | I/O145 CX1 | VCC        | I/O153 DX1 | I/O123 P3  | VCC        | I/O96 M0  | VCC       | I/O104 N0 | I/O111 N7 | VCC       | I/O119 O7 | GND       | I/O87 K7  | I/O84 K4  | I/O82 K2 | W        |          |   |
| Y  | I/O171 FX3 | I/O174 FX6 | GND        | I/O141 BX5 | I/O138 BX2 | I/O136 BX0 | I/O147 CX3 | I/O158 DX6 | I/O156 DX4 | CLK2       | I/O132 AX4 | I/O121 P1  | I/O125 P5 | I/O99 M3  | I/O101 M5 | I/O106 N2 | I/O110 N6 | I/O115 O3 | I/O118 O6 | GND       | TMS       | I/O85 K5 | Y        |          |   |
| AA | I/O175 FX7 | GND        | I/O142 BX6 | I/O140 BX4 | I/O151 CX7 | I/O149 CX5 | I/O144 CX0 | I/O157 DX5 | I/O154 DX2 | I/O134 AX6 | I/O130 AX2 | I/O128 AX0 | CLK1      | I/O127 P7 | I/O100 M4 | I/O103 M7 | I/O108 N4 | I/O109 N5 | I/O113 O1 | I/O116 O4 | GND       | TCK      | AA       |          |   |
| AB | GND        | N/C        | I/O139 BX3 | I/O137 BX1 | I/O148 CX4 | I/O146 CX2 | I/O159 DX7 | I/O155 DX3 | I/O135 AX7 | I/O133 AX5 | I/O129 AX1 | I/O120 P0  | I/O124 P4 | I/O126 P6 | I/O97 M1  | I/O102 M6 | I/O105 N1 | I/O107 N3 | I/O112 O0 | I/O114 O2 | I/O117 O5 | GND      | AB       |          |   |

#### PIN DESIGNATIONS

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m4a3.512.256\_388bga

# ispMACH 4A PRODUCT ORDERING INFORMATION

## ispMACH 4A Devices Commercial and Industrial - 3.3V and 5V

Lattice programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

|   |                      |                      |                    |                      |                    |                      |                      |                      |  |  |  |  |  |  |  |
|---|----------------------|----------------------|--------------------|----------------------|--------------------|----------------------|----------------------|----------------------|--|--|--|--|--|--|--|
|   | <b>M4A3-</b>         | <b>256 / 128</b>     | <b>-7</b>          | <b>Y</b>             | <b>C</b>           |                      |                      |                      |  |  |  |  |  |  |  |
| <p><b>FAMILY TYPE</b></p> <p>M4A3- = ispMACH 4A Family Low Voltage Advanced Feature (3.3-V <math>V_{CC}</math>)</p> <p>M4A5- = ispMACH 4A Family Advanced Feature (5-V <math>V_{CC}</math>)</p> <p><b>MACROCELL DENSITY</b></p> <table border="0" style="width: 100%;"> <tr> <td>32 = 32 Macrocells</td> <td>192 = 192 Macrocells</td> </tr> <tr> <td>64 = 64 Macrocells</td> <td>256 = 256 Macrocells</td> </tr> <tr> <td>96 = 96 Macrocells</td> <td>384 = 384 Macrocells</td> </tr> <tr> <td>128 = 128 Macrocells</td> <td>512 = 512 Macrocells</td> </tr> </table> <p><b>I/Os</b></p> <p>/32 = 32 I/Os in 44-pin PLCC, 44-pin TQFP or 48-pin TQFP</p> <p>/48 = 48 I/Os in 100-pin TQFP</p> <p>/64 = 64 I/Os in 100-pin TQFP, 100-pin PQFP, or 100-ball caBGA</p> <p>/96 = 96 I/Os in 144-pin TQFP or 144-ball fpBGA</p> <p>/128 = 128 I/Os in 208-pin PQFP, 256-ball BGA or 256-ball fpBGA</p> <p>/160 = 160 I/Os in 208-pin PQFP</p> <p>/192 = 192 I/Os in 256-ball BGA or 256-ball fpBGA</p> <p>/256 = 256 I/Os in 388-ball fpBGA</p> | 32 = 32 Macrocells   | 192 = 192 Macrocells | 64 = 64 Macrocells | 256 = 256 Macrocells | 96 = 96 Macrocells | 384 = 384 Macrocells | 128 = 128 Macrocells | 512 = 512 Macrocells |  |  |  |  |  |  | <p><b>OPERATING CONDITIONS</b></p> <p>C = Commercial (0°C to +70°C)</p> <p>I = Industrial (-40°C to +85°C)</p> <p><b>PACKAGE TYPE</b></p> <p>SA = Ball Grid Array (BGA)</p> <p>J = Plastic Leaded Chip Carrier (PLCC)</p> <p>JN = Lead-free Plastic Leaded Chip Carrier (PLCC)</p> <p>V = Thin Quad Flat Pack (TQFP)</p> <p>VN = Lead-free Thin Quad Flat Pack (TQFP)</p> <p>Y = Plastic Quad Flat Pack (PQFP)</p> <p>YN = Lead-free Plastic Quad Flat Pack (PQFP)</p> <p>FA = Fine-pitch Ball Grid Array (fpBGA)</p> <p>FAN = Lead-free Fine-pitch Ball Grid Array (fpBGA)</p> <p>CA = Chip-array Ball Grid Array (caBGA)</p> <p><b>SPEED</b></p> <p>-5 = 5.0 ns <math>t_{PD}</math></p> <p>-55 = 5.5 ns <math>t_{PD}</math></p> <p>-6 = 6.0 ns <math>t_{PD}</math></p> <p>-65 = 6.5 ns <math>t_{PD}</math></p> <p>-7 = 7.5 ns <math>t_{PD}</math></p> <p>-10 = 10 ns <math>t_{PD}</math></p> <p>-12 = 12 ns <math>t_{PD}</math></p> <p>-14 = 14 ns <math>t_{PD}</math></p> |
| 32 = 32 Macrocells  | 192 = 192 Macrocells |                      |                    |                      |                    |                      |                      |                      |  |  |  |  |  |  |  |
| 64 = 64 Macrocells  | 256 = 256 Macrocells |                      |                    |                      |                    |                      |                      |                      |  |  |  |  |  |  |  |
| 96 = 96 Macrocells  | 384 = 384 Macrocells |                      |                    |                      |                    |                      |                      |                      |  |  |  |  |  |  |  |
| 128 = 128 Macrocells  | 512 = 512 Macrocells |                      |                    |                      |                    |                      |                      |                      |  |  |  |  |  |  |  |

\*Package obsolete, contact factory.

### Conventional Packaging

| 3.3V Commercial Combinations |                                 |              |
|------------------------------|---------------------------------|--------------|
| M4A3-32/32                   | -5, -7, -10                     | JC, VC, VC48 |
| M4A3-64/32                   |                                 | JC, VC, VC48 |
| M4A3-64/64                   |                                 | VC           |
| M4A3-96/48                   | -55, -7, -10                    | VC           |
| M4A3-128/64                  |                                 | YC, VC, CAC  |
| M4A3-192/96                  | -6, -7, -10                     | VC, FAC      |
| M4A3-256/128                 | -55, -65 <sup>1</sup> , -7, -10 | YC, FAC, SAC |
| M4A3-256/160                 |                                 | YC           |
| M4A3-256/192                 | -7, -10                         | FAC          |
| M4A3-384/160                 |                                 | YC           |
| M4A3-384/192                 | -65, -10, -12                   | SAC, FAC     |
| M4A3-512/160                 |                                 | YC           |
| M4A3-512/192                 | -7, -10, -12                    | FAC          |
| M4A3-512/256                 |                                 | FAC          |

| 3.3V Industrial Combinations |               |              |
|------------------------------|---------------|--------------|
| M4A3-32/32                   |               | JI, VI, VI48 |
| M4A3-64/32                   |               | JI, VI, VI48 |
| M4A3-64/64                   |               | VI           |
| M4A3-96/48                   | -7, -10, -12  | VI           |
| M4A3-128/64                  |               | YI, VI, CAI  |
| M4A3-192/96                  |               | VI, FAI      |
| M4A3-256/128                 |               | YI, FAI, SAI |
| M4A3-256/160                 |               | YI           |
| M4A3-256/192                 | -10, -12      | FAI          |
| M4A3-384/160                 |               | YI           |
| M4A3-384/192                 |               | FAI          |
| M4A3-512/160                 | -10, -12, -14 | YI           |
| M4A3-512/192                 |               | FAI          |
| M4A3-512/256                 |               | FAI          |

1. Use 5.5ns for new designs.

| 5V Commercial Combinations |              |              |
|----------------------------|--------------|--------------|
| M4A5-32/32                 | -5, -7, -10, | JC, VC, VC48 |
| M4A5-64/32                 | -55, -7, -10 | JC, VC, VC48 |
| M4A5-96/48                 |              | VC           |
| M4A5-128/64                |              | YC, VC       |
| M4A5-192/96                | -6, -7, -10  | VC           |
| M4A5-256/128               | -65, -7, -10 | YC           |

| 5V Industrial Combinations |              |              |
|----------------------------|--------------|--------------|
| M4A5-32/32                 | -7, -10, -12 | JJ, VI, VI48 |
| M4A5-64/32                 | -7, -10, -12 | JJ, VI, VI48 |
| M4A5-96/48                 |              | VI           |
| M4A5-128/64                |              | YI, VI       |
| M4A5-192/96                | -7, -10, -12 | VI           |
| M4A5-256/128               | -10, -12     | YI           |

## Lead-free Packaging

| 3.3V Commercial Combinations |               |                 |
|------------------------------|---------------|-----------------|
| M4A3-32/32                   | -5, -7, -10   | VNC, VNC48, JNC |
| M4A3-64/32                   | -55, -7, -10  | VNC, VNC48, JNC |
| M4A3-64/64                   |               | VNC             |
| M4A3-128/64                  |               | VNC             |
| M4A3-192/96                  | -6, -7, -10   | VNC             |
| M4A3-256/128                 | -55, -7, -10  | FANC, YNC       |
| M4A3-256/160                 | -7, -10       | YNC             |
| M4A3-256/192                 |               | FANC            |
| M4A3-384/192                 | -65, -10, -12 | FANC            |
| M4A3-512/192                 | -7, -10, -12  | FANC            |

| 3.3V Industrial Combinations |               |                 |
|------------------------------|---------------|-----------------|
| M4A3-32/32                   | -7, -10, -12  | VNI, VNI48, JNI |
| M4A3-64/32                   |               | VNI, VNI48, JNI |
| M4A3-64/64                   |               | VNI             |
| M4A3-128/64                  |               | VNI             |
| M4A3-192/96                  | -10, -12      | VNI             |
| M4A3-256/128                 |               | FANI, YNI       |
| M4A3-256/160                 |               | YNI             |
| M4A3-256/192                 | -10, -12, -14 | FANI            |
| M4A3-384/192                 |               | FANI            |
| M4A3-512/192                 |               | FANI            |

| 5V Commercial Combinations |              |                 |
|----------------------------|--------------|-----------------|
| M4A5-32/32                 | -5, -7, -10  | VNC, VNC48, JNC |
| M4A5-64/32                 | -55, -7, -10 | VNC, VNC48, JNC |
| M4A5-96/48                 |              | VNC             |
| M4A5-128/64                |              | VNC, YNC        |
| M4A5-192/96                | -6, -7, -10  | VNC             |
| M4A5-256/128               | -65, -7, -10 | YNC             |

| 5V Industrial Combinations |              |                 |
|----------------------------|--------------|-----------------|
| M4A5-32/32                 | -7, -10, -12 | VNI, VNI48, JNI |
| M4A5-64/32                 |              | VNI, VNI48, JNI |
| M4A5-96/48                 |              | VNI             |
| M4A5-128/64                |              | VNI, YNI        |
| M4A5-192/96                |              | VNI             |
| M4A5-256/128               |              | YNI             |

Most ispMACH devices are dual-marked with both Commercial and Industrial grades. The Industrial speed grade is slower, i.e., M4A3-256/128-7YC-10YI

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.

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## Revision History

| Date           | Version | Change Summary  |
|----------------|---------|---|
| -              | K       | Previous Lattice release.                             |
| August 2006    | L       | Updated for lead-free package options.                |
| September 2006 | M       | Revised M4A3-256/160 208-pin PQFP connection diagram. |