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New 8FX 8-bit Microcontrollers

The MB95710M/770M Series is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of this series contain a variety of peripheral resources.

Features

- F²MC-8FX CPU core
 - □ Instruction set optimized for controllers
 - · Multiplication and division instructions
 - · 16-bit arithmetic operations
 - · Bit test branch instructions
 - · Bit manipulation instructions, etc.

■ Clock

- □ Selectable main clock source
 - Main oscillation clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
 - External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
 - Main CR clock (4 MHz ±2%)
 - · Main CR PLL clock
 - The main CR PLL clock frequency becomes $8\,\text{MHz}\,\pm2\%$ when the PLL multiplication rate is 2.
 - The main CR PLL clock frequency becomes 10 MHz $\pm 2\%$ when the PLL multiplication rate is 2.5.
 - The main CR PLL clock frequency becomes 12 MHz $\pm 2\%$ when the PLL multiplication rate is 3.
 - The main CR PLL clock frequency becomes 16 MHz $\pm 2\%$ when the PLL multiplication rate is 4.
 - •Main PLL clock (up to 16.25 MHz, maximum machine clock frequency: 16.25 MHz)
- □ Selectable subclock source
 - · Suboscillation clock (32.768 kHz)
 - External clock (32.768 kHz)
 - Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 150 kHz)

■ Timer

- □ 8/16-bit composite timer × 2 channels
- □ 8/16-bit PPG × 2 channels
- □ 16-bit reload timer × 1 channel
- □ Event counter × 1 channel
- ☐ Time-base timer × 1 channel
- □ Watch counter × 1 channel
- □ Watch prescaler × 1 channel
- UART/SIO × 3 channels
 - □ Full duplex double buffer
 - Capable of clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer
- I²C bus interface × 1 channel
 - Built-in wake-up function
- External interrupt × 8 channels

- Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
- Can be used to wake up the device from different low power consumption (standby) modes
- 8/12-bit A/D converter × 8 channels
 - 8-bit or 12-bit resolution can be selected.
- LCD controller (LCDC)
 - On MB95F714J/F714M/F716J/F716M/F718J/F718M, LCD output can be selected from 40 SEG × 4 COM and 36 SEG × 8 COM.
 - $\hfill \square$ On MB95F774J/F774M/F776J/F776M/F778J/F778M, LCD output can be selected from 32 SEG \times 4 COM and 28 SEG \times 8 COM.
 - $exttt{ in}$ Internal divider resistor whose resistance value can be selected from 10 k $exttt{ in}$ or 100 k $exttt{ in}$ through software
 - Interrupt in sync with the LCD module frame frequency
 - Blinking function
 - Inverted display function
- Low power consumption (standby) modes
 - There are four standby modes as follows:
 - Stop mode
 - Sleep mode
 - · Watch mode
 - · Time-base timer mode

■ I/O port

- MB95F714J/F716J/F718J (number of I/O ports: 75)
 - General-purpose I/O ports (CMOS I/O): 71
- General-purpose I/O ports (N-ch open drain): 4
- □ MB95F714M/F716M/F718M (number of I/O ports: 74)
- General-purpose I/O ports (CMOS I/O): 71
- General-purpose I/O ports (N-ch open drain): 3
- □ MB95F774J/F776J/F778J (number of I/O ports: 59)
 - General-purpose I/O ports (CMOS I/O): 55
 - · General-purpose I/O ports (N-ch open drain): 4
- ☐ MB95F774M/F776M/F778M (number of I/O ports: 58)
 - General-purpose I/O ports (CMOS I/O): 55
- General-purpose I/O ports (N-ch open drain): 3
- On-chip debug
 - □ 1-wire serial control
 - ☐ Serial writing supported (asynchronous mode)
- Hardware/software watchdog timer
 - Built-in hardware watchdog timer
 - □ Built-in software watchdog timer
- Power-on reset
 - A power-on reset is generated when the power is switched on.

Revised September 29, 2017



- Low-voltage detection (LVD) circuit (only available on MB95F714J/F716J/F718J/F774J/F776J/F778J)
 - □ Built-in low-voltage detection function
- Comparator × 1 channel
- Clock supervisor counter
 - □ Built-in clock supervisor counter

- Dual operation Flash memory
 - ☐ The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.
- Flash memory security function
 - □ Protects the content of the Flash memory.

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MB95710M Series MB95770M Series



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1. Product Line-up

1.1 MB95710M Series

Part number	Series									
	MB95F714J	MB95F716J	MB95F718J	MB95F714M	MB95F716M	MB95F718M				
Parameter		2001 7 700	2001 7 700		2001 1 10					
Туре			Flash mem	ory product						
Clock			1 14011 1110111	ory product						
	It supervises the	supervises the main clock oscillation and the subclock oscillation.								
Flash memory capacity	20 Kbyte	36 Kbyte	60 Kbyte	20 Kbyte	36 Kbyte	60 Kbyte				
RAM capacity	512 bytes	1 Kbyte	2 Kbyte	512 bytes	1 Kbyte	2 Kbyte				
Power-on reset			Ye	es						
Low-voltage detection reset		Yes			No					
Reset input	Sele	cted through soft	ware	With	dedicated reset	input				
CPU functions	Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8 and 16 bits Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)									
General- purpose I/O	I/O portCMOS I/ON-ch open drai	: 75 : 71 n : 4		I/O portCMOS I/ON-ch open dra	: 74 : 71 in : 3					
Time-base timer	Interval time: 0.2	56 ms to 8.3 s (e	xternal clock freq	uency = 4 MHz)						
	The sub-CR clean	on clock at 10 MF ock can be used	as the source clo	ock of the softwar	e watchdog timer	:				
		replace 3 bytes	of data.							
0/12 510	8 channels									
		solution can be se	elected.							
	2 channels									
8/16-bit composite timer	 It has the follow function. 	can be selected t	erval timer functi	on, PWC functior	n, PWM function a	and input capture				
	8 channels									
External interrupt		ge detection (The		•	-	selected.)				
On-chip debug	1-wire serial coIt supports seri	ontrol al writing (asynch	nronous mode).							



Vart number ■											
	MB95F714J	MB95F716J	MB95F718J	MB95F714M	MB95F716M	MB95F718M					
Parameter	2001 7 7 10	2001 7 100	200. 7 100			2001 7 10					
i didilietei	3 channels										
UART/SIO	 Data transfer w It has a full duperand an error de It uses the NR2 LSB-first data to 										
	1 channel										
l ² C bus interface	 It has the follow 	ansmission and i ving functions: bu -up function, and		arbitration functio erating and detec	n, transmission d ting repeated ST	irection detection ART conditions.					
	2 channels										
8/16-bit PPG			n "8-bit timer \times 2 n be selected from			nannel".					
	1 channel										
16-bit reload timer	It can output soCount clock: it	quare wave. can be selected t	ter operating mod from internal cloc reload mode and	ks (seven types)		cks.					
Event counter	posite timer ch	. 1. nt counter functio				and 8/16-bit com- posite timer ch. 1					
LCD controller (LCDC)	 SEG output: 36 If the number maximum nu If the number maximum nu 	 COM output: 4 or 8 (max) (selectable) SEG output: 36 or 40 (max) (selectable) If the number of COM outputs is 4, the maximum number of SEG outputs is 40, and the maximum number of pixels that can be displayed 160 (4 × 40). If the number of COM outputs is 8, the maximum number of SEG outputs is 36, and the maximum number of pixels that can be displayed 288 (8 × 36). LCD drive power supply (bias) pins: 5 (max) 									
	 Duty LCD mode LCD standby mode Blinking function Internal divider resistor whose resistance value can be selected from 10 kΩ or 100 kΩ through software Interrupt in sync with the LCD module frame frequency Inverted display function 										
Watch counter	 Count clock: four selectable clock sources (125 ms, 250 ms, 500 ms or 1 s) The counter value can be selected from 0 to 63. (The watch counter can count for one minute when the clock source is one second and the counter value is set to 60.) 										
Watch prescaler	Eight different tin	ne intervals can b	oe selected.								
Comparator	1 channel										



Part number Parameter	MB95F714J	MB95F716J	MB	95F718J	MB95	5F714M	MB95F7 ²	16M	MB95F718M	
Flash memory	It has a flag in Flash security	uspend/erase-resume commands. thas a flag indicating the completion of the operation of Embedded Algorithm. lash security feature for protecting the content of the Flash memory								
	Number of program/erase cycle Data retention time			1000 20 years		years	100000 5 years	1		
						ycars	o years	J		
Standby mode	There are four standby modes as follows: • Stop mode • Sleep mode • Watch mode • Time-base timer mode									
Package		LQH080								



1.2 MB95770M Series

1.2 MB95//0M											
Part number	MB95F774J	MB95F776J	MB95F778J	MB95F774M	MB95F776M	MB95F778M					
Parameter											
Туре		Flash memory product									
Clock supervisor counter	It supervises the	main clock oscill	ation and the sub	oclock oscillation.							
Flash memory capacity	20 Kbyte	36 Kbyte	60 Kbyte	20 Kbyte	36 Kbyte	60 Kbyte					
RAM capacity	512 bytes	1 Kbyte	2 Kbyte	512 bytes	1 Kbyte	2 Kbyte					
Power-on reset			Ye	es							
Low-voltage detection reset		Yes			No						
Reset input	Sele	cted through soft	ware		Dedicated						
CPU functions	Number of basic instructions Instruction bit length Instruction length										
General- purpose I/O	I/O portCMOS I/ON-ch open drai	• CMOS I/O : 55 • CMOS I/O : 55									
Time-base timer	Interval time: 0.2	56 ms to 8.3 s (e	xternal clock fred	uency = 4 MHz)							
Hardware/ software watchdog timer	 Reset generati Main oscillation The sub-CR classifier 	on clock at 10 MF		ock of the softwar	e watchdog timer						
Wild register	It can be used to	replace 3 bytes	of data.								
8/12-bit	8 channels										
A/D converter	8-bit or 12-bit res	solution can be se	elected.								
	2 channels										
8/16-bit composite timer	 The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". It has the following functions: interval timer function, PWC function, PWM function and input capture function. Count clock: it can be selected from internal clocks (seven types) and external clocks. It can output square wave. 										
Externel	8 channels										
External interrupt				ing edge, and bot ent standby mode		selected.)					
On-chip debug	1-wire serial coIt supports serial	ontrol ial writing (asynch	nronous mode).								



─ Part number												
	MB95F774J	MB95F776J	MB95F778J	MB95F774M	MB95F776M	MB95F778M						
Parameter												
r drameter	3 channels											
UART/SIO	 Data transfer w It has a full duper and an error de It uses the NR2 LSB-first data 	Data transfer with UART/SIO is enabled. It has a full duplex double buffer, variable data length (5/6/7/8 bits), an internal baud rate generator and an error detection function. It uses the NRZ type transfer format. LSB-first data transfer and MSB-first data transfer are available to use. Both clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer are enabled.										
	1 channel											
I ² C bus interface	 It has the follow 	Master/slave transmission and reception It has the following functions: bus error function, arbitration function, transmission direction detection function, wake-up function, and functions of generating and detecting repeated START conditions.										
	2 channels											
8/16-bit PPG		Each channel can be used as an "8-bit timer \times 2 channels" or a "16-bit timer \times 1 channel". The counter operating clock can be selected from eight clock sources.										
	1 channel											
16-bit reload timer	It can output soCount clock: it	quare wave. can be selected	ter operating mod from internal cloc reload mode and	ks (seven types)		cks.						
Event counter	posite timer ch	. 1. nt counter functio				and 8/16-bit com- posite timer ch. 1						
LCD controller (LCDC)	 SEG output: 28 If the number maximum nu If the number maximum nu 	 COM output: 4 or 8 (max) (selectable) SEG output: 28 or 32 (max) (selectable) If the number of COM outputs is 4, the maximum number of SEG outputs is 32, and the maximum number of pixels that can be displayed 128 (4 × 32). If the number of COM outputs is 8, the maximum number of SEG outputs is 28, and the maximum number of pixels that can be displayed 224 (8 × 28). LCD drive power supply (bias) pins: 4 (max) 										
	 Duty LCD mode LCD standby mode Blinking function Internal divider resistor whose resistance value can be selected from 10 kΩ or 100 kΩ through software Interrupt in sync with the LCD module frame frequency Inverted display function 											
Watch counter	 Count clock: four selectable clock sources (125 ms, 250 ms, 500 ms or 1 s) The counter value can be selected from 0 to 63. (The watch counter can count for one minute when the clock source is one second and the counter value is set to 60.) 											
Watch prescaler	Eight different tin	ne intervals can b	oe selected.									
Comparator	1 channel											



Part number Parameter	MB95F774J	MB95F776J	MBS	95F778J	MB95F	774M	MB95F7	76M	MB95F778M	
Flash memory	 It supports automatic programming (Embedded Algorithm), and program/erase/erase suspend/erase-resume commands. It has a flag indicating the completion of the operation of Embedded Algorithm. Flash security feature for protecting the content of the Flash memory Number of program/erase cycles 1000 10000 									
		Data retention time 20 years 10 years 5 years						}		
Standby mode	Stop modeSleep modeWatch mode	Sleep mode								
Package		LQD064 LQG064								

2. Packages And Corresponding Products

Part number Package	MB95F714J	MB95F716J	MB95F718J	MB95F714M	MB95F716M	MB95F718M
LQH080	О	О	O	O	О	O

Part number Package	MB95F774J	MB95F776J	MB95F778J	MB95F774M	MB95F776M	MB95F778M
LQD064	О	О	О	О	О	О
LQG064	0	О	О	О	О	O

O: Available



3. Differences Among Products And Notes On Product Selection

Current consumption

When using the on-chip debug function, take account of the current consumption of Flash memory program/erase. For details of current consumption, see "Electrical Characteristics".

Package

For details of information on each package, see "Packages And Corresponding Products" and "Package Dimension".

· Operating voltage

The operating voltage varies, depending on whether the on-chip debug function is used or not. For details of operating voltage, see "Electrical Characteristics".

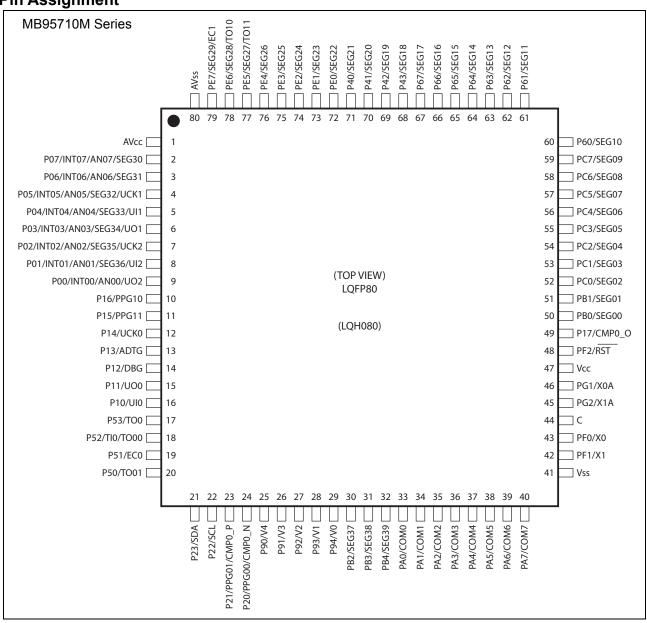
· On-chip debug function

The on-chip debug function requires that Vcc, Vss and one serial wire be connected to an evaluation tool. For details of the connection method, refer to "CHAPTER 26 EXAMPLE OF SERIAL PROGRAMMING CONNECTION" in "New 8FX MB95710M/770M Series Hardware Manual".

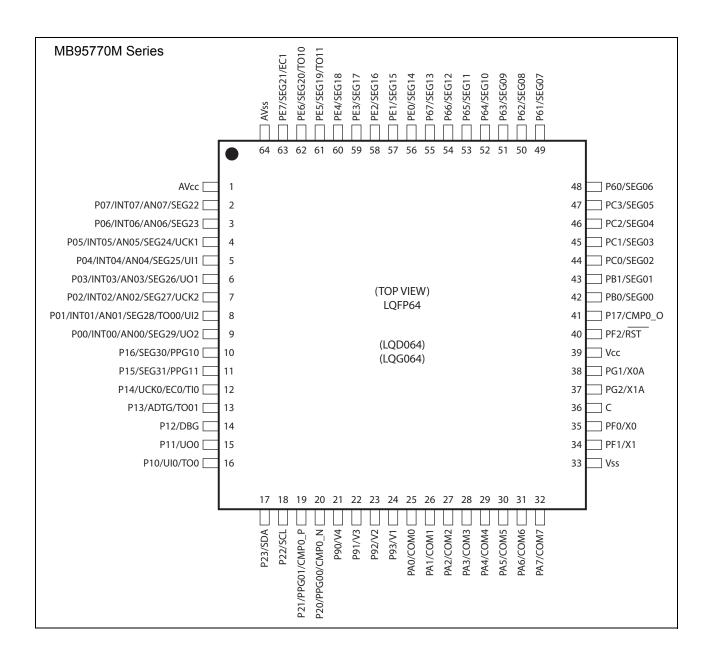
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4. Pin Assignment









5. Pin Functions (MB95710M Series)

Di	D:	I/O circuit	Function		I/O type		
Pin no.	Pin name	type*1	Function	Input	Output	OD*2	PU*3
1	AVcc		Power supply pin for 8/12-bit A/D converter and comparator	_	_	_	_
	P07		General-purpose I/O port				
2	INT07	S	External interrupt input pin	Hysteresis/	CMOS/		
2	AN07	3	8/12-bit A/D converter analog input pin	analog	LCD		
	SEG30		LCDC SEG30 output pin				
	P06		General-purpose I/O port				
3	INT06	S	External interrupt input pin	Hysteresis/	CMOS/		
3	AN06	3	8/12-bit A/D converter analog input pin	analog	LCD		
	SEG31		LCDC SEG31 output pin				
	P05		General-purpose I/O port				
	INT05		External interrupt input pin] <i>.</i>	0.100/	_	
4	AN05	S	8/12-bit A/D converter analog input pin	Hysteresis/ analog	CMOS/ LCD		_
	SEG32		LCDC SEG32 output pin	analog			
	UCK1		UART/SIO ch. 1 clock I/O pin	1			
	P04		General-purpose I/O port				
	INT04		External interrupt input pin				
5	AN04	V	8/12-bit A/D converter analog input pin	CMOS/ analog	CMOS/ LCD	_	
	SEG33		LCDC SEG33 output pin	andiog	LOD		
	UI1		UART/SIO ch. 1 data input pin				
	P03		General-purpose I/O port				
	INT03		External interrupt input pin	1	CMOS/ LCD		
6	AN03	S	8/12-bit A/D converter analog input pin	Hysteresis/ analog		_	
	SEG34		LCDC SEG34 output pin	analog	LOD		
	UO1		UART/SIO ch. 1 data output pin				
	P02		General-purpose I/O port				
	INT02		External interrupt input pin	1			
7	AN02	S	8/12-bit A/D converter analog input pin	Hysteresis/ analog	CMOS/ LCD	_	_
	SEG35		LCDC SEG35 output pin	analog	LOD		
	UCK2		UART/SIO ch. 2 clock I/O pin				
	P01		General-purpose I/O port				
	INT01		External interrupt input pin	1			
8	AN01	V	8/12-bit A/D converter analog input pin	CMOS/ analog	CMOS/ LCD	_	_
	SEG36		LCDC SEG36 output pin	anaiog	LOD		
	UI2		UART/SIO ch. 2 data input pin	1			



Din no	D:	I/O circuit	Function		I/O type				
Pin no.	Pin name	type*1	Function	Input	Output	OD*2	PU*3		
	P00		General-purpose I/O port						
	INT00	147	External interrupt input pin	Hysteresis/	CMOS/				
9	AN00	W	8/12-bit A/D converter analog input pin	analog	LCD		_		
	UO2		UART/SIO ch. 2 data output pin						
40	P16	.,	General-purpose I/O port	Livetanasia	CMCC				
10	PPG10	Y	8/16-bit PPG ch. 1 output pin	Hysteresis	CMOS				
44	P15	Y	General-purpose I/O port	Liveteresia	01400				
11	PPG11	Y	8/16-bit PPG ch. 1 output pin	Hysteresis	CMOS	_	_		
40	P14	1.1	General-purpose I/O port	Livetanasia	CMCC				
12	UCK0	Н	UART/SIO ch. 0 clock I/O pin	Hysteresis	CMOS	_	О		
40	P13	11	General-purpose I/O port	Liveteresia	CMOC		0		
13	ADTG	Н	8/12-bit A/D converter trigger input pin	Hysteresis	CMOS		О		
14	P12	D	General-purpose I/O port	Lluctoropio	Hysteresis	CMOS	О		
14	DBG	D	DBG input pin	пузістезіз	CIVIOS				
15	P11	Н	General-purpose I/O port	Llyotoropio	CMOS		0		
15	UO0	П	UART/SIO ch. 0 data output pin	Hysteresis	CIVIOS		U		
16	P10	G	General-purpose I/O port	CMOS	CMOS		О		
10	UI0	G	UART/SIO ch. 0 data input pin	CIVIOS	CIVIOS		U		
17	P53	Н	General-purpose I/O port	Hysteresis	CMOS				О
17	TO0	11	16-bit reload timer ch. 0 output pin	Trysteresis					
	P52		General-purpose I/O port						
18	TI0	Н	16-bit reload timer ch. 0 input pin	Hysteresis	CMOS	_	О		
	TO00		8/16-bit composite timer ch. 0 output pin						
	P51		General-purpose I/O port						
19	EC0	Н	8/16-bit composite timer ch. 0 clock input pin	Hysteresis	CMOS		О		
20	P50	Н	General-purpose I/O port	Hysteresis	CMOS		О		
20	TO01	11	8/16-bit composite timer ch. 0 output pin	Trysteresis	OWO		O		
21	P23	ı	General-purpose I/O port	CMOS	CMOS	О			
21	SDA	•	I ² C bus interface ch. 0 data I/O pin	OWICO	OWO	O			
22	P22	ı	General-purpose I/O port	CMOS	CMOS	О			
	SCL	'	I ² C bus interface ch. 0 clock I/O pin	CIVIOO	3,4100				
	P21		General-purpose I/O port						
23	PPG01	Т	8/16-bit PPG ch. 0 output pin	Hysteresis/	CMOS	_	О		
	CMP0_P	•	Comparator ch. 0 non-inverting analog input (positive input) pin	analog	CIVIOS		,		



D'	D:	I/O circuit	F		I/O type		
Pin no.	Pin name	type*1	Function	Input	Output	CMOS/LCD power supply CMOS/LCD cmos/L	PU*3
	P20		General-purpose I/O port				
24	PPG00	Т	8/16-bit PPG ch. 0 output pin	Hysteresis/	CMOS		О
24	CMP0_N	ı	Comparator ch. 0 inverting analog input (negative input) pin	analog	CIVIOO		
	P90		General-purpose I/O port	Hysteresis/	CMOS/		
25	V4	R	LCD drive power supply pin	LCD power supply	LCD power supply		_
	P91		General-purpose I/O port	Hysteresis/	CMOS/		
26	V3	R	LCD drive power supply pin	LCD power supply	LCD power supply		
	P92		General-purpose I/O port	Hysteresis/	CMOS/		
27	V2	R	LCD drive power supply pin	LCD power supply	power supply	_	_
	P93		General-purpose I/O port	Hysteresis/	CMOS/		
28	V1	R	LCD drive power supply pin	LCD power supply	LCD power supply		_
	P94		General-purpose I/O port	Hysteresis/	, CMOS/		
29	V0	R	LCD drive power supply pin	LCD power supply	LCD power supply		_
30	PB2	M	General-purpose I/O port	Hysteresis	CMOS/		
30	SEG37	IVI	LCDC SEG37 output pin	Trysteresis	LCD		
31	PB3	M	General-purpose I/O port	Hysteresis	CMOS/		
5	SEG38	IVI	LCDC SEG38 output pin	Trysteresis	LCD		
32	PB4	M	General-purpose I/O port	Hysteresis	CMOS/		
02	SEG39	171	LCDC SEG39 output pin	Tryotorcolo	LCD		
33	PA0	M	General-purpose I/O port	Hysteresis	CMOS/		
33	COM0	IVI	LCDC COM0 output pin	Trysteresis	LCD		
34	PA1	M	General-purpose I/O port	Hysteresis	CMOS/		
	COM1	171	LCDC COM1 output pin	nysieresis	LCD		
35	PA2	M	General-purpose I/O port	Hysteresis	CMOS/		
	COM2	.,,	LCDC COM2 output pin	1 IYSICICSIS	LCD		
36	PA3	M	General-purpose I/O port	Hysteresis	CMOS/	_	_
	COM3	•••	LCDC COM3 output pin	11,510.0010	LCD		
37	PA4	M	General-purpose I/O port	Hysteresis	CMOS/		_
	COM4		LCDC COM4 output pin	,	LCD		



		I/O circuit			I/O type		
Pin no.	Pin name	type*1	Function	Input	Output	OD*2	PU*3
38	PA5	M	General-purpose I/O port	Lluotorogio	CMOS/		
30	COM5	IVI	LCDC COM5 output pin	Hysteresis	LCD	_	_
39	PA6	M	General-purpose I/O port	Lluotorogia	CMOS/		
39	COM6	IVI	LCDC COM6 output pin	Hysteresis	LCD		
40	PA7	M	General-purpose I/O port	Hyetorocie	CMOS/		
40	COM7	IVI	LCDC COM7 output pin	Hysteresis	LCD		
41	Vss		Power supply pin (GND)	_		_	_
42	PF1	В	General-purpose I/O port	Hysteresis	CMOS		
42	X1	Ь	Main clock I/O oscillation pin	Hysteresis	CIVIOS		
43	PF0	В	General-purpose I/O port	Hysteresis	CMOS		
43	X0	ь	Main clock input oscillation pin	Trysteresis	CIVIOS		
44	С		Decoupling capacitor connection pin	_		_	_
45	PG2	С	General-purpose I/O port	Lluotorogia	CMOS		0
45	X1A	C	Subclock I/O oscillation pin	Hysteresis	CMOS		О
46	PG1	С	General-purpose I/O port	Hyptoropio	CMOS		О
40	X0A	C	Subclock input oscillation pin	Hysteresis	CIVIOS		U
47	Vcc	_	Power supply pin	_	_	_	_
	PF2		General-purpose I/O port				
48	RST	Α	Reset pin Dedicated reset pin on MB95F714M/F716M/F718M	Hysteresis	CMOS	О	_
40	P17	1.1	General-purpose I/O port	I locata na alia			
49	CMP0_O	Н	Comparator ch. 0 digital output pin	Hysteresis	CMOS	—	О
50	PB0	M	General-purpose I/O port	Llyotoropio	CMOS/		
50	SEG00	IVI	LCDC SEG00 output pin	Hysteresis	LCD		
51	PB1	M	General-purpose I/O port	Hysteresis	CMOS/		
51	SEG01	IVI	LCDC SEG01 output pin	Tiysteresis	LCD		
52	PC0	M	General-purpose I/O port	Hysteresis	CMOS/		
52	SEG02	IVI	LCDC SEG02 output pin	Tiyateresis	LCD		
53	PC1	M	General-purpose I/O port	Hysteresis	CMOS/		
33	SEG03	IVI	LCDC SEG03 output pin	Trystorosis	LCD		
54	PC2	M	General-purpose I/O port	Hysteresis	CMOS/		
J-7	SEG04	141	LCDC SEG04 output pin		LCD		
55	PC3	M	General-purpose I/O port	Hysteresis	CMOS/	_	
	SEG05	171	LCDC SEG05 output pin	nysieresis	LCD		
56	PC4	M	General-purpose I/O port	Hysteresis	CMOS/	_	_
90	SEG06		LCDC SEG06 output pin	. 17 0101 0010	LCD		



D'	D'	I/O circuit	Forestina		I/O type		
Pin no.	Pin name	type*1	Function	Input	Output	OD*2	PU*3
57	PC5	M	General-purpose I/O port	Llyotoropio	CMOS/		
57	SEG07	IVI	LCDC SEG07 output pin	Hysteresis	LCD	_	
58	PC6	М	General-purpose I/O port	Lluctoropio	CMOS/		
56	SEG08	IVI	LCDC SEG08 output pin	Hysteresis	LCD	_	
59	PC7	M	General-purpose I/O port	Lluctoropio	CMOS/		
59	SEG09	IVI	LCDC SEG09 output pin	Hysteresis	LCD	_	
60	P60	M	General-purpose I/O port	Hysteresis	CMOS/		
60	SEG10	IVI	LCDC SEG10 output pin	пузістезіз	LCD	_	
61	P61	M	General-purpose I/O port	Lluctorooio	CMOS/		
01	SEG11	M	LCDC SEG11 output pin	Hysteresis	LCD	_	
62	P62	M	General-purpose I/O port	Llyotoropio	CMOS/		
02	SEG12	IVI	LCDC SEG12 output pin	Hysteresis	LCD	_	
63	P63	M	General-purpose I/O port	Llyotoropio	CMOS/		
03	SEG13	IVI	LCDC SEG13 output pin	Hysteresis	LCD	_	
64	P64	NA	General-purpose I/O port	- Hysteresis	CMOS/		
64	SEG14	M	LCDC SEG14 output pin		LCD		
G.E.	65 P65	NA	General-purpose I/O port	Lluctoropio	CMOS/	_	
00	SEG15	M	LCDC SEG15 output pin	Hysteresis	LCD		
66	P66	M	General-purpose I/O port	Llyotoropio	CMOS/		
00	SEG16	IVI	LCDC SEG16 output pin	Hysteresis	LCD		
67	P67	M	General-purpose I/O port	Llyotoropio	CMOS/		
07	SEG17	IVI	LCDC SEG17 output pin	Hysteresis	LCD	_	
68	P43	M	General-purpose I/O port	Llyotoropio	CMOS/		
00	SEG18	IVI	LCDC SEG18 output pin	Hysteresis	LCD	_	
69	P42	М	General-purpose I/O port	Llyotoropio	CMOS/		
09	SEG19	IVI	LCDC SEG19 output pin	Hysteresis	LCD	_	
70	P41	М	General-purpose I/O port	Llyotoropio	CMOS/		
70	SEG20	IVI	LCDC SEG20 output pin	Hysteresis	LCD	_	
71	P40	М	General-purpose I/O port	Llyotoropio	CMOS/		
7 1	SEG21	IVI	LCDC SEG21 output pin	Hysteresis	LCD	_	_
72	PE0	М	General-purpose I/O port	Hysteresis	CMOS/		
1 4	SEG22	IVI	LCDC SEG22 output pin		LCD	_	
72	PE1	Ŋ.A	General-purpose I/O port	Llyotoroois	CMOS/		
73	SEG23	M	LCDC SEG23 output pin	Hysteresis	LCD		
74	PE2	N 4	General-purpose I/O port	Llyotoroois	CMOS/		
74	SEG24	M	LCDC SEG24 output pin	Hysteresis	LCD		



Din no	Din nama	I/O circuit	Function		I/O type		
PIII IIO.	Pin no. Pin name	type*1	Function	Input	Output	OD*2	PU*3
75	PE3	M	General-purpose I/O port	Hysteresis	CMOS/		
7.5	SEG25	IVI	LCDC SEG25 output pin		LCD		
76	PE4	M	General-purpose I/O port	Hyetoroeie	CMOS/		
70	SEG26	IVI	LCDC SEG26 output pin	Hysteresis	LCD		
	PE5		General-purpose I/O port				
77	SEG27	M	LCDC SEG27 output pin	Hysteresis	CMOS/ LCD		
	TO11		8/16-bit composite timer ch. 1 output pin				
	PE6		General-purpose I/O port	Hysteresis	01400/		
78	SEG28	M	LCDC SEG28 output pin		CMOS/ LCD		
	TO10		8/16-bit composite timer ch. 1 output pin		LOD		
	PE7		General-purpose I/O port				
79	SEG29	М	LCDC SEG27 output pin	Hysteresis	CMOS/		
	EC1	•••	8/16-bit composite timer ch. 1 clock input pin	11901010010	LCD	, — , —	
80	AVss	_	Power supply pin (GND) for 8/12-bit A/D converter and comparator	_	_	_	—

O: Available

^{*1:} For the I/O circuit types, see "I/O Circuit Type".

^{*2:} N-ch open drain

^{*3:} Pull-up



6. Pin Functions (MB95770M Series)

		I/O circuit			I/O type			
Pin no.	Pin name	type*1	Function	Input	Output	OD*2	PU*3	
1	AVcc	_	Power supply pin for 8/12-bit A/D converter and comparator	_	_	_	_	
	P07		General-purpose I/O port					
2	INT07	S	External interrupt input pin	Hysteresis/	CMOS/			
۷	AN07	3	8/12-bit A/D converter analog input pin	analog	LCD			
	SEG22		LCDC SEG22 output pin					
	P06		General-purpose I/O port					
3	INT06	S	External interrupt input pin	Hysteresis/	CMOS/			
3	AN06	3	8/12-bit A/D converter analog input pin	analog	LCD		_	
	SEG23		LCDC SEG23 output pin					
	P05		General-purpose I/O port					
	INT05		External interrupt input pin	Hysteresis/ analog	0.100/	_		
4	AN05	S	8/12-bit A/D converter analog input pin		CMOS/ LCD		_	
	SEG24		LCDC SEG24 output pin		LOD			
	UCK1		UART/SIO ch. 1 clock I/O pin					
	P04		General-purpose I/O port					
	INT04		External interrupt input pin					
5	AN04	V	8/12-bit A/D converter analog input pin	CMOS/ analog	CMOS/ LCD	_	_	
	SEG25		LCDC SEG25 output pin		LOD			
	UI1		UART/SIO ch. 1 data input pin					
	P03		General-purpose I/O port					
	INT03		External interrupt input pin	l	0.100/			
6	AN03	S	8/12-bit A/D converter analog input pin	Hysteresis/ analog	CMOS/ LCD	_	_	
	SEG26		LCDC SEG26 output pin	analog	LOD			
	UO1		UART/SIO ch. 1 data output pin					
	P02		General-purpose I/O port					
	INT02		External interrupt input pin	l	0.100/			
7	AN02	S	8/12-bit A/D converter analog input pin	Hysteresis/ analog	CMOS/ LCD	_	_	
	SEG27		LCDC SEG27 output pin	analog	LOD			
	UCK2		UART/SIO ch. 2 clock I/O pin					
	P01		General-purpose I/O port					
	INT01		External interrupt input pin					
0	AN01	\/	8/12-bit A/D converter analog input pin	CMOS/	CMOS/			
8	SEG28	V	LCDC SEG28 output pin	analog	LCD	_	_	
	TO00		8/16-bit composite timer ch. 0 output pin]				
	UI2		UART/SIO ch. 2 data input pin	1				



D'-	D'	I/O circuit	F 17		I/O type		
Pin no.	Pin name	type*1	Function	Input	Output	OD*2	PU*3
	P00		General-purpose I/O port				
	INT00		External interrupt input pin	l			
9	AN00	S	8/12-bit A/D converter analog input pin	Hysteresis/ analog	CMOS/ LCD	_	_
	SEG29		LCDC SEG29 output pin	analog	LOD		
	UO2		UART/SIO ch. 2 data output pin				
	P16		General-purpose I/O port				
10	SEG30	М	LCDC SEG30 output pin	Hysteresis	CMOS/ LCD		
	PPG10		8/16-bit PPG ch. 1 output pin		LOD		
	P15		General-purpose I/O port				
11	SEG31	М	LCDC SEG31 output pin	Hysteresis	CMOS/ LCD	_	_
	PPG11		8/16-bit PPG ch. 1 output pin		LCD		
	P14		General-purpose I/O port			_	
	UCK0		UART/SIO ch. 0 clock I/O pin				
12	EC0	Н	8/16-bit composite timer ch. 0 clock input	Hysteresis	CMOS		О
	ECU		pin				
	TI0		16-bit reload timer ch. 0 input pin				
	P13		General-purpose I/O port		CMOS	_	
13	ADTG	Н	8/12-bit A/D converter trigger input pin	Hysteresis			О
	TO01		8/16-bit composite timer ch. 0 output pin				
14	P12	D	General-purpose I/O port	- Hysteresis	CMOS	О	
14	DBG	D	DBG input pin	Trysteresis	CIVIOS		
15	P11	Н	General-purpose I/O port	Llyotoropio	CMOS		О
15	UO0	П	UART/SIO ch. 0 data output pin	Hysteresis	CIVIOS		
	P10		General-purpose I/O port				
16	UI0	G	UART/SIO ch. 0 data input pin	CMOS	CMOS	_	О
	TO0		16-bit reload timer ch. 0 output pin				
17	P23	ı	General-purpose I/O port	CMOS	CMOS	О	
17	SDA	I	I ² C bus interface ch. 0 data I/O pin	CIVIOS	CIVIOS	U	
10	P22	ı	General-purpose I/O port	CMOS	CMOS	0	
18	SCL	I	I ² C bus interface ch. 0 clock I/O pin	CMOS	CMOS	О	
	P21		General-purpose I/O port				
19	PPG01	Т	8/16-bit PPG ch. 0 output pin	Hysteresis/	CMOS		О
19	CMP0_P	ľ	Comparator ch. 0 non-inverting analog input (positive input) pin	analog	CIVIOO		
	P20		General-purpose I/O port				
20	PPG00	Т	8/16-bit PPG ch. 0 output pin	Hysteresis/	CMOS		
20	CMP0_N	I	Comparator ch. 0 inverting analog input (negative input) pin	analog	CIVIUS		О



D:	D:	I/O circuit	Franchica		I/O type		
Pin no.	Pin name	type*1	Function	Input	Output	OD*2	PU*3
	P90		General-purpose I/O port	Hysteresis/	CMOS/		
21		R		LCD power	LCD		_
	V4		LCD drive power supply pin	supply	power supply		
	P91		General-purpose I/O port		CMOS/		
22	1 31	R	Constant part posts in a post	Hysteresis/ LCD power	LCD		
22	V3	IX	LCD drive power supply pin	supply	power		
	P92		General-purpose I/O port		supply CMOS/		
	F92	_	General-purpose 1/O port	Hysteresis/	LCD		
23	V2	R	LCD drive power supply pin	LCD power supply	power		
				Зарріу	supply		
	P93		General-purpose I/O port	Hysteresis/	CMOS/ LCD		
24	V1	R	LCD drive power supply pin	LCD power	power		
			Los anto ponor supply pin	supply	supply		
25	PA0	M	General-purpose I/O port	Hysteresis	CMOS/		
25	COM0	IVI	LCDC COM0 output pin	Trysteresis	LCD		
26	PA1	M	General-purpose I/O port	- Hysteresis	CMOS/		
20	COM1	IVI	LCDC COM1 output pin	Trystorosis	LCD		
27	PA2	M	General-purpose I/O port	- Hysteresis	CMOS/		
	COM2	141	LCDC COM2 output pin	Tryotorcolo	LCD		
28	PA3	M	General-purpose I/O port	Hysteresis	CMOS/		
	COM3		LCDC COM3 output pin	11,000.00.0	LCD		
29	PA4	M	General-purpose I/O port	Hysteresis	CMOS/	_	
	COM4		LCDC COM4 output pin	1.7010.00.0	LCD		
30	PA5	M	General-purpose I/O port	Hysteresis	CMOS/	_	
	COM5		LCDC COM5 output pin	,	LCD		
31	PA6	M	General-purpose I/O port	Hysteresis	CMOS/	_	_
	COM6		LCDC COM6 output pin	,	LCD		
32	PA7	М	General-purpose I/O port	Hysteresis	CMOS/	_	_
	COM7		LCDC COM7 output pin		LCD		
33	Vss		Power supply pin (GND)	_		_	
34	PF1	В	General-purpose I/O port	Hysteresis	CMOS	_	
	X1		Main clock I/O oscillation pin	,			
35	PF0	В	General-purpose I/O port	Hysteresis	CMOS	_	_
	X0		Main clock input oscillation pin				
36	С		Decoupling capacitor connection pin	_	_		_
37	PG2	С	General-purpose I/O port	Hysteresis	CMOS	_	О
31	X1A	-	Subclock I/O oscillation pin	,			



		I/O circuit			I/O type	O type		
Pin no.	Pin name	type*1	Function	Input	Output	OD*2	PU*3	
38	PG1	С	General-purpose I/O port	Hysteresis	CMOS		0	
30	X0A	C	Subclock input oscillation pin	nysteresis	CMOS	_	O	
39	Vcc	_	Power supply pin	_		_	_	
	PF2		General-purpose I/O port					
40	RST	А	Reset pin Dedicated reset pin on MB95F774M/F776M/F778M	Hysteresis	CMOS	О		
41	P17	Н	General-purpose I/O port	Hysteresis	CMOS		О	
41	CMP0_O	П	Comparator ch. 0 digital output pin	Tysieresis	CIVIOS		U	
42	PB0	M	General-purpose I/O port	Hysteresis	CMOS/			
42	SEG00	IVI	LCDC SEG00 output pin	Tiysteresis	LCD			
43	PB1	M	General-purpose I/O port	Hysteresis	CMOS/			
43	SEG01	IVI	LCDC SEG01 output pin	Tiysteresis	LCD			
44	PC0	M	General-purpose I/O port	Hysteresis	CMOS/			
44	SEG02	IVI	LCDC SEG02 output pin	Trysteresis	LCD			
45	PC1	M	General-purpose I/O port	Hysteresis	CMOS/			
70	SEG03	IVI	LCDC SEG03 output pin		LCD			
46	PC2	M	General-purpose I/O port	Hysteresis	CMOS/			
70	SEG04	IVI	LCDC SEG04 output pin	Trysteresis	LCD			
47	PC3	M	General-purpose I/O port	Hysteresis	CMOS/			
77	SEG05	IVI	LCDC SEG05 output pin	Trysteresis	LCD			
48	P60	M	General-purpose I/O port	Hysteresis	CMOS/			
70	SEG06	IVI	LCDC SEG06 output pin	Trysteresis	LCD			
49	P61	M	General-purpose I/O port	Hysteresis	CMOS/			
70	SEG07	IVI	LCDC SEG07 output pin	Trysteresis	LCD			
50	P62	M	General-purpose I/O port	Hysteresis	CMOS/			
30	SEG08	IVI	LCDC SEG08 output pin	Trysteresis	LCD			
51	P63	M	General-purpose I/O port	Hysteresis	CMOS/		_	
	SEG09	141	LCDC SEG09 output pin	11901010010	LCD			
52	P64	M	General-purpose I/O port	Hysteresis	CMOS/			
02	SEG10	141	LCDC SEG10 output pin	Tryotorcolo	LCD			
53	P65	M	General-purpose I/O port	Hysteresis	CMOS/	_		
	SEG11	141	LCDC SEG11 output pin	Tryotorodo	LCD			
54	P66	M	General-purpose I/O port	Hysteresis	CMOS/			
	SEG12	141	LCDC SEG12 output pin	Tryotorodo	LCD			
55	P67	М	General-purpose I/O port	Hysteresis	CMOS/			
55	SEG13	IVI	LCDC SEG13 output pin	Trysiciesis	LCD			



Din	D:	I/O circuit	Function		I/O type		
Pin no.	Pin name	type*1	Function	Input	Output	OD*2	PU*3
56	PE0	M	General-purpose I/O port	Hysteresis	CMOS/		
50	SEG14	IVI	LCDC SEG14 output pin	Trysteresis	LCD		
57	PE1	M	General-purpose I/O port	Hysteresis	CMOS/		
57	SEG15	IVI	LCDC SEG15 output pin	пуѕістеѕіѕ	LCD		_
58	PE2	М	General-purpose I/O port	Hysteresis	CMOS/		
56	SEG16	IVI	LCDC SEG16 output pin	пуѕістеѕіѕ	LCD		_
59	PE3	M	General-purpose I/O port	Hysteresis	CMOS/		
59	SEG17	IVI	LCDC SEG17 output pin		LCD		_
60	PE4	M	General-purpose I/O port	Hysteresis	CMOS/ LCD		
60	SEG18	IVI	LCDC SEG18 output pin				_
	PE5		General-purpose I/O port	Hysteresis	CMOS/ LCD	_	
61	SEG19	М	LCDC SEG19 output pin				_
	TO11		8/16-bit composite timer ch. 1 output pin				
	PE6		General-purpose I/O port				
62	SEG20	М	LCDC SEG20 output pin	Hysteresis	CMOS/ LCD	_	_
	TO10		8/16-bit composite timer ch. 1 output pin		LOD		
	PE7		General-purpose I/O port				
63	SEG21	М	LCDC SEG21 output pin	Hysteresis	CMOS/		
	EC1	IVI	8/16-bit composite timer ch. 1 clock input pin	Tiyatereala	LCD		
64	AVss	—	Power supply pin (GND) for 8/12-bit A/D converter and comparator	_	_	_	_

O: Available

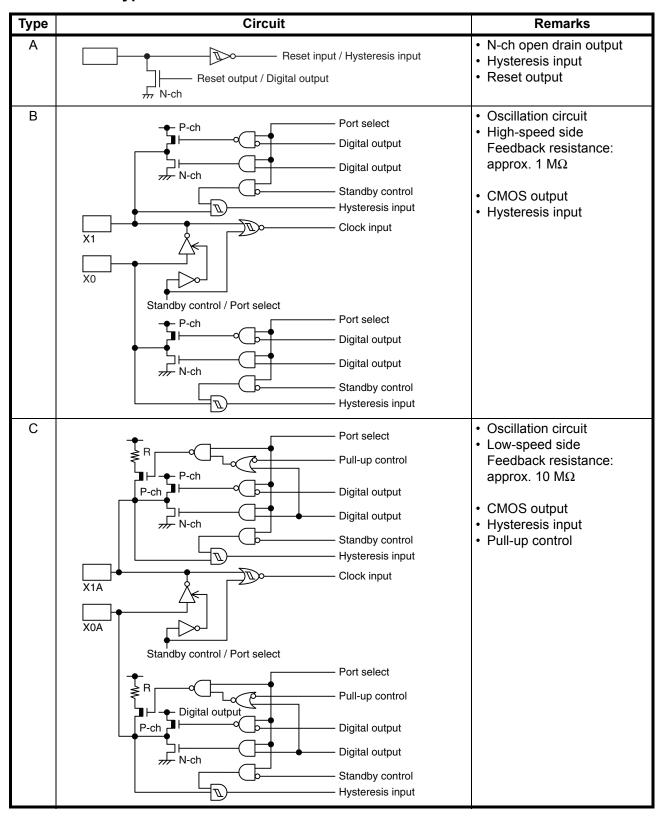
^{*1:} For the I/O circuit types, see "I/O Circuit Type".

^{*2:} N-ch open drain

^{*3:} Pull-up



7. I/O Circuit Type





Туре	Circuit	Remarks
D	Standby control Hysteresis input Digital output	N-ch open drain outputHysteresis input
G	Pull-up control P-ch Digital output Digital output Standby control CMOS input	CMOS output CMOS input Pull-up control
Н	Pull-up control P-ch Digital output Digital output Standby control Hysteresis input	CMOS output Hysteresis input Pull-up control
ı	Standby control CMOS input Digital output N-ch	N-ch open drain outputCMOS input
M	P-ch Digital output Digital output LCD output LCD control Standby control Hysteresis input	CMOS outputLCD outputHysteresis input
R	P-ch Digital output Digital output LCD internal divider resistor I/O LCD control Standby control Hysteresis input	CMOS outputLCD power supplyHysteresis input



Type	Circuit	Remarks
S	P-ch Digital output N-ch Analog input	CMOS output LCD output Hysteresis input Analog input
	LCD output LCD control A/D control Standby control Hysteresis input	
Т	Pull-up control Digital output Digital output Analog input Analog input control Standby control Hysteresis input	CMOS output Hysteresis input Analog input Pull-up control
V	P-ch Digital output Digital output Analog input LCD output LCD control A/D control Standby control CMOS input	CMOS output CMOS input LCD output Analog input



Type	Circuit	Remarks
W	P-ch Digital output Digital output Analog input Analog input control Standby control Hysteresis input	CMOS output Hysteresis input Analog input
Y	P-ch Digital output Digital output Standby control Hysteresis input	CMOS outputHysteresis input



8. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

8.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

• Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

• Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.



(2) Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

8.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.



Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
- (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
 - When you open Dry Package that recommends humidity 40% to 70% relative humidity.
- (3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- (1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
- (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 M Ω).
 - Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (4) Ground all fixtures and instruments, or protect with anti-static measures.
- (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

8.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.



(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

9. Notes On Device Handling

Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than Vcc or a voltage lower than Vss is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in "22.1 Absolute Maximum Ratings" of "Electrical Characteristics" is applied to the Vcc pin or the Vss pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

· Stabilizing supply voltage

Supply voltage must be stabilized.

A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the Vcc power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in Vcc ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard Vcc value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

· Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

10. Pin Connection

· Treatment of unused pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latchups. Always pull up or pull down an unused input pin through a resistor of at least $2 \text{ k}\Omega$. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the Vcc pin and the Vss pin to the power supply and ground outside the device. In addition, connect the current supply source to the Vcc pin and the Vss pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 1.0 μ F as a bypass capacitor between the Vcc pin and the Vss pin at a location close to this device.



• DBG pin

Connect the DBG pin to an external pull-up resistor of 2 $k\Omega$ or above.

After power-on, ensure that the DBG pin does not stay at "L" level until the reset output is released.

The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

RST pin

Connect the RST pin to an external pull-up resistor of 2 $k\Omega$ or above.

To prevent the device from unintentionally entering the reset mode due to noise, minimize the interconnection length between a pull-up resistor and the RST pin and that between a pull-up resistor and the Vcc pin when designing the layout of the printed circuit board.

The PF2/RST pin functions as the reset input/output pin after power-on. In addition, the reset output of the PF2/RST pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function and the general-purpose I/O function can be selected by the RSTEN bit in the SYSC register.

Analog power supply

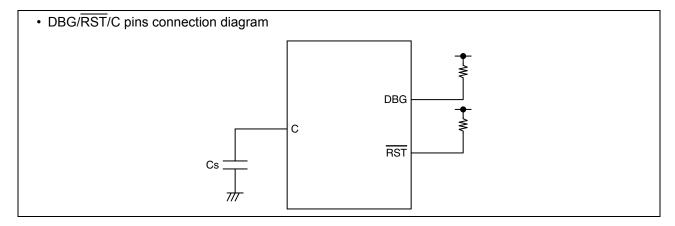
Always set the same potential to the AVcc pin and the Vcc pin. When Vcc is larger than AVcc, the current may flow through the AN00 to AN07 pins.

• Treatment of power supply pins on the 8/12-bit A/D converter

Ensure that AVcc is equal to Vcc and AVss equal to Vss even when the 8/12-bit A/D converter is not in use. Noise riding on the AVcc pin may cause accuracy degradation. Therefore, connect a ceramic capacitor of 0.1 μF (approx.) as a bypass capacitor between the AVcc pin and the AVss pin in the vicinity of this device.

C pin

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the Vcc pin must have a capacitance equal to or larger than the capacitance of Cs. For the connection to a decoupling capacitor Cs, see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and Cs and the distance between Cs and the Vss pin when designing the layout of a printed circuit board.

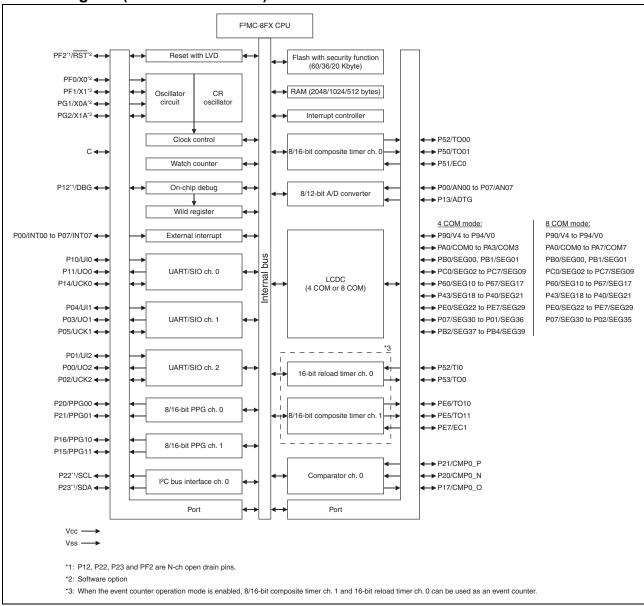


· Note on serial communication

In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, take measures such as adding a checksum to the end of data in order to detect errors. If an error is detected, retransmit the data.

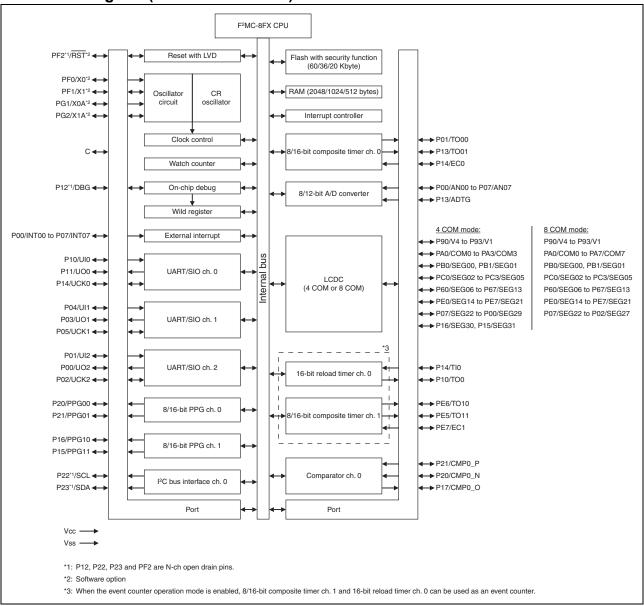


11. Block Diagram (MB95710M Series)





12. Block Diagram (MB95770M Series)



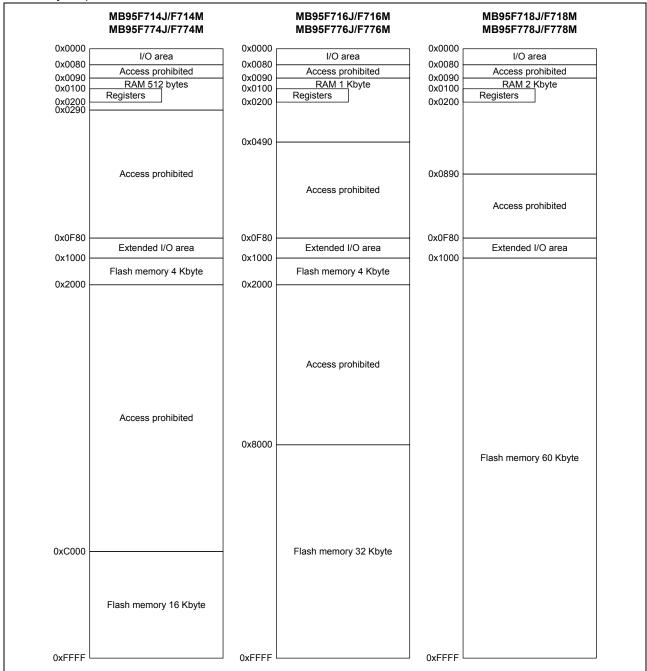


13. CPU Core

Memory space

The memory space of the MB95710M/770M Series is 64 Kbyte in size, and consists of an I/O area, an extended I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95710M/770M Series are shown below.

Memory maps





14. Memory Space

The memory space of the MB95710M/770M Series is 64 Kbyte in size, and consists of an I/O area, an extended I/O area, a data area, and a program area. The memory space includes areas for specific applications such as general-purpose registers and a vector table.

- I/O area (addresses: 0x0000 to 0x007F)
 - This area contains the control registers and data registers for built-in peripheral functions.
 - As the I/O area forms part of the memory space, it can be accessed in the same way as the memory. It can also be accessed at high-speed by using direct addressing instructions.
- Extended I/O area (addresses: 0x0F80 to 0x0FFF)
 - This area contains the control registers and data registers for built-in peripheral functions.
 - As the extended I/O area forms part of the memory space, it can be accessed in the same way as the memory.

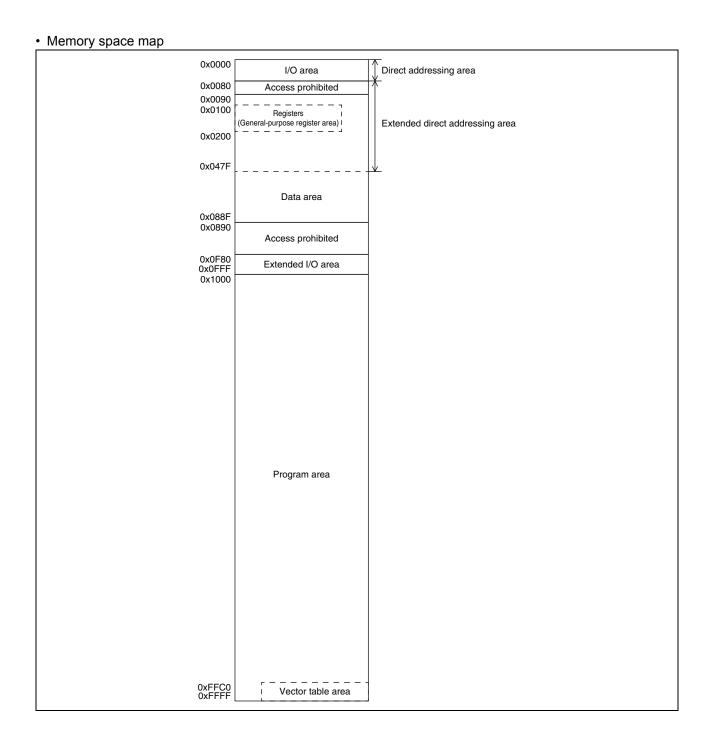
· Data area

- Static RAM is incorporated in the data area as the internal data area.
- The internal RAM size varies according to product.
- The RAM area from 0x0090 to 0x00FF can be accessed at high-speed by using direct addressing instructions.
- In MB95F716J/F716M/F718J/F718M/F776J/F776M/F778J/F778M, the area from 0x0090 to 0x047F is an extended direct addressing area. It can be accessed at high-speed by direct addressing instructions with a direct bank pointer set.
- In MB95F714J/F714M/F774J/F774M, the area from 0x0090 to 0x028F is an extended direct addressing area. It can be accessed at high-speed by direct addressing instructions with a direct bank pointer set.
- The area from 0x0100 to 0x01FF can be used as a general-purpose register area.

Program area

- The Flash memory is incorporated in the program area as the internal program area.
- The Flash memory size varies according to product.
- The area from 0xFFC0 to 0xFFFF is used as the vector table.
- The area from 0xFFBB to 0xFFBF is used to store data of the non-volatile register.







15. Areas For Specific Applications

The general-purpose register area and vector table area are used for the specific applications.

- General-purpose register area (Addresses: 0x0100 to 0x01FF)
 - This area contains the auxiliary registers used for 8-bit arithmetic operations, transfer, etc.
 - As this area forms part of the RAM area, it can also be used as conventional RAM.
 - When the area is used as general-purpose registers, general-purpose register addressing enables high-speed access with short instructions.
- Non-volatile register data area (Addresses: 0xFFBB to 0xFFBF)
 - The area from 0xFFBB to 0xFFBF is used to store data of the non-volatile register. For details, refer to "CHAPTER 28 NON-VOLATILE REGISTER (NVR) INTERFACE" in "New 8FX MB95710M/770M Series Hardware Manual"
- Vector table area (Addresses: 0xFFC0 to 0xFFFF)
 - This area is used as the vector table for vector call instructions (CALLV), interrupts, and resets.
 - The top of the Flash memory area is allocated to the vector table area. The start address of a service routine is set to an address in the vector table in the form of data.

"Interrupt Source Table" lists the vector table addresses corresponding to vector call instructions, interrupts, and resets.

For details, refer to "CHAPTER 4 RESET", "CHAPTER 5 INTERRUPTS", and "A.2 Special Instruction ■ Special Instruction ■ CALLV #vct" in "APPENDIX" in "New 8FX MB95710M/770M Series Hardware Manual".

Direct bank pointer and access area

Direct bank pointer (DP[2:0])	Operand-specified dir	Access area
0bXXX (It does not affect mapping.)	0x0000 to 0x007F	0x0000 to 0x007F
0b000 (Initial value)	0x0090 to 0x00FF	0x0090 to 0x00FF
0b001		0x0100 to 0x017F
0b010	_	0x0180 to 0x01FF
0b011		0x0200 to 0x027F
0b100	0x0080 to 0x00FF	0x0280 to 0x02FF*
0b101		0x0300 to 0x037F
0b110	_	0x0380 to 0x03FF
0b111		0x0400 to 0x047F

^{*:} Due to the memory size limit, the available access area is up to "0x028F" in MB95F714J/F714M/F774J/F774M.

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16. I/O Map (MB95710M Series)

Address	Register abbreviation	Register name	R/W	Initial value
0x0000	PDR0	Port 0 data register	R/W	0b00000000
0x0001	DDR0	Port 0 direction register	R/W	0b00000000
0x0002	PDR1	Port 1 data register	R/W	0b00000000
0x0003	DDR1	Port 1 direction register	R/W	0b00000000
0x0004	_	(Disabled)	_	_
0x0005	WATR	Oscillation stabilization wait time setting register	R/W	0b11111111
0x0006	PLLC	PLL control register	R/W	0b000X0000
0x0007	SYCC	System clock control register	R/W	0bXXX11011
0x0008	STBC	Standby control register	R/W	0b00000000
0x0009	RSRR	Reset source register	R/W	0b000XXXXX
0x000A	TBTC	Time-base timer control register	R/W	0b00000000
0x000B	WPCR	Watch prescaler control register	R/W	0b00000000
0x000C	WDTC	Watchdog timer control register	R/W	0b00XX0000
0x000D	SYCC2	System clock control register 2	R/W	0bXXXX0011
0x000E	PDR2	Port 2 data register	R/W	0b00000000
0x000F	DDR2	Port 2 direction register	R/W	0b00000000
0x0010, 0x0011	_	(Disabled)	_	_
0x0012	PDR4	Port 4 data register	R/W	0b00000000
0x0013	DDR4	Port 4 direction register	R/W	0b00000000
0x0014	PDR5	Port 5 data register	R/W	0b00000000
0x0015	DDR5	Port 5 direction register	R/W	0b00000000
0x0016	PDR6	Port 6 data register	R/W	0b0000000
0x0017	DDR6	Port 6 direction register	R/W	0b00000000
0x0018		(D) 11 15		
to 0x001B	_	(Disabled)	_	_
0x001B	PDR9	Port 9 data register	R/W	0b00000000
0x001D	DDR9	Port 9 direction register	R/W	0b00000000
0x001E	PDRA	Port A data register	R/W	0b00000000
0x001F	DDRA	Port A direction register	R/W	0b00000000
0x0020	PDRB	Port B data register	R/W	0b00000000
0x0021	DDRB	Port B direction register	R/W	0b00000000
0x0022	PDRC	Port C data register	R/W	0b00000000
0x0023	DDRC	Port C direction register	R/W	0b00000000
0x0024, 0x0025		(Disabled)	_	_



Address	Register abbreviation	Register name	R/W	Initial value
0x0026	PDRE	Port E data register	R/W	0b00000000
0x0027	DDRE	Port E direction register	R/W	0b00000000
0x0028	PDRF	Port F data register	R/W	0b00000000
0x0029	DDRF	Port F direction register	R/W	0b00000000
0x002A	PDRG	Port G data register	R/W	0b00000000
0x002B	DDRG	Port G direction register	R/W	0b00000000
0x002C	_	(Disabled)	_	_
0x002D	PUL1	Port 1 pull-up register	R/W	0b00000000
0x002E	PUL2	Port 2 pull-up register	R/W	0b00000000
0x002F, 0x0030	_	(Disabled)	_	_
0x0031	PUL5	Port 5 pull-up register	R/W	0b00000000
0x0032 to 0x0034	_	(Disabled)	_	_
0x0035	PULG	Port G pull-up register	R/W	0b00000000
0x0036	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	0b00000000
0x0037	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	0b00000000
0x0038	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	0b00000000
0x0039	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	0b00000000
0x003A	PC01	8/16-bit PPG timer 01 control register	R/W	0b00000000
0x003B	PC00	8/16-bit PPG timer 00 control register	R/W	0b00000000
0x003C	PC11	8/16-bit PPG timer 11 control register	R/W	0b00000000
0x003D	PC10	8/16-bit PPG timer 10 control register	R/W	0b00000000
0x003E	TMCSRH0	16-bit reload timer control status register (upper) ch. 0	R/W	0b00000000
0x003F	TMCSRL0	16-bit reload timer control status register (lower) ch. 0	R/W	0b00000000
0x0040 to 0x0047	_	(Disabled)	_	_
0x0048	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	0b00000000
0x0049	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	0b00000000
0x004A	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	0b00000000
0x004B	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	0b00000000
0x004C, 0x004D	_	(Disabled)		_
0x004E	LVDC	LVD control register	R/W	0b00000100
0x004F	LCDCC2	LCDC control register 2	R/W	0b00010100
0x0050	CMR0	Comparator control register ch. 0	R/W	0b00000001



Address	Register abbreviation	Register name	R/W	Initial value
0x0051 to 0x0055	_	(Disabled)	_	_
0x0056	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	0b00000000
0x0057	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	0b00100000
0x0058	SSR0	UART/SIO serial status and data register ch. 0	R/W	0b00000001
0x0059	TDR0	UART/SIO serial output data register ch. 0	R/W	0b00000000
0x005A	RDR0	UART/SIO serial input data register ch. 0	R	0b00000000
0x005B	SMC11	UART/SIO serial mode control register 1 ch. 1	R/W	0b00000000
0x005C	SMC21	UART/SIO serial mode control register 2 ch. 1	R/W	0b00100000
0x005D	SSR1	UART/SIO serial status and data register ch. 1	R/W	0b00000001
0x005E	TDR1	UART/SIO serial output data register ch. 1	R/W	0b00000000
0x005F	RDR1	UART/SIO serial input data register ch. 1	R	0b00000000
0x0060	IBCR00	I ² C bus control register 0 ch. 0	R/W	0b00000000
0x0061	IBCR10	I ² C bus control register 1 ch. 0	R/W	0b00000000
0x0062	IBSR0	I ² C bus status register ch. 0	R/W	0b00000000
0x0063	IDDR0	I ² C data register ch. 0	R/W	0b00000000
0x0064	IAAR0	I ² C address register ch. 0	R/W	0b00000000
0x0065	ICCR0	I ² C clock control register ch. 0	R/W	0b00000000
0x0066	SMC12	UART/SIO serial mode control register 1 ch. 2	R/W	0b00000000
0x0067	SMC22	UART/SIO serial mode control register 2 ch. 2	R/W	0b00100000
0x0068	SSR2	UART/SIO serial status and data register ch. 2	R/W	0b00000001
0x0069	TDR2	UART/SIO serial output data register ch. 2	R/W	0b00000000
0x006A	RDR2	UART/SIO serial input data register ch. 2	R	0b00000000
0x006B	ADC3	8/12-bit A/D converter control register 3	R/W	0b01111100
0x006C	ADC1	8/12-bit A/D converter control register 1	R/W	0b00000000
0x006D	ADC2	8/12-bit A/D converter control register 2	R/W	0b00000000
0x006E	ADDH	8/12-bit A/D converter data register (upper)	R/W	0b00000000
0x006F	ADDL	8/12-bit A/D converter data register (lower)	R/W	0b00000000
0x0070	WCSR	Watch counter control register	R/W	0b00000000
0x0071	FSR2	Flash memory status register 2	R/W	0b00000000
0x0072	FSR	Flash memory status register	R/W	0b000X0000
0x0073	SWRE0	Flash memory sector write control register 0	R/W	0b00000000
0x0074	FSR3	Flash memory status register 3	R	0b000XXXXX
0x0075	FSR4	Flash memory status register 4	R/W	0b00000000
0x0076	WREN	Wild register address compare enable register	R/W	0b00000000
0x0077	WROR	Wild register data test setting register	R/W	0b00000000



Address	Register abbreviation	Register name	R/W	Initial value
0x0078	_	Mirror of register bank pointer (RP) and direct bank pointer (DP)	_	_
0x0079	ILR0	Interrupt level setting register 0	R/W	0b11111111
0x007A	ILR1	Interrupt level setting register 1	R/W	0b11111111
0x007B	ILR2	Interrupt level setting register 2	R/W	0b11111111
0x007C	ILR3	Interrupt level setting register 3	R/W	0b11111111
0x007D	ILR4	Interrupt level setting register 4	R/W	0b11111111
0x007E	ILR5	Interrupt level setting register 5	R/W	0b11111111
0x007F	_	(Disabled)	_	_
0x0F80	WRARH0	Wild register address setting register (upper) ch. 0	R/W	0b00000000
0x0F81	WRARL0	Wild register address setting register (lower) ch. 0	R/W	0b00000000
0x0F82	WRDR0	Wild register data setting register ch. 0	R/W	0b00000000
0x0F83	WRARH1	Wild register address setting register (upper) ch. 1	R/W	0b00000000
0x0F84	WRARL1	Wild register address setting register (lower) ch. 1	R/W	0b00000000
0x0F85	WRDR1	Wild register data setting register ch. 1	R/W	0b00000000
0x0F86	WRARH2	Wild register address setting register (upper) ch. 2	R/W	0b00000000
0x0F87	WRARL2	Wild register address setting register (lower) ch. 2	R/W	0b00000000
0x0F88	WRDR2	Wild register data setting register ch. 2	R/W	0b00000000
0x0F89				
to 0x0F91	_	(Disabled)		_
0x0F92	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	0b00000000
0x0F93	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	0b00000000
0x0F94	T01DR	8/16-bit composite timer 01 data register	R/W	0b00000000
0x0F95	T00DR	8/16-bit composite timer 00 data register	R/W	0b00000000
0x0F96	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	0b00000000
0x0F97	T11CR0	8/16-bit composite timer 11 status control register 0	R/W	0b00000000
0x0F98	T10CR0	8/16-bit composite timer 10 status control register 0	R/W	0b00000000
0x0F99	T11DR	8/16-bit composite timer 11 data register	R/W	0b00000000
0x0F9A	T10DR	8/16-bit composite timer 10 data register	R/W	0b00000000
0x0F9B	TMCR1	8/16-bit composite timer 10/11 timer mode control register	R/W	0b00000000
0x0F9C	PPS01	8/16-bit PPG01 cycle setting buffer register	R/W	0b11111111
0x0F9D	PPS00	8/16-bit PPG00 cycle setting buffer register	R/W	0b11111111
0x0F9E	PDS01	8/16-bit PPG01 duty setting buffer register	R/W	0b11111111
0x0F9F	PDS00	8/16-bit PPG00 duty setting buffer register	R/W	0b11111111
0x0FA0	PPS11	8/16-bit PPG11 cycle setting buffer register	R/W	0b11111111



Address	Register abbreviation	Register name	R/W	Initial value
0x0FA1	PPS10	8/16-bit PPG10 cycle setting buffer register	R/W	0b11111111
0x0FA2	PDS11	8/16-bit PPG11 duty setting buffer register	R/W	0b11111111
0x0FA3	PDS10	8/16-bit PPG10 duty setting buffer register	R/W	0b11111111
0x0FA4	PPGS	8/16-bit PPG start register	R/W	0b00000000
0x0FA5	REVC	8/16-bit PPG output inversion register	R/W	0b00000000
0x0FA6	TMRH0	16-bit reload timer timer register (upper) ch. 0	R/W	0b00000000
UXUFAU	TMRLRH0	16-bit reload timer reload register (upper) ch. 0	- K/VV	000000000
0x0FA7	TMRL0	16-bit reload timer timer register (lower) ch. 0	R/W	0b00000000
UXUFAI	TMRLRL0	16-bit reload timer reload register (lower) ch. 0	- F/VV	000000000
0x0FA8	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch. 0	R/W	0b00000000
0x0FA9	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	0b00000000
0x0FAA	PSSR1	UART/SIO dedicated baud rate generator prescaler select register ch. 1	R/W	0b00000000
0x0FAB	BRSR1	UART/SIO dedicated baud rate generator baud rate setting register ch. 1	R/W	0b00000000
0x0FAC	PSSR2	UART/SIO dedicated baud rate generator prescaler select register ch. 2	R/W	0b00000000
0x0FAD	BRSR2	UART/SIO dedicated baud rate generator baud rate setting register ch. 2	R/W	0b00000000
0x0FAE	_	(Disabled)	_	_
0x0FAF	AIDRL	A/D input disable register (lower)	R/W	0b00000000
0x0FB0	LCDCC1	LCDC control register 1	R/W	0b00000000
0x0FB1	_	(Disabled)	_	_
0x0FB2	LCDCE1	LCDC enable register 1	R/W	0b00111110
0x0FB3	LCDCE2	LCDC enable register 2	R/W	0b00000000
0x0FB4	LCDCE3	LCDC enable register 3	R/W	0b00000000
0x0FB5	LCDCE4	LCDC enable register 4	R/W	0b00000000
0x0FB6	LCDCE5	LCDC enable register 5	R/W	0b00000000
0x0FB7	LCDCE6	LCDC enable register 6	R/W	0b00000000
0x0FB8	LCDCE7	LCDC enable register 7	R/W	0b00000000
0x0FB9	LCDCB1	LCDC blinking setting register 1	R/W	0b00000000
0x0FBA	LCDCB2	LCDC blinking setting register 2	R/W	0b00000000
0x0FBB, 0x0FBC	_	(Disabled)		_
0x0FBD to 0x0FE0	LCDRAM	LCDC display RAM (36 bytes)	R/W	0b00000000



Address	Register abbreviation	Register name	R/W	Initial value
0x0FE1	_	(Disabled)	_	_
0x0FE2	EVCR	Event counter control register	R/W	0b00000000
0x0FE3	WCDR	Watch counter data register	R/W	0b00111111
0x0FE4	CRTH	Main CR clock trimming register (upper)	R/W	0b000XXXXX
0x0FE5	CRTL	Main CR clock trimming register (lower)	R/W	0b000XXXXX
0x0FE6	SYSC2	System configuration register 2	R/W	0b00000000
0x0FE7	CRTDA	Main CR clock temperature dependent adjustment register	R/W	0b000XXXXX
0x0FE8	SYSC	System configuration register	R/W	0b00111111
0x0FE9	CMCR	Clock monitoring control register	R/W	0b00000000
0x0FEA	CMDR	Clock monitoring data register	R	0b00000000
0x0FEB	WDTH	Watchdog timer selection ID register (upper)	R	0bXXXXXXXX
0x0FEC	WDTL	Watchdog timer selection ID register (lower)	R	0bXXXXXXXX
0x0FED, 0x0FEE	_	(Disabled)	_	_
0x0FEF	WICR	Interrupt pin selection circuit control register	R/W	0b01000000
0x0FF0 to 0x0FFF	_	(Disabled)	_	_

• R/W access symbols

R/W : Readable/Writable

R : Read only
• Initial value symbols

The initial value of this bit is "0".The initial value of this bit is "1".

X : The initial value of this bit is undefined.

Note: Do not write to an address that is "(Disabled)". If a "(Disabled)" address is read, an indeterminate value is returned.



17. I/O Map (MB95770M Series)

Address	Register abbreviation	Register name	R/W	Initial value
0x0000	PDR0	Port 0 data register	R/W	0b00000000
0x0001	DDR0	Port 0 direction register	R/W	0b00000000
0x0002	PDR1	Port 1 data register	R/W	0b00000000
0x0003	DDR1	Port 1 direction register	R/W	0b00000000
0x0004	_	(Disabled)	_	_
0x0005	WATR	Oscillation stabilization wait time setting register	R/W	0b11111111
0x0006	PLLC	PLL control register	R/W	0b000X0000
0x0007	SYCC	System clock control register	R/W	0bXXX11011
0x0008	STBC	Standby control register	R/W	0b00000000
0x0009	RSRR	Reset source register	R/W	0b000XXXXX
0x000A	TBTC	Time-base timer control register	R/W	0b00000000
0x000B	WPCR	Watch prescaler control register	R/W	0b00000000
0x000C	WDTC	Watchdog timer control register	R/W	0b00XX0000
0x000D	SYCC2	System clock control register 2	R/W	0bXXXX0011
0x000E	PDR2	Port 2 data register	R/W	0b00000000
0x000F	DDR2	Port 2 direction register	R/W	0b00000000
0x0010 to 0x0015	_	(Disabled)	_	_
0x0016	PDR6	Port 6 data register	R/W	0b00000000
0x0017	DDR6	Port 6 direction register	R/W	0b00000000
0x0018 to 0x001B	_	(Disabled)		_
0x001C	PDR9	Port 9 data register	R/W	0b00000000
0x001D	DDR9	Port 9 direction register	R/W	0b00000000
0x001E	PDRA	Port A data register	R/W	0b00000000
0x001F	DDRA	Port A direction register	R/W	0b00000000
0x0020	PDRB	Port B data register	R/W	0b00000000
0x0021	DDRB	Port B direction register	R/W	0b00000000
0x0022	PDRC	Port C data register	R/W	0b00000000
0x0023	DDRC	Port C direction register	R/W	0b00000000
0x0024, 0x0025		(Disabled)	_	_
0x0026	PDRE	Port E data register	R/W	0b00000000
0x0027	DDRE	Port E direction register	R/W	0b00000000
0x0028	PDRF	Port F data register	R/W	0b00000000



Address	Register	Posictor name	R/W	Initial value
Address	abbreviation	Register name	FK/ VV	miliai vaiue
0x0029	DDRF	Port F direction register	R/W	0b00000000
0x002A	PDRG	Port G data register	R/W	0b00000000
0x002B	DDRG	Port G direction register	R/W	0b00000000
0x002C		(Disabled)	_	_
0x002D	PUL1	Port 1 pull-up register	R/W	0b00000000
0x002E	PUL2	Port 2 pull-up register	R/W	0b00000000
0x002F to	_	(Disabled)		
0x0034				
0x0035	PULG	Port G pull-up register	R/W	0b00000000
0x0036	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	0b00000000
0x0037	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	0b00000000
0x0038	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	0b00000000
0x0039	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	0b00000000
0x003A	PC01	8/16-bit PPG timer 01 control register	R/W	0b00000000
0x003B	PC00	8/16-bit PPG timer 00 control register	R/W	0b00000000
0x003C	PC11	8/16-bit PPG timer 11 control register	R/W	0b00000000
0x003D	PC10	8/16-bit PPG timer 10 control register	R/W	0b00000000
0x003E	TMCSRH0	16-bit reload timer control status register (upper) ch. 0	R/W	0b00000000
0x003F	TMCSRL0	16-bit reload timer control status register (lower) ch. 0	R/W	0b00000000
0x0040				
to 0x0047	_	(Disabled)	_	_
0x0048	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	0b00000000
0x0049	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	0b00000000
0x004A	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	0b00000000
0x004B	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	0b00000000
0x004C, 0x004D	_	(Disabled)	_	_
0x004E	LVDC	LVD control register	R/W	0b00000100
0x004F	LCDCC2	LCDC control register 2	R/W	0b00010100
0x0050	CMR0	Comparator control register ch. 0	R/W	0b00000001
0x0051 to 0x0055	_	(Disabled)	_	_
0x0056	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	0b00000000
0x0057	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	0b00100000
0x0058	SSR0	UART/SIO serial status and data register ch. 0	R/W	0b00000001
0x0059	TDR0	UART/SIO serial output data register ch. 0	R/W	0b00000000



Address	Register abbreviation	Register name	R/W	Initial value
0x005A	RDR0	UART/SIO serial input data register ch. 0	R	0b00000000
0x005B	SMC11	UART/SIO serial mode control register 1 ch. 1	R/W	0b00000000
0x005C	SMC21	UART/SIO serial mode control register 2 ch. 1	R/W	0b00100000
0x005D	SSR1	UART/SIO serial status and data register ch. 1	R/W	0b00000001
0x005E	TDR1	UART/SIO serial output data register ch. 1	R/W	0b00000000
0x005F	RDR1	UART/SIO serial input data register ch. 1	R	0b00000000
0x0060	IBCR00	I ² C bus control register 0 ch. 0	R/W	0b00000000
0x0061	IBCR10	I ² C bus control register 1 ch. 0	R/W	0b00000000
0x0062	IBSR0	I ² C bus status register ch. 0	R/W	0b00000000
0x0063	IDDR0	I ² C data register ch. 0	R/W	0b00000000
0x0064	IAAR0	I ² C address register ch. 0	R/W	0b00000000
0x0065	ICCR0	I ² C clock control register ch. 0	R/W	0b00000000
0x0066	SMC12	UART/SIO serial mode control register 1 ch. 2	R/W	0b00000000
0x0067	SMC22	UART/SIO serial mode control register 2 ch. 2	R/W	0b00100000
0x0068	SSR2	UART/SIO serial status and data register ch. 2	R/W	0b00000001
0x0069	TDR2	UART/SIO serial output data register ch. 2	R/W	0b00000000
0x006A	RDR2	UART/SIO serial input data register ch. 2	R	0b00000000
0x006B	ADC3	8/12-bit A/D converter control register 3	R/W	0b01111100
0x006C	ADC1	8/12-bit A/D converter control register 1	R/W	0b00000000
0x006D	ADC2	8/12-bit A/D converter control register 2	R/W	0b00000000
0x006E	ADDH	8/12-bit A/D converter data register (upper)	R/W	0b0000000
0x006F	ADDL	8/12-bit A/D converter data register (lower)	R/W	0b00000000
0x0070	WCSR	Watch counter control register	R/W	0b00000000
0x0071	FSR2	Flash memory status register 2	R/W	0b00000000
0x0072	FSR	Flash memory status register	R/W	0b000X0000
0x0073	SWRE0	Flash memory sector write control register 0	R/W	0b00000000
0x0074	FSR3	Flash memory status register 3	R	0b000XXXXX
0x0075	FSR4	Flash memory status register 4	R/W	0b00000000
0x0076	WREN	Wild register address compare enable register	R/W	0b00000000
0x0077	WROR	Wild register data test setting register	R/W	0b00000000
0x0078	_	Mirror of register bank pointer (RP) and direct bank pointer (DP)	_	_
0x0079	ILR0	Interrupt level setting register 0	R/W	0b11111111
0x007A	ILR1	Interrupt level setting register 1	R/W	0b11111111
0x007B	ILR2	Interrupt level setting register 2	R/W	0b11111111
0x007C	ILR3	Interrupt level setting register 3	R/W	0b11111111
0x007D	ILR4	Interrupt level setting register 4	R/W	0b11111111



Address	Register abbreviation	Register name	R/W	Initial value
0x007E	ILR5	Interrupt level setting register 5	R/W	0b11111111
0x007F	_	(Disabled)	_	_
0x0F80	WRARH0	Wild register address setting register (upper) ch. 0	R/W	0b00000000
0x0F81	WRARL0	Wild register address setting register (lower) ch. 0	R/W	0b00000000
0x0F82	WRDR0	Wild register data setting register ch. 0	R/W	0b00000000
0x0F83	WRARH1	Wild register address setting register (upper) ch. 1	R/W	0b00000000
0x0F84	WRARL1	Wild register address setting register (lower) ch. 1	R/W	0b00000000
0x0F85	WRDR1	Wild register data setting register ch. 1	R/W	0b00000000
0x0F86	WRARH2	Wild register address setting register (upper) ch. 2	R/W	0b00000000
0x0F87	WRARL2	Wild register address setting register (lower) ch. 2	R/W	0b00000000
0x0F88	WRDR2	Wild register data setting register ch. 2	R/W	0b00000000
0x0F89 to 0x0F91	_	(Disabled)		_
0x0F92	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	0b00000000
0x0F93	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	0b00000000
0x0F94	T01DR	8/16-bit composite timer 01 data register	R/W	0b00000000
0x0F95	T00DR	8/16-bit composite timer 00 data register	R/W	0b00000000
0x0F96	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	0b00000000
0x0F97	T11CR0	8/16-bit composite timer 11 status control register 0	R/W	0b00000000
0x0F98	T10CR0	8/16-bit composite timer 10 status control register 0	R/W	0b00000000
0x0F99	T11DR	8/16-bit composite timer 11 data register	R/W	0b00000000
0x0F9A	T10DR	8/16-bit composite timer 10 data register	R/W	0b00000000
0x0F9B	TMCR1	8/16-bit composite timer 10/11 timer mode control register	R/W	0b00000000
0x0F9C	PPS01	8/16-bit PPG01 cycle setting buffer register	R/W	0b11111111
0x0F9D	PPS00	8/16-bit PPG00 cycle setting buffer register	R/W	0b11111111
0x0F9E	PDS01	8/16-bit PPG01 duty setting buffer register	R/W	0b11111111
0x0F9F	PDS00	8/16-bit PPG00 duty setting buffer register	R/W	0b11111111
0x0FA0	PPS11	8/16-bit PPG11 cycle setting buffer register	R/W	0b11111111
0x0FA1	PPS10	8/16-bit PPG10 cycle setting buffer register	R/W	0b11111111
0x0FA2	PDS11	8/16-bit PPG11 duty setting buffer register	R/W	0b11111111
0x0FA3	PDS10	8/16-bit PPG10 duty setting buffer register	R/W	0b11111111
0x0FA4	PPGS	8/16-bit PPG start register	R/W	0b00000000
0x0FA5	REVC	8/16-bit PPG output inversion register	R/W	0b00000000
0.0546	TMRH0	16-bit reload timer timer register (upper) ch. 0	DAA	050000000
0x0FA6	TMRLRH0	16-bit reload timer reload register (upper) ch. 0	R/W	0b00000000



Address	Register abbreviation	Register name	R/W	Initial value
00547	TMRL0	16-bit reload timer timer register (lower) ch. 0	DAM	01-0000000
0x0FA7	TMRLRL0	16-bit reload timer reload register (lower) ch. 0	R/W	0b00000000
0x0FA8	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch. 0	R/W	0b00000000
0x0FA9	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	0b00000000
0x0FAA	PSSR1	UART/SIO dedicated baud rate generator prescaler select register ch. 1	R/W	0b00000000
0x0FAB	BRSR1	UART/SIO dedicated baud rate generator baud rate setting register ch. 1	R/W	0ь00000000
0x0FAC	PSSR2	UART/SIO dedicated baud rate generator prescaler select register ch. 2	R/W	0ь00000000
0x0FAD	BRSR2	UART/SIO dedicated baud rate generator baud rate setting register ch. 2	R/W	0ь00000000
0x0FAE	_	(Disabled)		_
0x0FAF	AIDRL	A/D input disable register (lower)	R/W	0b00000000
0x0FB0	LCDCC1	LCDC control register 1	R/W	0b00000000
0x0FB1	_	(Disabled)	<u> </u>	_
0x0FB2	LCDCE1	LCDC enable register 1	R/W	0b00111110
0x0FB3	LCDCE2	LCDC enable register 2	R/W	0b00000000
0x0FB4	LCDCE3	LCDC enable register 3	R/W	0b00000000
0x0FB5	LCDCE4	LCDC enable register 4	R/W	0b00000000
0x0FB6	LCDCE5	LCDC enable register 5	R/W	0b00000000
0x0FB7	LCDCE6	LCDC enable register 6	R/W	0b00000000
0x0FB8	_	(Disabled)	—	_
0x0FB9	LCDCB1	LCDC blinking setting register 1	R/W	0b00000000
0x0FBA	LCDCB2	LCDC blinking setting register 2	R/W	0b00000000
0x0FBB, 0x0FBC	_	(Disabled)	_	_
0x0FBD to 0x0FD8	LCDRAM	LCDC display RAM (28 bytes)	R/W	0600000000
0x0FD9 to 0x0FE1	_	(Disabled)	_	
0x0FE2	EVCR	Event counter control register	R/W	0b00000000
0x0FE3	WCDR	Watch counter data register	R/W	0b00111111
0x0FE4	CRTH	Main CR clock trimming register (upper)	R/W	0b000XXXXX
0x0FE5	CRTL	Main CR clock trimming register (lower)	R/W	0b000XXXXX
0x0FE6	SYSC2	System configuration register 2	R/W	0b00000000



Address	Register abbreviation	Register name	R/W	Initial value
0x0FE7	CRTDA	Main CR clock temperature dependent adjustment register	R/W	0b000XXXXX
0x0FE8	SYSC	System configuration register	R/W	0b00111111
0x0FE9	CMCR	Clock monitoring control register	R/W	0b0000000
0x0FEA	CMDR	Clock monitoring data register	R	0b00000000
0x0FEB	WDTH	Watchdog timer selection ID register (upper)	R	0bXXXXXXXX
0x0FEC	WDTL	Watchdog timer selection ID register (lower)	R	0bXXXXXXXX
0x0FED, 0x0FEE	_	(Disabled)	_	_
0x0FEF	WICR	Interrupt pin selection circuit control register	R/W	0b01000000
0x0FF0 to 0x0FFF	_	(Disabled)	_	_

• R/W access symbols

R/W : Readable/Writable

R : Read only
• Initial value symbols

The initial value of this bit is "0".The initial value of this bit is "1".

X : The initial value of this bit is undefined.

Note: Do not write to an address that is "(Disabled)". If a "(Disabled)" address is read, an indeterminate value is returned.



18. I/O Ports (MB95710M Series)

· List of port registers

Register name		Read/Write	Initial value
Port 0 data register	PDR0	R, RM/W	0b00000000
Port 0 direction register	DDR0	R/W	0b00000000
Port 1 data register	PDR1	R, RM/W	0b0000000
Port 1 direction register	DDR1	R/W	0b00000000
Port 2 data register	PDR2	R, RM/W	0b00000000
Port 2 direction register	DDR2	R/W	0b00000000
Port 4 data register	PDR4	R, RM/W	0b0000000
Port 4 direction register	DDR4	R/W	0b00000000
Port 5 data register	PDR5	R, RM/W	0b0000000
Port 5 direction register	DDR5	R/W	0b00000000
Port 6 data register	PDR6	R, RM/W	0b0000000
Port 6 direction register	DDR6	R/W	0b00000000
Port 9 data register	PDR9	R, RM/W	0b00000000
Port 9 direction register	DDR9	R/W	0b00000000
Port A data register	PDRA	R, RM/W	0b00000000
Port A direction register	DDRA	R/W	0b00000000
Port B data register	PDRB	R, RM/W	0b00000000
Port B direction register	DDRB	R/W	0b0000000
Port C data register	PDRC	R, RM/W	0b0000000
Port C direction register	DDRC	R/W	0b0000000
Port E data register	PDRE	R, RM/W	0b0000000
Port E direction register	DDRE	R/W	0b0000000
Port F data register	PDRF	R, RM/W	0b0000000
Port F direction register	DDRF	R/W	0b00000000
Port G data register	PDRG	R, RM/W	0b0000000
Port G direction register	DDRG	R/W	0b00000000
Port 1 pull-up register	PUL0	R/W	0b0000000
Port 2 pull-up register	PUL1	R/W	0b0000000
Port 5 pull-up register	PUL5	R/W	0b0000000
Port G pull-up register	PULG	R/W	0b00000000
A/D input disable register (lower)	AIDRL	R/W	0b0000000

R/W : Readable/writable (The read value is the same as the write value.)

R, RM/W: Readable/writable (The read value is different from the write value. The write value is read by the read-modify-write (RMW) type of instruction.)



18.1 Port 0

Port 0 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

18.1.1 Port 0 configuration

Port 0 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 0 data register (PDR0)
- Port 0 direction register (DDR0)
- · A/D input disable register (lower) (AIDRL)

18.1.2 Block diagrams of port 0

P00/INT00/AN00/UO2 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT00)
- 8/12-bit A/D converter analog input pin (AN00)
- UART/SIO ch. 2 data output pin (UO2)

P02/INT02/AN02/SEG35/UCK2 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT02)
- 8/12-bit A/D converter analog input pin (AN02)
- LCDC SEG35 output pin (SEG35)
- UART/SIO ch. 2 clock I/O pin (UCK2)

P03/INT03/AN03/SEG34/UO1 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT03)
- 8/12-bit A/D converter analog input pin (AN03)
- LCDC SEG34 output pin (SEG34)
- UART/SIO ch. 1 data output pin (UO1)

P05/INT05/AN05/SEG32/UCK1 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT05)
- 8/12-bit A/D converter analog input pin (AN05)
- LCDC SEG32 output pin (SEG32)
- UART/SIO ch. 1 clock I/O pin (UCK1)

• P06/INT06/AN06/SEG31 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT06)
- 8/12-bit A/D converter analog input pin (AN06)
- LCDC SEG31 output pin (SEG31)

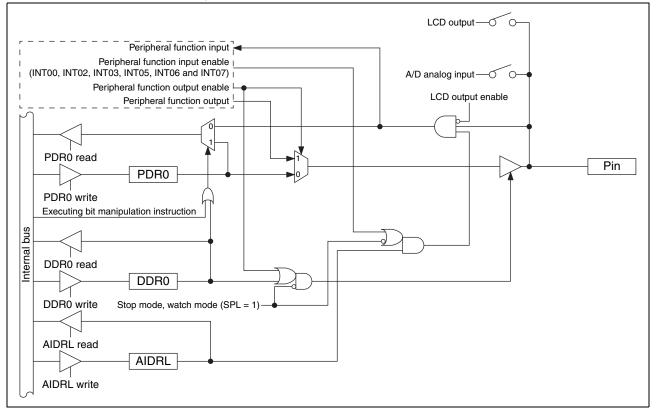
P07/INT07/AN07/SEG30 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT07)
- 8/12-bit A/D converter analog input pin (AN07)
- LCDC SEG30 output pin (SEG30)



 Block diagram of P00/INT00/AN00/UO2, P02/INT02/AN02/SEG35/UCK2, P03/INT03/AN03/SEG34/UO1, P05/INT05/AN05/SEG32/UCK1, P06/INT06/AN06/SEG31 and P07/INT07/AN07/SEG30



• P01/INT01/AN01/SEG36/UI2 pin

This pin has the following peripheral functions:

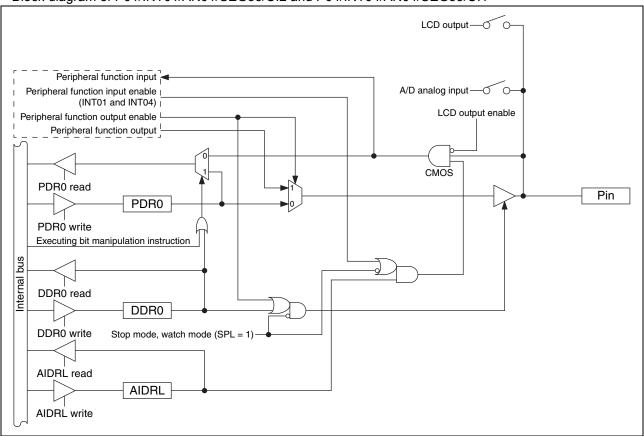
- External interrupt input pin (INT01)
- 8/12-bit A/D converter analog input pin (AN01)
- LCDC SEG36 output pin (SEG36)
- UART/SIO ch. 2 data input pin (UI2)
- P04/INT04/AN04/SEG33/UI1 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT04)
- 8/12-bit A/D converter analog input pin (AN04)
- LCDC SEG33 output pin (SEG33)
- UART/SIO ch. 1 data input pin (UI1)



Block diagram of P01/INT01/AN01/SEG36/UI2 and P04/INT04/AN04/SEG33/UI1



18.1.3 Port 0 registers

• Port 0 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write			
PDR0	0	Pin state is "L" level.	PDR0 value is "0".	As output port, outputs "L" level.			
PDRU	1	Pin state is "H" level.	PDR0 value is "1".	As output port, outputs "H" level.			
DDR0	0		Port input enabled				
DDRO	1		Port output enabled				
AIDRL	0		Analog input enabled				
AIDKL	1		Port input enabled	d			

• Correspondence between registers and pins for port 0

		Correspondence between related register bits and pins							
Pin name	P07	P06	P05	P04	P03	P02	P01	P00	
PDR0									
DDR0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
AIDRL									



18.1.4 Port 0 operations

- Operation as an output port
 - A pin becomes an output port if the bit in the DDR0 register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDR0 register to external pins.
 - If data is written to the PDR0 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDR0 register returns the PDR0 register value.
 - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 6 (LCDCE6:SEG[31:30]) or in the LCDC enable register 7 (LCDCE7:SEG[36:32]) to "0" to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LC-DCE1:PICTL) to "1".

· Operation as an input port

- A pin becomes an input port if the bit in the DDR0 register corresponding to that pin is set to "0".
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- When using an analog input shared pin as an input port, set the corresponding bit in the A/D input disable register (lower) (AIDRL) to "1".
- If data is written to the PDR0 register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDR0 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.
- To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 6 (LCDCE6:SEG[31:30]) or in the LCDC enable register 7 (LCDCE7:SEG[36:32]) to "0" to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to "1".

Operation as a peripheral function output pin

- A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- The pin value can be read from the PDR0 register even if the peripheral function output is enabled. Therefore, the
 output value of a peripheral function can be read by the read operation on the PDR0 register. However, if the readmodify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

· Operation as a peripheral function input pin

- To set a pin as an input port, set the bit in the DDR0 register corresponding to the input pin of a peripheral function to "0".
- When using the analog input shared pin as another peripheral function input pin, configure it as an input port, which is the same as the operation as an input port.
- Reading the PDR0 register returns the pin value, regardless of whether the peripheral function uses that pin as its
 input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0
 register value is returned.

· Operation as an LCDC segment output pin

- Set the bit in the DDR0 register corresponding to an LCDC segment output pin to "0".
- To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 6 (LCDCE6:SEG[31:30]) or in the LCDC enable register 7 (LCDCE7:SEG[36:32]) to "1" to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to "1".

Operation at reset

If the CPU is reset, all bits in the DDR0 register are initialized to "0" and port input is enabled. As for a pin shared with analog input, its port input is disabled because the AIDRL register is initialized to "0".



- Operation in stop mode and watch mode
 - If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR0 register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open. However, if the interrupt input is enabled for the external interrupt (INT00 to INT07), the input is enabled and not blocked.
 - If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.
- · Operation as an analog input pin
 - Set the bit in the DDR0 register bit corresponding to the analog input pin to "0" and the bit corresponding to that pin in the AIDRL register to "0".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- Operation as an external interrupt input pin
 - Set the bit in the DDR0 register corresponding to the external interrupt input pin to "0".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - The pin value is always input to the external interrupt circuit. When using a pin for a function other than the interrupt, disable the external interrupt function corresponding to that pin.

18.2 Port 1

Port 1 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

18.2.1 Port 1 configuration

Port 1 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 1 data register (PDR1)
- Port 1 direction register (DDR1)
- Port 1 pull-up register (PUL1)

18.2.2 Block diagrams of port 1

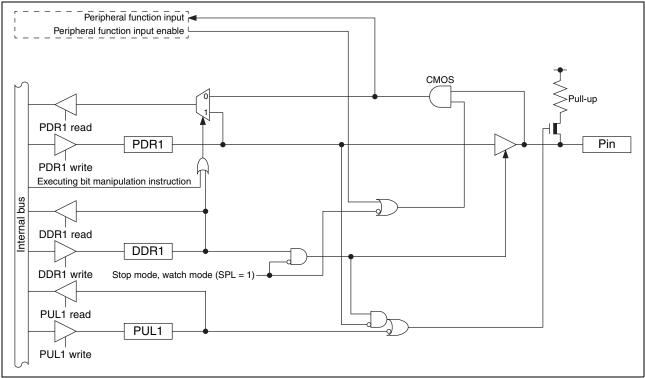
• P10/UI0 pin

This pin has the following peripheral function:

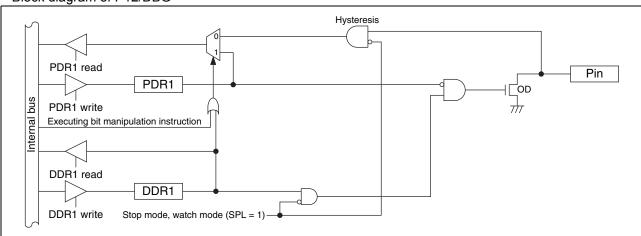
• UART/SIO ch. 0 data input pin (UI0)



Block diagram of P10/UI0



- P12/DBG pin
 - This pin has the following peripheral function:
 - DBG input pin (DBG)
- Block diagram of P12/DBG





• P11/U00 pin

This pin has the following peripheral function:

- UART/SIO ch. 0 data output pin (UO0)
- P13/ADTG pin

This pin has the following peripheral function:

- 8/12-bit A/D converter trigger input pin (ADTG)
- P14/UCK0 pin

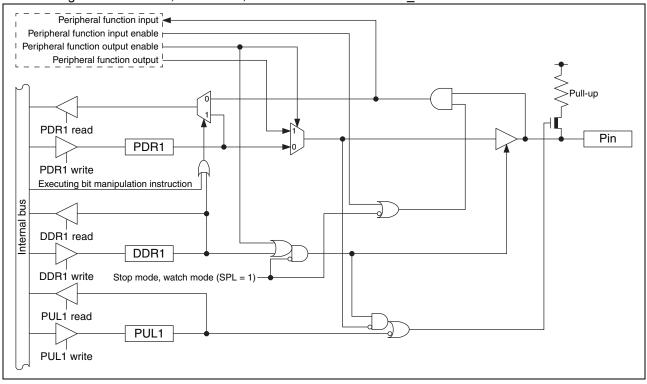
This pin has the following peripheral function:

- UART/SIO ch. 0 clock I/O pin (UCK0)
- P17/CMP0_O pin

This pin has the following peripheral function:

• Comparator ch. 0 digital output pin (CMP0_O)

• Block diagram of P11/UO0, P13/ADTG, P14/UCK0 and P17/CMP0 O





• P15/PPG11 pin

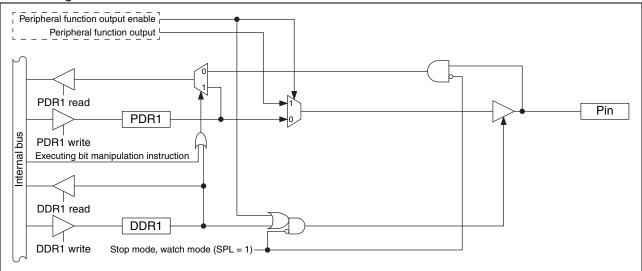
This pin has the following peripheral function:

- 8/16-bit PPG ch. 1 output pin (PPG11)
- P16/PPG10 pin

This pin has the following peripheral function:

• 8/16-bit PPG ch. 1 output pin (PPG10)

• Block diagram of P15/PPG11 and P16/PPG10



18.2.3 Port 1 registers

· Port 1 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write			
PDR1	0	Pin state is "L" level.	PDR1 value is "0".	As output port, outputs "L" level.			
PDRI	1	Pin state is "H" level.	PDR1 value is "1".	As output port, outputs "H" level.*			
DDR1	0		Port input enabled				
DDK1	1		Port output enabled				
PUL1	0		Pull-up disabled				
POLI	1		Pull-up enabled				

^{*:} If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

· Correspondence between registers and pins for port 1

		Correspondence between related register bits and pins							
Pin name	P17	P16	P15	P14	P13	P12	P11	P10	
PDR1		bit6	bit5			bit2			
DDR1	bit7	Dito	טונט	bit4	bit3	DILZ	bit1	bit0	
PUL1		-	-			-			



18.2.4 Port 1 operations

- Operation as an output port
 - · A pin becomes an output port if the bit in the DDR1 register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDR1 register to external pins.
 - If data is written to the PDR1 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDR1 register returns the PDR1 register value.
- · Operation as an input port
 - A pin becomes an input port if the bit in the DDR1 register corresponding to that pin is set to "0".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - If data is written to the PDR1 register, the value is stored in the output latch but is not output to the pin set as an input port.
 - Reading the PDR1 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is
 used to read the PDR1 register, the PDR1 register value is returned.
- Operation as a peripheral function output pin
 - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
 - The pin value can be read from the PDR1 register even if the peripheral function output is enabled. Therefore, the
 output value of a peripheral function can be read by the read operation on the PDR1 register. However, if the readmodify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.
- Operation as a peripheral function input pin
 - To set a pin as an input port, set the bit in the DDR1 register corresponding to the input pin of a peripheral function to "0".
 - Reading the PDR1 register returns the pin value, regardless of whether the peripheral function uses that pin as its
 input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1
 register value is returned.
- Operation at reset

If the CPU is reset, all bits in the DDR1 register are initialized to "0" and port input is enabled.

- Operation in stop mode and watch mode
 - If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR1 register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open. However, if the interrupt input of P10/UI0 and P14/UCK0 is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
 - If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.
- · Operation of the pull-up register

Setting the bit in the PUL1 register to "1" makes the pull-up resistor be internally connected to the pin. When the pin output is "L" level, the pull-up resistor is disconnected regardless of the value of the PUL1 register.



18.3 Port 2

Port 2 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

18.3.1 Port 2 configuration

Port 2 is made up of the following elements.

- · General-purpose I/O pins/peripheral function I/O pins
- Port 2 data register (PDR2)
- Port 2 direction register (DDR2)
- Port 2 pull-up register (PUL2)

18.3.2 Block diagrams of port 2

P20/PPG00/CMP0 N pin

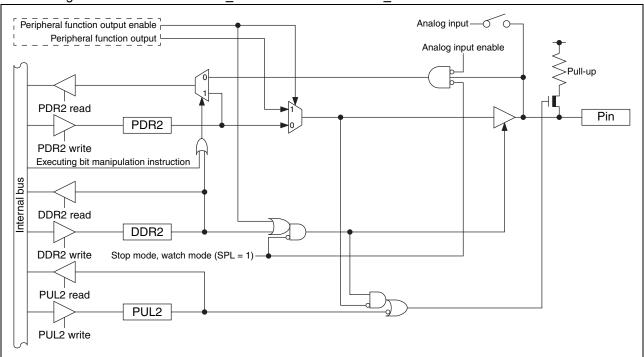
This pin has the following peripheral functions:

- 8/16-bit PPG ch. 0 output pin (PPG00)
- Comparator ch. 0 inverting analog input (negative input) pin (CMP0_N)
- P21/PPG01/CMP0 P pin

This pin has the following peripheral functions:

- 8/16-bit PPG ch. 0 output pin (PPG01)
- Comparator ch. 0 non-inverting analog input (positive input) pin (CMP0 P)

Block diagram of P20/PPG00/CMP0 N and P21/PPG01/CMP0 P





• P22/SCL pin

This pin has the following peripheral function:

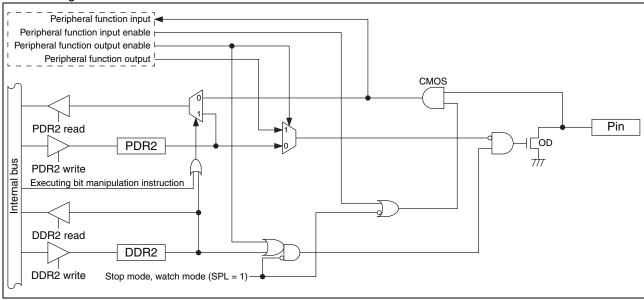
• I2C bus interface ch. 0 clock I/O pin (SCL)

• P23/SDA pin

This pin has the following peripheral function:

• I²C bus interface ch. 0 data I/O pin (SDA)

· Block diagram of P22/SCL and P23/SDA



18.3.3 Port 2 registers

· Port 2 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write			
PDR2	0	Pin state is "L" level.	PDR2 value is "0".	As output port, outputs "L" level.			
FDRZ	1	Pin state is "H" level.	PDR2 value is "1".	As output port, outputs "H" level.*			
DDR2	0		Port input enabled				
DDRZ	1		Port output enable	d			
PUL2	0		Pull-up disabled				
PUL2	1		Pull-up enabled				

^{*:} If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

• Correspondence between registers and pins for port 2

		Correspondence between related register bits and pins							
Pin name		=	=	-	P23	P22	P21	P20	
PDR2					bit3	bit2			
DDR2	-	-	-	-	มแจ	DILZ	bit1	bit0	
PUL2					-	-			



18.3.4 Port 2 operations

- Operation as an output port
 - · A pin becomes an output port if the bit in the DDR2 register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDR2 register to external pins.
 - If data is written to the PDR2 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDR2 register returns the PDR2 register value.
- · Operation as an input port
 - A pin becomes an input port if the bit in the DDR2 register corresponding to that pin is set to "0".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - If data is written to the PDR2 register, the value is stored in the output latch but is not output to the pin set as an
 input port.
 - Reading the PDR2 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is
 used to read the PDR2 register, the PDR2 register value is returned.
- Operation as a peripheral function output pin
 - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
 - The pin value can be read from the PDR2 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR2 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR2 register, the PDR2 register value is returned.
- Operation as a peripheral function input pin
 - To set a pin as an input port, set the bit in the DDR2 register corresponding to the input pin of a peripheral function to "0".
 - Reading the PDR2 register returns the pin value, regardless of whether the peripheral function uses that pin as its
 input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR2 register, the PDR2
 register value is returned.
- Operation at reset

If the CPU is reset, all bits in the DDR2 register are initialized to "0" and port input is enabled.

- Operation in stop mode and watch mode
 - If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR2 register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.
 - If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.
- Operation of the pull-up register

Setting the bit in the PUL2 register to "1" makes the pull-up resistor be internally connected to the pin. When the pin output is "L" level, the pull-up resistor is disconnected regardless of the value of the PUL2 register.

- · Operation as a comparator input pin
 - Regardless of the value of the PDR2 register and that of the DDR2 register, if the comparator analog input enable bit in the comparator control register ch. 0 (CMR0:VCID) is set to "0", the comparator input function is enabled.
 - To disable the comparator input function, set the VCID bit to "1".
 - For details of the comparator, refer to "CHAPTER 29 COMPARATOR" in "New 8FX MB95710M/770M Series Hardware Manual".



18.4 Port 4

Port 4 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

18.4.1 Port 4 configuration

Port 4 is made up of the following elements.

- · General-purpose I/O pins/peripheral function I/O pins
- Port 4 data register (PDR4)
- Port 4 direction register (DDR4)

18.4.2 Block diagrams of port 4

P40/SEG21 pin

This pin has the following peripheral function:

- LCDC SEG21 output pin (SEG21)
- P41/SEG20 pin

This pin has the following peripheral function:

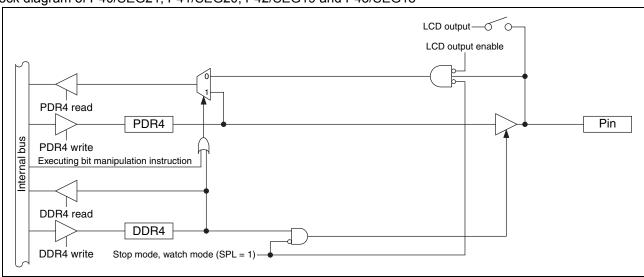
- · LCDC SEG20 output pin (SEG20)
- P42/SEG19 pin

This pin has the following peripheral function:

- LCDC SEG19 output pin (SEG19)
- P43/SEG18 pin

This pin has the following peripheral function:

- LCDC SEG18 output pin (SEG18)
- Block diagram of P40/SEG21, P41/SEG20, P42/SEG19 and P43/SEG18





18.4.3 Port 4 registers

Port 4 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR4	0	Pin state is "L" level.	PDR4 value is "0".	As output port, outputs "L" level.
r DIX4	1	Pin state is "H" level.	PDR4 value is "1".	As output port, outputs "H" level.
DDR4	0		Port input enabled	d
DDR4	1		Port output enable	d

· Correspondence between registers and pins for port 4

		Correspondence between related register bits and pins							
Pin name	-	-	-	-	P43	P42	P41	P40	
PDR4		_			bit3	bit2	bit1	bit0	
DDR4	-	-	-	-	טונט	DILZ	DILI	Dito	

18.4.4 Port 4 operations

- Operation as an output port
 - A pin becomes an output port if the bit in the DDR4 register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - · When a pin is used as an output port, it outputs the value of the PDR4 register to external pins.
 - If data is written to the PDR4 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDR4 register returns the PDR4 register value.
 - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[21:18]) to "0" to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to "1".

Operation as an input port

- A pin becomes an input port if the bit in the DDR4 register corresponding to that pin is set to "0".
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- If data is written to the PDR4 register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDR4 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.
- To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[21:18]) to "0" to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to "1".

· Operation as an LCDC segment output pin

- Set the bit in the DDR4 register corresponding to an LCDC segment output pin to "0".
- To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[21:18]) to "1" to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to "1".

Operation at reset

If the CPU is reset, all bits in the DDR4 register are initialized to "0" and port input is enabled.



- Operation in stop mode and watch mode
 - If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR4 register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.
 - If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

18.5 Port 5

Port 5 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

18.5.1 Port 5 configuration

Port 5 is made up of the following elements.

- · General-purpose I/O pins/peripheral function I/O pins
- Port 5 data register (PDR5)
- Port 5 direction register (DDR5)
- Port 5 pull-up register (PUL5)

18.5.2 Block diagrams of port 5

P50/TO01 pin

This pin has the following peripheral function:

• 8/16-bit composite timer ch. 0 output pin (TO01)

• P51/EC0 pin

This pin has the following peripheral function:

• 8/16-bit composite timer ch. 0 clock input pin (EC0)

• P52/TI0/TO00 pin

This pin has the following peripheral functions:

- 16-bit reload timer ch. 0 input pin (TI0)
- 8/16-bit composite timer ch. 0 output pin (TO00)

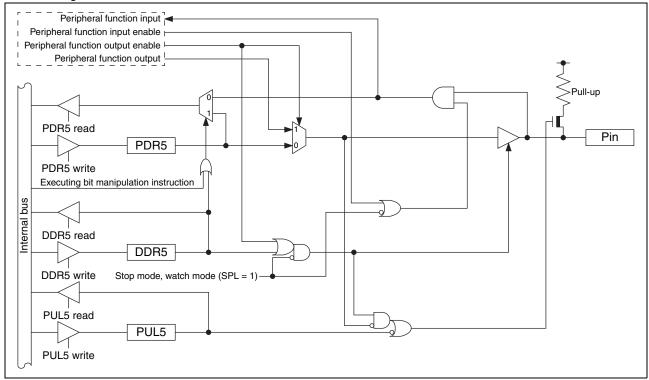
P53/TO0 pin

This pin has the following peripheral function:

• 16-bit reload timer ch. 0 output pin (TO0)



Block diagram of P50/TO01, P51/EC0, P52/TI0/TO00 and P53/TO0



18.5.3 Port 5 registers

• Port 5 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write			
PDR5	0	Pin state is "L" level.	PDR5 value is "0".	As output port, outputs "L" level.			
PDRS	1	Pin state is "H" level.	PDR5 value is "1".	As output port, outputs "H" level.			
DDR5	0		Port input enabled				
DDRS	1		Port output enabled				
PUL5	0		Pull-up disabled				
F ULS	1		Pull-up enabled				

• Correspondence between registers and pins for port 5

		Correspondence between related register bits and pins							
Pin name	•	•	•	-	P53	P52	P51	P50	
PDR5									
DDR5	-	-	-	-	bit3	bit2	bit1	bit0	
PUL5									



18.5.4 Port 5 operations

- Operation as an output port
 - A pin becomes an output port if the bit in the DDR5 register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDR5 register to external pins.
 - If data is written to the PDR5 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDR5 register returns the PDR5 register value.
- · Operation as an input port
 - A pin becomes an input port if the bit in the DDR5 register corresponding to that pin is set to "0".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - If data is written to the PDR5 register, the value is stored in the output latch but is not output to the pin set as an input port.
 - Reading the PDR5 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is
 used to read the PDR5 register, the PDR5 register value is returned.
- Operation as a peripheral function output pin
 - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
 - The pin value can be read from the PDR5 register even if the peripheral function output is enabled. Therefore, the
 output value of a peripheral function can be read by the read operation on the PDR5 register. However, if the readmodify-write (RMW) type of instruction is used to read the PDR5 register, the PDR5 register value is returned.
- Operation as a peripheral function input pin
 - To set a pin as an input port, set the bit in the DDR5 register corresponding to the input pin of a peripheral function to "0".
 - Reading the PDR5 register returns the pin value, regardless of whether the peripheral function uses that pin as its
 input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR5 register, the PDR5
 register value is returned.
- Operation at reset

If the CPU is reset, all bits in the DDR5 register are initialized to "0" and port input is enabled.

- Operation in stop mode and watch mode
 - If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR5 register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.
 - If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.
- Operation of the pull-up register

Setting the bit in the PUL5 register to "1" makes the pull-up resistor be internally connected to the pin. When the pin output is "L" level, the pull-up resistor is disconnected regardless of the value of the PUL5 register.



18.6 Port 6

Port 6 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

18.6.1 Port 6 configuration

Port 6 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 6 data register (PDR6)
- Port 6 direction register (DDR6)

18.6.2 Block diagrams of port 6

P60/SEG10 pin

This pin has the following peripheral function:

- LCDC SEG10 output pin (SEG10)
- P61/SEG11 pin

This pin has the following peripheral function:

- · LCDC SEG11 output pin (SEG11)
- P62/SEG12 pin

This pin has the following peripheral function:

- LCDC SEG12 output pin (SEG12)
- P63/SEG13 pin

This pin has the following peripheral function:

- · LCDC SEG13 output pin (SEG13)
- P64/SEG14 pin

This pin has the following peripheral function:

- LCDC SEG14 output pin (SEG14)
- P65/SEG15 pin

This pin has the following peripheral function:

- LCDC SEG15 output pin (SEG15)
- P66/SEG16 pin

This pin has the following peripheral function:

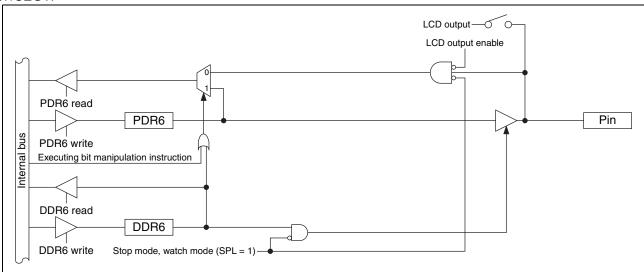
- LCDC SEG16 output pin (SEG16)
- P67/SEG17 pin

This pin has the following peripheral function:

LCDC SEG17 output pin (SEG17)



 Block diagram of P60/SEG10, P61/SEG11, P62/SEG12, P63/SEG13, P64/SEG14, P65/SEG15, P66/SEG16 and P67/SEG17



18.6.3 Port 6 registers

• Port 6 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write			
PDR6	0	Pin state is "L" level.	PDR6 value is "0".	As output port, outputs "L" level.			
	1	Pin state is "H" level.	PDR6 value is "1".	As output port, outputs "H" level.			
DDR6	0	Port input enabled					
	1	Port output enabled					

· Correspondence between registers and pins for port 6

		Correspondence between related register bits and pins									
Pin name	P67	P66	P65	P64	P63	P62	P61	P60			
PDR6	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0			
DDR6											



18.6.4 Port 6 operations

- Operation as an output port
 - A pin becomes an output port if the bit in the DDR6 register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDR6 register to external pins.
 - If data is written to the PDR6 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDR6 register returns the PDR6 register value.
 - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 4 (LCDCE4:SEG[15:10]) or in the LCDC enable register 5 (LCDCE5:SEG[17:16]) to "0" to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LC-DCE1:PICTL) to "1".

· Operation as an input port

- A pin becomes an input port if the bit in the DDR6 register corresponding to that pin is set to "0".
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- If data is written to the PDR6 register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDR6 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is
 used to read the PDR6 register, the PDR6 register value is returned.
- To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 4 (LCDCE4:SEG[15:10]) or in the LCDC enable register 5 (LCDCE5:SEG[17:16]) to "0" to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to "1".

Operation as an LCDC segment output pin

- Set the bit in the DDR6 register corresponding to an LCDC segment output pin to "0".
- To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 4 (LCDCE4:SEG[15:10]) or in the LCDC enable register 5 (LCDCE5:SEG[17:16]) to "1" to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to "1".

Operation at reset

If the CPU is reset, all bits in the DDR6 register are initialized to "0" and port input is enabled.

· Operation in stop mode and watch mode

- If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR6 register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.
- If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.



18.7 Port 9

Port 9 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

18.7.1 Port 9 configuration

Port 9 is made up of the following elements.

- · General-purpose I/O pins/peripheral function I/O pins
- Port 9 data register (PDR9)
- Port 9 direction register (DDR9)

18.7.2 Block diagrams of port 9

P90/V4 pin

This pin has the following peripheral function:

- LCD drive power supply pin (V4)
- P91/V3 pin

This pin has the following peripheral function:

- LCD drive power supply pin (V3)
- P92/V2 pin

This pin has the following peripheral function:

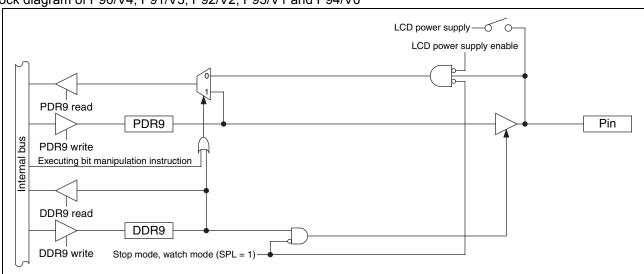
- LCD drive power supply pin (V2)
- P93/V1 pin

This pin has the following peripheral function:

- LCD drive power supply pin (V1)
- P94/V0 pin

This pin has the following peripheral function:

- LCD drive power supply pin (V0)
- Block diagram of P90/V4, P91/V3, P92/V2, P93/V1 and P94/V0





18.7.3 Port 9 registers

Port 9 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write		
PDR9	0	Pin state is "L" level.	PDR9 value is "0".	As output port, outputs "L" level.		
r Diva	1	Pin state is "H" level.	PDR9 value is "1".	As output port, outputs "H" level.		
DDR9	0	Port input enabled				
DDK9	1	Port output enabled				

· Correspondence between registers and pins for port 9

		Correspondence between related register bits and pins								
Pin name	-	-	-	P94	P93	P92	P91	P90		
PDR9			_	bit4	bit3	bit2	bit1	bit0		
DDR9	-	-	-	DIL4	טונט	DILZ	DILI	Dito		

18.7.4 Port 9 operations

- Operation as an output port
 - A pin becomes an output port if the bit in the DDR9 register corresponding to that pin is set to "1".
 - When a pin is used as an output port, it outputs the value of the PDR9 register to external pins.
 - If data is written to the PDR9 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDR9 register returns the PDR9 register value.
 - To use a pin shared with the LCDC as an output port, set the bit corresponding to that pin in the VE[4:0] bits in the LCDC enable register 1 (LCDCE1) to "0" to select the general-purpose I/O port function.
- Operation as an input port
 - A pin becomes an input port if the bit in the DDR9 register corresponding to that pin is set to "0".
 - If data is written to the PDR9 register, the value is stored in the output latch but is not output to the pin set as an input port.
 - Reading the PDR9 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR9 register, the PDR9 register value is returned.
 - To use a pin shared with the LCDC as an input port, set the bit corresponding to that pin in the VE[4:0] bits in the LCDCE1 register to "0" to select the general-purpose I/O port function.
- Operation at reset

If the CPU is reset, all bits in the DDR9 register are initialized to "0" and port input is enabled.

- · Operation in stop mode and watch mode
 - If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR9 register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.
 - If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.
- Operation as an LCD drive power supply pin
 - Set the bit in the DDR9 register corresponding to an LCD drive power supply pin to "0".
 - To use a pin shared with a general-purpose I/O port as an LCD drive power supply pin, set the bit corresponding to that pin in the VE[4:0] bits in the LCDCE1 register to "1" to select the LCD drive power supply function.



18.8 Port A

Port A is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

18.8.1 Port A configuration

Port A is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port A data register (PDRA)
- Port A direction register (DDRA)

18.8.2 Block diagrams of port A

• PA0/COM0 pin

This pin has the following peripheral function:

- LCDC COM0 output pin (COM0)
- PA1/COM1 pin

This pin has the following peripheral function:

- LCDC COM1 output pin (COM1)
- PA2/COM2 pin

This pin has the following peripheral function:

- LCDC COM2 output pin (COM2)
- PA3/COM3 pin

This pin has the following peripheral function:

- LCDC COM3 output pin (COM3)
- PA4/COM4 pin

This pin has the following peripheral function:

- LCDC COM4 output pin (COM4)
- PA5/COM5 pin

This pin has the following peripheral function:

- LCDC COM5 output pin (COM5)
- PA6/COM6 pin

This pin has the following peripheral function:

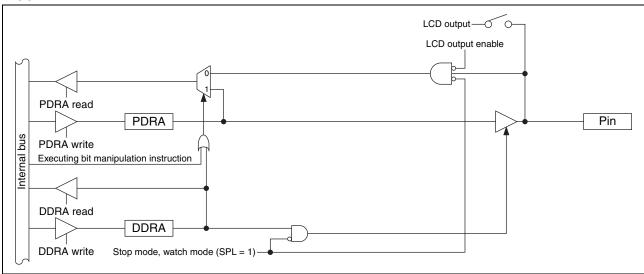
- LCDC COM6 output pin (COM6)
- PA7/COM7 pin

This pin has the following peripheral function:

• LCDC COM7 output pin (COM7)



 Block diagram of PA0/COM0, PA1/COM1, PA2/COM2, PA3/COM3, PA4/COM4, PA5/COM5, PA6/COM6 and PA7/COM7



18.8.3 Port A registers

Port A register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write	
PDRA	0	Pin state is "L" level.	PDRA value is "0".	As output port, outputs "L" level.	
FDRA	1	Pin state is "H" level.	PDRA value is "1".	As output port, outputs "H" level.	
DDRA 0 Port input enabled					
DDRA	1		Port output enable	d	

· Correspondence between registers and pins for port A

		Correspondence between related register bits and pins								
Pin name	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0		
PDRA	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0		
DDRA	DIL!	Dilo	ນແລ	DIL4	טונט	UILZ	DILI	טונט		



18.8.4 Port A operations

- Operation as an output port
 - A pin becomes an output port if the bit in the DDRA register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDRA register to external pins.
 - If data is written to the PDRA register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDRA register returns the PDRA register value.
 - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 2 (LCDCE2:COM[7:0]) to "0" to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to "1".

Operation as an input port

- A pin becomes an input port if the bit in the DDRA register corresponding to that pin is set to "0".
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- If data is written to the PDRA register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDRA register returns the pin value. However, if the read-modify-write (RMW) type of instruction is
 used to read the PDRA register, the PDRA register value is returned.
- To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 2 (LCDCE2:COM[7:0]) to "0" to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to "1".

· Operation as an LCDC common output pin

- Set the bit in the DDRA register corresponding to an LCDC common output pin to "0".
- To use a pin shared with a general-purpose I/O port as an LCDC common output pin, set a corresponding function select bit in the LCDC enable register 2 (LCDCE2:COM[7:0]) to "1" to select the LCDC common output function, and then set the PICTL bit in the LCDCE1 register to "1".

· Operation at reset

If the CPU is reset, all bits in the DDRA register are initialized to "0" and port input is enabled.

· Operation in stop mode and watch mode

- If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRA register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.
- If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

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18.9 Port B

Port B is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

18.9.1 Port B configuration

Port B is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port B data register (PDRB)
- · Port B direction register (DDRB)

18.9.2 Block diagrams of port B

PB0/SEG00 pin

This pin has the following peripheral function:

- LCDC SEG00 output pin (SEG00)
- PB1/SEG01 pin

This pin has the following peripheral function:

- LCDC SEG01 output pin (SEG01)
- PB2/SEG37 pin

This pin has the following peripheral function:

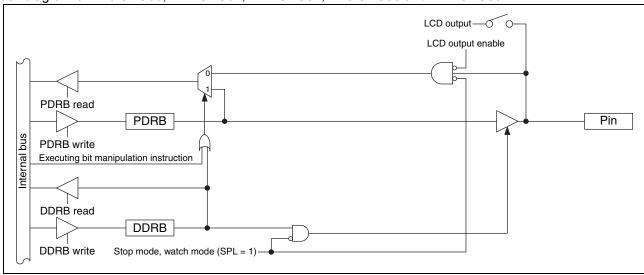
- · LCDC SEG37 output pin (SEG37)
- PB3/SEG38 pin

This pin has the following peripheral function:

- LCDC SEG38 output pin (SEG38)
- · PB4/SEG39 pin

This pin has the following peripheral function:

- LCDC SEG39 output pin (SEG39)
- Block diagram of PB0/SEG00, PB1/SEG01, PB2/SEG37, PB3/SEG38 and PB4/SEG39





18.9.3 Port B registers

Port B register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write	
PDRB	0	Pin state is "L" level.	PDRB value is "0".	As output port, outputs "L" level.	
FDIXB	1	Pin state is "H" level.	PDRB value is "1".	As output port, outputs "H" level.	
DDRB 0 Port input enabled				d	
DDNB	1		Port output enable	d	

Correspondence between registers and pins for port B

		Correspondence between related register bits and pins							
Pin name	-	-	-	PB4	PB3	PB2	PB1	PB0	
PDRB		_	_	bit4	bit3	bit2	bit1	bit0	
DDRB	-	-	-	DIL4	טונט	DILZ	DILI	DILO	

18.9.4 Port B operations

- Operation as an output port
 - A pin becomes an output port if the bit in the DDRB register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDRB register to external pins.
 - If data is written to the PDRB register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDRB register returns the PDRB register value.
 - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[01:00]) or in the LCDC enable register 7 (LCDCE7:SEG[39:37]) to "0" to select the general-purpose I/O port function, and then set the port input control bit (PICTL) in the LCDC enable register 1 (LC-DCE1) to "1".
- Operation as an input port
 - A pin becomes an input port if the bit in the DDRB register corresponding to that pin is set to "0".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - If data is written to the PDRB register, the value is stored in the output latch but is not output to the pin set as an input port.
 - Reading the PDRB register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRB register, the PDRB register value is returned.
 - To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[01:00]) or in the LCDC enable register 7 (LCDCE7:SEG[39:37]) to "0" to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to "1".
- Operation as an LCDC segment output pin
 - Set the bit in the DDRB register corresponding to an LCDC segment output pin to "0".
 - To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[01:00]) or in the LCDC enable register 7 (LCDCE7:SEG[39:37]) to "1" to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to "1".



Operation at reset

If the CPU is reset, all bits in the DDRB register are initialized to "0" and port input is enabled.

- · Operation in stop mode and watch mode
 - If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRB register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.
 - If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

18.10 Port C

Port C is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

18.10.1 Port C configuration

Port C is made up of the following elements.

- · General-purpose I/O pins/peripheral function I/O pins
- Port C data register (PDRC)
- Port C direction register (DDRC)

18.10.2 Block diagrams of port C

PC0/SEG02 pin

This pin has the following peripheral function:

- LCDC SEG02 output pin (SEG02)
- PC1/SEG03 pin

This pin has the following peripheral function:

- LCDC SEG03 output pin (SEG03)
- PC2/SEG04 pin

This pin has the following peripheral function:

- LCDC SEG04 output pin (SEG04)
- PC3/SEG05 pin

This pin has the following peripheral function:

- LCDC SEG05 output pin (SEG05)
- · PC4/SEG06 pin

This pin has the following peripheral function:

- LCDC SEG06 output pin (SEG06)
- PC5/SEG07 pin

This pin has the following peripheral function:

- LCDC SEG07 output pin (SEG07)
- PC6/SEG08 pin

This pin has the following peripheral function:

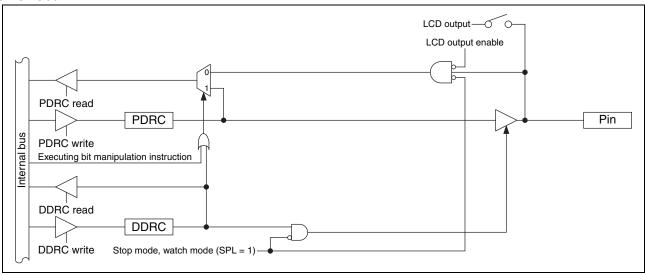
- LCDC SEG08 output pin (SEG08)
- PC7/SEG09 pin

This pin has the following peripheral function:

LCDC SEG09 output pin (SEG09)



 Block diagram of PC0/SEG02, PC1/SEG03, PC2/SEG04, PC3/SEG05, PC4/SEG06, PC5/SEG07, PC6/SEG08 and PC7/SEG09



18.10.3 Port C registers

• Port C register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write				
PDRC	0	Pin state is "L" level.	PDRC value is "0".	As output port, outputs "L" level.				
FDRC	1	Pin state is "H" level.	PDRC value is "1".	As output port, outputs "H" level.				
DDRC	0		Port input enabled					
DDRC	1		Port output enable	d				

· Correspondence between registers and pins for port C

		Correspondence between related register bits and pins							
Pin name	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	
PDRC	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
DDRC	DIL!	Dilo	טונט	DIL4	טונט	DILZ	DILI	DilU	



18.10.4 Port C operations

- Operation as an output port
 - A pin becomes an output port if the bit in the DDRC register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDRC register to external pins.
 - If data is written to the PDRC register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDRC register returns the PDRC register value.
 - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:02]) or in the LCDC enable register 4 (LCDCE4:SEG[09:08]) to "0" to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LC-DCE1:PICTL) to "1".

· Operation as an input port

- A pin becomes an input port if the bit in the DDRC register corresponding to that pin is set to "0".
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- If data is written to the PDRC register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDRC register returns the pin value. However, if the read-modify-write (RMW) type of instruction is
 used to read the PDRC register, the PDRC register value is returned.
- To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:02]) or in the LCDC enable register 4 (LCDCE4:SEG[09:08]) to "0" to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to "1".

Operation as an LCDC segment output pin

- Set the bit in the DDRC register corresponding to an LCDC segment output pin to "0".
- To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:02]) or in the LCDC enable register 4 (LCDCE4:SEG[09:08]) to "1" to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to "1".

Operation at reset

If the CPU is reset, all bits in the DDRC register are initialized to "0" and port input is enabled.

Operation in stop mode and watch mode

- If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRC register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.
- If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.



18.11 Port E

Port E is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

18.11.1 Port E configuration

Port E is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port E data register (PDRE)
- Port E direction register (DDRE)

18.11.2 Block diagrams of port E

PE0/SEG22 pin

This pin has the following peripheral function:

- LCDC SEG22 output pin (SEG22)
- PE1/SEG23 pin

This pin has the following peripheral function:

- LCDC SEG23 output pin (SEG23)
- PE2/SEG24 pin

This pin has the following peripheral function:

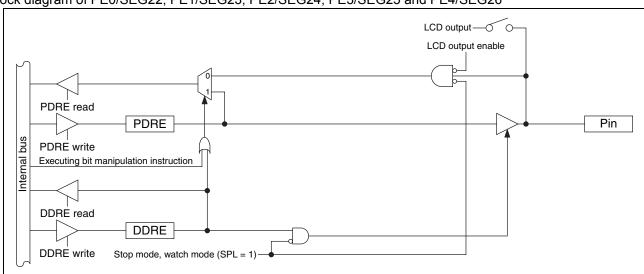
- LCDC SEG24 output pin (SEG24)
- PE3/SEG25 pin

This pin has the following peripheral function:

- LCDC SEG25 output pin (SEG25)
- PE4/SEG26 pin

This pin has the following peripheral function:

- LCDC SEG26 output pin (SEG26)
- Block diagram of PE0/SEG22, PE1/SEG23, PE2/SEG24, PE3/SEG25 and PE4/SEG26





• PE5/SEG27/TO11 pin

This pin has the following peripheral functions:

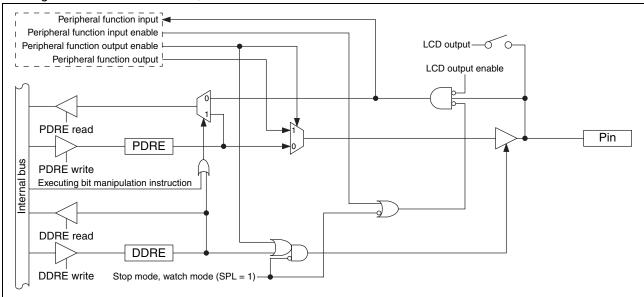
- LCDC SEG27 output pin (SEG27)
- 8/16-bit composite timer ch. 1 output pin (TO11)
- PE6/SEG28/TO10 pin

This pin has the following peripheral functions:

- LCDC SEG28 output pin (SEG28)
- 8/16-bit composite timer ch. 1 output pin (TO10)
- PE7/SEG29/EC1 pin

This pin has the following peripheral functions:

- LCDC SEG29 output pin (SEG29)
- 8/16-bit composite timer ch. 1 clock input pin (EC1)
- Block diagram of PE5/SEG27/TO11, PE6/SEG28/TO10 and PE7/SEG29/EC1



18.11.3 Port E registers

· Port E register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write				
PDRE	0	Pin state is "L" level.	PDRE value is "0".	As output port, outputs "L" level.				
FUNE	1	Pin state is "H" level.	PDRE value is "1".	As output port, outputs "H" level.				
DDRE	0		Port input enabled					
DUKE	1		Port output enable	d				

Correspondence between registers and pins for port E

		Correspondence between related register bits and pins							
Pin name	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	
PDRE	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
DDRE	DIL!	Dito	טונט	DIL4	טונט	DILZ	DILI	טונט	



18.11.4 Port E operations

- Operation as an output port
 - A pin becomes an output port if the bit in the DDRE register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDRE register to external pins.
 - If data is written to the PDRE register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - · Reading the PDRE register returns the PDRE register value.
 - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[23:22]) or in the LCDC enable register 6 (LCDCE6:SEG[29:24]) to "0" to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LC-DCE1:PICTL) to "1".

· Operation as an input port

- A pin becomes an input port if the bit in the DDRE register corresponding to that pin is set to "0".
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- If data is written to the PDRE register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDRE register returns the pin value. However, if the read-modify-write (RMW) type of instruction is
 used to read the PDRE register, the PDRE register value is returned.
- To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[23:22]) or in the LCDC enable register 6 (LCDCE6:SEG[29:24]) to "0" to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to "1".

Operation as a peripheral function output pin

- A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- The pin value can be read from the PDRE register even if the peripheral function output is enabled. Therefore, the
 output value of a peripheral function can be read by the read operation on the PDRE register. However, if the readmodify-write (RMW) type of instruction is used to read the PDRE register, the PDRE register value is returned.

· Operation as a peripheral function input pin

- To set a pin as an input port, set the bit in the DDRE register corresponding to the input pin of a peripheral function to "0".
- Reading the PDRE register returns the pin value, regardless of whether the peripheral function uses that pin as its
 input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDRE register, the PDRE
 register value is returned.

Operation as an LCDC segment output pin

- Set the bit in the DDRE register corresponding to an LCDC segment output pin to "0".
- To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[23:22]) or in the LCDC enable register 6 (LC-DCE6:SEG[29:24]) to "1" to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to "1".

Operation at reset

If the CPU is reset, all bits in the DDRE register are initialized to "0" and port input is enabled.

· Operation in stop mode and watch mode

• If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRE register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.



• If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

18.12 Port F

Port F is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

18.12.1 Port F configuration

Port F is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port F data register (PDRF)
- Port F direction register (DDRF)

18.12.2 Block diagrams of port F

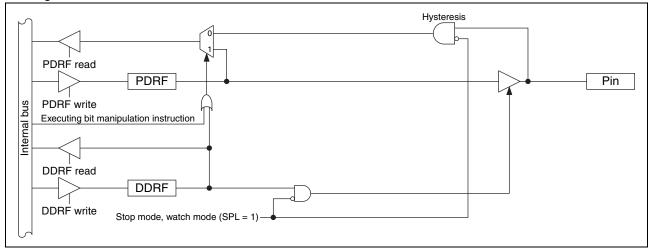
PF0/X0 pin

This pin has the following peripheral function:

- Main clock input oscillation pin (X0)
- PF1/X1 pin

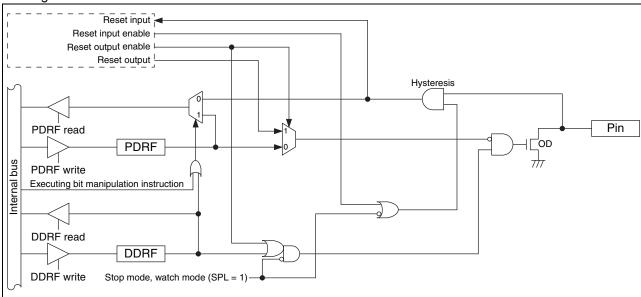
This pin has the following peripheral function:

- Main clock I/O oscillation pin (X1)
- Block diagram of PF0/X0 and PF1/X1





- PF2/RST pin
 - This pin has the following peripheral function:
 - Reset pin (RST)
- Block diagram of PF2/RST



18.12.3 Port F registers

• Port F register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write	
PDRF	0	Pin state is "L" level.	PDRF value is "0".	As output port, outputs "L" level.	
FURF	1	Pin state is "H" level.	PDRF value is "1".	As output port, outputs "H" level.*	
DDRF	d				
DDRF	1		Port output enable	d	

^{*:} If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

· Correspondence between registers and pins for port F

		Correspondence between related register bits and pins								
Pin name	-	-	-	-	-	PF2*	PF1	PF0		
PDRF						bit2	bit1	bit0		
DDRF	1	-	-	-	1	DILZ	DILI	DILU		

^{*:} PF2/RST is the dedicated reset pin on MB95F714M/F716M/F718M.



18.12.4 Port F operations

- Operation as an output port
 - A pin becomes an output port if the bit in the DDRF register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDRF register to external pins.
 - If data is written to the PDRF register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - · Reading the PDRF register returns the PDRF register value.
- · Operation as an input port
 - A pin becomes an input port if the bit in the DDRF register corresponding to that pin is set to "0".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - If data is written to the PDRF register, the value is stored in the output latch but is not output to the pin set as an input port.
 - Reading the PDRF register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRF register, the PDRF register value is returned.
- Operation at reset

If the CPU is reset, all bits in the DDRF register are initialized to "0" and port input is enabled.

- · Operation in stop mode and watch mode
 - If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop
 mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRF register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.
 - If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

18.13 Port G

Port G is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

18.13.1 Port G configuration

Port G is made up of the following elements.

- · General-purpose I/O pins/peripheral function I/O pins
- Port G data register (PDRG)
- Port G direction register (DDRG)
- · Port G pull-up register (PULG)

18.13.2 Block diagram of port G

PG1/X0A pin

This pin has the following peripheral function:

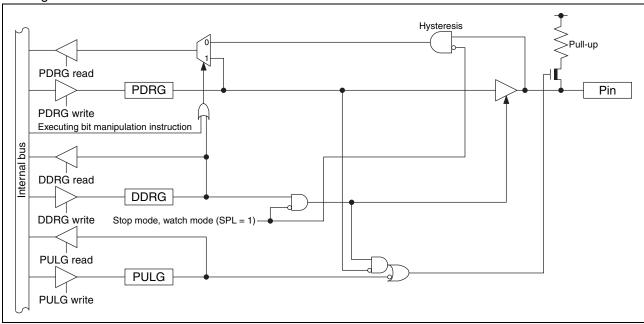
- Subclock input oscillation pin (X0A)
- PG2/X1A pin

This pin has the following peripheral function:

Subclock I/O oscillation pin (X1A)



· Block diagram of PG1/X0A and PG2/X1A



18.13.3 Port G registers

• Port G register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write					
PDRG	0	Pin state is "L" level.	PDRG value is "0".	As output port, outputs "L" level.					
FBRG	1	Pin state is "H" level.	PDRG value is "1".	As output port, outputs "H" level.					
DDRG	0		Port input enabled	1					
DDRG	1		Port output enable	d					
PULG	0		Pull-up disabled						
FOLG	1		Pull-up enabled						

• Correspondence between registers and pins for port G

		Correspondence between related register bits and pins						
Pin name	-	-	-	-	-	PG2	PG1	-
PDRG								
DDRG	-	-	-	-	-	bit2	bit1	-
PULG								



18.13.4 Port G operations

- · Operation as an output port
 - A pin becomes an output port if the bit in the DDRG register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDRG register to external pins.
 - If data is written to the PDRG register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - · Reading the PDRG register returns the PDRG register value.
- · Operation as an input port
 - A pin becomes an input port if the bit in the DDRG register corresponding to that pin is set to "0".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - If data is written to the PDRG register, the value is stored in the output latch but is not output to the pin set as an input port.
 - Reading the PDRG register returns the pin value. However, if the read-modify-write (RMW) type of instruction is
 used to read the PDRG register, the PDRG register value is returned.
- Operation at reset

If the CPU is reset, all bits in the DDRG register are initialized to "0" and port input is enabled.

- · Operation in stop mode and watch mode
 - If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRG register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.
 - If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.
- Operation of the pull-up register

Setting the bit in the PULG register to "1" makes the pull-up resistor be internally connected to the pin. When the pin output is "L" level, the pull-up resistor is disconnected regardless of the value of the PULG register.

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19. I/O Ports (MB95770M Series)

· List of port registers

Register name		Read/Write	Initial value
Port 0 data register	PDR0	R, RM/W	0b00000000
Port 0 direction register	DDR0	R/W	0b00000000
Port 1 data register	PDR1	R, RM/W	0b00000000
Port 1 direction register	DDR1	R/W	0b00000000
Port 2 data register	PDR2	R, RM/W	0b00000000
Port 2 direction register	DDR2	R/W	0b00000000
Port 6 data register	PDR6	R, RM/W	0b00000000
Port 6 direction register	DDR6	R/W	0b00000000
Port 9 data register	PDR9	R, RM/W	0b00000000
Port 9 direction register	DDR9	R/W	0b00000000
Port A data register	PDRA	R, RM/W	0b00000000
Port A direction register	DDRA	R/W	0b0000000
Port B data register	PDRB	R, RM/W	0b00000000
Port B direction register	DDRB	R/W	0b00000000
Port C data register	PDRC	R, RM/W	0b00000000
Port C direction register	DDRC	R/W	0b00000000
Port E data register	PDRE	R, RM/W	0b00000000
Port E direction register	DDRE	R/W	0b0000000
Port F data register	PDRF	R, RM/W	000000000
Port F direction register	DDRF	R/W	0b00000000
Port G data register	PDRG	R, RM/W	0b00000000
Port G direction register	DDRG	R/W	0b0000000
Port 1 pull-up register	PUL1	R/W	0b0000000
Port 2 pull-up register	PUL2	R/W	0b0000000
Port G pull-up register	PULG	R/W	0b0000000
A/D input disable register (lower)	AIDRL	R/W	0b0000000

R/W : Readable/writable (The read value is the same as the write value.)

R, RM/W: Readable/writable (The read value is different from the write value. The write value is read by the read-modify-write (RMW) type of instruction.)



19.1 Port 0

Port 0 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

19.1.1 Port 0 configuration

Port 0 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 0 data register (PDR0)
- Port 0 direction register (DDR0)
- A/D input disable register (lower) (AIDRL)

19.1.2 Block diagrams of port 0

P00/INT00/AN00/SEG29/UO2 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT00)
- 8/12-bit A/D converter analog input pin (AN00)
- LCDC SEG29 output pin (SEG29)
- UART/SIO ch. 2 data output pin (UO2)

• P02/INT02/AN02/SEG27/UCK2 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT02)
- 8/12-bit A/D converter analog input pin (AN02)
- · LCDC SEG27 output pin (SEG27)
- UART/SIO ch. 2 clock I/O pin (UCK2)

P03/INT03/AN03/SEG26/UO1 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT03)
- 8/12-bit A/D converter analog input pin (AN03)
- LCDC SEG26 output pin (SEG26)
- UART/SIO ch. 1 data output pin (UO1)

P05/INT05/AN05/SEG24/UCK1 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT05)
- 8/12-bit A/D converter analog input pin (AN05)
- LCDC SEG24 output pin (SEG24)
- UART/SIO ch. 1 clock I/O pin (UCK1)

P06/INT06/AN06/SEG23 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT06)
- 8/12-bit A/D converter analog input pin (AN06)
- LCDC SEG23 output pin (SEG23)

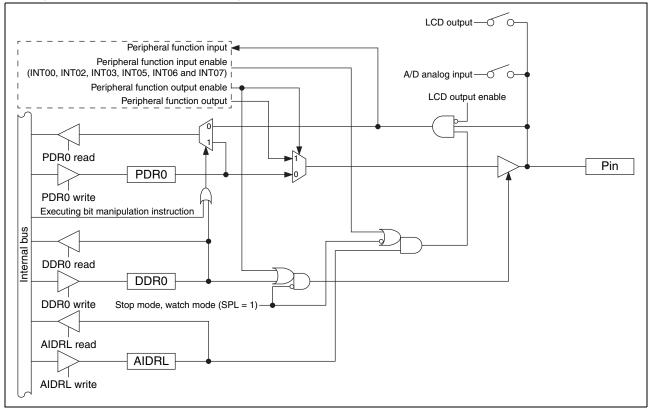
• P07/INT07/AN07/SEG22 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT07)
- 8/12-bit A/D converter analog input pin (AN07)
- LCDC SEG22 output pin (SEG22)



Block diagram of P00/INT00/AN00/SEG29/UO2, P02/INT02/AN02/SEG27/UCK2, P03/INT03/AN03/SEG26/UO1, P05/INT05/AN05/SEG24/UCK1, P06/INT06/AN06/SEG23 and P07/INT07/AN07/SEG22



• P01/INT01/AN01/SEG28/TO00/UI2 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT01)
- 8/12-bit A/D converter analog input pin (AN01)
- LCDC SEG28 output pin (SEG28)
- 8/16-bit composite timer ch. 0 output pin (TO00)
- UART/SIO ch. 2 data input pin (UI2)

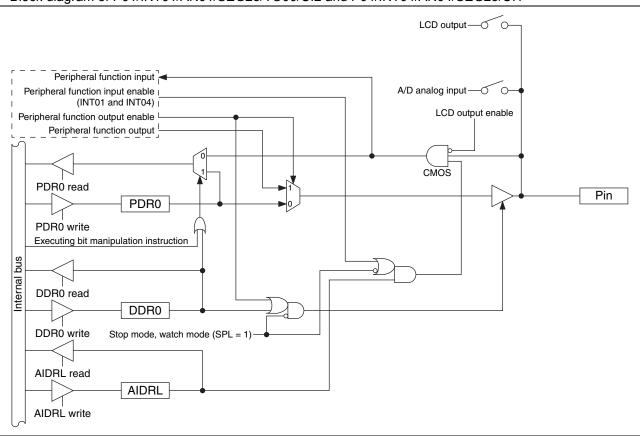
• P04/INT04/AN04/SEG25/UI1 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT04)
- 8/12-bit A/D converter analog input pin (AN04)
- LCDC SEG25 output pin (SEG25)
- UART/SIO ch. 1 data input pin (UI1)



Block diagram of P01/INT01/AN01/SEG28/T000/UI2 and P04/INT04/AN04/SEG25/UI1



19.1.3 Port 0 registers

Port 0 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write					
PDR0	0	Pin state is "L" level.	PDR0 value is "0".	As output port, outputs "L" level.					
FDRU	1	Pin state is "H" level.	PDR0 value is "1".	As output port, outputs "H" level.					
DDR0	0	Port input enabled							
DDRO	1		Port output enable	d					
AIDRL	0		Analog input enabled						
AIDKL	1		Port input enabled	d					

• Correspondence between registers and pins for port 0

	Correspondence between related register bits and pins							
Pin name	P07	P06	P05	P04	P03	P02	P01	P00
PDR0								
DDR0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
AIDRL								



19.1.4 Port 0 operations

- · Operation as an output port
 - · A pin becomes an output port if the bit in the DDR0 register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDR0 register to external pins.
 - If data is written to the PDR0 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDR0 register returns the PDR0 register value.
 - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[23:22]) or in the LCDC enable register 6 (LCDCE6:SEG[29:24]) to "0" to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LC-DCE1:PICTL) to "1".

· Operation as an input port

- A pin becomes an input port if the bit in the DDR0 register corresponding to that pin is set to "0".
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- When using an analog input shared pin as an input port, set the corresponding bit in the A/D input disable register (lower) (AIDRL) to "1".
- If data is written to the PDR0 register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDR0 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.
- To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[23:22]) or in the LCDC enable register 6 (LCDCE6:SEG[29:24]) to "0" to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to "1".

Operation as a peripheral function output pin

- A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- The pin value can be read from the PDR0 register even if the peripheral function output is enabled. Therefore, the
 output value of a peripheral function can be read by the read operation on the PDR0 register. However, if the readmodify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

• Operation as a peripheral function input pin

- To set a pin as an input port, set the bit in the DDR0 register corresponding to the input pin of a peripheral function to "0".
- When using the analog input shared pin as another peripheral function input pin, configure it as an input port, which
 is the same as the operation as an input port.
- Reading the PDR0 register returns the pin value, regardless of whether the peripheral function uses that pin as its
 input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0
 register value is returned.

· Operation as an LCDC segment output pin

- Set the bit in the DDR0 register corresponding to an LCDC segment output pin to "0".
- To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 5 (LCDCE5:SEG[23:22]) or in the LCDC enable register 6 (LCDCE6:SEG[29:24]) to "1" to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to "1".

Operation at reset

If the CPU is reset, all bits in the DDR0 register are initialized to "0" and port input is enabled. As for a pin shared with analog input, its port input is disabled because the AIDRL register is initialized to "0".

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- · Operation in stop mode and watch mode
 - If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR0 register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open. However, if the interrupt input is enabled for the external interrupt (INT00 to INT07), the input is enabled and not blocked.
 - If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.
- · Operation as an analog input pin
 - Set the bit in the DDR0 register bit corresponding to the analog input pin to "0" and the bit corresponding to that pin in the AIDRL register to "0".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- Operation as an external interrupt input pin
 - Set the bit in the DDR0 register corresponding to the external interrupt input pin to "0".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - The pin value is always input to the external interrupt circuit. When using a pin for a function other than the interrupt, disable the external interrupt function corresponding to that pin.

19.2 Port 1

Port 1 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

19.2.1 Port 1 configuration

Port 1 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 1 data register (PDR1)
- Port 1 direction register (DDR1)
- Port 1 pull-up register (PUL1)

19.2.2 Block diagrams of port 1

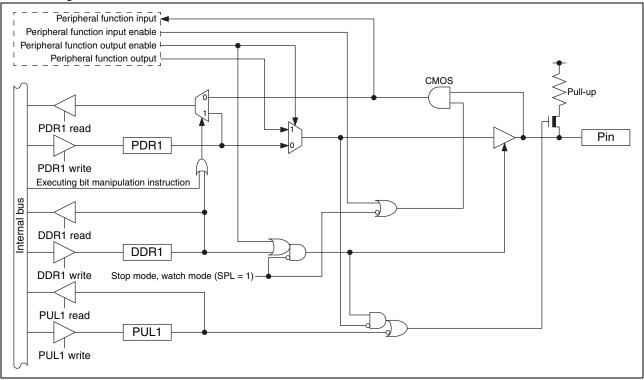
P10/UI0/TO0 pin

This pin has the following peripheral functions:

- UART/SIO ch. 0 data input pin (UI0)
- 16-bit reload timer ch. 0 output pin (TO0)



Block diagram of P10/UI0/TO0

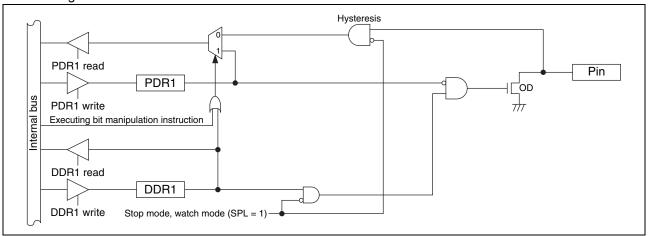


• P12/DBG pin

This pin has the following peripheral function:

• DBG input pin (DBG)

· Block diagram of P12/DBG





• P11/UO0 pin

This pin has the following peripheral function:

• UART/SIO ch. 0 data output pin (UO0)

• P13/ADTG/TO01 pin

This pin has the following peripheral functions:

- 8/12-bit A/D converter trigger input pin (ADTG)
- 8/16-bit composite timer ch. 0 output pin (TO01)

• P14/UCK0/EC0/TI0 pin

This pin has the following peripheral functions:

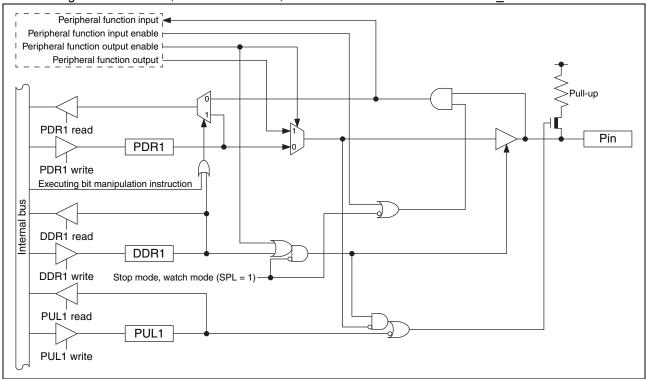
- UART/SIO ch. 0 clock I/O pin (UCK0)
- 8/16-bit composite timer ch. 0 clock input pin (EC0)
- 16-bit reload timer ch. 0 input pin (TI0)

• P17/CMP0_O pin

This pin has the following peripheral function:

• Comparator ch. 0 digital output pin (CMP0_O)

Block diagram of P11/UO0, P13/ADTG/TO01, P14/UCK0/EC0/TI0 and P17/CMP0_O





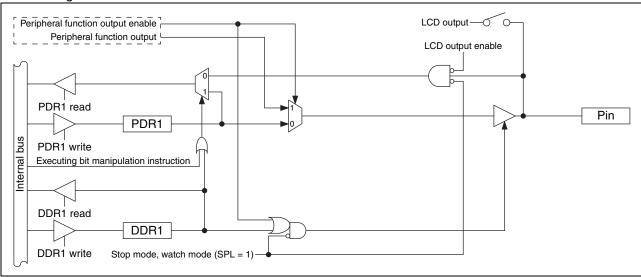
• P15/SEG31/PPG11 pin

This pin has the following peripheral functions:

- LCDC SEG31 output pin (SEG31)
- 8/16-bit PPG ch. 1 output pin (PPG11)
- P16/SEG30/PPG10 pin

This pin has the following peripheral functions:

- LCDC SEG30 output pin (SEG30)
- 8/16-bit PPG ch. 1 output pin (PPG10)
- Block diagram of P15/SEG31/PPG11 and P16/SEG30/PPG10



19.2.3 Port 1 registers

• Port 1 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write					
PDR1	0	Pin state is "L" level.	PDR1 value is "0".	As output port, outputs "L" level.					
PDKI	1	Pin state is "H" level.	PDR1 value is "1".	As output port, outputs "H" level.*					
DDR1	0		Port input enabled	d					
DDK1	1		Port output enable	d					
PUL1	0		Pull-up disabled						
FULI	1		Pull-up enabled						

^{*:} If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

· Correspondence between registers and pins for port 1

	Correspondence between related register bits and pins							
Pin name	P17	P16	P15	P14	P13	P12	P11	P10
PDR1		bit6	bit5			bit2		
DDR1	bit7	Dito	טונט	bit4	bit3	DILZ	bit1	bit0
PUL1		-	-			-		

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19.2.4 Port 1 operations

- Operation as an output port
 - A pin becomes an output port if the bit in the DDR1 register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDR1 register to external pins.
 - If data is written to the PDR1 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDR1 register returns the PDR1 register value.
 - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 6 (LCDCE6:SEG[31:30]) to "0" to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to "1".

Operation as an input port

- A pin becomes an input port if the bit in the DDR1 register corresponding to that pin is set to "0".
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- If data is written to the PDR1 register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDR1 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is
 used to read the PDR1 register, the PDR1 register value is returned.
- To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 6 (LCDCE6:SEG[31:30]) to "0" to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to "1".

· Operation as a peripheral function output pin

- A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- The pin value can be read from the PDR1 register even if the peripheral function output is enabled. Therefore, the
 output value of a peripheral function can be read by the read operation on the PDR1 register. However, if the readmodify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

· Operation as a peripheral function input pin

- To set a pin as an input port, set the bit in the DDR1 register corresponding to the input pin of a peripheral function to "0".
- Reading the PDR1 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

· Operation as an LCDC segment output pin

- Set the bit in the DDR1 register corresponding to an LCDC segment output pin to "0".
- To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 6 (LCDCE6:SEG[31:30]) to "1" to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to "1".

Operation at reset

If the CPU is reset, all bits in the DDR1 register are initialized to "0" and port input is enabled.

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- · Operation in stop mode and watch mode
 - If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR1 register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open. However, if the interrupt input of P10/UI0/TO0 and P14/UCK0/EC0/TI0 is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
 - If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.
- · Operation of the pull-up register

Setting the bit in the PUL1 register to "1" makes the pull-up resistor be internally connected to the pin. When the pin output is "L" level, the pull-up resistor is disconnected regardless of the value of the PUL1 register.

19.3 Port 2

Port 2 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

19.3.1 Port 2 configuration

Port 2 is made up of the following elements.

- · General-purpose I/O pins/peripheral function I/O pins
- Port 2 data register (PDR2)
- Port 2 direction register (DDR2)
- Port 2 pull-up register (PUL2)

19.3.2 Block diagrams of port 2

P20/PPG00/CMP0 N pin

This pin has the following peripheral functions:

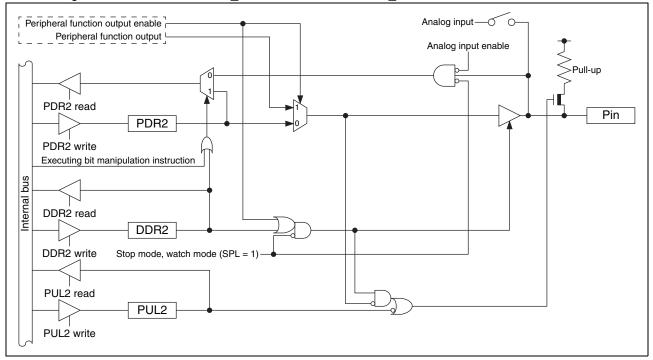
- 8/16-bit PPG ch. 0 output pin (PPG00)
- Comparator ch. 0 inverting analog input (negative input) pin (CMP0_N)
- P21/PPG01/CMP0 P pin

This pin has the following peripheral functions:

- 8/16-bit PPG ch. 0 output pin (PPG01)
- Comparator ch. 0 non-inverting analog input (positive input) pin (CMP0 P)



Block diagram of P20/PPG00/CMP0_N and P21/PPG01/CMP0_P



· P22/SCL pin

This pin has the following peripheral function:

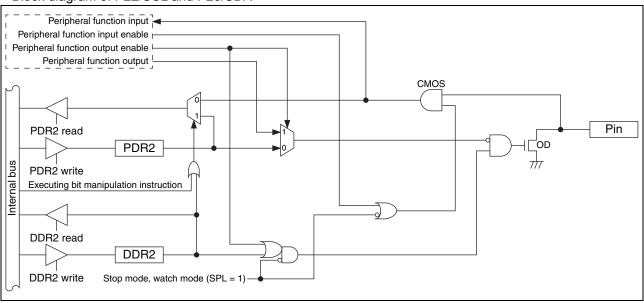
• I2C bus interface ch. 0 clock I/O pin (SCL)

• P23/SDA pin

This pin has the following peripheral function:

• I2C bus interface ch. 0 data I/O pin (SDA)

· Block diagram of P22/SCL and P23/SDA





19.3.3 Port 2 registers

· Port 2 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write					
PDR2	0	Pin state is "L" level.	PDR2 value is "0".	As output port, outputs "L" level.					
FDI	1	Pin state is "H" level.	PDR2 value is "1".	As output port, outputs "H" level.*					
DDR2	0		Port input enabled	d					
DDRZ	1		Port output enable	d					
PUL2	0		Pull-up disabled						
F OLZ	1		Pull-up enabled						

^{*:} If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

· Correspondence between registers and pins for port 2

		Correspondence between related register bits and pins							
Pin name	-	-	-	-	P23	P22	P21	P20	
PDR2					bit3	bit2			
DDR2	-	-	-	-	มแจ	DILZ	bit1	bit0	
PUL2					-	-			

19.3.4 Port 2 operations

- · Operation as an output port
 - A pin becomes an output port if the bit in the DDR2 register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDR2 register to external pins.
 - If data is written to the PDR2 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDR2 register returns the PDR2 register value.
- Operation as an input port
 - A pin becomes an input port if the bit in the DDR2 register corresponding to that pin is set to "0".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - If data is written to the PDR2 register, the value is stored in the output latch but is not output to the pin set as an input port.
 - Reading the PDR2 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR2 register, the PDR2 register value is returned.
- Operation as a peripheral function output pin
 - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
 - The pin value can be read from the PDR2 register even if the peripheral function output is enabled. Therefore, the
 output value of a peripheral function can be read by the read operation on the PDR2 register. However, if the readmodify-write (RMW) type of instruction is used to read the PDR2 register, the PDR2 register value is returned.
- · Operation as a peripheral function input pin
 - To set a pin as an input port, set the bit in the DDR2 register corresponding to the input pin of a peripheral function to "0".



- Reading the PDR2 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR2 register, the PDR2 register value is returned.
- · Operation at reset

If the CPU is reset, all bits in the DDR2 register are initialized to "0" and port input is enabled.

- · Operation in stop mode and watch mode
 - If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR2 register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.
 - If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.
- Operation of the pull-up register

Setting the bit in the PUL2 register to "1" makes the pull-up resistor be internally connected to the pin. When the pin output is "L" level, the pull-up resistor is disconnected regardless of the value of the PUL2 register.

- Operation as a comparator input pin
 - Regardless of the value of the PDR2 register and that of the DDR2 register, if the comparator analog input enable bit in the comparator control register ch. 0 (CMR0:VCID) is set to "0", the comparator input function is enabled.
 - To disable the comparator input function, set the VCID bit to "1".
 - For details of the comparator, refer to "CHAPTER 29 COMPARATOR" in "New 8FX MB95710M/770M Series Hardware Manual".

19.4 Port 6

Port 6 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

19.4.1 Port 6 configuration

Port 6 is made up of the following elements.

- · General-purpose I/O pins/peripheral function I/O pins
- Port 6 data register (PDR6)
- Port 6 direction register (DDR6)

19.4.2 Block diagrams of port 6

P60/SEG06 pin

This pin has the following peripheral function:

- LCDC SEG06 output pin (SEG06)
- P61/SEG07 pin

This pin has the following peripheral function:

- LCDC SEG07 output pin (SEG07)
- P62/SEG08 pin

This pin has the following peripheral function:

- LCDC SEG08 output pin (SEG08)
- P63/SEG09 pin

This pin has the following peripheral function:

LCDC SEG09 output pin (SEG09)



• P64/SEG10 pin

This pin has the following peripheral function:

- LCDC SEG10 output pin (SEG10)
- P65/SEG11 pin

This pin has the following peripheral function:

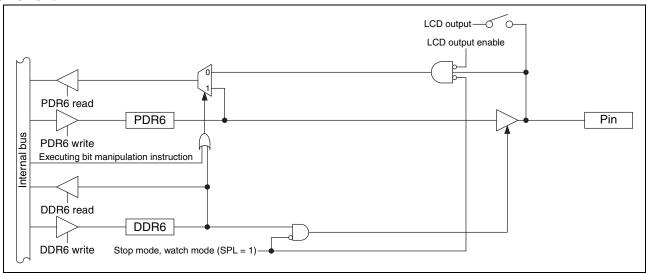
- LCDC SEG11 output pin (SEG11)
- P66/SEG12 pin

This pin has the following peripheral function:

- LCDC SEG12 output pin (SEG12)
- P67/SEG13 pin

This pin has the following peripheral function:

- LCDC SEG13 output pin (SEG13)
- Block diagram of P60/SEG06, P61/SEG07, P62/SEG08, P63/SEG09, P64/SEG10, P65/SEG11, P66/SEG12 and P67/SEG13



19.4.3 Port 6 registers

• Port 6 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write					
PDR6	0	Pin state is "L" level.	PDR6 value is "0".	As output port, outputs "L" level.					
FBRO	1	Pin state is "H" level.	PDR6 value is "1".	As output port, outputs "H" level.					
DDR6	0		Port input enabled						
DDR0	1		Port output enable	d					

· Correspondence between registers and pins for port 6

		Correspondence between related register bits and pins						
Pin name	P67	P67 P66 P65 P64 P63 P62 P61 P60						
PDR6	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR6	DILI	bilo	טונט	DIL4	טונס	DILZ	DILI	bito



19.4.4 Port 6 operations

- Operation as an output port
 - A pin becomes an output port if the bit in the DDR6 register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDR6 register to external pins.
 - If data is written to the PDR6 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDR6 register returns the PDR6 register value.
 - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:06]) or in the LCDC enable register 4 (LCDCE4:SEG[13:08]) to "0" to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LC-DCE1:PICTL) to "1".

· Operation as an input port

- A pin becomes an input port if the bit in the DDR6 register corresponding to that pin is set to "0".
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- If data is written to the PDR6 register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDR6 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is
 used to read the PDR6 register, the PDR6 register value is returned.
- To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:06]) or in the LCDC enable register 4 (LCDCE4:SEG[13:08]) to "0" to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to "1".

Operation as an LCDC segment output pin

- Set the bit in the DDR6 register corresponding to an LCDC segment output pin to "0".
- To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[07:06]) or in the LCDC enable register 4 (LCDCE4:SEG[13:08]) to "1" to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to "1".

Operation at reset

If the CPU is reset, all bits in the DDR6 register are initialized to "0" and port input is enabled.

Operation in stop mode and watch mode

- If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR6 register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.
- If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.



19.5 Port 9

Port 9 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

19.5.1 Port 9 configuration

Port 9 is made up of the following elements.

- · General-purpose I/O pins/peripheral function I/O pins
- Port 9 data register (PDR9)
- Port 9 direction register (DDR9)

19.5.2 Block diagrams of port 9

• P90/V4 pin

This pin has the following peripheral function:

- LCD drive power supply pin (V4)
- P91/V3 pin

This pin has the following peripheral function:

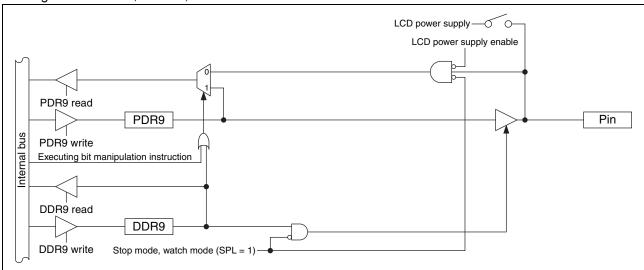
- LCD drive power supply pin (V3)
- P92/V2 pin

This pin has the following peripheral function:

- LCD drive power supply pin (V2)
- P93/V1 pin

This pin has the following peripheral function:

- LCD drive power supply pin (V1)
- Block diagram of P90/V4, P91/V3, P92/V2 and P93/V1





19.5.3 Port 9 registers

Port 9 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write					
PDR9	0	Pin state is "L" level.	PDR9 value is "0".	As output port, outputs "L" level.					
I DIG	1	Pin state is "H" level.	PDR9 value is "1".	As output port, outputs "H" level.					
DDR9	0		Port input enabled						
DDK9	1		Port output enable	d					

· Correspondence between registers and pins for port 9

	Correspondence between related register bits and pins							
Pin name	-	=	=	-	P93	P92	P91	P90
PDR9	_	-	-	-	bit3	bit2	bit1	bit0
DDR9								

19.5.4 Port 9 operations

- Operation as an output port
 - A pin becomes an output port if the bit in the DDR9 register corresponding to that pin is set to "1".
 - When a pin is used as an output port, it outputs the value of the PDR9 register to external pins.
 - If data is written to the PDR9 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDR9 register returns the PDR9 register value.
 - To use a pin shared with the LCDC as an output port, set the bit corresponding to that pin in the VE[4:1] bits in the LCDC enable register 1 (LCDCE1) to "0" to select the general-purpose I/O port function.

Operation as an input port

- A pin becomes an input port if the bit in the DDR9 register corresponding to that pin is set to "0".
- If data is written to the PDR9 register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDR9 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR9 register, the PDR9 register value is returned.
- To use a pin shared with the LCDC as an input port, set the bit corresponding to that pin in the VE[4:1] bits in the LCDCE1 register to "0" to select the general-purpose I/O port function.

Operation at reset

If the CPU is reset, all bits in the DDR9 register are initialized to "0" and port input is enabled.

- Operation in stop mode and watch mode
 - If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR9 register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.
 - If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.
- Operation as an LCD drive power supply pin
 - Set the bit in the DDR9 register corresponding to an LCD drive power supply pin to "0".
 - To use a pin shared with a general-purpose I/O port as an LCD drive power supply pin, set the bit corresponding to that pin in the VE[4:1] bits in the LCDCE1 register to "1" to select the LCD drive power supply function.



19.6 Port A

Port A is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

19.6.1 Port A configuration

Port A is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port A data register (PDRA)
- Port A direction register (DDRA)

19.6.2 Block diagrams of port A

• PA0/COM0 pin

This pin has the following peripheral function:

- LCDC COM0 output pin (COM0)
- PA1/COM1 pin

This pin has the following peripheral function:

- LCDC COM1 output pin (COM1)
- PA2/COM2 pin

This pin has the following peripheral function:

- LCDC COM2 output pin (COM2)
- PA3/COM3 pin

This pin has the following peripheral function:

- LCDC COM3 output pin (COM3)
- PA4/COM4 pin

This pin has the following peripheral function:

- LCDC COM4 output pin (COM4)
- PA5/COM5 pin

This pin has the following peripheral function:

- LCDC COM5 output pin (COM5)
- PA6/COM6 pin

This pin has the following peripheral function:

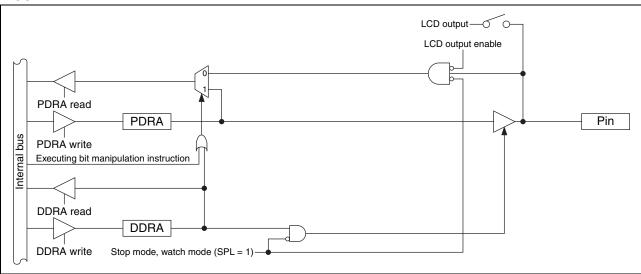
- LCDC COM6 output pin (COM6)
- PA7/COM7 pin

This pin has the following peripheral function:

• LCDC COM7 output pin (COM7)



 Block diagram of PA0/COM0, PA1/COM1, PA2/COM2, PA3/COM3, PA4/COM4, PA5/COM5, PA6/COM6 and PA7/COM7



19.6.3 Port A registers

· Port A register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write			
PDRA	0	Pin state is "L" level.	PDRA value is "0".	As output port, outputs "L" level.			
FDIVA	1	Pin state is "H" level.	PDRA value is "1".	As output port, outputs "H" level.			
DDRA	0		Port input enabled	d			
DDKA	1		Port output enabled				

· Correspondence between registers and pins for port A

		Correspondence between related register bits and pins								
Pin name	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0		
PDRA	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0		
DDRA	Dit/	טונט	טונט	DIL4	טונט	DILZ	וווט	DilU		



19.6.4 Port A operations

- Operation as an output port
 - A pin becomes an output port if the bit in the DDRA register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDRA register to external pins.
 - If data is written to the PDRA register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDRA register returns the PDRA register value.
 - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 2 (LCDCE2:COM[7:0]) to "0" to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to "1".

Operation as an input port

- A pin becomes an input port if the bit in the DDRA register corresponding to that pin is set to "0".
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- If data is written to the PDRA register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDRA register returns the pin value. However, if the read-modify-write (RMW) type of instruction is
 used to read the PDRA register, the PDRA register value is returned.
- To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 2 (LCDCE2:COM[7:0]) to "0" to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to "1".

· Operation as an LCDC common output pin

- Set the bit in the DDRA register corresponding to an LCDC common output pin to "0".
- To use a pin shared with a general-purpose I/O port as an LCDC common output pin, set a corresponding function select bit in the LCDC enable register 2 (LCDCE2:COM[7:0]) to "1" to select the LCDC common output function, and then set the PICTL bit in the LCDCE1 register to "1".

· Operation at reset

If the CPU is reset, all bits in the DDRA register are initialized to "0" and port input is enabled.

Operation in stop mode and watch mode

- If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRA register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.
- If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.



19.7 Port B

Port B is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

19.7.1 Port B configuration

Port B is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port B data register (PDRB)
- Port B direction register (DDRB)

19.7.2 Block diagrams of port B

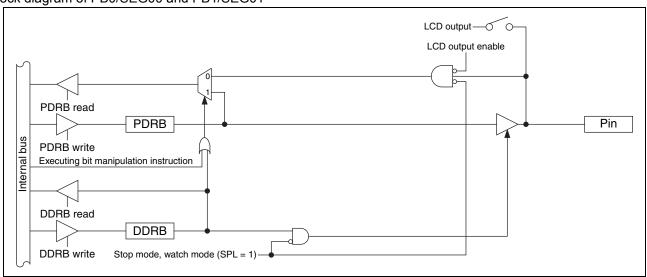
• PB0/SEG00 pin

This pin has the following peripheral function:

- LCDC SEG00 output pin (SEG00)
- PB1/SEG01 pin

This pin has the following peripheral function:

- LCDC SEG01 output pin (SEG01)
- Block diagram of PB0/SEG00 and PB1/SEG01





19.7.3 Port B registers

· Port B register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write	
PDRB	0	Pin state is "L" level.	PDRB value is "0".	As output port, outputs "L" level.	
FDIXB	1	Pin state is "H" level.	PDRB value is "1".	As output port, outputs "H" level.	
DDRB	0		Port input enabled	d	
DDKB	1		Port output enable	d	

· Correspondence between registers and pins for port B

		Correspondence between related register bits and pins								
Pin name		=	=	-	=	=	PB1	PB0		
PDRB		_	_				bit1	bit0		
DDRB	-	-	-	_	_	-	DILI	Dito		

19.7.4 Port B operations

- Operation as an output port
 - A pin becomes an output port if the bit in the DDRB register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDRB register to external pins.
 - If data is written to the PDRB register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDRB register returns the PDRB register value.
 - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[01:00]) to "0" to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to "1".

Operation as an input port

- · A pin becomes an input port if the bit in the DDRB register corresponding to that pin is set to "0".
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- If data is written to the PDRB register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDRB register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRB register, the PDRB register value is returned.
- To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[01:00]) to "0" to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to "1".

· Operation as an LCDC segment output pin

- Set the bit in the DDRB register corresponding to an LCDC segment output pin to "0".
- To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[01:00]) to "1" to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to "1".

Operation at reset

If the CPU is reset, all bits in the DDRB register are initialized to "0" and port input is enabled.

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- Operation in stop mode and watch mode
 - If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRB register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.
 - If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

19.8 Port C

Port C is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

19.8.1 Port C configuration

Port C is made up of the following elements.

- · General-purpose I/O pins/peripheral function I/O pins
- Port C data register (PDRC)
- Port C direction register (DDRC)

19.8.2 Block diagrams of port C

PC0/SEG02 pin

This pin has the following peripheral function:

- LCDC SEG02 output pin (SEG02)
- PC1/SEG03 pin

This pin has the following peripheral function:

- · LCDC SEG03 output pin (SEG03)
- PC2/SEG04 pin

This pin has the following peripheral function:

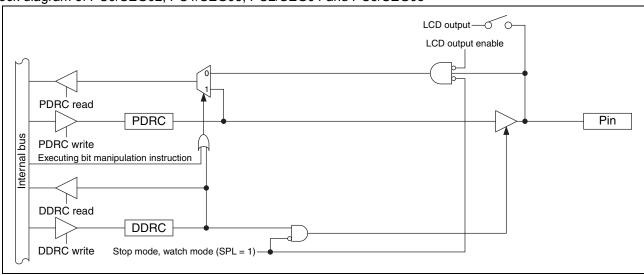
- LCDC SEG04 output pin (SEG04)
- PC3/SEG05 pin

This pin has the following peripheral function:

• LCDC SEG05 output pin (SEG05)



• Block diagram of PC0/SEG02, PC1/SEG03, PC2/SEG04 and PC3/SEG05



19.8.3 Port C registers

Port C register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write			
PDRC	0	Pin state is "L" level.	PDRC value is "0".	As output port, outputs "L" level.			
FBRC	1	Pin state is "H" level.	PDRC value is "1".	As output port, outputs "H" level.			
DDRC	0		Port input enabled				
DDRC	1		Port output enabled				

· Correspondence between registers and pins for port C

		Correspondence between related register bits and pins								
Pin name	-	-	-	-	PC3	PC2	PC1	PC0		
PDRC		_			bit3	bit2	bit1	bit0		
DDRC	-	-	1	-	มเเอ	UILZ	DILI	טונט		



19.8.4 Port C operations

- · Operation as an output port
 - · A pin becomes an output port if the bit in the DDRC register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDRC register to external pins.
 - If data is written to the PDRC register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDRC register returns the PDRC register value.
 - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[05:02]) to "0" to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LCDCE1:PICTL) to "1".

· Operation as an input port

- A pin becomes an input port if the bit in the DDRC register corresponding to that pin is set to "0".
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- If data is written to the PDRC register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDRC register returns the pin value. However, if the read-modify-write (RMW) type of instruction is
 used to read the PDRC register, the PDRC register value is returned.
- To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[05:02]) to "0" to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to "1".

Operation as an LCDC segment output pin

- Set the bit in the DDRC register corresponding to an LCDC segment output pin to "0".
- To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 3 (LCDCE3:SEG[05:02]) to "1" to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to "1".

· Operation at reset

If the CPU is reset, all bits in the DDRC register are initialized to "0" and port input is enabled.

Operation in stop mode and watch mode

- If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRC register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.
- If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.



19.9 Port E

Port E is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

19.9.1 Port E configuration

Port E is made up of the following elements.

- · General-purpose I/O pins/peripheral function I/O pins
- Port E data register (PDRE)
- Port E direction register (DDRE)

19.9.2 Block diagrams of port E

PE0/SEG14 pin

This pin has the following peripheral function:

- LCDC SEG14 output pin (SEG14)
- PE1/SEG15 pin

This pin has the following peripheral function:

- · LCDC SEG15 output pin (SEG15)
- PE2/SEG16 pin

This pin has the following peripheral function:

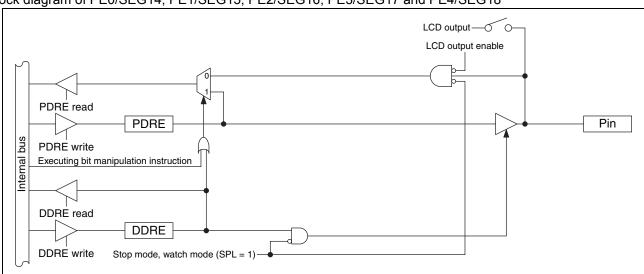
- LCDC SEG16 output pin (SEG16)
- PE3/SEG17 pin

This pin has the following peripheral function:

- LCDC SEG17 output pin (SEG17)
- PE4/SEG18 pin

This pin has the following peripheral function:

- LCDC SEG18 output pin (SEG18)
- Block diagram of PE0/SEG14, PE1/SEG15, PE2/SEG16, PE3/SEG17 and PE4/SEG18





• PE5/SEG19/TO11 pin

This pin has the following peripheral functions:

- LCDC SEG19 output pin (SEG19)
- 8/16-bit composite timer ch. 1 output pin (TO11)

• PE6/SEG20/TO10 pin

This pin has the following peripheral functions:

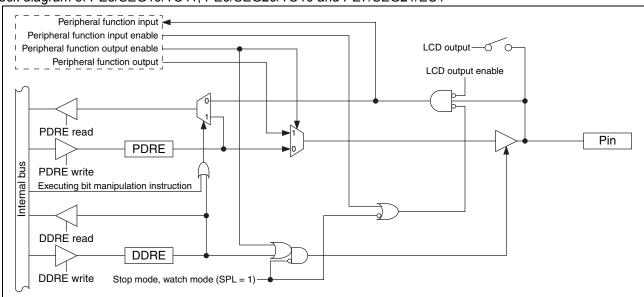
- LCDC SEG20 output pin (SEG20)
- 8/16-bit composite timer ch. 1 output pin (TO10)

• PE7/SEG21/EC1 pin

This pin has the following peripheral functions:

- LCDC SEG21 output pin (SEG21)
- 8/16-bit composite timer ch. 1 clock input pin (EC1)

• Block diagram of PE5/SEG19/TO11, PE6/SEG20/TO10 and PE7/SEG21/EC1



19.9.3 Port E registers

• Port E register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write			
PDRE	0	Pin state is "L" level.	PDRE value is "0".	As output port, outputs "L" level.			
FURE	1	Pin state is "H" level.	PDRE value is "1".	As output port, outputs "H" level.			
DDRE	0	Port input enabled					
DDRE	1		Port output enable	d			

Correspondence between registers and pins for port E

		Correspondence between related register bits and pins								
Pin name	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0		
PDRE	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0		
DDRE	DIL!	טונס	טונט	DIL4	טונט	DILZ	DILI	טונט		

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19.9.4 Port E operations

- Operation as an output port
 - A pin becomes an output port if the bit in the DDRE register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDRE register to external pins.
 - If data is written to the PDRE register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - · Reading the PDRE register returns the PDRE register value.
 - To use a pin shared with the LCDC as an output port, set a corresponding function select bit in the LCDC enable register 4 (LCDCE4:SEG[15:14]) or in the LCDC enable register 5 (LCDCE5:SEG[21:16]) to "0" to select the general-purpose I/O port function, and then set the port input control bit in the LCDC enable register 1 (LC-DCE1:PICTL) to "1".

· Operation as an input port

- A pin becomes an input port if the bit in the DDRE register corresponding to that pin is set to "0".
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- If data is written to the PDRE register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDRE register returns the pin value. However, if the read-modify-write (RMW) type of instruction is
 used to read the PDRE register, the PDRE register value is returned.
- To use a pin shared with the LCDC as an input port, set a corresponding function select bit in the LCDC enable register 4 (LCDCE4:SEG[15:14]) or in the LCDC enable register 5 (LCDCE5:SEG[21:16]) to "0" to select the general-purpose I/O port function, and then set the PICTL bit in the LCDCE1 register to "1".

Operation as a peripheral function output pin

- A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- The pin value can be read from the PDRE register even if the peripheral function output is enabled. Therefore, the
 output value of a peripheral function can be read by the read operation on the PDRE register. However, if the readmodify-write (RMW) type of instruction is used to read the PDRE register, the PDRE register value is returned.

· Operation as a peripheral function input pin

- To set a pin as an input port, set the bit in the DDRE register corresponding to the input pin of a peripheral function to "0".
- Reading the PDRE register returns the pin value, regardless of whether the peripheral function uses that pin as its
 input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDRE register, the PDRE
 register value is returned.

Operation as an LCDC segment output pin

- Set the bit in the DDRE register corresponding to an LCDC segment output pin to "0".
- To use a pin shared with a general-purpose I/O port as an LCDC segment output pin, set a corresponding function select bit in the LCDC enable register 4 (LCDCE4:SEG[15:14]) or in the LCDC enable register 5 (LC-DCE5:SEG[21:16]) to "1" to select the LCDC segment output function, and then set the PICTL bit in the LCDCE1 register to "1".

Operation at reset

If the CPU is reset, all bits in the DDRE register are initialized to "0" and port input is enabled.

· Operation in stop mode and watch mode

• If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRE register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.



• If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

19.10 Port F

Port F is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

19.10.1 Port F configuration

Port F is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port F data register (PDRF)
- Port F direction register (DDRF)

19.10.2 Block diagrams of port F

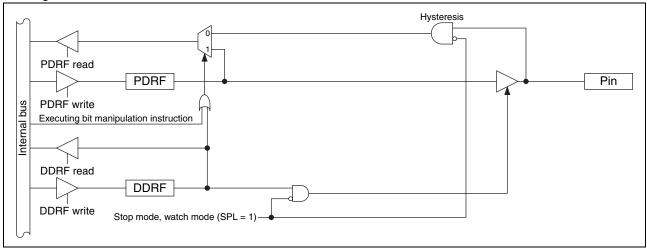
PF0/X0 pin

This pin has the following peripheral function:

- Main clock input oscillation pin (X0)
- PF1/X1 pin

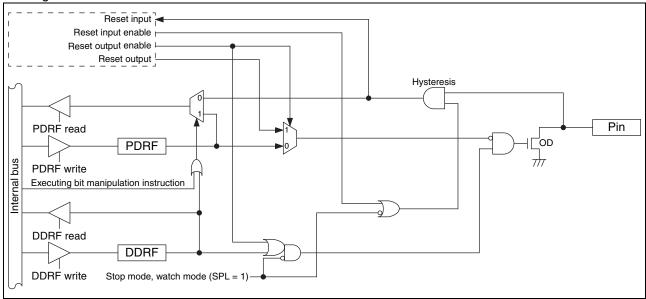
This pin has the following peripheral function:

- Main clock I/O oscillation pin (X1)
- Block diagram of PF0/X0 and PF1/X1





- PF2/RST pin
 - This pin has the following peripheral function:
 - Reset pin (RST)
- Block diagram of PF2/RST



19.10.3 Port F registers

Port F register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write	
PDRF	0	Pin state is "L" level.	PDRF value is "0".	As output port, outputs "L" level.	
FURF	1	Pin state is "H" level.	PDRF value is "1".	As output port, outputs "H" level.*	
DDRF	Port input enabled				
DDKF	1		Port output enable	d	

^{*:} If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

· Correspondence between registers and pins for port F

		Correspondence between related register bits and pins								
Pin name	-	-	-	-	-	PF2*	PF1	PF0		
PDRF						bit2	bit1	bit0		
DDRF	1	-	-	-	1	DILZ	DILI	DILU		

^{*:} PF2/RST is the dedicated reset pin on MB95F774M/F776M/F778M.



19.10.4 Port F operations

- Operation as an output port
 - A pin becomes an output port if the bit in the DDRF register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDRF register to external pins.
 - If data is written to the PDRF register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - · Reading the PDRF register returns the PDRF register value.
- · Operation as an input port
 - A pin becomes an input port if the bit in the DDRF register corresponding to that pin is set to "0".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - If data is written to the PDRF register, the value is stored in the output latch but is not output to the pin set as an input port.
 - Reading the PDRF register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRF register, the PDRF register value is returned.
- Operation at reset

If the CPU is reset, all bits in the DDRF register are initialized to "0" and port input is enabled.

- · Operation in stop mode and watch mode
 - If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop
 mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRF register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.
 - If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

19.11 Port G

Port G is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in "New 8FX MB95710M/770M Series Hardware Manual".

19.11.1 Port G configuration

Port G is made up of the following elements.

- · General-purpose I/O pins/peripheral function I/O pins
- Port G data register (PDRG)
- Port G direction register (DDRG)
- · Port G pull-up register (PULG)

19.11.2 Block diagram of port G

PG1/X0A pin

This pin has the following peripheral function:

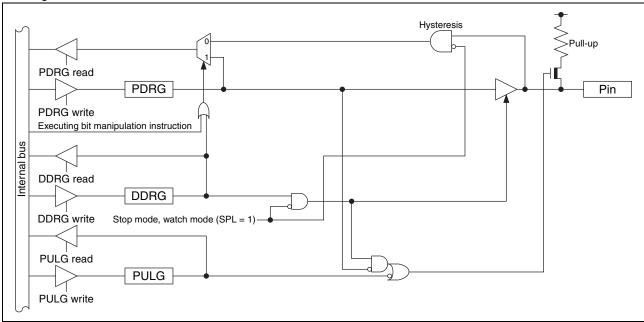
- Subclock input oscillation pin (X0A)
- PG2/X1A pin

This pin has the following peripheral function:

Subclock I/O oscillation pin (X1A)



• Block diagram of PG1/X0A and PG2/X1A



19.11.3 Port G registers

• Port G register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write			
PDRG	0	Pin state is "L" level.	PDRG value is "0".	As output port, outputs "L" level.			
FDRG	1	Pin state is "H" level.	PDRG value is "1".	As output port, outputs "H" level.			
DDRG	0		Port input enabled				
DDRG	1		Port output enabled				
PULG	0		Pull-up disabled				
FULG	1		Pull-up enabled				

• Correspondence between registers and pins for port G

		Correspondence between related register bits and pins								
Pin name	-	-	-	-	-	PG2	PG1	-		
PDRG										
DDRG	-	-	-	-	-	bit2	bit1	-		
PULG										



19.11.4 Port G operations

- Operation as an output port
 - A pin becomes an output port if the bit in the DDRG register corresponding to that pin is set to "1".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - When a pin is used as an output port, it outputs the value of the PDRG register to external pins.
 - If data is written to the PDRG register, the value is stored in the output latch and is output to the pin set as an output port as it is.
 - Reading the PDRG register returns the PDRG register value.
- · Operation as an input port
 - A pin becomes an input port if the bit in the DDRG register corresponding to that pin is set to "0".
 - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
 - If data is written to the PDRG register, the value is stored in the output latch but is not output to the pin set as an input port.
 - Reading the PDRG register returns the pin value. However, if the read-modify-write (RMW) type of instruction is
 used to read the PDRG register, the PDRG register value is returned.
- Operation at reset

If the CPU is reset, all bits in the DDRG register are initialized to "0" and port input is enabled.

- · Operation in stop mode and watch mode
 - If the pin state setting bit in the standby control register (STBC:SPL) is set to "1" and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRG register value. The input of that pin is locked to "L" level and blocked in order to prevent leaks due to input open.
 - If the pin state setting bit is "0", the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.
- Operation of the pull-up register

Setting the bit in the PULG register to "1" makes the pull-up resistor be internally connected to the pin. When the pin output is "L" level, the pull-up resistor is disconnected regardless of the value of the PULG register.



20. Interrupt Source Table

lutamint a com-	Interrupt		r table ress		pt level register	Priority order of interrupt sources
Interrupt source	request number	Upper	Lower	Register	Bit	of the same level (occurring simultaneously)
External interrupt ch. 0	IRQ00	0xFFFA	0xFFFB	ILR0	L00 [1:0]	High
External interrupt ch. 4	INQUU	UXFFFA	UXFFFB	ILKU	L00 [1.0]	A
External interrupt ch. 1	IRQ01	0xFFF8	0xFFF9	ILR0	L01 [1:0]	
External interrupt ch. 5	INQUI	021110	UXFFF9	ILKU	LU1[1.0]	
External interrupt ch. 2	IRQ02	0xFFF6	0xFFF7	ILR0	L02 [1:0]	
External interrupt ch. 6	INQUZ	UXFFFO	UXFFF7	ILKU	LUZ [1.0]	
External interrupt ch. 3	IRQ03	0xFFF4	0xFFF5	ILR0	L03 [1:0]	
External interrupt ch. 7	INQUS	UXFFF4	UXFFF3	ILKU	LU3 [1.0]	
UART/SIO ch. 0	IRQ04	0xFFF2	0xFFF3	ILR1	1.04 [4:0]	
Low-voltage detection circuit	IRQ04	UXFFF2	021113	ILKI	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	0xFFF0	0xFFF1	ILR1	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	0xFFEE	0xFFEF	ILR1	L06 [1:0]	
UART/SIO ch. 2	IRQ07	0xFFEC	0xFFED	ILR1	L07 [1:0]	
LCDC	IRQ08	0xFFEA	0xFFEB	ILR2	L08 [1:0]	
8/16-bit PPG ch. 1 (lower)	IDOOO	٥٧٢٢٥	0xFFE9	ILR2	1.00 [4:0]	
UART/SIO ch. 1	- IRQ09	0xFFE8	UXFFE9	ILKZ	L09 [1:0]	
8/16-bit PPG ch. 1 (upper)	IRQ10	0xFFE6	0xFFE7	ILR2	L10 [1:0]	
16-bit reload timer ch. 0	IRQ11	0xFFE4	0xFFE5	ILR2	L11 [1:0]	
8/16-bit PPG ch. 0 (upper)	IRQ12	0xFFE2	0xFFE3	ILR3	L12 [1:0]	
8/16-bit PPG ch. 0 (lower)	IRQ13	0xFFE0	0xFFE1	ILR3	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	0xFFDE	0xFFDF	ILR3	L14 [1:0]	
Comparator ch. 0	IRQ15	0xFFDC	0xFFDD	ILR3	L15 [1:0]	
I ² C bus interface ch. 0	IRQ16	0xFFDA	0xFFDB	ILR4	L16 [1:0]	
_	IRQ17	0xFFD8	0xFFD9	ILR4	L17 [1:0]	
8/12-bit A/D converter	IRQ18	0xFFD6	0xFFD7	ILR4	L18 [1:0]	
Time-base timer	IRQ19	0xFFD4	0xFFD5	ILR4	L19 [1:0]	
Watch prescaler	IDO20	OVECDO	OVEEDS	II D5	1 20 [4.0]	
Watch counter	IRQ20	0xFFD2	0xFFD3	ILR5	L20 [1:0]	
_	IRQ21	0xFFD0	0xFFD1	ILR5	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	0xFFCE	0xFFCF	ILR5	L22 [1:0]	
Flash memory	IRQ23	0xFFCC	0xFFCD	ILR5	L23 [1:0]	Low



21. Pin States In Each Mode

D:	Normal	01	Stop	mode	Watch	mode	0
Pin name	operation	Sleep mode	SPL=0	SPL=1	SPL=0	SPL=1	On reset
	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Oscillation input*1
PF0/X0	I/O port*2	I/O port*2	 Previous state kept Input blocked*2,*3 	- Hi-Z - Input blocked*2,*3	- Previous state kept - Input blocked*2,*3	- Hi-Z - Input blocked*2,*3	- Hi-Z - Input enabled*4 (However, it does not function.)
	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Oscillation input*1
PF1/X1	I/O port*2	I/O port*2	- Previous state kept - Input blocked*2,*3	- Hi-Z - Input blocked*2,*3	- Previous state kept - Input blocked*2,*3	- Hi-Z - Input blocked*2,*3	- Hi-Z - Input enabled*4 (However, it does not function.)
	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input*5
PF2/RST	I/O port*2	I/O port*2	 Previous state kept Input blocked*2,*3 	- Hi-Z - Input blocked*2,*3	 Previous state kept Input blocked*2,*3 	- Hi-Z - Input blocked*2, *3	 Hi-Z Input enabled*4 (However, it does not function.)
	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Oscillation input*6
PG1/X0A	I/O port*2 I/O port*2		- Previous state kept - Input blocked*2,*3	- Hi-Z*7 - Input blocked*2,*3	- Previous state kept - Input blocked*2, *3	- Hi-Z*7 - Input blocked*2,*3	- Hi-Z - Input enabled*4 (However, it does not function.)
	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Oscillation input*6
PG2/X1A	I/O port*2	I/O port*2 I/O port*2		- Hi-Z*7 - Input blocked*2,*3	- Previous state kept - Input blocked*2,*3	- Hi-Z* ⁷ - Input blocked* ^{2,*3}	- Hi-Z - Input enabled*4 (However, it does not function.)
D00/INT02/	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	- Previous state kept - Input blocked* ³ , * ¹⁰	- Hi-Z - Input blocked* ³ , * ¹⁰	- Previous state kept - Input blocked* ³ , * ¹⁰	- Hi-Z - Input blocked* ³ , * ¹⁰	- Hi-Z - Input blocked* ³



Din nama	Normal	Clean made	Stop	mode	Watch	mode	On recet
Pin name	operation	Sleep mode	SPL=0	SPL=1	SPL=0	SPL=1	On reset
SEG32*8/ UCK1	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	- Previous state kept - Input blocked* ³ , * ¹⁰	- Hi-Z - Input blocked* ³ , * ¹⁰	- Previous state kept - Input blocked*3, *10	- Hi-Z - Input blocked* ³ , * ¹⁰	- Hi-Z - Input blocked* ³
P10/UI0/	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3	- Hi-Z* ⁷ - Input blocked* ³	- Previous state kept - Input blocked*3	- Hi-Z* ⁷ - Input blocked* ³	- Hi-Z - Input enabled*4 (However, it does not function.)
	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	 Previous state kept Input blocked*3 	"H"	 Previous state kept Input blocked*3 	"H"	"H"
	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3	- Hi-Z* ⁷ - Input blocked* ³	- Previous state kept - Input blocked*3	- Hi-Z* ⁷ - Input blocked* ³	- Hi-Z - Input enabled*4 (However, it does not function.)
P15/ SEG31*8/ PPG11 P16/ SEG30*8/ PPG10	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Previous state kept - Input blocked*3	- Hi-Z - Input blocked*3	- Hi-Z - Input blocked* ³
CMP0_O	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept*11 - Input blocked*3	- Hi-Z* ⁷ - Input blocked* ³	- Previous state kept*11 - Input blocked*3	- Hi-Z* ⁷ - Input blocked* ³	 Hi-Z Input enabled*4 (However, it does not function.)
CMP0_N P21/	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	- Previous state kept - Input blocked*3, *12	- Hi-Z* ⁷ - Input blocked* ^{3,} *12	 Previous state kept Input blocked*3, *12 	- Hi-Z* ⁷ - Input blocked* ^{3,} *12	- Hi-Z - Input enabled* ⁴
P22/SCL	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	 Previous state kept Input blocked*3, *13 	- Hi-Z - Input blocked*3,*13	 Previous state kept Input blocked*3, *13 	- Hi-Z - Input blocked*3, *13	- Hi-Z - Input enabled*4



	Normal		Stop	mode	Watch	mode	
Pin name	operation	Sleep mode	SPL=0	SPL=1	SPL=0	SPL=1	On reset
P40/ SEG21* ¹⁴	•						
P41/ SEG20* ¹⁴	I/O port/ peripheral	I/O port/ peripheral	- Previous state kept	- Hi-Z	- Previous state kept	- Hi-Z	- Hi-Z
P42/ SEG19* ¹⁴	function I/O	function I/O	- Input blocked*3	- Input blocked*3	- Input blocked*3	- Input blocked*3	- Input blocked*3
P43/ SEG18* ¹⁴							
P50/ TO01* ¹⁴							- Hi-Z
	I/O port/ peripheral	I/O port/ peripheral	 Previous state kept 	- Hi-Z* ⁷	- Previous state kept	- Hi-Z* ⁷	 Input enabled*4 (However, it
P52/TI0/ TO00* ¹⁴	function I/O	function I/O	- Input blocked*3	- Input blocked*3	- Input blocked*3	- Input blocked*3	does not function.)
P53/TO0* ¹⁴							
P60/ SEG06* ⁸ / SEG10* ⁸							
P61/ SEG07* ⁸ / SEG11* ⁸							
P62/ SEG08*8/							
	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept	- Hi-Z - Input blocked*3	- Previous state kept	- Hi-Z - Input blocked*3	- Hi-Z - Input blocked*3
P64/ SEG10*8/ SEG14*8	nunction i/O	iuriction i/O	- Input blocked*3		- Input blocked*3		
P65/ SEG11*8/							
SEG15*8 P66/ SEG12*8/							
SEG12 ⁹ / SEG16*8 P67/							
SEG13*8/ SEG17*8							
	I/O port/	I/O port/	- Previous state	- Hi-Z	- Previous state	- Hi-Z	- Hi-Z
P92/V2 P93/V1 P94/V0* ¹⁴	peripheral function I/O	peripheral function I/O	kept - Input blocked*3	- Input blocked*3	kept - Input blocked*3	- Input blocked*3	- Input blocked*3



	Normal		Stop	mode	Watch	mode	• .
Pin name	operation	Sleep mode	SPL=0	SPL=1	SPL=0	SPL=1	On reset
PA0/COM0 PA1/COM1	•						
PA2/COM2 PA3/COM3	I/O port/ peripheral	I/O port/ peripheral	- Previous state kept	- Hi-Z	- Previous state kept	- Hi-Z	- Hi-Z
PA4/COM4 PA5/COM5	function I/O	function I/O	- Input blocked*3	- Input blocked*3	- Input blocked*3	- Input blocked*3	- Input blocked*3
PA6/COM6 PA7/COM7							
PB0/SEG00 PB1/SEG01 PB2/							
SEG37*14	I/O port/ peripheral	I/O port/ peripheral	 Previous state kept 	- Hi-Z	 Previous state kept 	- Hi-Z	- Hi-Z
PB3/ SEG38* ¹⁴		function I/O	- Input blocked*3	- Input blocked*3	- Input blocked*3	- Input blocked*3	- Input blocked*3
PB4/ SEG39* ¹⁴							
PC0/ SEG02							
PC1/ SEG03							
PC2/ SEG04							
PC3/ SEG05	I/O port/	I/O port/	- Previous state	- Hi-Z	- Previous state	- Hi-Z	- Hi-Z
PC4/ SEG06* ¹⁴	-peripheral peripheral function I/O function I/O	' '	kept - Input blocked*3	- Input blocked*3	kept - Input blocked*3	- Input blocked*3	
PC5/							
SEG07*14							
PC6/ SEG08* ¹⁴							
PC7/ SEG09* ¹⁴							



Din nome	Normal	Clean made	Stop	mode	Watch	Watch mode			
Pin name	operation	Sieep mode	SPL=0	SPL=1	SPL=0	SPL=1	On reset		
SEG18*8/		I/O port/ peripheral function I/O			SPL=0 - Previous state		- Hi-Z - Input blocked*3		

SPL: Pin state setting bit in the standby control register (STBC:SPL)

Hi-Z: High impedance

- *1: PF0/X0 and PF1/X1 transit to this state on a reset when configured as a main clock oscillation pins.
- *2: The pin stays at the state shown when configured as a general-purpose I/O port.
- *3: "Input blocked" means direct input gate operation from the pin is disabled.
- *4: "Input enabled" means that the input function is enabled. While the input function is enabled, execute a pull-up operation or a pull-down operation to prevent leaks due to external input. If a pin is used as an output port, its pin state is the same as that of other ports.
- *5: The PF2/RST pin stays at the state shown when configured as a reset pin.
- *6: PG1/X0A and PG2/X1A transit to this state on a reset when configured as subclock oscillation pins.
- *7: The pull-up control setting is still effective.
- *8: The MB95710M Series and the MB95770M Series have different SEG output assignment as shown below.

SEG output	Pin on MB95710M Series	Pin on MB95770M Series
SEG06	PC4	P60
SEG07	PC5	P61
SEG08	PC6	P62
SEG09	PC7	P63
SEG10	P60	P64
SEG11	P61	P65
SEG12	P62	P66
SEG13	P63	P67
SEG14	P64	PE0
SEG15	P65	PE1
SEG16	P66	PE2



SEG output	Pin on MB95710M Series	Pin on MB95770M Series
SEG17	P67	PE3
SEG18	P43	PE4
SEG19	P42	PE5
SEG20	P41	PE6
SEG21	P40	PE7
SEG22	PE0	P07
SEG23	PE1	P06
SEG24	PE2	P05
SEG25	PE3	P04
SEG26	PE4	P03
SEG27	PE5	P02
SEG28	PE6	P01
SEG29	PE7	P00
SEG30	P07	P16
SEG31	P06	P15
SEG32	P05	_
SEG33	P04	_
SEG34	P03	_
SEG35	P02	_
SEG36	P01	_

- *9: On the MB95770M Series, TO00 is assigned to P01, TO0 to P10, TO01 to P13, and EC0 and TI0 to P14.
- *10: Though input is blocked, an external interrupt can be input when the external interrupt request is enabled.
- *11: The output function of the comparator is still in operation in stop mode and watch mode.
- *12: Though input is blocked, an analog signal can also be input to generate a comparator interrupt when the comparator interrupt is enabled.
- *13: The I²C bus interface can wake up the MCU in stop mode or watch mode when its MCU standby mode wakeup function is enabled. For details of the MCU standby mode wakeup function, refer to "CHAPTER 23 I²C BUS INTER-FACE" in "New 8FX MB95710M/770M Series Hardware Manual".
- *14: P40/SEG21, P41/SEG20, P42/SEG19, P43/SEG18, P50/T001, P51/EC0, P52/TI0/T000, P53/T00, P94/V0, PB2/SEG37, PB3/SEG38, PB4/SEG39, PC4/SEG06, PC5/SEG07, PC6/SEG08 and PC7/SEG09 are only available on the MB95710M Series.



22. Electrical Characteristics

22.1 Absolute Maximum Ratings

Donomoton	Cumbal	Rat	ing	Unit	Domonico
Parameter	Symbol	Min	Max	Unit	Remarks
Power supply voltage*1	Vcc	Vss - 0.3	Vss + 6	V	
Input voltage*1	Vı	Vss - 0.3	Vss + 6	V	*2
Output voltage*1	Vo	Vss - 0.3	Vss + 6	V	*2
Maximum clamp current	ICLAMP	-2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	Σ $ CLAMP $	_	20	mA	Applicable to specific pins*3
"L" level maximum output current	lol	_	15	mA	
"L" level average current	lolav	_	4	mA	Average output current = operating current × operating ratio (1 pin)
"L" level total maximum output current	Σ loL	_	100	mA	
"L" level total average output current	Σ lolav	_	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
"H" level maximum output current	Іон	_	-15	mA	
"H" level average current	Іонач	_	-4	mA	Average output current = operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣІон	_	-100	mA	
"H" level total average output current	Σ Iohav	_	–50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	Pd		320	mW	
Operating temperature	Та	-40	+85	°C	
Storage temperature	Tstg	-55	+150	°C	

^{*1:} These parameters are based on the condition that Vss is 0.0 V.

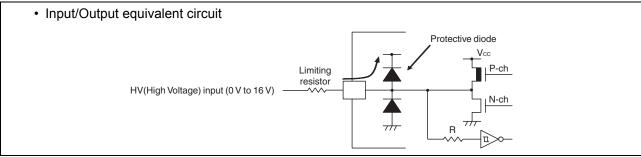
- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the Vcc voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.

^{*2:} V₁ and V₀ must not exceed Vcc + 0.3 V. V₁ must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the Iclamp rating is used instead of the V₁ rating.

^{*3:} Specific pins: P00 to P07, P10, P11, P13 to P16, P20 to P22, P40 to P43, P50 to P53, P60 to P67, P90 to P94, PA0 to PA7, PB0 to PB4, PC0 to PC7, PE0 to PE7, PF0, PF1, PG1, PG2 (P40 to P43, P50 to P53, P94, PB2 to PB4 and PC4 to PC7 are only available on the MB95710M Series.)



- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the Vcc pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit:



WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.

Do not exceed any of these ratings.

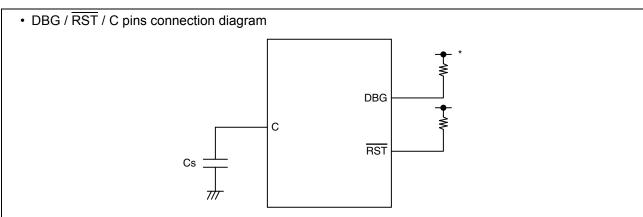


22.2 Recommended Operating Conditions

(Vss = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
Farameter	Syllibol	Min	Max	Oilit	Remarks
Power supply voltage	Vcc	1.8*1	5.5	V	In normal operation
Decoupling capacitor	Cs	0.2	10	μF	A capacitor of about 1.0 μF is recommended. *2
Operating temperature	TA	-40	+85	°C	Other than on-chip debug mode
Operating temperature	IA	+5	+35		On-chip debug mode

- *1: The minimum power supply voltage becomes 2.18 V when a product with the low-voltage detection reset is used or when the on-chip debug mode is used.
- *2: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. For the connection to a decoupling capacitor Cs, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and Cs and the distance between Cs and the Vss pin when designing the layout of a printed circuit board.



*: Connect the DBG pin to an external pull-up resistor of $2 \text{ k}\Omega$ or above. After power-on, ensure that the DBG pin does not stay at "L" level until the reset output is released. The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.



22.3 DC Characteristics

(Vcc = 3.0 V \pm 10%, Vss = 0.0 V, TA = -40 °C to +85 °C)

Davamatav	Crembal	Din nome	Candition	<u> </u>	Value			Powerks
Parameter	Symbol	Pin name	Condition	Min	Тур	Max	Unit	Remarks
	Viнi	P01, P04, P10, P22, P23	*1	0.7 Vcc		Vcc + 0.3	>	
"H" level input voltage	Vihs	P00 to P07, P10 to P17, P20 to P23, P40 to P43*2, P50 to P53*2, P60 to P67, P90 to P93, P94*2, PA0 to PA7, PB0, PB1, PB2 to PB4*2, PC0 to PC3, PC4 to PC7*2, PE0 to PE7, PF0, PF1, PG1, PG2	*1	0.8 Vcc		Vcc + 0.3	>	Hysteresis input
	Vінм	PF2	_	0.7 Vcc		Vcc + 0.3	V	Hysteresis input
	VILI	P01, P04, P10, P22, P23	*1	Vss - 0.3	-	0.3 Vcc	V	
"L" level input voltage	Vils	P00 to P07, P10 to P17, P20 to P23, P40 to P43*2, P50 to P53*2, P60 to P67, P90 to P93, P94*2, PA0 to PA7, PB0, PB1, PB2 to PB4*2, PC0 to PC3, PC4 to PC7*2, PE0 to PE7, PF0, PF1, PG1, PG2	*1	Vss - 0.3	_	0.2 Vcc		Hysteresis input
	VILM	PF2	_	Vss – 0.3		0.3 Vcc	V	Hysteresis input
Open-drain output application voltage	VD	P12, P22, P23, PF2	_	Vss - 0.3	_	Vss + 5.5	V	
"H" level output voltage	Vон	Output pins other than P12, P22, P23, PF2	Iон = -4 mA*3	Vcc – 0.5		_	V	



(Vcc = 3.0 V \pm 10%, Vss = 0.0 V, TA = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition		Value		Unit	Remarks	
Parameter	Syllibol	Fill Hallie	Condition	Min	Тур	Max	Ullit	Remarks	
"L" level output voltage	Vol	All output pins	IoL = 4 mA*4	_	_	0.4	V		
Input leak current (Hi-Z output leak current)	lu	All input pins	0.0 V < V _I < V _{CC}	-5	_	+5	μΑ	When the internal pull-up resistor is disabled	
Internal pull-up resistor	Rpull	P10, P11, P13, P14, P17, P20, P21, P50 to P53* ² , PG1, PG2	V _I = 0 V	75	100	150	kΩ	When the internal pull-up resistor is enabled	
Input capacitance	Cin	Other than Vcc and Vss	f = 1 MHz	_	5	15	pF		



(Vcc = 3.0 V \pm 10%, Vss = 0.0 V, TA = -40 °C to +85 °C)

				Value				
Parameter	Symbol	Pin name	Condition	Min	Typ*1	Max*5	Unit	Remarks
	Icc	-Voc	Fcн = 32 МНz Fмp = 16 МНz	_	4.7	7.3	mA	Except during Flash memory programming and erasing
			Main clock mode (divided by 2)	I	9.8	15.8	mA	During Flash memory programming and erasing
Power supply current*6	Iccs		F _{CH} = 32 MHz F _{MP} = 16 MHz Main sleep mode (divided by 2)	l	2.1	3.4	mA	
	Iccl		F _{CL} = 32 kHz F _{MPL} = 16 kHz Subclock mode (divided by 2) T _A = +25 °C		35	60	μΑ	
	Iccls		Fcl = 32 kHz FMPl = 16 kHz Subsleep mode (divided by 2) T _A = +25 °C		2	7	μΑ	
	Ісст		F _{CL} = 32 kHz Watch mode Main stop mode T _A = +25 °C	ı	1.2	6.2	μΑ	
	ICCMPLL		FMPLL = 16 MHz FMP = 16 MHz Main PLL clock mode (multiplied by 4)	I	5.3	8.5	mA	
	ICCMCRPLL	Vcc	FMCRPLL = 16 MHz FMP = 16 MHz Main CR PLL clock mode (multiplied by 4)		4.9	8.3	mA	
	Іссмск		F _{CRH} = 4 MHz F _{MP} = 4 MHz Main CR clock mode	_	1.7	3.4	mA	
	Iccscr		Sub-CR clock mode T _A = +25 °C	_	54	100	μΑ	



(Vcc = $3.0 \text{ V} \pm 10\%$, Vss = 0.0 V, T_A = $-40 \,^{\circ}\text{C}$ to $+85 \,^{\circ}\text{C}$)

	Symbol		ì		Value	,		Remarks
Parameter		Pin name	Condition	Min	Typ*1	Max*5	Unit	
Power supply current*6	Ісстѕ	Vcc (External clock	FCH = 32 MHz Time-base timer mode	_	450	500	μΑ	
	Іссн	operation)	T _A = +25 °C Substop mode T _A = +25 °C	_	0.7	5	μΑ	
	la	AVcc	FCH = 16 MHz Current consumption of the A/D converter	_	1.8	3.2	mA	
	Іан		FcH = 16 MHz Current consumption with the A/D converter halted		0.1	1.7	μА	
	lv		Fch = 16 MHz Current consumption of the comparator		160	700	μΑ	
	I PLVD		Current consumption of the low-voltage detection reset circuit in operation		6	26	μΑ	
	lilvd		Current consumption of the low-voltage detection interrupt circuit operating in normal mode	1	6	14	μΑ	
	lilvdl	Vcc	Current consumption of the low-voltage detection interrupt circuit operating in low power consumption mode	_	3	10	μΑ	
	Іскн		Current consumption of the main CR oscillator	_	270	320	μΑ	
	Icrl		Current consumption of the sub-CR oscillator oscillating at 100 kHz	_	5	20	μΑ	_
	Isosc		Current consumption of the suboscillator	_	0.8	7	μΑ	



 $(Vcc = 3.0 V\pm 10\%, Vss = 0.0 V, T_A = -40 ^{\circ}C to +85 ^{\circ}C)$

Parameter	Symbol	Pin name	Condition		Value		Unit	Remarks
Farameter	Syllibol	Fili lialile	Condition	Min	Typ*1	Max*5	Ollit	Remarks
LCD internal	D. 05		Between V4 and	_	400		kΩ	
division resistance	RLCD	_	Vss	_	40	_	$k\Omega$	
COM0 to COM7 output impedance	Rvсом	COM0 to COM7	V1 to V4 = 4.1 V	_	_	5	kΩ	
SEG00 to SEG39* ⁷ output impedance	Rvseg	SEG00 to SEG39*7	V 1 (0 V4 = 4.1 V	_	_	7	kΩ	
LCD leakage current	ILCDL	V0*8 to V4, COM0 to COM7, SEG00 to SEG39*7	_	-1	_	+1	μΑ	

^{*1:} Vcc = 3.0 V, TA = +25 °C

- See "4. AC Characteristics Clock Timing" for Fch, Fcl, Fcrh, Fmcrpll and Fmpll.
- See "4. AC Characteristics Source Clock/Machine Clock" for FMP and FMPL.
- The power supply current in subclock mode is determined by the external clock. In subclock mode, current consumption in using the crystal oscillator is higher than that in using the external clock. When the crystal oscillator is used, the power supply current is the sum of adding Isosc (current consumption of the suboscillator) to the power supply current in using the external clock. For details of controlling the subclock, refer to "CHAPTER 3 CLOCK CONTROLLER" and "CHAPTER 30 SYSTEM CONFIGURATION REGISTER" in "New 8FX MB95710M/770M Series Hardware Manual".

^{*2:} P40 to P43, P50 to P53, P94, PB2 to PB4 are only available on the MB95710M Series.

^{*3:} When V_{CC} is smaller than 4.5 V, the condition becomes $I_{OH} = -2$ mA.

^{*4:} When Vcc is smaller than 4.5 V, the condition becomes IoL = 2 mA.

^{*5:} V_{CC} = 3.3 V, T_A = +85 °C (unless otherwise specified)

^{*6: •} The power supply current is determined by the external clock. When the low-voltage detection reset circuit is selected, the power supply current is the sum of adding the current consumption of the low-voltage detection reset circuit (IPLVD) to one of the values from Icc to Icch. In addition, when both the low-voltage detection reset circuit and a CR oscillator are selected, the power supply current is the sum of adding up the current consumption of the low-voltage detection reset circuit (IPLVD), the current consumption of the CR oscillator (ICRH or ICRL) and one of the values from Icc to Icch. In on-chip debug mode, the main CR oscillator (ICRH) and the low-voltage detection reset circuit are always in operation, and current consumption therefore increases accordingly.

^{*7:} SEG32 to SEG39 are only available on the MB95710M Series.

^{*8:} V0 is only available on the MB95710M Series.



22.4 AC Characteristics

22.4.1 Clock Timing

 $(Vcc = 1.8 \text{ V to } 5.5 \text{ V}, \text{Vss} = 0.0 \text{ V}, \text{TA} = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C})$

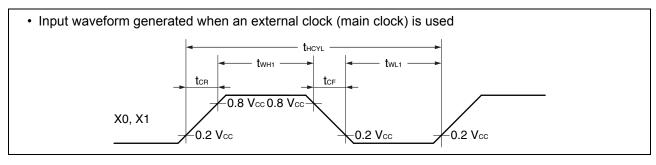
Parameter	Symbol	Pin name	Condition		Value		Unit	Remarks	
Faranietei	Symbol		Condition	Min	Тур	Max			
		X0, X1	_	1	_	16.25	MHz	When the main oscillation circuit is used	
		X0	_	1	_	32.5	MHz	When the main external clock is used	
				4	_	8.13	MHz	Operating conditions The main clock is used. PLL multiplication rate: 2	
	Fсн	V0 V1		4	_	6.5	MHz	Operating conditions The main clock is used. PLL multiplication rate: 2.5	
		X0, X1		4	_	5.41	MHz	Operating conditions The main clock is used. PLL multiplication rate: 3	
				4	_	4.06	MHz	Operating conditions The main clock is used. PLL multiplication rate: 4	
	Fcrh	_	_	3.92	4	4.08	MHz	 Operating conditions The main CR clock is used. 0 °C ≤ T_A ≤ +70 °C 	
Clock frequency				3.8	4	4.2	MHz	 Operating conditions The main CR clock is used. - 40 °C ≤ TA < 0 °C, + 70 °C < TA ≤ + 85 °C 	
	FMCRPLL	ц —		7.84	8	8.16	MHz	Operating conditions • PLL multiplication rate: 2 • 0 °C ≤ T _A ≤ +70 °C	
				7.6	8	8.4	MHz	Operating conditions • PLL multiplication rate: 2 • − 40 °C ≤ TA < 0 °C, + 70 °C < TA ≤ + 85 °C	
				9.8	10	10.2	MHz	Operating conditions • PLL multiplication rate: 2.5 • 0 °C ≤ T _A ≤ +70 °C	
			_	_	9.5	10	10.5	MHz	Operating conditions • PLL multiplication rate: 2.5 • − 40 °C ≤ T _A < 0 °C, + 70 °C < T _A ≤ + 85 °C
				11.76	12	12.24	MHz	Operating conditions • PLL multiplication rate: 3 • 0 °C ≤ T _A ≤ +70 °C	
				11.4	12	12.6	MHz	Operating conditions • PLL multiplication rate: 3 • − 40 °C ≤ TA < 0 °C, + 70 °C < TA ≤ + 85 °C	

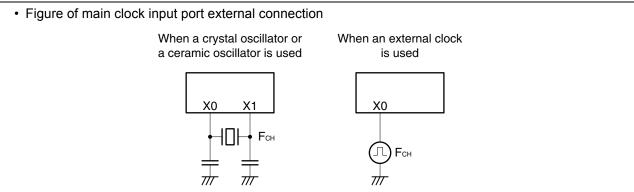


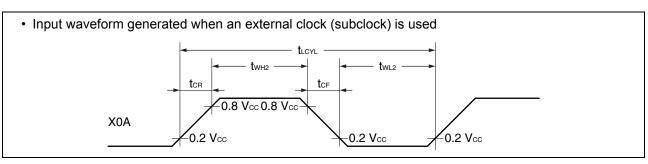
 $(Vcc = 1.8 V to 5.5 V, Vss = 0.0 V, T_A = -40 °C to +85 °C)$

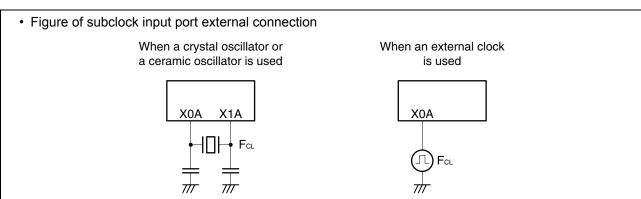
				Value				
Parameter	Symbol	Pin name	Condition	Min	Тур	Max	Unit	Remarks
	FMCRPLL			15.68	16	16.32	MHz	Operating conditions • PLL multiplication rate: 4 • 0 °C ≤ T _A ≤ +70 °C
		_	_	15.2	16	16.8	MHz	Operating conditions • PLL multiplication rate: 4 • − 40 °C ≤ TA < 0 °C, + 70 °C < TA ≤ + 85 °C
Clock frequency	FMPLL	_	_	8		16	MHz	When the main PLL clock is used
	FcL	X0A, X1A			32.768	_	kHz	When the sub-oscillation circuit is used
	T CL	ДОД, ДТД		l	32.768		kHz	When the sub-external clock is used
	FCRL	_		50	100	150	kHz	When the sub-CR clock is used
	thcyl	X0, X1		61.5		1000	ns	When the main oscillation circuit is used
Clock cycle time		X0	_	30.8		1000	ns	When an external clock is used
ume		X0, X1	_	_	250	_	ns	When the main PLL clock is used
	t LCYL	X0A, X1A	_	_	30.5	_	μs	When the subclock is used
	twH1,	X0	_	12.4		_	ns	When an external clock is used, the duty ratio should range between 40% and 60%.
Input clock pulse width		X0, X1	_		125	_	ns	When the main PLL clock is used
	twH2,	X0A	_	_	15.2	_	μs	When an external clock is used, the duty ratio should range between 40% and 60%.
Input clock rising time and falling time	tcr, tcf	X0, X0A	_	_	_	5	ns	When an external clock is used
CR oscillation	tcrhwk	_	_		_	50	μs	When the main CR clock is used
start time	tcrlwk	_	_	_		30	μs	When the sub-CR clock is used
PLL oscillation start time	t MCRPLLWK	_	_	_		100	μs	When the main CR PLL clock is used



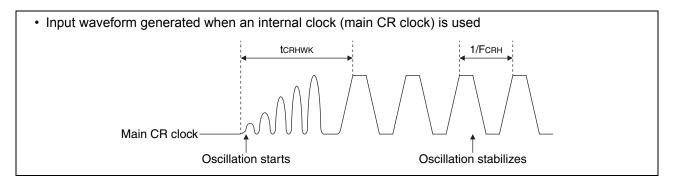


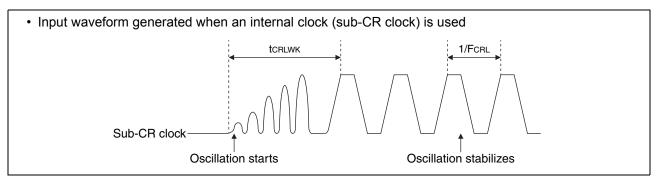


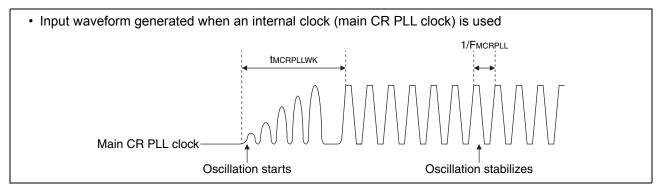














22.4.2 Source Clock/Machine Clock

(Vcc = 1.8 V to 5.5 V, Vss = 0.0 V, $T_A = -40 \, ^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$)

	Symbol	Pin	Value					
Parameter		name	Min	Тур	Max	Unit	Remarks	
Source clock			61.5	_	2000	ns	When the main external clock is used Min: FcH = 32.5 MHz, divided by 2 Max: FcH = 1 MHz, divided by 2	
			_	250	_	ns	When the main CR clock is used	
	tscik	_		62.5	_	250	ns	When the main PLL clock is used Min: FcH = 4 MHz, multiplied by 4 Max: FcH = 4 MHz, no division
cycle time*1	ISCLK		62.5	_	250	ns	When the main CR PLL clock is used Min: Fcrh = 4 MHz, multiplied by 4 Max: Fcrh = 4 MHz, no division	
				61		μs	When the sub-oscillation clock is used FcL = 32.768 kHz, divided by 2	
			_	20	_	μs	When the sub-CR clock is used FcL = 100 kHz, divided by 2	
	Fsp		0.5	_	16.25	MHz	When the main oscillation clock is used	
				4	_	MHz	When the main CR clock is used	
Source clock			8	_	16	MHz	When the main PLL clock is used	
frequency			8		16	MHz	When the main CR PLL clock is used	
. ,	Fspl		_	16.384	_	kHz	When the sub-oscillation clock is used	
			_	50	_	kHz	When the sub-CR clock is used FCRL = 100 kHz, divided by 2	
			61.5	_	32000	ns	When the main oscillation clock is used Min: F _{SP} = 16.25 MHz, no division Max: F _{SP} = 0.5 MHz, divided by 16	
		< —	250	_	4000	ns	When the main CR clock is used Min: F _{SP} = 4 MHz, no division Max: F _{SP} = 4 MHz, divided by 16	
Machine clock cycle time*2 (minimum instruction execution time)	tuous		62.5	_	2000	ns	When the main PLL clock is used Min: F _{SP} = 4 MHz, multiplied by 4 Max: F _{SP} = 4 MHz, divided by 16	
	t мсLк			62.5	_	2000	ns	When the main CR PLL clock is used Min: F _{SP} = 4 MHz, multiplied by 4 Max: F _{SP} = 4 MHz, divided by 16
				61	_	976.5	μs	When the sub-oscillation clock is used Min: Fspl = 16.384 kHz, no division Max: Fspl = 16.384 kHz, divided by 16
			20	_	320	μs	When the sub-CR clock is used Min: Fspl = 50 kHz, no division Max: Fspl = 50 kHz, divided by 16	

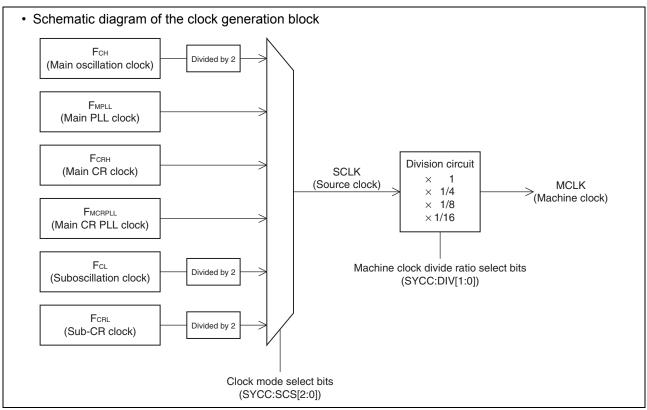


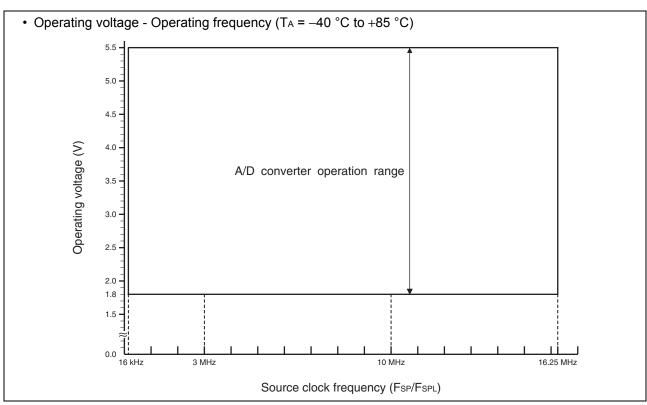
 $(Vcc = 1.8 V to 5.5 V, Vss = 0.0 V, T_A = -40 °C to +85 °C)$

Parameter Symbo		Pin		Value		Unit	Remarks		
Farameter	Syllibol	name	Min	Тур	Max	Ullit	Kemarks		
			0.031	_	16.25	MHz	When the main oscillation clock is used		
	Fмp		0.25	_	4	MHz	When the main CR clock is used		
Machine clock			0.5	_	16	MHz	When the main PLL clock is used		
frequency		_	0.5		16	MHz	When the main CR PLL clock is used		
' '			1.024 — 16.384 kHz When the sub-oscillat		When the sub-oscillation clock is used				
	FMPL		3.125	_	50	kHz	When the sub-CR clock is used FCRL = 100 kHz		

- *1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). In addition, a source clock can be selected from the following.
 - Main clock divided by 2
 - PLL multiplication of main clock (Select a multiplication rate from 2, 2.5, 3 and 4.)
 - Main CR clock
 - PLL multiplication of main CR clock (Select a multiplication rate from 2, 2.5, 3 and 4.)
 - Subclock divided by 2
 - Sub-CR clock divided by 2
- *2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.
 - Source clock (no division)
 - · Source clock divided by 4
 - · Source clock divided by 8
 - Source clock divided by 16





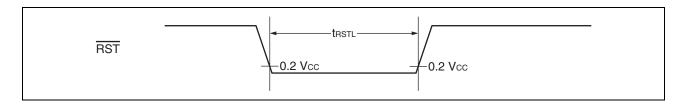




22.4.3 External Reset

Parameter	Symbol	Value		Unit	Domarke
Parameter	Syllibol	Min	Max Unit Remarks	Remarks	
RST "L" level pulse width	t RSTL	2 tmcLK*	l	ns	

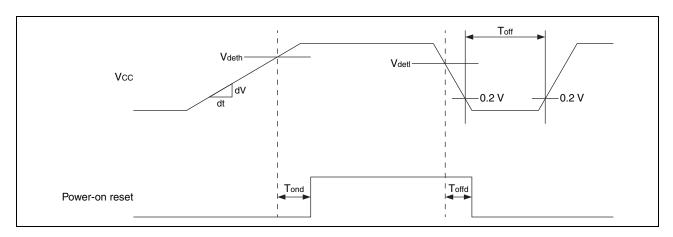
^{*:} See "Source Clock/Machine Clock" for tmclk.



22.4.4 Power-on Reset

$$(Vss = 0.0 V, T_A = -40 °C to +85 °C)$$

Parameter	Symbol	Pin		Value		Unit	Remarks
Farameter	Syllibol	name	Min	Тур	Max	Oilit	Remarks
Power supply rising time	dV/dt		0.1	_	_	V/ms	
Power supply cutoff time	Toff		1	_	_	ms	
Reset release voltage	Vdeth	Vcc	1.44	1.60	1.76	V	At voltage rise
Reset detection voltage	Vdetl	VCC	1.39	1.55	1.71	V	At voltage fall
Reset release delay time	Tond		_	_	10	ms	dV/dt ≥ 0.1 mV/µs
Reset detection delay time	Toffd		_	_	0.4	ms	dV/dt ≥ −0.04 mV/μs

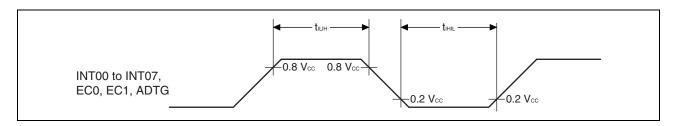




22.4.5 Peripheral Input Timing

Parameter	Symbol	Pin name	Va	lue	Unit
Farameter	Symbol	Fili lialile	Min	Max	Offic
Peripheral input "H" pulse width	tılıH	INT00 to INT07, EC0, EC1,	2 tmclk*		ns
Peripheral input "L" pulse width	tıнıL	ADTG	2 tmclk*	_	ns

^{*:} See "Source Clock/Machine Clock" for tmclk.



22.4.6 Low-voltage Detection

Normal mode

 $(V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}, \text{Vss} = 0.0 \text{ V}, \text{TA} = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C})$

	•					$V_1 = V_2 = 0.0 \text{ V}, V_3 = -40 \text{ C to } +8$	
Parameter	Symbol	hol Value			Unit	Remarks	
i didilietei	Symbol	Min	Тур	Max	Offic	Remarks	
Reset release voltage	V_{PDL+}	1.88	2.03	2.18	V	At power supply rise	
Reset detection voltage	V _{PDL}	1.8	1.93	2.06	V	At power supply fall	
Interrupt release voltage 0	VIDL0+	2.13	2.3	2.47	V	At power supply rise	
Interrupt detection voltage 0	VIDL0-	2.05	2.2	2.35	V	At power supply fall	
Interrupt release voltage 1	VIDL1+	2.41	2.6	2.79	V	At power supply rise	
Interrupt detection voltage 1	VIDL1-	2.33	2.5	2.67	V	At power supply fall	
Interrupt release voltage 2	VIDL2+	2.69	2.9	3.11	V	At power supply rise	
Interrupt detection voltage 2	VIDL2-	2.61	2.8	2.99	V	At power supply fall	
Interrupt release voltage 3	VIDL3+	3.06	3.3	3.54	V	At power supply rise	
Interrupt detection voltage 3	VIDL3-	2.98	3.2	3.42	V	At power supply fall	
Interrupt release voltage 4	VIDL4+	3.43	3.7	3.97	V	At power supply rise	
Interrupt detection voltage 4	VIDL4-	3.35	3.6	3.85	V	At power supply fall	
Interrupt release voltage 5	VIDL5+	3.81	4.1	4.39	V	At power supply rise	
Interrupt detection voltage 5	VIDL5-	3.73	4	4.27	V	At power supply fall	
Power supply start voltage	Voff	_	_	1.6	V		
Power supply end voltage	Von	4.39	_	_	V		
Power supply voltage change time (at power supply rise)	t r	697.5	_	_	μs	Slope of power supply that the reset release signal generates within the rating (VPDL+/VIDL+)	
Power supply voltage change time (at power supply fall)	tr	697.5	_	_	μs	Slope of power supply that the reset detection signal generates within the rating (VPDL-/VIDL-)	
Reset release delay time	t dp1	_	_	30	μs		
Reset detection delay time	tdp2		_	30	μs		
Interrupt release delay time	t di1	_	_	30	μs		
Interrupt detection delay time	t di2	_	_	30	μs		
Interrupt threshold voltage transition stabilization time	t stb		_	30	μs		



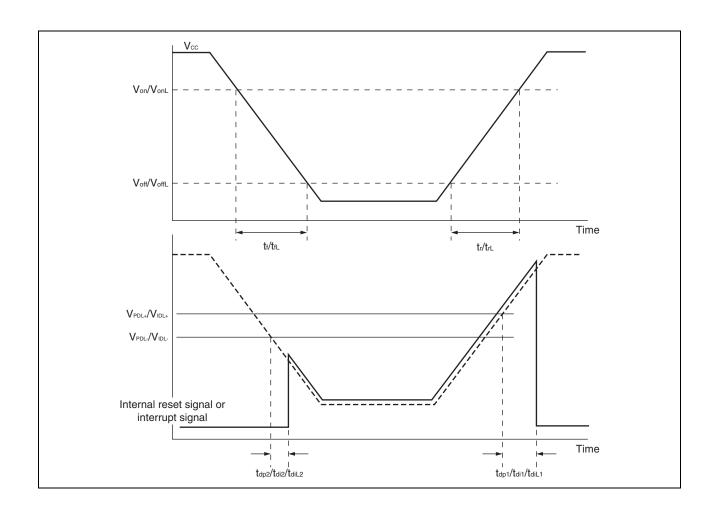
• Low power consumption mode

(Vcc = 1.8 V to 5.5 V, Vss = 0.0 V, TA = -40 °C to +85 °C)

Parameter	Symbol		Value		Unit	Remarks
Farameter	Symbol	Min	Тур	Max	Ullit	Remarks
Interrupt release voltage 0	VIDLL0+	2.06	2.3	2.54	V	At power supply rise
Interrupt detection voltage 0	VIDLL0-	1.98	2.2	2.42	V	At power supply fall
Interrupt release voltage 1	VIDLL1+	2.33	2.6	2.87	V	At power supply rise
Interrupt detection voltage 1	VIDLL1-	2.25	2.5	2.75	V	At power supply fall
Interrupt release voltage 2	VIDLL2+	2.6	2.9	3.2	V	At power supply rise
Interrupt detection voltage 2	VIDLL2-	2.52	2.8	3.08	V	At power supply fall
Interrupt release voltage 3	VIDLL3+	2.96	3.3	3.64	V	At power supply rise
Interrupt detection voltage 3	VIDLL3-	2.88	3.2	3.52	V	At power supply fall
Interrupt release voltage 4	VIDLL4+	3.32	3.7	4.08	V	At power supply rise
Interrupt detection voltage 4	VIDLL4-	3.24	3.6	3.96	V	At power supply fall
Interrupt release voltage 5	VIDLL5+	3.68	4.1	4.52	V	At power supply rise
Interrupt detection voltage 5	VIDLL5-	3.6	4	4.4	V	At power supply fall
Power supply start voltage	VoffL	_	_	1.6	V	
Power supply end voltage	VonL	4.52	_	_	V	
Power supply voltage change time (at power supply rise)	tr∟	7300	_	_	μs	Slope of power supply that the interrupt release signal generates within the rating (VIDLL+)
Power supply voltage change time (at power supply fall)	t₁∟	7300	_	_	μs	Slope of power supply that the interrupt detection signal generates within the rating (VIDLL-)
Interrupt release delay time	t diL1			400	μs	
Interrupt detection delay time	t diL2	_	_	400	μs	
Interrupt threshold voltage transition stabilization time	t stbL	_	_	400	μs	
Interrupt low-voltage detection mode switch time	tmdsw	_	_	400	μs	Normal mode ⇔ Low power consumption mode

Note: When being used for interrupt, the low-voltage detection circuit can be switched between normal mode and low power consumption mode. Compared with normal mode, in low power consumption mode, while the detection voltage and release voltage are less accurate, and the detection delay time and the release delay time become longer, there is less power consumption. For the difference in power consumption between normal mode and low power consumption mode, see "22.3 DC Characteristics". For the method of switching between normal mode and low power consumption mode, refer to "CHAPTER 16 LOW-VOLTAGE DETECTION CIRCUIT" in "New 8FX MB95710M/770M Series Hardware Manual".





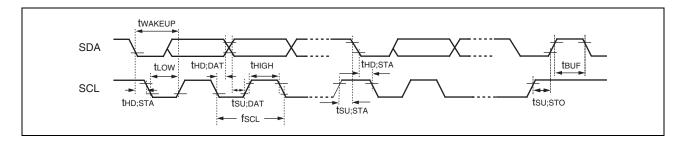


22.4.7 I2C Bus Interface Timing

 $(Vcc = 3.0 \text{ V to } 5.5 \text{ V}, AVss = Vss = 0.0 \text{ V}, T_A = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C})$

				Value				
Parameter	Symbol	Pin name	Condition	Standard- mode		Fast-mode		Unit
				Min	Max	Min	Max	
SCL clock frequency	fscL	SCL		0	100	0	400	kHz
(Repeated) START condition hold time SDA $\downarrow \rightarrow$ SCL \downarrow	thd;sta	SCL, SDA		4.0	_	0.6	_	μs
SCL clock "L" width	tLOW	SCL		4.7	_	1.3	_	μs
SCL clock "H" width	t HIGH	SCL		4.0	_	0.6	_	μs
(Repeated) START condition setup time SCL $\uparrow \rightarrow$ SDA \downarrow	tsu;sta	SCL, SDA	R = 1.7 kΩ, C = 50 pF*1	4.7	_	0.6	_	μs
Data hold time SCL \downarrow \rightarrow SDA \downarrow \uparrow	thd;dat	SCL, SDA	00 pi	0	3.45*2	0	0.9*3	μs
Data setup time SDA $\downarrow\uparrow$ \rightarrow SCL \uparrow	tsu;dat	SCL, SDA		0.25		0.1	_	μs
STOP condition setup time SCL $\uparrow \rightarrow$ SDA \uparrow	t su;sто	SCL, SDA		4	_	0.6	_	μs
Bus free time between STOP condition and START condition	t BUF	SCL, SDA		4.7	_	1.3	_	μs

- *1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.
- *2: The maximum thd; DAT in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at "L" (tLow) does not extend.
- *3: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, provided that the condition of tsu;DAT ≥ 250 ns is fulfilled.





(Vcc = 3.0 V to 5.5 V, AVss = Vss = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Symbol	Pin	Condition		ue*2	Unit	Remarks
	Cymbol	name	Condition	Min	Max	Oilit	Remarks
SCL clock "L" width	t LOW	SCL		(2 + nm/2)tмсLк – 20	<u> </u>	ns	Master mode
SCL clock "H" width	t HIGH	SCL		(nm/2)tмсLк – 20	(nm/2)tмсLк + 20	ns	Master mode
START condition hold time	thd;sta	SCL, SDA		(-1 + nm/2)tмсLк – 20	(-1 + nm)tмсLк + 20	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
STOP condition setup time	t su;sто	SCL, SDA		(1 + nm/2)tмсLк – 20	(1 + nm/2)tмсLк + 20	ns	Master mode
START condition setup time	t su;sta	SCL, SDA		(1 + nm/2)tмсLк – 20	(1 + nm/2)tmcLk + 20	ns	Master mode
Bus free time between STOP condition and START condition	t BUF	SCL, SDA	-R = 1.7 kΩ,	(2 nm + 4)tмсLк – 20	_	ns	
Data hold time	thd;dat	SCL, SDA	$C = 50 \text{ pF}^{*1}$	3 tмськ — 20	_	ns	Master mode
Data setup time	tsu;dat	SCL, SDA		(-2 + nm/2)tмсLк — 20	(-1 + nm/2)tмсLк + 20	ns	Master mode It is assumed that "L" of SCL is not extended. The minimum value is applied to the first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	tsu;int	SCL		(nm/2)tмсLк — 20	(1 + nm/2)tмсLк + 20	ns	The minimum value is applied to the interrupt at the ninth SCL\$\(\psi\$. The maximum value is applied to the interrupt at the eighth SCL\$\(\psi\$.
SCL clock "L" width	tLOW	SCL		4 tmcLK - 20	_	ns	At reception
SCL clock "H" width	t HIGH	SCL		4 tмськ — 20	_	ns	At reception



(Vcc = 3.0 V to 5.5 V, AVss = Vss = 0.0 V, TA = -40 °C to +85 °C)

Parameter	Symbol	Pin	Condition	Value* ²		Unit	Remarks
Parameter	Syllibol	name	Condition	Min	Max	Ullit	
START condition detection	t HD;STA	SCL, SDA		2 tмськ — 20	_	ns	No START condition is detected when 1 tmclk is used at reception.
STOP condition detection	t su;sto	SCL, SDA		2 tмсLк — 20		ns	No STOP condition is detected when 1 tmclk is used at reception.
RESTART condition detection condition	tsu;sta	SCL, SDA	R = 1.7 kΩ, C = 50 pF*1	2 tмс∟к – 20	-	ns	No RESTART condition is detected when 1 tmclk is used at reception.
Bus free time	t BUF	SCL, SDA	C = 50 pr	2 tмськ — 20	_	ns	At reception
Data hold time	t HD;DAT	SCL, SDA		2 tмськ — 20	_	ns	At slave transmission mode
Data setup time	tsu;dat	SCL, SDA		tLow — 3 tмсLк — 20	_	ns	At slave transmission mode
Data hold time	thd;dat	SCL, SDA		0	_	ns	At reception
Data setup time	tsu;dat	SCL, SDA		tмсLк — 20	_	ns	At reception
SDA↓ → SCL↑ (with wakeup function in use)	twakeup	SCL, SDA		Oscillation stabilization wait time +2 tmclk – 20		ns	

^{*1:} R represents the pull-up resistance of the SCL and SDA lines, and C the load capacitance of the SCL and SDA lines.

- m represents the CS[4:3] bits in the I²C clock control register ch.0 (ICCR0).
- n represents the CS[2:0] bits in the I²C clock control register ch.0 (ICCR0).
- The actual timing of the I²C bus interface is determined by the values of m and n set by the machine clock (tmclk) and the CS[4:0] bits in the ICCR0 register.
- · Standard-mode:

m and n can be set to values in the following range: 0.9 MHz < tmcLk (machine clock) < 16.25 MHz.

The usable frequencies of the machine clock are determined by the settings of m and n as shown below.

 $\begin{array}{lll} \text{(m, n)} = (1, 8) & \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 1 \text{ MHz} \\ \text{(m, n)} = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4) & \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 2 \text{ MHz} \\ \text{(m, n)} = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8) & \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 4 \text{ MHz} \\ \text{(m, n)} = (1, 98), (5, 22), (6, 22), (7, 22) & \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 10 \text{ MHz} \\ \text{(m, n)} = (8, 22) & \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \le 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \ge 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} < \text{tmclk} \ge 16.25 \text{ MHz} \\ \text{: } 0.9 \text{ MHz} <$

· Fast-mode:

m and n can be set to values in the following range: 3.3 MHz < tmcLk (machine clock) < 16.25 MHz.

The usable frequencies of the machine clock are determined by the settings of m and n as shown below.

 $\begin{array}{lll} (m,\,n) = (1,\,8) & : 3.3 \; \text{MHz} < \text{tmclk} \le 4 \; \text{MHz} \\ (m,\,n) = (1,\,22),\,(5,\,4) & : 3.3 \; \text{MHz} < \text{tmclk} \le 8 \; \text{MHz} \\ (m,\,n) = (1,\,38),\,(6,\,4),\,(7,\,4),\,(8,\,4) & : 3.3 \; \text{MHz} < \text{tmclk} \le 10 \; \text{MHz} \\ (m,\,n) = (5,\,8) & : 3.3 \; \text{MHz} < \text{tmclk} \le 16.25 \; \text{MHz} \end{array}$

^{*2: •} See "Source Clock/Machine Clock" for tmclk.

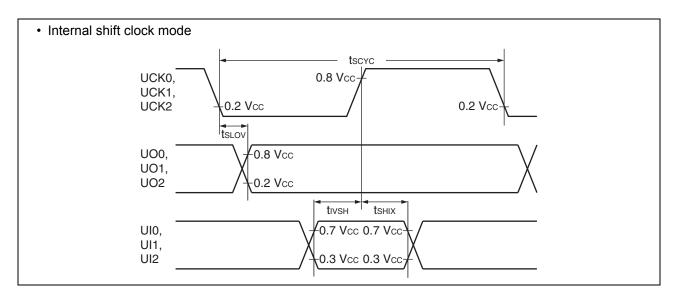


22.4.8 UART/SIO, Serial I/O Timing

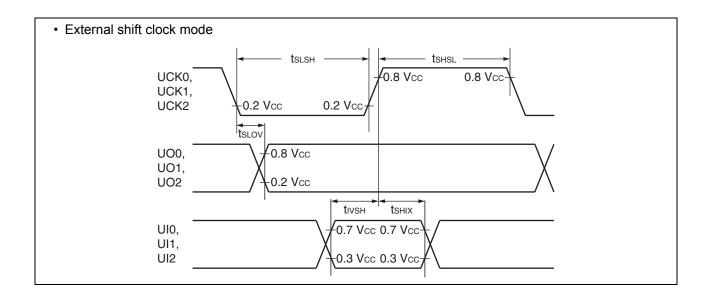
(Vcc = 3.0 V to 5.5 V, AVss = Vss = 0.0 V, TA = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Val	Unit	
Farameter	Symbol	Fili liallie	Condition	Min	Max	Oilit
Serial clock cycle time	tscyc	UCK0, UCK1, UCK2		4 t мськ*	_	ns
$UCK \downarrow \to UO$ time	tslov	UCK0, UCK1, UCK2, UO0, UO1, UO2	Internal clock	-190	+190	ns
Valid UI → UCK \uparrow	tıvsн	UCK0, UCK1, UCK2, UI0, UI1, UI2	operation output pin: C _L = 80 pF + 1 TTL	2 tmclk*	_	ns
UCK $\uparrow \rightarrow$ valid UI hold time	t sнıx	UCK0, UCK1, UCK2, UI0, UI1, UI2		2 tmclk*	_	ns
Serial clock "H" pulse width	tshsl	UCK0, UCK1, UCK2		4 t мськ*		ns
Serial clock "L" pulse width	t slsh	UCK0, UCK1, UCK2		4 t мськ*	_	ns
$UCK \downarrow \to UO$ time	tslov	UCK0, UCK1, UCK2, UO0, UO1, UO2	External clock operation output pin:	_	190	ns
Valid UI → UCK \uparrow	tıvsн	UCK0, UCK1, UCK2, UI0, UI1, UI2	C _L = 80 pF + 1 TTL	2 tmclk*		ns
UCK $\uparrow \rightarrow$ valid UI hold time	t sнıx	UCK0, UCK1, UCK2, UI0, UI1, UI2		2 tmclk*	_	ns

^{*:} See "Source Clock/Machine Clock" for tmclk.







22.4.9 Comparator Timing

 $(AVcc = 1.8 \text{ V to } 5.5 \text{ V}, AVss = 0.0 \text{ V}, T_A = -40 ^{\circ}C \text{ to } +85 ^{\circ}C)$

Doromotor	Din nama	Value		l lm!4	Remarks		
Parameter	Pin name	Min	Тур	Max	Unit	Remarks	
Voltage range	CMP0_P, CMP0_N	0	_	AVcc	V		
Offset voltage	CMP0_P, CMP0_N	-20	_	+20	mV		
Delay time	CMP0_O	_	600	1200	ns	Overdrive 5 mV	
Delay time		_	120	420	ns	Overdrive 50 mV	
Power down delay	CMP0_O	_	_	1200	ns	Power down recovery PD: 1 → 0	
Fower down delay		0		150	ns	Power down PD: 0 → 1	
Power up stabilization time	CMP0_O			1200	ns	Output stabilization time at power up	
Bandgap reference voltage	_	1.15	1.21	1.27	V		



22.5 A/D Converter

22.5.1 A/D Converter Electrical Characteristics

(AVcc = 1.8 V to 5.5 V, Vss = 0.0 V, Ta = -40 °C to +85 °C)

Parameter	Symbol		Value		Unit	Remarks
Parameter	Symbol	Min	Min Typ Max			Kemarks
Resolution		_		12	bit	
Total error		-6		+6	LSB	Vcc ≥ 2.7 V
Total error		-10		+10	LSB	Vcc < 2.7 V
Linearity error	_	-3		+3	LSB	Vcc ≥ 2.7 V
Linearity error		-5		+5	LSB	Vcc < 2.7 V
Differential linearity		-1.9		+1.9	LSB	Vcc ≥ 2.7 V
error		-2.9		+2.9	LSB	Vcc < 2.7 V
Zero transition voltage	Vот	Vss – 6 LSB	_	Vss + 8.2 LSB	V	
Full-scale transition voltage	VFST	AVcc - 6.2 LSB	_	AVcc + 9.2 LSB	V	
Sampling time	Ts	*	_	10	μs	
Compare time	Tcck	0.861	_	14	μs	Vcc ≥ 2.7 V
Compare time	I CCK	2.8	_	14	μs	Vcc < 2.7 V
Time for transiting to operation enabled state	Tstt	1	_	_	μs	
Analog input current	Iain	-0.3	_	+0.3	μΑ	
Analog input voltage	Vain	Vss		AVcc	٧	

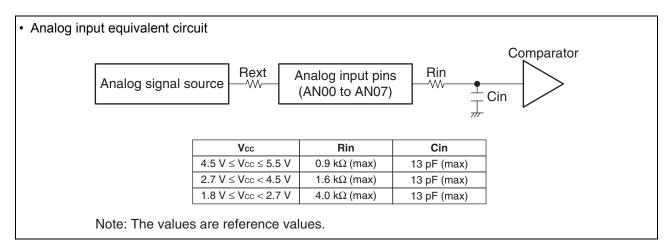
^{*:} See "Notes on Using A/D Converter" for details of the minimum sampling time.



22.5.2 Notes on Using A/D Converter

· External impedance of analog input and its sampling time

The A/D converter of the MB95710M/770M Series has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 μ F to the analog input pin.



Relationship between external impedance and minimum sampling time
 The necessary sampling time varies according to external impedance. Ensure that the following conditions are fulfilled when setting the sampling time.

 $Ts \ge (Rin + Rext) \times Cin \times 9$

T_s: Sampling time

Rin: Input resistance of A/D converter
Cin: Input capacitance of A/D converter
Rext: Output impedance of external circuit

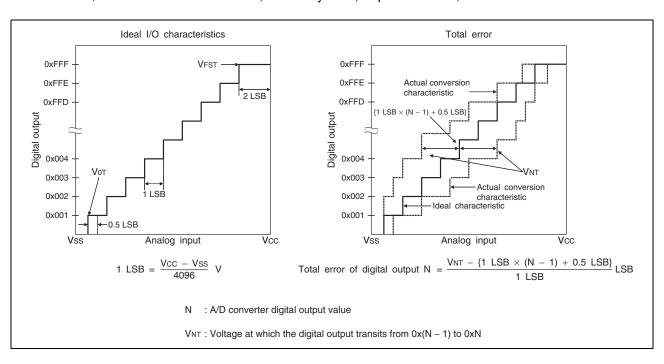
A/D conversion error

As |Vcc - Vss| decreases, the A/D conversion error increases proportionately.

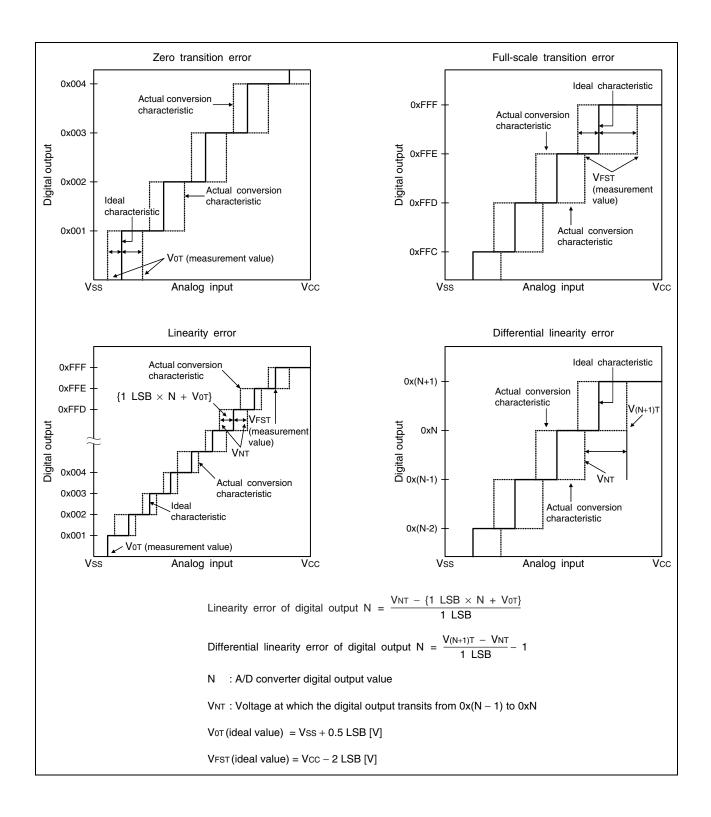


22.5.3 Definitions of A/D Converter Terms

- · Resolution
 - It indicates the level of analog variation that can be distinguished by the A/D converter.
- When the number of bits is 12, analog voltage can be divided into 2^{12} = 4096.
- · Linearity error (unit: LSB)
 - It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point ("00000000000" \leftarrow "000000000001") of a device to the full-scale transition point ("11111111111") \leftarrow "111111111111") of the same device.
- · Differential linear error (unit: LSB)
 - It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.
- Total error (unit: LSB)
 - It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.









22.6 Flash Memory Program/Erase Characteristics

Parameter	Value		Unit	Remarks	
Parameter	Min	Тур	Max	Ullit	Remarks
Sector erase time (2 Kbyte sector)		0.3*1	1.6*2	s	The time of writing "0x00" prior to erasure is excluded.
Sector erase time (24 Kbyte sector and 32 Kbyte sector)	_	0.6*1	3.1*2	s	The time of writing "0x00" prior to erasure is excluded.
Byte writing time	_	17	272	μs	System-level overhead is excluded.
Program/erase cycle	100000	_	_	cycle	
Power supply voltage at program/erase	1.8	_	5.5	V	
	20*3	_	_		Average T _A = +85 °C Number of program/erase cycles: 1000 or below
Flash memory data retention time	10*3	_	_	year	Average T _A = +85 °C Number of program/erase cycles: 1001 to 10000 inclusive
	5 *³	_	_		Average T _A = +85 °C Number of program/erase cycles: 10001 or above

^{*1:} $\sqrt{\text{cc}} = 5.5 \text{ V}$, $I_A = +25 \text{ °C}$, 0 cycle

^{*2:} Vcc = 1.8 V, TA = +85 °C, 100000 cycles

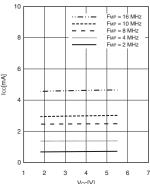
^{*3:} These values were converted from the result of a technology reliability assessment. (These values were converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85 °C.)



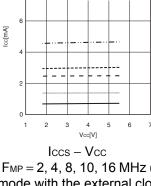
23. Sample Characteristics

Power supply current temperature characteristics

 $T_A = +25$ °C, $F_{MP} = 2, 4, 8, 10, 16$ MHz (divided by 2) Main clock mode with the external clock operating



 $T_A = +25$ °C, $F_{MP} = 2, 4, 8, 10, 16$ MHz (divided by 2) Main sleep mode with the external clock operating



Vcc = 3.3 V, Fmp = 2, 4, 8, 10, 16 MHz (divided by 2) Main sleep mode with the external clock operating

-50

Icc - Ta

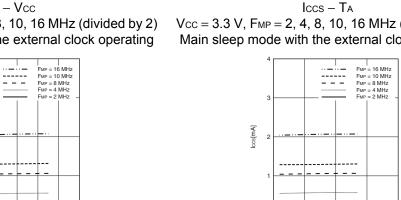
Vcc = 3.3 V, Fmp = 2, 4, 8, 10, 16 MHz (divided by 2)

Main clock mode with the external clock operating

+100

Ta[°C]

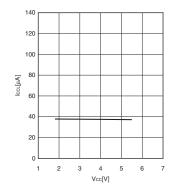
+150



 $\mathsf{Iccl}-\mathsf{Vcc}$

5 6

 $T_A = +25$ °C, $F_{MPL} = 16$ kHz (divided by 2) Subclock mode with the external clock operating



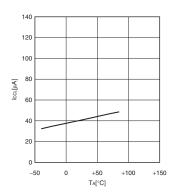
ICCL - TA Vcc = 3.3 V, Fmpl = 16 kHz (divided by 2) Subclock mode with the external clock operating

+50

Ta[°C]

+100

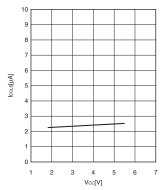
+150





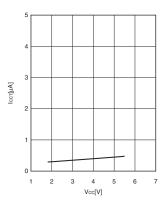
 $I_{CCLS} - V_{CC}$

 $T_A = +25$ °C, $F_{MPL} = 16$ kHz (divided by 2) Subsleep mode with the external clock operating



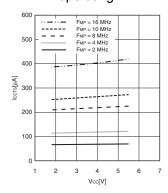
Iсст — Vсс

 $T_A = +25$ °C, $F_{MPL} = 16$ kHz (divided by 2) Watch mode with the external clock operating



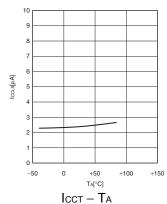
Iccts - Vcc

 $T_A = +25$ °C, $F_{MP} = 2$, 4, 8, 10, 16 MHz (divided by 2) Time-base timer mode with the external clock operating

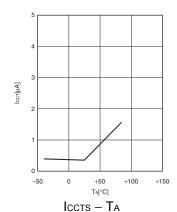


Iccls - Ta

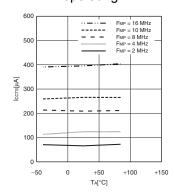
Vcc = 3.3 V, $F_{MPL} = 16 \text{ kHz}$ (divided by 2) Subsleep mode with the external clock operating



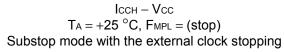
 $V_{\text{CC}} = 3.3 \text{ V}, \text{ F}_{\text{MPL}} = 16 \text{ kHz}$ (divided by 2) Watch mode with the external clock operating

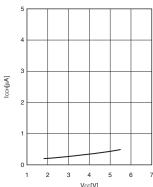


Vcc = 3.3 V, FMP = 2, 4, 8, 10, 16 MHz (divided by 2) Time-base timer mode with the external clock operating

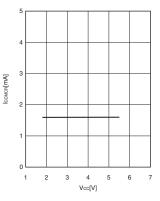




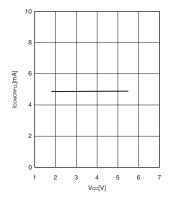




ICCMCR - VCC $T_A = +25$ °C, $F_{MP} = 4$ MHz (no division) Main CR clock mode

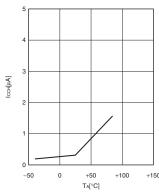


 $\mathsf{ICCMCRPLL} - \mathsf{VCC}$

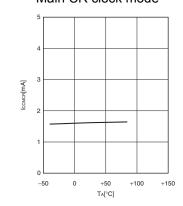


Main CR PLL clock mode

Іссн – Та Vcc = 3.3 V, Fmpl = (stop)Substop mode with the external clock stopping

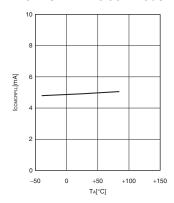


ICCMCR - TA Vcc = 3.3 V, Fmp = 4 MHz (no division)Main CR clock mode



ICCMCRPLL - TA

 $T_A = +25$ °C, $F_{MP} = 16$ MHz (PLL multiplication rate: 4) $V_{CC} = 3.3$ V, $F_{MP} = 16$ MHz (PLL multiplication rate: 4) Main CR PLL clock mode

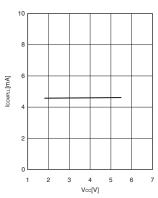




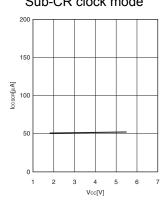
(Continued)

ICCMPLL - VCC

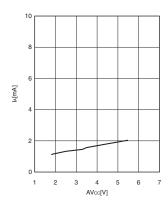
 $T_A = +25$ °C, $F_{MP} = 16$ MHz (PLL multiplication rate: 4) $V_{CC} = 3.3$ V, $F_{MP} = 16$ MHz (PLL multiplication rate: 4) Main PLL clock mode



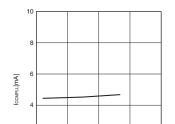
 $I_{CCSCR} - V_{CC}$ TA = +25 °C, FMPL = 50 kHz (divided by 2) Sub-CR clock mode



 $I_A - AVcc$ $T_A = +25~^{\circ}C,~F_{MP} = 16~MHz~(divided~by~2)$ Main clock mode with the external clock operating



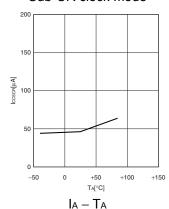
ICCMPLL — TA



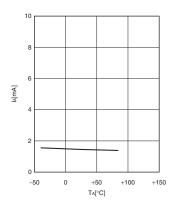
ICCSCR - TA

+150

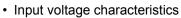
Vcc = 3.3 V, F_{MPL} = 50 kHz (divided by 2) Sub-CR clock mode

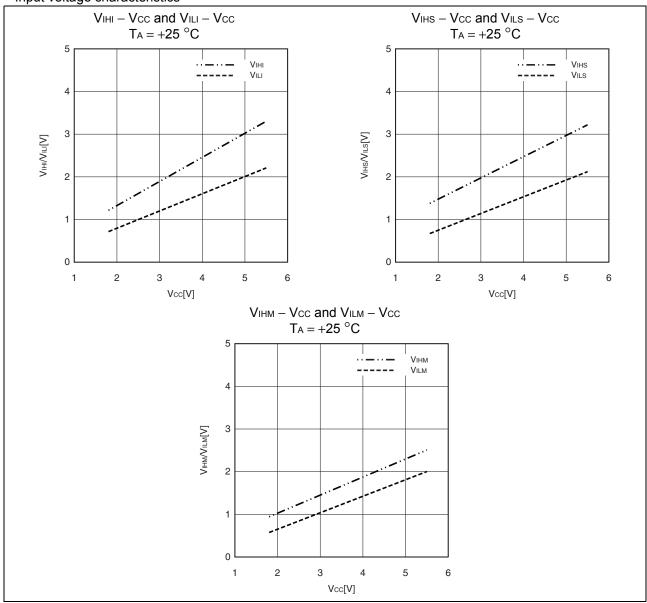


 $Vcc = 3.3 \text{ V}, F_{\text{MP}} = 16 \text{ MHz}$ (divided by 2) Main clock mode with the external clock operating



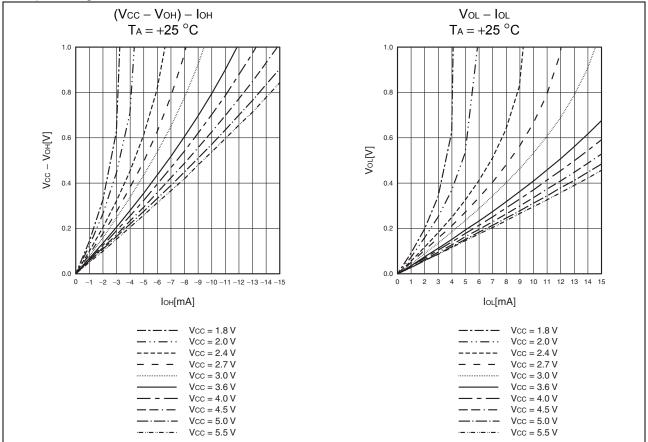




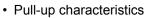


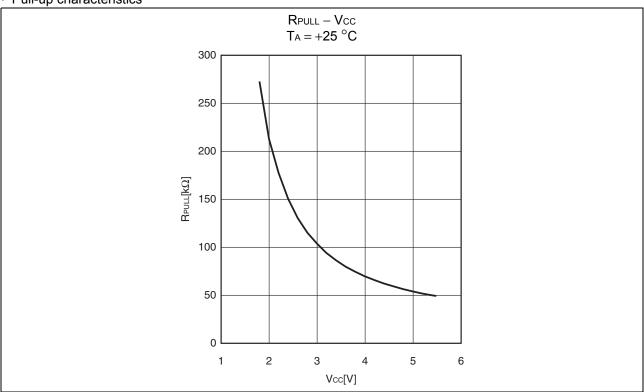


· Output voltage characteristics









24. Mask Options

No.	Part number	MB95F714J MB95F714M MB95F716J MB95F716M MB95F718J MB95F718M MB95F774J MB95F774M MB95F776J MB95F776M MB95F778J MB95F778M	
	Selectable/Fixed		ked
1	Low-voltage detection reset	With low-voltage detection reset	Without low-voltage detection reset
2	Reset	Without dedicated reset input	With dedicated reset input



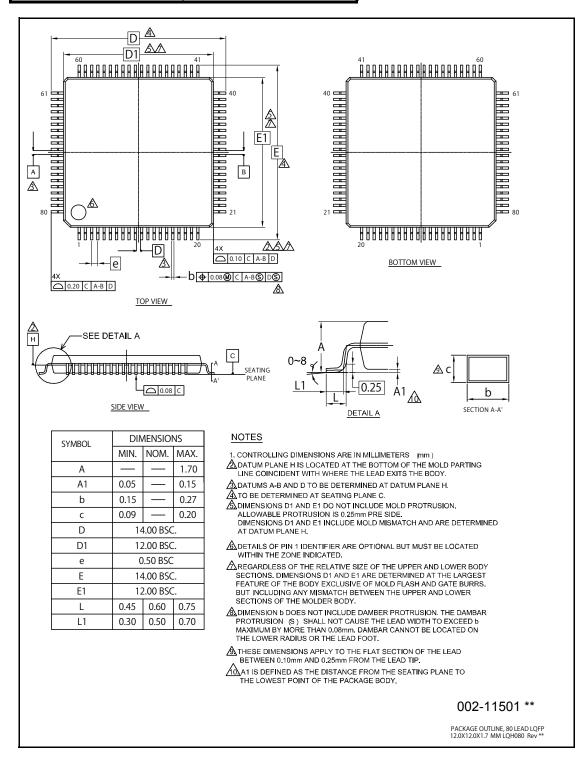
25. Ordering Information

Part number	Package
MB95F714JPMC-G-SNE2 MB95F714MPMC-G-SNE2 MB95F716JPMC-G-SNE2 MB95F716MPMC-G-SNE2 MB95F718JPMC-G-UNE2 MB95F718MPMC-G-SNE2	80-pin plastic LQFP (LQH080)
MB95F774JPMC1-G-SNE2 MB95F774MPMC1-G-SNE2 MB95F776JPMC1-G-SNE2 MB95F776MPMC1-G-SNE2 MB95F778JPMC1-G-SNE2 MB95F778MPMC1-G-SNE2	64-pin plastic LQFP (LQD064)
MB95F774JPMC2-G-SNE2 MB95F774MPMC2-G-SNE2 MB95F776JPMC2-G-SNE2 MB95F776MPMC2-G-SNE2 MB95F778JPMC2-G-UNE2 MB95F778MPMC2-G-SNE2	64-pin plastic LQFP (LQG064)



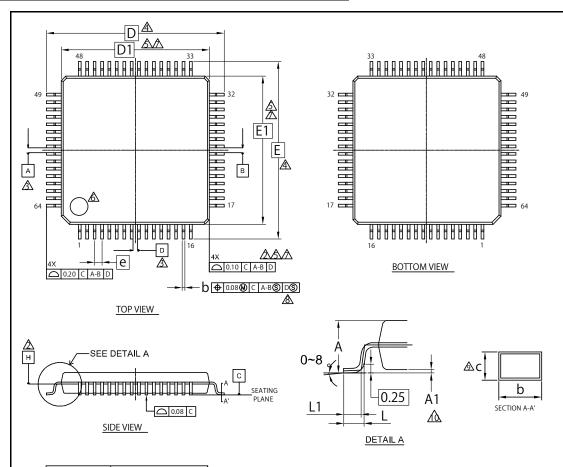
26. Package Dimension

Package Type	Package Code
LQFP 80	LQH 080





Package Type	Package Code
LQFP 64	LQD 064



SYMBOL	DIN	MENSIO	NS	
STIVIBUL	MIN.	NOM.	MAX.	
Α	_	_	1.70	
A1	0.00	_	0.20	
b	0.15	_	0.2 7	
С	0.09	_	0.20	
D	12.00 BSC.			
D1	10.00 BSC.			
е	0.50 BSC			
E	12.00 BSC.			
E1	10.00 BSC.			
L	0.45	0.60	0.75	
L1	0.30	0.50	0.70	

NOTES

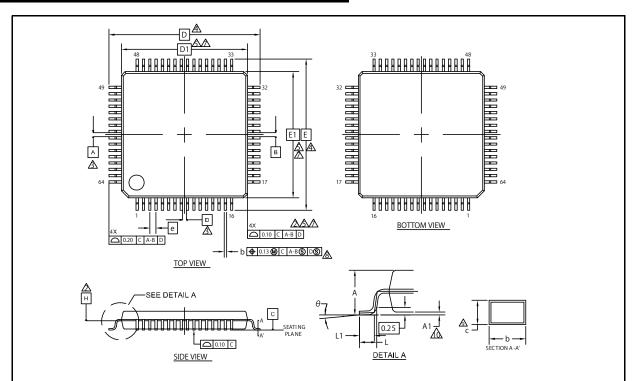
- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
- ⚠DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- ⚠DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- ADIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
 ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE.
 DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- ⚠DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- ÀDIMENSION 6 DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION. (\$) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 6 MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- ATHESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- 0) A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11499 **

PACKAGE OUTLINE, 64 LEAD LQFP 10.0X10.0X1.7 MM LQD064 Rev**



Package Type	Package Code
LQFP 64	LQG 064



SYMBOL	DII	MENSIO	N		
STIVIBOL	MIN.	NOM.	MAX.		
А			1.70		
A1	0.00		0.20		
b	0.27	0.32	0.37		
С	0.09		0.20		
D	14	4.00 BSC	,		
D1	12.00 BSC				
е	0.65 BSC				
E	14.00 BSC				
E1	1.	2.00 BSC	-		
L	0.45	0.60	0.75		
L1	0.30	0.50	0.70		
θ	0°	_	8°		

NOTES

- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
- ⚠ DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- ⚠ DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- $\overline{\triangle}$ TO BE DETERMINED AT SEATING PLANE C.
- ⚠ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
 ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE.
 DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED
 - AT DATUM PLANE H.
- ⚠ DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- AREGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- ⚠ DIMENSION 6 DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (6) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 6 MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13881 **

PACKAGE OUTLINE, 64 LEAD LQFP 12.0X12.0X1.7 MM LQG064 REV**



Document History Page

	Document Title: MB95710M Series, MB95770M Series, New 8FX 8-bit Microcontrollers Document Number: 002-09307				
Revision	ECN	Orig. of Change	Submission Date	Description of Change	
**	-	YSKA	07/31/2013	Migrated Spansion DS702-00019-1v0-E to Cypress and assigned document number 002-09307. No change to document contents or format.	
*A	5511943	YSKA	11/08/2016	Updated to Cypress template	
*B	5633448	HTER	03/07/2017	Changed the package codes as the following from "FPT-80P-M37" to "LQH080" from "FPT-64P-M38" to "LQD064" from "FPT-64P-M39" to "LQD064" in chapter: 1.Product Line-up (Page 6, 9) 2.Packages And Corresponding Products (Page 9) 4.Pin Assignment (Page 11 to 12) 25.Ordering Information (Page 167) 26.Package Dimensions (Page 168 to 170). Changed the Part numbers from "MB95F778JPMC2-G-SNE2" to "MB95F778JPMC2-G-UNE2" in chapter 25.Ordering Information (Page 167).	
*C	5772061	YSAT	06/15/2017	Adapted new Cypress logo	
*D	5900838	HUAL	09/29/2017	Modified from "MB95F718JPMC-G-SNE2" to "MB95F718JPMC-G-UNE2" in 25.Ordering Information (Page 167).	



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