The Future of Analog IC Technology

MP2625B

2A Switching Charger with NVDC Power Path Management For Single Cell Li+ Battery

DESCRIPTION

The MP2625B is a monolithic switch mode battery charger with power path management for single-cell Li-ion batteries in a wide range of tablet and other portable devices. It integrates a synchronous BUCK regulator to provide regulated voltage for powering the system output and at the same time charging the battery. This device supports both USB and high power DC adapter input. In USB mode, the input current limit can be programmed to 450mA or 825mA via the logic pins to cover the USB2.0 and USB3.0 specifications. When the adapter input is present, the input current can also be limited in order to avoid overloading of the DC adapter. Input current limit can be programmed up to 2A.

The smart power path management allows MP2625B to regulate the system voltage for powering an external load and charging the battery independently and simultaneously. This allows immediate system operation even under missing or deeply discharged battery. When the input current limit is reached, the system load is satisfied in priority, then the charger will take the remaining current to charge the battery. Additionally, the smart power path control allows an internal connection from battery to the system in order to supplement additional power to the load in the event the system power demand increases over the input limited power or the input is removed.

The MP2625B features high integration with all the power switches integrated inside. No external MOSFET, blocking diodes, or current sense resistor is required.

Two status monitor output pins are provided to indicate the battery charge status and power source status. Other features include trickle charge, battery temperature monitoring, timer and thermal limiting regulation on chip.

MP2625B is available in QFN 3mmx4mm package.

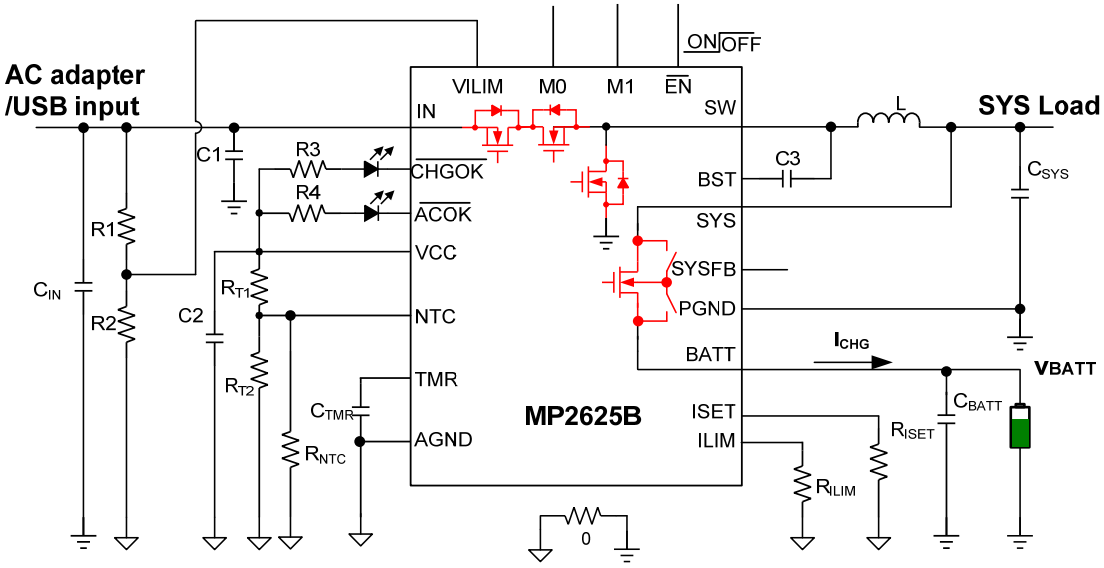
FEATURES

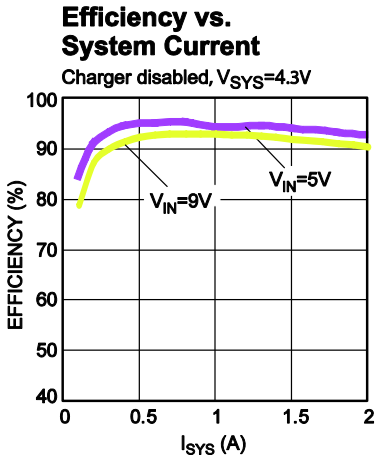
- 4V to 10V Operating Input Voltage
- Smart Power Path Management
- Five Control Loops: Input Current Limit, Input Voltage Limit, Constant Charge Current, Terminal Battery Control and Thermal Fold-Back.
- 1.6MHz Switching Frequency
- Programmable Input Current Limit
- Programmable Charge Current
- Single Input for USB and AC adapter
- Cover USB2.0 and USB3.0 Input Specification
- Fully Integrated Power Switches
- No External Blocking Diode and Sense Resistor Required
- Charging Operation Indicator
- Built-in Programmable Charging Timer
- Thermal Limiting Regulation on Chip
- Battery Temperature Monitor
- Tiny Package Features Small Size

APPLICATIONS

- Smart Phone
- E-Book
- GPS
- Portable Media Player
- Portable Hand-held Solution
- Tablet PC

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2625BGL	QFN-20 (3mmx4mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP2625BGL–Z);

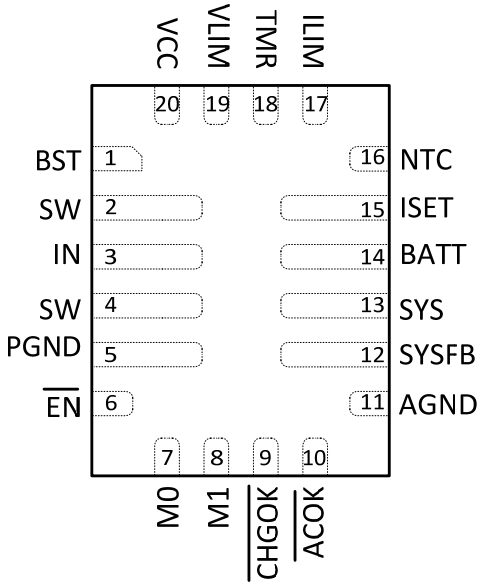
TOP MARKING

MPYW
2625
BLLL

MP: MPS prefix
Y: year code
W: week code
2625B: part number
LLL: lot number

PACKAGE REFERENCE

TOP VIEW



QFN-20 (3mmx4mm)

PIN FUNCTIONS

Package Pin #	Name	Description
1	BST	Bootstrap. A capacitor is connected between SW and BST pin to form a floating supply across the power switch driver to drive the power switch's gate above the supply voltage.
3	IN	Power input of the IC from adapter or USB.
2,4	SW	Switch output.
5	PGND	Power ground.
6	$\overline{EN}$	Function logic control pin of the IC. Logic low to enable the part and logic high to disable the part.
7	M0	Mode Select Input Pin, in combination with M1 pin, setting the input current limit mode.
8	M1	Mode Select Input Pin, in combination with M0 pin, setting the input current limit mode.
9	$\overline{CHGOK}$	Open drain output. It is pulled low during charging. And it is pulled high through an external resistor to VCC to indicate charge completed.
10	$\overline{ACOK}$	Open drain output. It is pulled low to indicate the presence of a valid input power supply. Otherwise, it is pulled high through an external resistor to VCC to indicate invalid input or removed input.
11	AGND	Analog ground.
12	SYSFB	SYS voltage program pin. Connect a resistor divider from the pin to SYS and AGND to program the system output voltage. Leave the pin float to disable the function.
13	SYS	DC-DC regulator output to power the system load and charge the battery.
14	BATT	Positive battery terminal.
15	ISET	Charge current program pin. A resistor from the pin to AGND can program the charge current during CC charge. Float the pin will disable the charge function.
16	NTC	Thermistor input. Connect a resistor from this pin to VCC and the thermistor from this pin to ground. The thermistor is usually inside the battery pack.
17	ILIM	Input current limit program pin. A resistor from the pin to AGND can program the input current limit with adapter input.
18	TMR	Set timer out period. Connect TMR pin to AGND to disable the internal timer.
19	VLIM	Input voltage clamp program pin.
20	VCC	Supply voltage of the IC.

ABSOLUTE MAXIMUM RATINGS (1)

IN, SW .....-0.3V to +20V
BATT, SYS .....-0.3V to +6V
BST.....-0.3V to +26V
All Other Pins.....-0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2)
QFN20 3mmx4mm..... 2.6W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature.....–65°C to 150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....4.0V to 10V
Operating Junction Temp. (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-20 (3mmx4mm).....	48	11...	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Power (IN)						
IN Operating Range	V_{IN}		4.0		10	V
IN Under Voltage Lockout Threshold		Rising	3.65	3.8	3.95	V
		Falling	3.35	3.5	3.65	V
IN vs. BATT Threshold		Rising	240	280	320	mV
		Falling	40	70	120	mV
BST Voltage Threshold	V_{BST}-V_{SW}	Rising	2.7	2.9	3.1	V
		Falling	2.55	2.75	2.95	V
Switching Frequency			1.4	1.6	1.8	MHz
Input Current Limit	I_{IN}	USB2.0 Mode	400	450	500	mA
		USB3.0 Mode	750	825	900	mA
		Default Mode	1840	2000	2160	mA
		Programmable Mode, R_{ILIM}=23k	1840	2000	2160	mA
Input Current Limit Reference Voltage	V_{ILIM}		1.1	1.14	1.18	V
High-side NMOS On Resistance	$R_{H\ DS(ON)}$	Include the BLOCK FET		120	130	mΩ
Low-side NMOS On Resistance	$R_{L\_DS(ON)}$			80	100	mΩ
High-side NMOS Peak Current limit			3.0	4.0	5.0	A
Input Voltage Clamp Threshold	V_{VLIM}	Voltage on VLIM	1.49	1.52	1.55	V
Input Quiescent Current	I_{IN}	Charger Enabled, USB2.0 Mode		2.4	5	mA
		Charger Enabled, USB3.0 Mode		2.8	5	mA
		Charger Enable, Programmable Mode		3.8	5	mA
		Charger Enabled, Default Mode		3.8	5	mA
		Disabled, EN=0V		3	5	uA
SYS to IN reverse current blocking		SYS=SW=4.5V,VIN=0V, monitor VIN leakage		0.01	0.2	uA
SYS Output						
Minimum SYS Regulation Voltage	V_{SYS}	SYS voltage @ V_{BATT}≤3.4V, SYSFB float	3.45	3.6	3.75	V
SYS Regulation Voltage	V_{SYS}	3.4V<V_{BATT}≤4.2V, SYSFB float BATT Float	3.5	V_{BATT}+ 0.2V	4.5	V
		User Programmed by SYSFB	4.08		4.4	V
SYS Reference Voltage	V_{SYS_REF}		1.135	1.152	1.170	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
BATT to SYS Resistance		V_{IN}=0V, I_{SYS}=200mA, V_{BATT}=4.2V		0.04	0.05	Ω
BATT to SYS Current Limit		V_{SYS}>V_{BATT}–800mV, V_{BATT}=4.2V	**4**	5	**6**	A
		SYS short		230		mA
Battery Charger						
Terminal Battery Voltage	V_{BATT}	V_{BATT}>V_{RECH}, I_{CHG}≤I_{BF}, SYSFB float	4.168	4.2	4.232	V
		V_{SYS}<4.2V Programmed by SYSFB Pin		V_{SYS}- 0.04 x I_{BF}		V
Recharge Threshold at V_{BATT}	V_{RECH}	SYSFB Float	3.9	4.0	4.1	V
		SYSFB programmed	3.85	3.95	4.05	V
Recharge Hysteresis				85		mV
Trickle Charge Threshold			2.9	3	3.1	V
Trickle Charger Hysteresis				200		mV
Trickle Charge Current	$I_{TRICKLE}$			10%		I_{CC}
Termination Charger Current	I_{BF}		5%	10%	15%	I_{CC}
I_{BF} Maximum Limit				150	200	mA
Constant Current Mode Charge Current	I_{CC}	R_{ISET}=1.05k	1.8	2.0	2.2	A
		R_{ISET}=1.53k	1.26	1.4	1.54	A
		R_{ISET}=4.6k	0.405	0.45	0.495	A
ISET Reference Voltage			1.1	1.15	1.2	V
Battery UVLO		Rising	2.4	2.6	2.8	V
		Falling	2.2	2.4	2.6	V
Idea Diode Regulation Voltage	V_{SYS}	Supplement Mode		V_{BATT}- 65mV		mV
BATT Leakage Current	I_{BATT}	V_{BATT}=4.2V, SYS float, V_{IN}=PGND		20	30	μA
$\overline{\text{ACOK}}$, $\overline{\text{CHGOK}}$						
$\overline{\text{ACOK}}$, $\overline{\text{CHGOK}}$ Pin Output Low Voltage		Sinking 5mA		270	350	mV
$\overline{\text{ACOK}}$,$\overline{\text{CHGOK}}$Pin Leakage Current		Connected to 3.3V		0.1	0.5	uA
Timer						
Trickle Charge Time		C_{TMR}=0.1μF, I_{CHG}=1A		45		Min
Total Charge Time		C_{TMR}=0.1μF, I_{CHG}=1A		6.5		Hour

ELECTRICAL CHARACTERISTICS *(continued)*

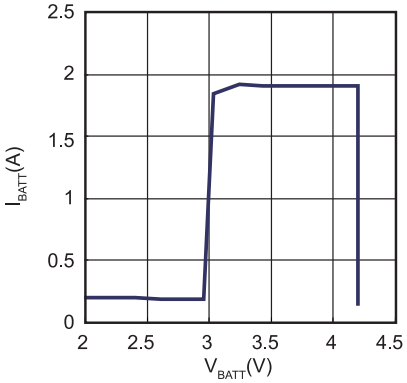
V_{IN} = 5.0V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Negative Temperature Coefficient (NTC) Control						
NTC Low Temp Rising Threshold	V_{THL}	R_{NTC}=NCP18XH103F 0°C	63	65	67	%V_{CC}
Hysteresis on Low Temp Threshold				35		mV
NTC High Temp Falling Threshold	V_{THH}	R_{NTC}=NCP18XH103F, 50°C	32	33.5	35	%V_{CC}
Hysteresis on High Temp Threshold				70		mV
VCC Supply						
VCC UVLO		Rising	3.15	3.35	3.55	V
		Falling	2.8	3	3.2	V
VCC Output Voltage		0mA<I_{VCC}<25mA, V_{IN}=6V	4.3	4.5	4.6	V
VCC Output Current Limit				40		mA
Logic						
$\overline{EN}$ Input Low Voltage					0.4	V
$\overline{EN}$ Input High Voltage			1.5			V
$\overline{EN}$ Input Current		$\overline{EN}$ =4V		4	8	µA
		$\overline{EN}$ =0V	-0.5	-0.1		
M0, M1		Logic High	1.5			V
		Logic Low			0.4	V
Protection						
Thermal Limit Temperature				120		°C
Thermal Shutdown				150		°C

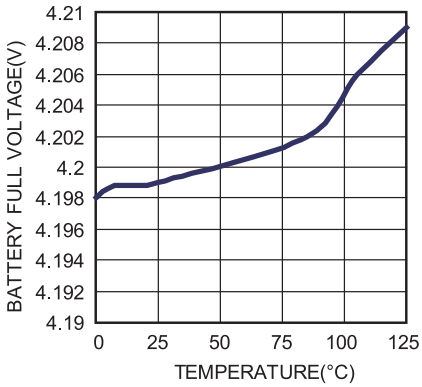
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5.0V, V_{BATT} = Full Range, Default Mode, I_{IN} Limit=2A, V_{SYS}=4.4V, R6 and R7 are float, I_{CHG}=2A, V_{IN} Clamp=4.5V, L = 1.2 µH, T_A = +25ºC, unless otherwise noted.

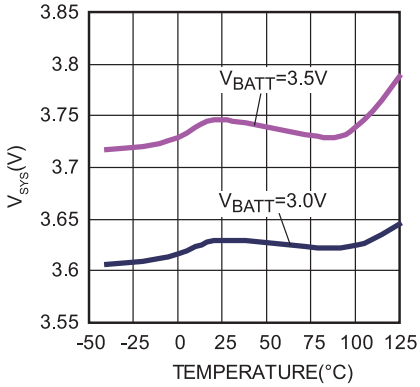
Charge Current vs. Battery Voltage



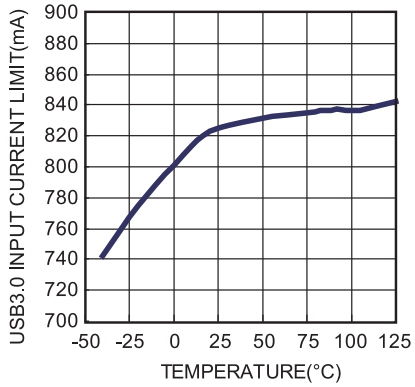
Battery Regulation vs. Temperature



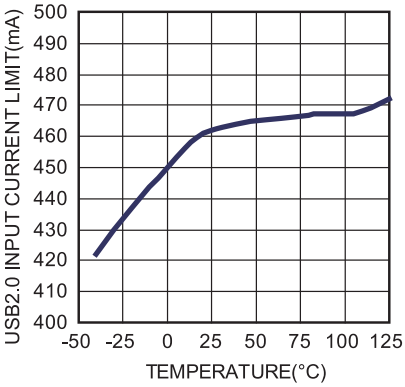
System Voltage Regulation vs. Temperature



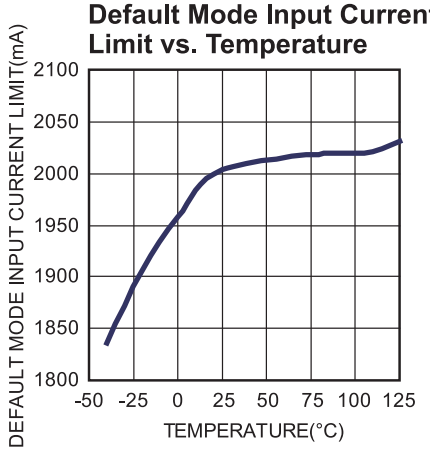
USB3.0 Input Current Limit vs. Temperature



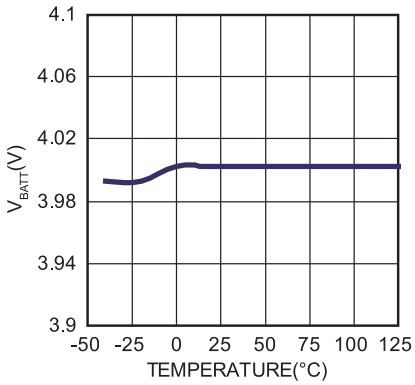
USB2.0 Input Current Limit vs. Temperature



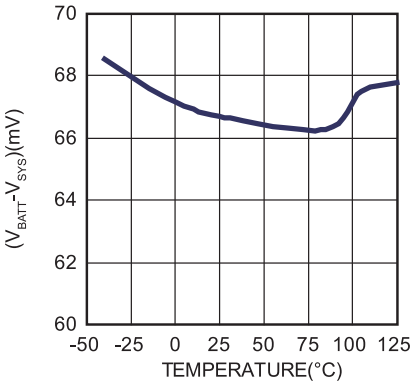
Default Mode Input Current Limit vs. Temperature



Battery Auto-recharge Threshold vs. Temperature



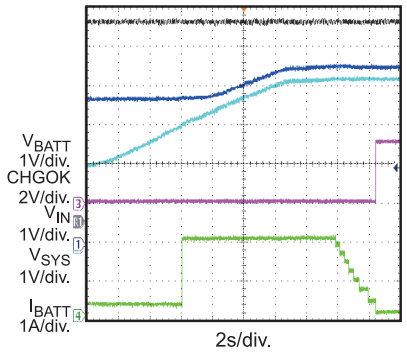
Ideal Diode Regulation vs. Temperature



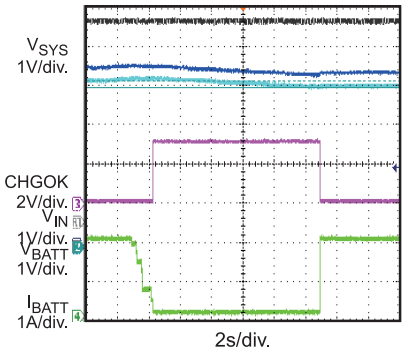
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = Full Range, Default Mode, I_{IN} Limit=2A, V_{SYS}=4.4V, R6 and R7 are float, I_{CHG}=2A, V_{IN} Clamp=4.5V, L = 1.2 µH, T_A = +25ºC, unless otherwise noted.

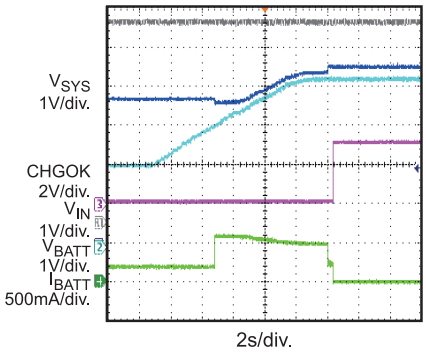
Battery Charge Curve
I_{SYS} = 0A



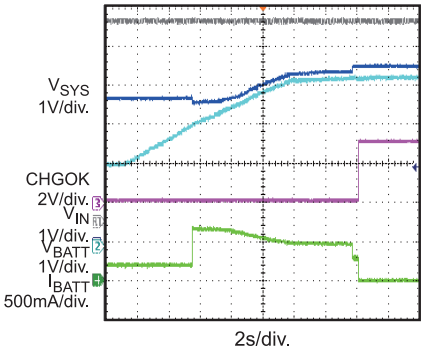
Auto-Recharge
I_{SYS} = 0A



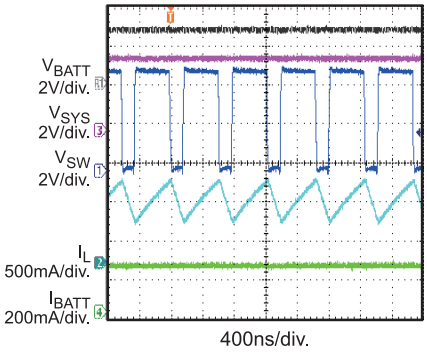
USB IN Battery Charge Curve
USB2.0 Mode, I_{SYS} = 0A



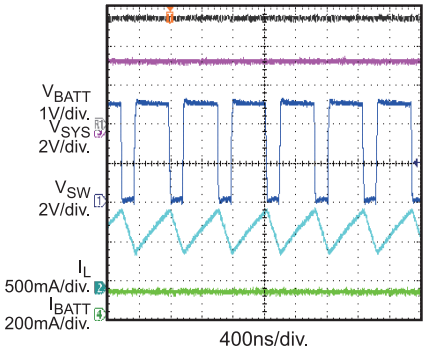
USB IN Battery Charge Curve
USB3.0 Mode, I_{SYS} = 0.5A



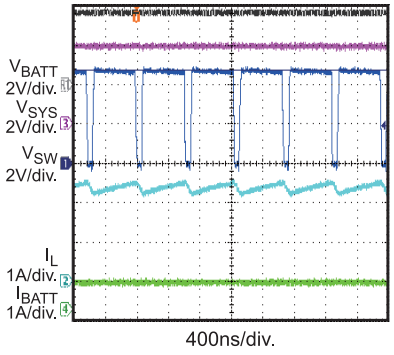
TC Steady State
V_{BATT} = 2.6V, I_{SYS} = 0.5A



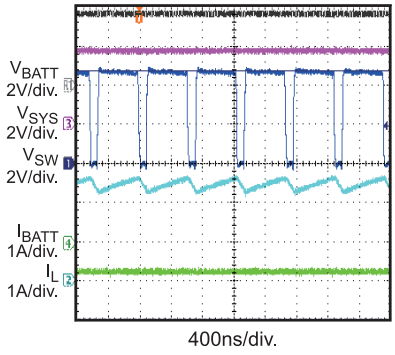
TC Steady State
USB2.0 Mode,V_{BATT} = 2.6V
I_{SYS} = 0.5A



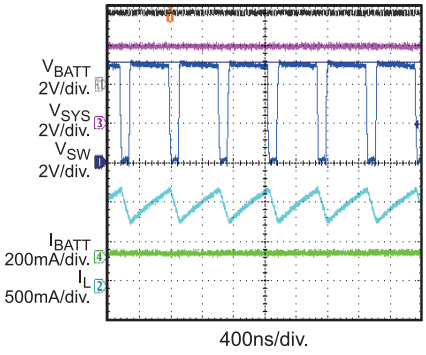
CC Steady State
V_{BATT} = 3.8V, I_{SYS} = 1.5A



CC Steady State @ Supplement Mode
V_{BATT} = 3.8V, I_{SYS} = 3A



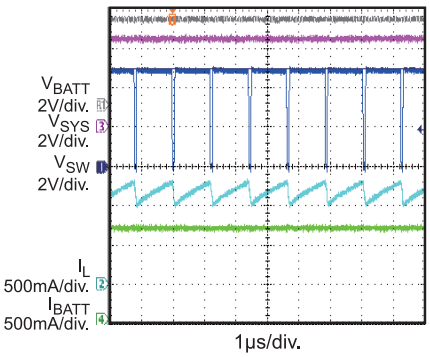
CC Steady State
USB3.0 Mode,V_{BATT} = 3.8V
I_{SYS} = 1.5A



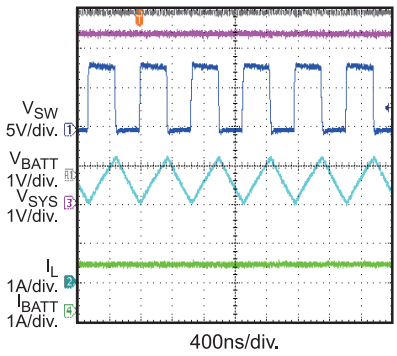
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = Full Range, Default Mode, I_{IN} Limit=2A, V_{SYS}=4.4V, R6 and R7 are float, I_{CHG}=2A, L = 1.2 µH, T_A = +25ºC, unless otherwise noted.

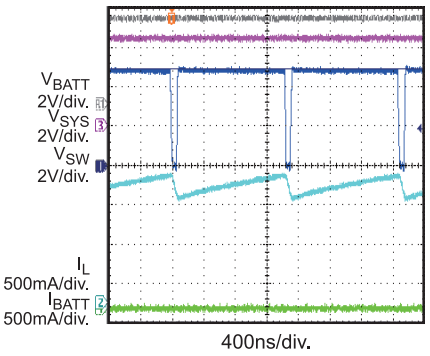
CV Steady State
V_{BATT} = 4.2V, I_{SYS} = 0A



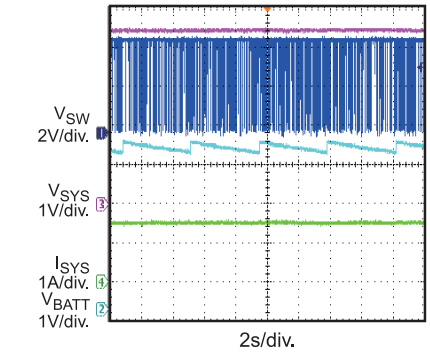
CV Steady State
V_{IN}=9V, V_{BATT}=4.2V, I_{SYS}=1.5A



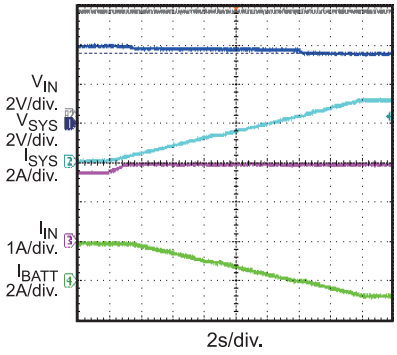
Battery Full Steady State
V_{BATT} = 4.2V, I_{SYS} = 1.5A



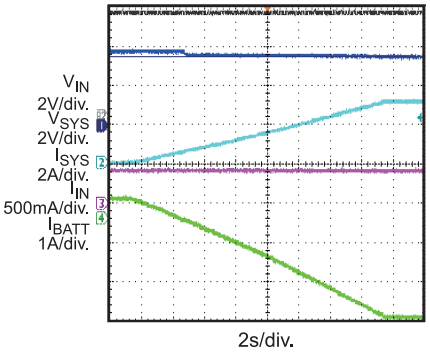
Battery Float Steady State
No Battery, I_{SYS} = 1.5A



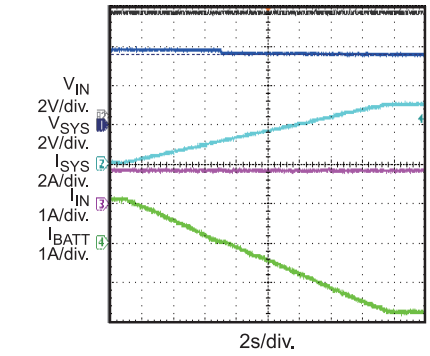
Input Current Limit
V_{BATT} = 3.7V, Ramp up I_{SYS}



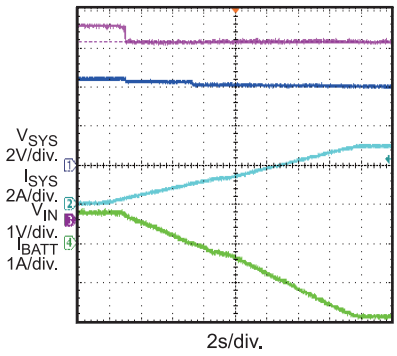
Input Current Limit
USB2.0 Mode,V_{BATT} = 3.7V
Ramp up I_{SYS}



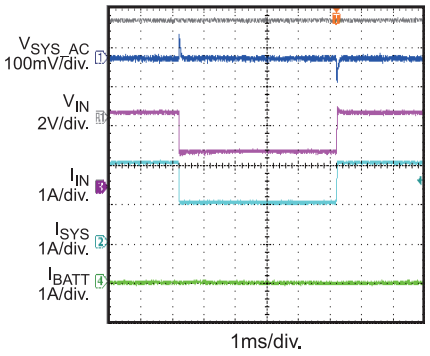
Input Current Limit
USB3.0 Mode,V_{BATT} = 3.7V
Ramp up I_{SYS}



Input Voltage Limit
5V/1A Adapter IN,V_{BATT} = 4.2V
Ramp up I_{SYS}



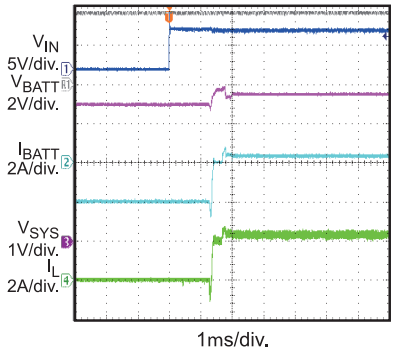
System Current Transient
Battery Full,I_{SYS} = 1-2A transient,0.05A/µs



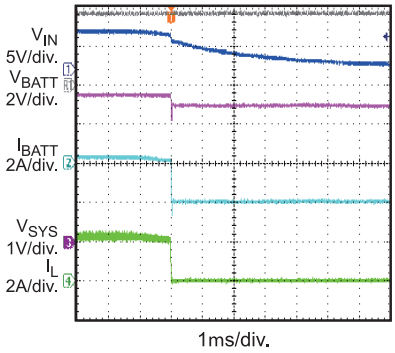
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = Full Range, Default Mode, I_{IN} Limit=2A, V_{SYS}=4.4V, R6 and R7 are float, I_{CHG}=2A, L = 1.2 µH, T_A = +25ºC, unless otherwise noted.

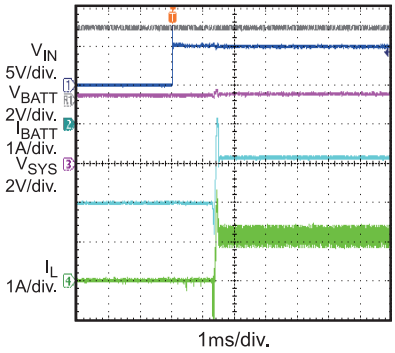
Plug in Adapter
V_{BATT} = 3.7V, I_{SYS} = 2A



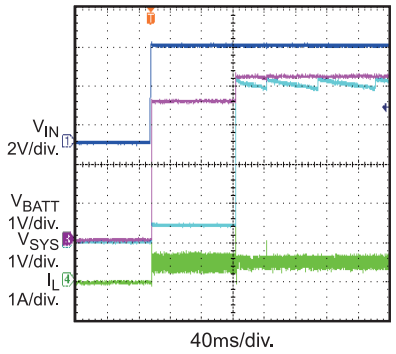
Remove Adapter
V_{BATT} = 3.7V, I_{SYS} = 2A



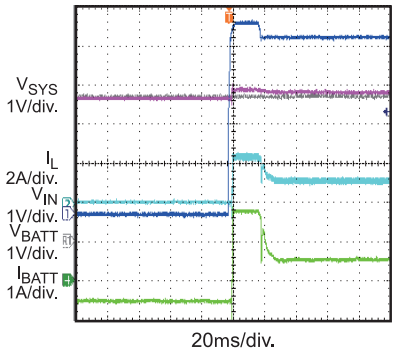
Plug in USB
USB 3.0 Mode, V_{BATT} = 3.7V
I_{SYS} = 2A



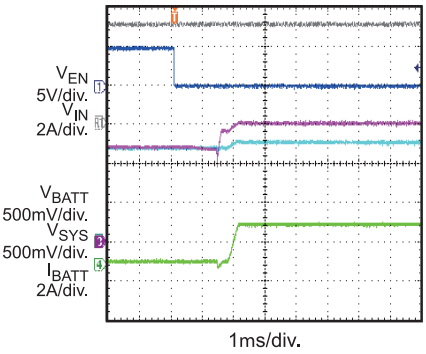
Plug in Adapter
No Battery, V_{SYS} = 4.2V, I_{SYS} = 0.5A



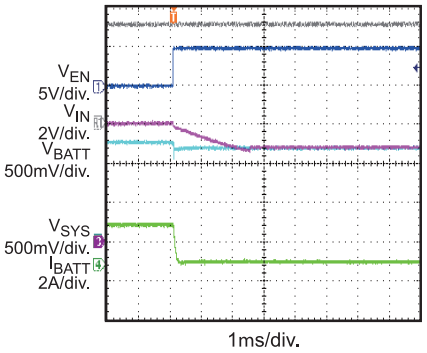
Plug in Adapter
V_{IN} = 5V/1A Adapter,
V_{BATT} = 3.7V, I_{SYS} = 0.5A



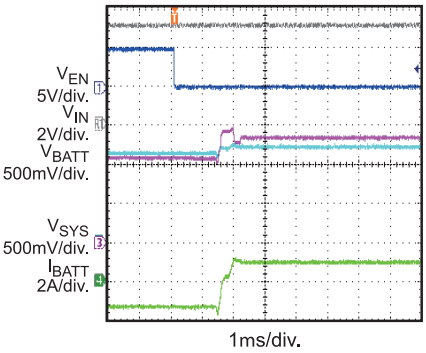
En On
V_{BATT} = 3.7V, I_{SYS} = 0A
(V_{BATT} & V_{SYS} has 2.5V Offset)



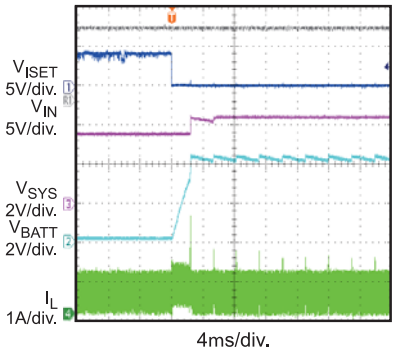
En Off
V_{BATT} = 3.7V, I_{SYS} = 0A
(V_{BATT} & V_{SYS} has 2.5V Offset)



En On
V_{BATT} = 3.7V, I_{SYS} = 1.5A
(V_{BATT} & V_{SYS} has 2.5V Offset)



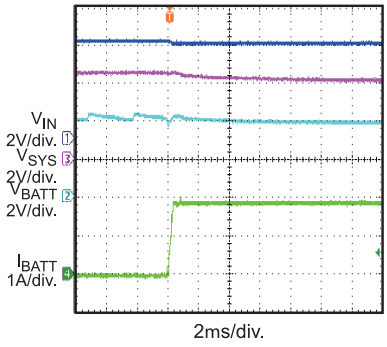
Charge On
V_{IN} = 9V, No Battery, I_{SYS} = 0.5A



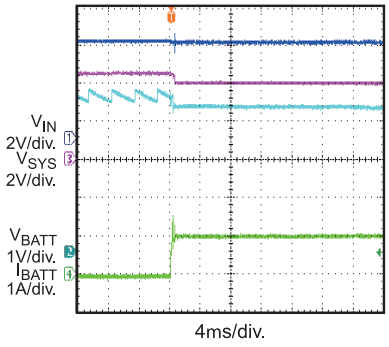
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = Full Range, Default Mode, I_{IN} Limit=2A, V_{SYS}=4.4V, R6 and R7 are float, I_{CHG}=2A, L = 1.2 µH, T_A = +25ºC, unless otherwise noted.

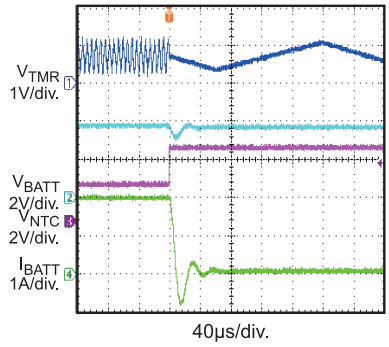
Battery Insertion
V_{BATT} = 3.7V, I_{SYS} = 0A



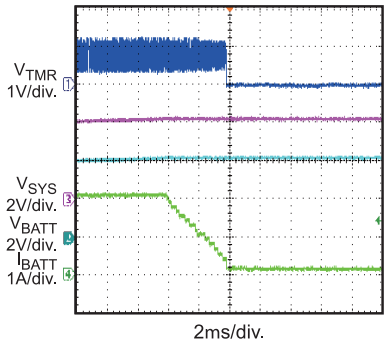
Battery Insertion
USB 3.0 Mode, V_{BATT} = 3.7V, I_{SYS} = 0A



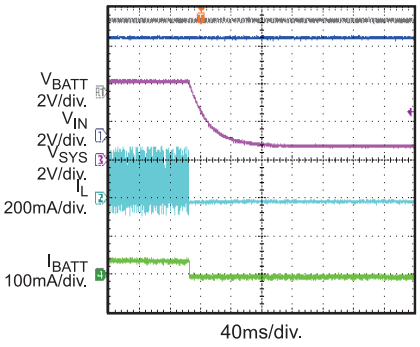
Time Suspend @ NTC Fault
V_{BATT} = 3.8V, I_{SYS} = 0A, C_{TMR} = 150pF



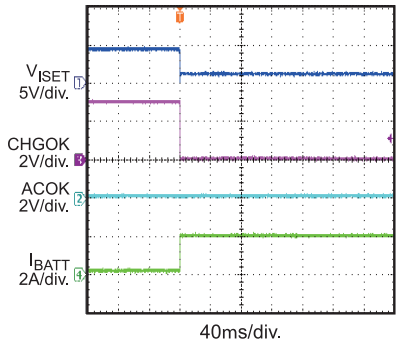
Timer Refreshed @ Battery Full
V_{BATT} = 4.2V, I_{SYS} = 0A, C_{TMR} = 150pF



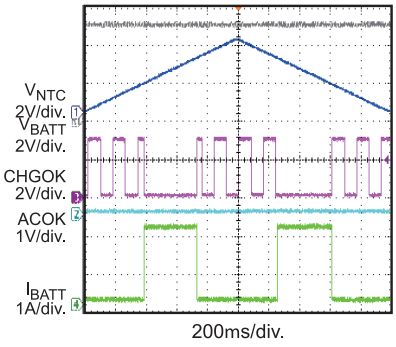
Thermal Shutdown
V_{BATT} = 3.7V, I_{SYS} = 0A
Increase the Ambier Temperature slowly



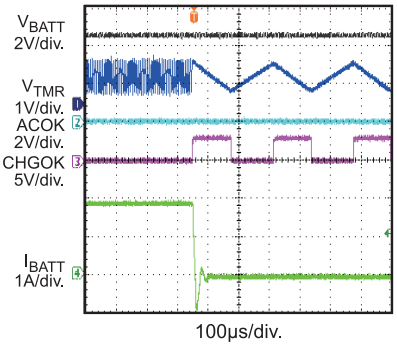
Indication @ Charge On/Off
V_{BATT} = 3.7V, I_{SYS} = 0A



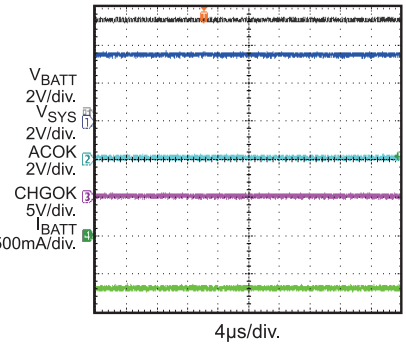
Indication @ NTC Fault
V_{BATT} = 3.7V, I_{SYS} = 0A



Indication @ Timer Out
V_{BATT} = 3.7V, I_{SYS} = 0A



Indication @ Supplement
V_{BATT} = 3.7V, I_{SYS} = 0A



OPERATION

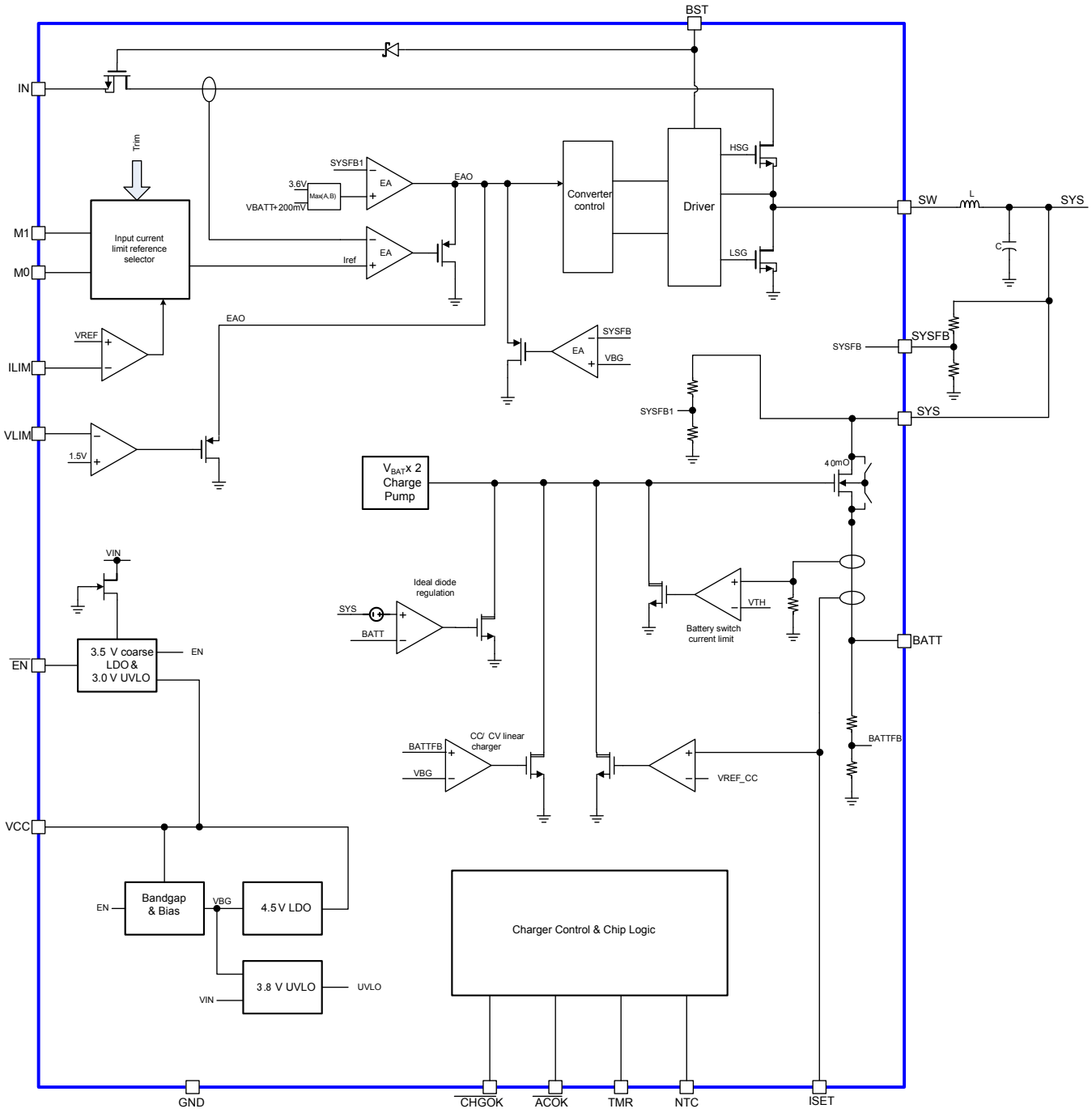


Figure 1: Function Block Diagram

Introduction

The MP2625B is a switching charger IC, with integrated smart power path management for powering the system and charging a single cell battery simultaneously and independently.

The MP2625B includes a high-voltage (up to 10V) input DC-DC step down converter for wide range of DC sources and USB inputs. It has precision average input current limit to make maximum use of the allowable input power. This feature allows fast charging when powering from an USB port, and ensures the input current never exceeds the input power specification especially when the input power comes from a USB port. Additionally, the input current limit threshold can be programmed by logic inputs or a resistor to ground from the ILIM pin.

The MP2625B implements an on-chip 40mΩ MOSFET which works as a full-featured linear charger with trickle charge, high accuracy constant current and constant voltage charge, charge termination, auto recharge, NTC monitor, built-in timer control, charge status indication, and thermal protection. The charge current can be programmed by an external resistor connected from the ISET pin to AGND. The IC limits the charge current when the die temperature exceeds 120°C.

The 40mΩ MOSFET works as an ideal diode to connecting the battery to the system load when the input power is not enough to power the system load. When the input is removed, the 40mΩ MOSFET is turned on allowing the battery to power up the system.

With smart power path management, the system load is satisfied in priority then the remaining current is used to charge the battery. The MP2625B will reduce charging current or even use power from the battery to satisfy the system load when its demand is over the input power capacity.

Figure 1 shows the function block diagram of MP2625B.

DC-DC Step Down Converter

The DC-DC converter is a 1.6MHz step-down switching regulator to provide the input power to the SYS, which drives the combination of the system load and battery charger. The regulator contains input current measurement and control scheme to ensure the average input current remains below the level programmed via ILIM pin or logic inputs M0&M1. This meets the adapter capacity limit or stays in compliance with USB specification.

When the input voltage is higher than UVLO and 280mV higher than the battery voltage, input voltage OK signal is active ($\overline{ACOK}$ turns low) and the DC-DC converter soft-starts. If the input power is sufficient to supply the combination of the system load and battery charger, and the input current limit loop is not triggered. The converter output voltage V_{SYS} will be regulated:

1) If BATT>3.4V, V_{SYS} is approximately 0.2V above the battery voltage to minimize the power loss of the battery charger during fast charging.

2) If BATT<3.4V, V_{SYS} is fixed at 3.6V to power the system immediately even when a drained battery is inserted to be charged. Figure 2 shows the relationship of V_{SYS} vs. V_{BATT}.

System voltage can also be regulated to any value between 4.08V to 4.4V by using a resistor divider on the SYSFB pin. This is shown as R6 and R7 in Figure 10. If the SYSFB is left floating, the system program is invalid, and V_{SYS} is regulated as Figure 2.

The converter adopts fixed off-time control to extend the duty cycle (close to 100%) when the input of the converter is close to V_{SYS}.

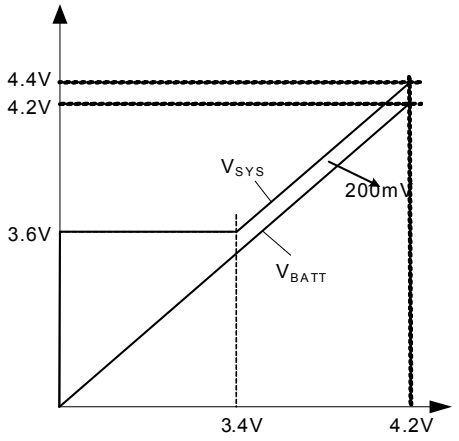


Figure 2: SYS Regulation Output

Close to 100% duty operation, BST refresh operation makes sure the driver voltage of the HS will be charged by turning on the LS until negative IL hit to a threshold. If the input power is insufficient to supply the combination of the system load and battery charger, the DC-DC converter will limit the total power requirement by restricting the input voltage, input current and the peak current through the MOSFET. The power path management will reduce the charge current to satisfy the external system load in priority. According to this feature, the USB specification is always satisfied first. Even if the charge current is set larger than the USB input current limit, the real charge current will be reduced as needed.

Input Limit State

If the input power is insufficient to supply the combination of the system load and battery charger, the MP2625B implements three input limit control loops to reduce the charge current and satisfy the external system load in priority. The input in this case might be limited as follows: input current limit, input voltage limit and DC-DC peak current limit.

Input Current Limit: When the input current is higher than the programmed input current limit the input current limit loop takes the control of the converter and regulates the input current at constant value. When the battery voltage is over 3.4V, the output voltage (V_{SYS}) will drop down according to the increase of the system current, and the charge current drops down after the BATT-to-SYS switch (40mΩ MOSFET) is fully on according to V_{SYS} dropping down. During this process, the system voltage is slightly higher than V_{BATT}. When the battery voltage is lower than 3.4V, to maintain the minimum system voltage and ensure the system operation, the input current limit control will pull down the charge current directly to reduce the load of the converter so that the system current is satisfied in priority.

Input Voltage Limit: A resistor divider from IN pin to VLIM pin to AGND is used for the input voltage limit control. When the voltage on VLIM pin hits the reference voltage of 1.52V, the output of the input voltage limit error amplifier will drop in to control the operation duty. In this mode, the input voltage will be clamped according to the value set by the resistor divider. The control to the system voltage and charge current is the same as the one explained in the input current limit. Charge current drops down to satisfy the system current request first. This feature provides a second protection to the input power and ensures the safe operation of the input adapter. Even if a wrong adapter is inserted, the MP2625B can continue operation, providing the maximum power to its load. User can program the input voltage limit value through the resistor divider from IN to VLIM to AGND.

Peak Current Limit: The peak current of the high side switch of the DC-DC converter is sensed during every cycle, it is compared to the reference 4A, if the peak current hits the threshold, the peak current limit mode is triggered. The control of the charge current is the same with the above two limits.

Input Current Limit Setting

The current at ILIM is a precise fraction of the adapter input current. When a programming resistor is connected from ILIM to AGND, the voltage on ILIM represents the average input current of the PWM converter. And the input current approaches the programmed limit, ILIM voltage reaches 1.14V.

The average input current limit can be set through the resistor connecting from ILIM to AGND according to the following expression:

$$I_{IN\_LIM}=1.14\times\frac{40000}{R_{ILIM}(k\Omega)}(mA)$$

When USB input, the input current limit is set internally and the programmed value is invalid. The MP2625B provides typical of 450mA input current limit for USB2.0 specification and a typical of 825mA for USB3.0 specification respectively.

The user can choose to set the input current limit through the two logic pins M0 and M1 as shown in Table 2 according to its input specification.

When both M0 and M1 are float, they are pulled to the logic high, under this condition, the input current is limited to a default value of 2A.

Table 1: Input Current Limit Setting

M0	M1	Mode
Low	Low	USB2.0 Mode
Low	High	USB3.0 Mode
High	Low	Programmable Mode
High/Float	High/Float	Default Mode

Input Voltage Limit Setting

The input voltage can be limited at a value set by a resistor divider from IN pin to VLIM pin to AGND according to the following expression (Typical Application Circuit):

$$V_{IN\_LIM}=1.52\times\frac{R1+R2}{R2}(V)$$

When the voltage on VLIM pin drops and hits the reference voltage 1.52V, the input voltage will be clamped to the setting value.

Battery Charger

The MP2625B completes charge operation consist of trickle charge, automatic charge termination, charge status indication, timer control, NTC indication, automatic recharge, and thermal limiting.

When the PWM converter is out of soft start, the battery charge cycle begins, the MP2625B first determines if the battery is deeply discharged. If the battery voltage is lower than the trick charge threshold (typical 3.0V), the battery charger starts in “trickle charge mode”. The trickle charge current is limited to 10% of the programmed charge current until the battery voltage reaches 3.0V. If the charge stays in the “trickle charging mode” for longer than “trickle charge timer period”, the “timer out” condition is triggered, the charge is terminated and $\overline{CHGOK}$ will start blinking to indicate that the battery is unresponsive. When the battery voltage is above 3.0V, the charger is operating at “constant current mode.” The current delivered to the battery will try to reach the value programmed by the ISET pin. Depending on the available input power and system load conditions,
the battery charger may or may not be able to charge at the full programmed rate. The system load is always satisfied first over the battery charge current. If the system load requirement is low, the battery can be charged at full constant current.

When the battery voltage reaches the battery full threshold, the charger enters the “constant voltage mode” operation.

End of Charge (EOC) and Indication

In constant voltage charge mode, the battery voltage is regulated at 4.2V (when SYSFB is float or SYS is programmed higher than battery full threshold) and the charge current decreases naturally. Once the charge current hits the battery full threshold I_{BF} (1/10 programmed charge current), the battery is fully charged and charge cycle is terminated.

If the charge current drops below I_{BF} because of any limit condition, the MP2625B will come out of CV mode, and the charge full detection is invalid.

A safe timer starts at the beginning of each new charge cycle and it monitors if the whole charge period is within the programmed time limit. After each charge cycle, when the battery is indicated as full, the timer counter will be reset. If the time is expired while the charging is still on going, the timer will force the MP2625B to terminate charging $\overline{CHGOK}$ is blinking to indicate the fault condition.

If system voltage is programmed lower than 4.2V by the resistor divider at the SYSFB pin, the battery will be charged most close to V_{SYS} until the charge current reaches the I_{BF} threshold.

Automatic Recharge

Once the battery charge cycle is completed, the MP2625B turns off indicating the battery full status. During this process, the battery power may be consumed by the system load or self discharge. If the input power is always on, to ensure the battery not to be exhausted, the new charge cycle will automatically begin when the battery voltage falls below the auto-recharge threshold V_{RCHG} which is typically 4V when the SYSFB is float, and 50mV lower if the SYSFB is connected to a resistor divider. The timer will re-start when the auto-recharge cycle begins.

During the charge off state when the battery is fully charged, if the input power is recycled, or the EN signal is refreshed, the charge cycle will re-start and the timer will refresh even if the

battery voltage is above the auto-recharge threshold.

Charge Current Setting

The charge current of the MP2625B is programmed using a single resistor from ISET pin to ground. The program resistor and charge current are calculated using the following equations:

$$I_{CHG} = 1.15 \times \frac{1800}{R_{SET}(k\Omega)}(mA)$$

At either constant current mode or constant voltage mode, the voltage at the ISET pin is proportional to the actual charge current

delivered to the battery, I_{BATT}. The charge current can be calculated by monitoring the ISET pin voltage with the following formula:

$$I_{BATT} = \frac{V_{ISET}}{1.15} \times I_{CHG}$$

Additionally, the actual battery charge current may be lower than the programmed current due to limited input power available and prioritization of the system load.

Battery charge full current threshold I_{BF} is set internally at 10% of the programmed charge current. However, I_{BF} has a 150mA maximum limit which can not be exceeded.

Ideal Diode Mode

If the system current requirement increases over the preset limit of the PWM converter, the additional current will be drawn from the battery via the BATT-to-SYS switch. To avoid very large currents being drawn from the battery which might affect the reliability of the device, the MP2625B controls the charge switch to work at the ideal diode mode regulating V_{SYS} to V_{BATT}-65mV when V_{SYS} is 40mV lower than V_{BATT} is detected. Only when V_{SYS} is 40mV higher than V_{BATT}, the charger switch exits the ideal diode mode, and the charge cycle softly restarts.

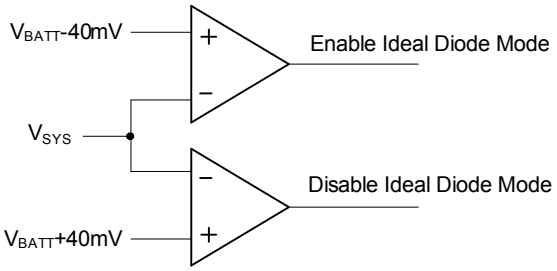


Figure 3: Ideal Diode Mode Enable/Disable

Logic Control

The MP2625B has two separate enable control pins.

$\overline{EN}$ is a logic control pin that controls the operation of the whole IC. When $\overline{EN}$ is low, the IC is enabled and the PWM converter output powers the system and the charger. When $\overline{EN}$ is high, both the PWM converter and the charger are disabled. The BATT to SYS switch turns fully on to connect the battery to power the system.

The ISET pin can be also used to control the operation of the charger. Setting ISET pin floating will disable the charger function while the output of PWM converter will continue supply power to system. On the other hand, a resistor from ISET to AGND will enable the charging at the programmed charge current.

The logic control of the ISET pin of the MP2625B can be realized as Figure 3. In this way, the user can choose logic low to be “off” signal or logic high to be ”on” signal with a N-MOSFET.

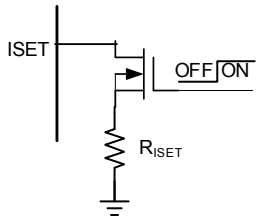


Figure 4: ISET Logic Control

Input Power Status Indication ($\overline{ACOK}$)

An internal under voltage lockout circuit monitors the input voltage and keeps the IC in off state until the input rises over the rising threshold (3.8V). When the input voltage decreases below threshold (3.5V), the IC will turn off, and the system load will be powered by the battery

automatically. $\overline{ACOK}$ is an open-drain, active-low output that indicates the status of input power. The input is considered valid when the input voltage is over the UVLO rising threshold, and 280mV higher than the battery voltage to ensure both the converter and the charger can operate normally. If the input voltage from an adapter or from a USB port is indicated OK, $\overline{ACOK}$ will turn low.

During $\overline{EN}$ off or thermal shutdown conditions, the $\overline{ACOK}$ turns high to indicate no power is provided by the input to the system. The $\overline{ACOK}$ signal indicates if input supplies power to the system load or not. Any other condition can not affect the $\overline{ACOK}$ indication as long as the input power is present.

Charge Status Indication ($\overline{CHGOK}$)

$\overline{CHGOK}$ is an open-drain, active-low output that indicates the status of charge. $\overline{CHGOK}$ will be low during normal charging operation, turn high after charge full, and blink if a fault condition happens including NTC fault (battery temperature invalid) and timer out (bad battery).

In the event of a fault condition, $\overline{CHGOK}$ switches at 6Hz with the 50% duty cycle and enter “blinking” mode. The user should check the application circuit to find out the root cause of the fault condition if the “blinking” signal is asserted.

For no battery condition, $\overline{CHGOK}$ is blinking according to the transition between charging and charge full. The blinking frequency is determined by the cycle of charge and discharge of the output capacitor.
When the charge current to the battery is low or in the event the battery is in supplement mode caused by the insufficient input power, $\overline{CHGOK}$ keeps low to avoid providing false charge full indication.

Table 2 shows the $\overline{ACOK}$ and $\overline{CHGOK}$ status under different charge conditions.

Table 2: Charger Status Indication

$\overline{ACOK}$	$\overline{CHGOK}$	**Charger Status**
low	low	In charging, supplement mode
low	high	End of charge, ISET disable charger only.
low	blinking at 6Hz	NTC fault, timer out
high	high	V_{IN} absent, $\overline{EN}$ disable, thermal shutdown

Timer Setting

The MP2625B uses an internal timer to terminate charge if the timer times out. The timer duration is programmed by an external capacitor at the TMR pin and related to the real charge current.

The trickle mode charge time is:

$$t_{Trickle\_TMR} = 45 \times \frac{C_{TMR}}{0.1\mu F} (min)\ (I_{CHG} = 1A)$$

The total charge time is:

$$t_{Total\_TMR} = 6.5 \times \frac{C_{TMR}}{0.1\mu F} (hr)\ (I_{CHG} = 1A)$$

The above equations are based on 1A charge current. As a result of power path management control, charge current might vary during normal operation, under this condition, the MP2625B automatically takes into account this variation and adjust the timer period accordingly.

When the charge current is set larger than 1A, the safe timer period is reduced accordingly with the same TMR capacitor. If the charge current is reduced because of insufficient input power, the timer period is increased proportionally by the same rate at which the charge current is reduced. If charge is stopped due to high system load, the timer is temporarily suspended.

This feature avoids indicating a false trigger indication for bad battery indication when there is little charge current delivered to the battery as a result of the insufficient input power.

When the timer out condition occurs, the MP2625B terminates the charge at once and $\overline{CHGOK}$ blinks to indicate the fault status. If one of the following events happens, the timer is refreshed and MP2625B re-starts the charge cycle.

- Input re-startup
- Refresh $\overline{EN}$ /ISET signal
- Auto-Recharge

NTC Thermistor

The NTC pin allows MP2625B to sense the battery temperature using the Negative Thermal Coefficient (NTC) thermistor usually available in the battery pack to ensure safe operating environment of the battery. A resistor with appropriate value should be connected from VCC to NTC and the NTC resistor is from NTC pin to AGND. The voltage on NTC pin is determined by the resistor divider whose divide ratio as the different resistance of the NTC thermistor depends on the ambient temperature of the battery.

The MP2625B has an internal NTC voltage comparator to set the upper and lower limit of the divide ratio. If NTC pin voltage falls out of this range it means the temperature is outside the safe operating range,

As a result, The MP2625B will stop charging and report it on indication pins. Charging will automatically resume after the temperature falls back into the safe range.

Thermal Protection

The MP2625B implements thermal protection to prevent the thermal damage to the IC or surrounding components. An internal thermal sense and feedback loop will automatically decrease the charge current when the die-temperature rises to about 120°C. This function is referred as charge current thermal fold-back. This feature protects the MP2625B from excessive temperature due to high power operation or high ambient thermal conditions. Another benefit of this feature is charge current can be set according to the requirement rather than worst-case conditions for a given application with the assurance of safe operation. The MP2625B will stop charging if the junction temperature rises above 150°C as the IC enters thermal shutdown protection.

Battery Discharge Protection

When the input power is removed or invalid, the system load will draw power from the battery via the battery switch. Under this condition, the battery switch is fully on to minimize the power loss. The MP2625B integrates battery discharge protection. If the battery discharge current is larger than the discharge current limit threshold I_{DIS} (5A), the current will be regulated at the preset limited value. And if the current increases further, the SYS voltage starts to decrease. When V_{SYS} drops to about 800mV lower than V_{BATT}, SYS short condition is detected. Under this condition, the discharge current is limited at 230mA. In the event of a short from system to GND the discharge current from the battery to the system is also limited to 230mA.

Furthermore, battery voltage UVLO is always monitored. If the battery voltage is lower than the battery UVLO threshold, the battery switch is turned off immediately. This feature makes sure the battery from over-discharged.

Dynamic Power Path Management (DPPM)

In the presence of a valid input source, the PWM converter will supply the current to both the system and the battery charger.
The voltage V_{SYS} is regulated based on the value of the battery voltage. When V_{BATT} is higher than 3.4V, V_{SYS} is regulated 200mv above V_{BATT} to charge the battery. When V_{BATT} is lower than 3.4V, to ensure the system can still be powered up even with a drained battery connected, V_{SYS} is regulated at constant 3.6V.

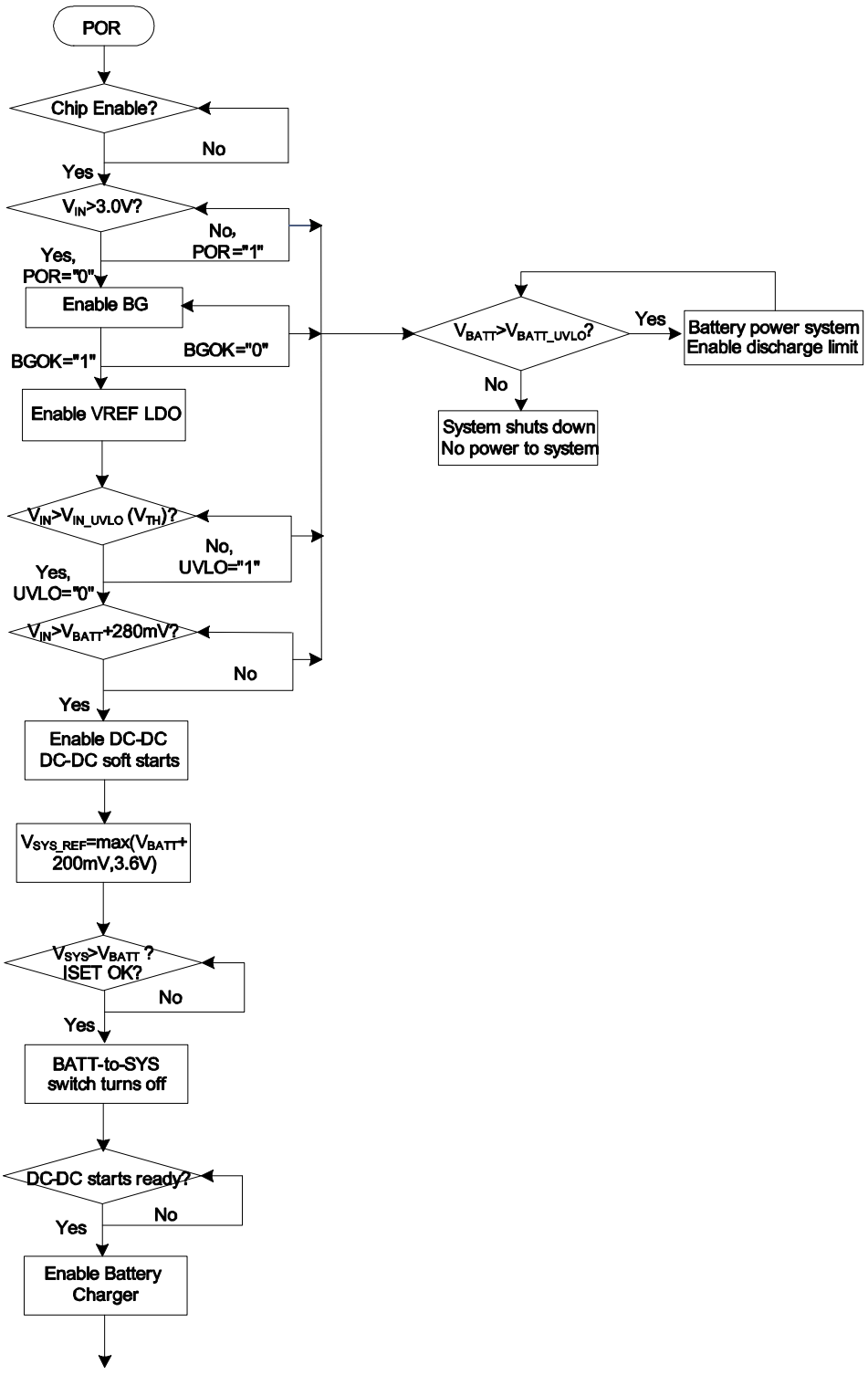
When the input source is overloaded, either the current exceeds the input current limit or the voltage falls below the input voltage limit, the MP2625B then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit. If the system current increases beyond the power allowed by the input source, additional power will be drawn from the battery via an on-chip 40mΩ MOSFET working as an ideal diode.

Additionally, if the input source is removed, the MP2625B will turn on the 40mΩ MOSFET allowing the battery to power the system load to keep the operation of the portable device.

Operation Flow Chart

Figure 5 shows the operation flow chart of the MP2625B.

Figure 6 shows the operation process.



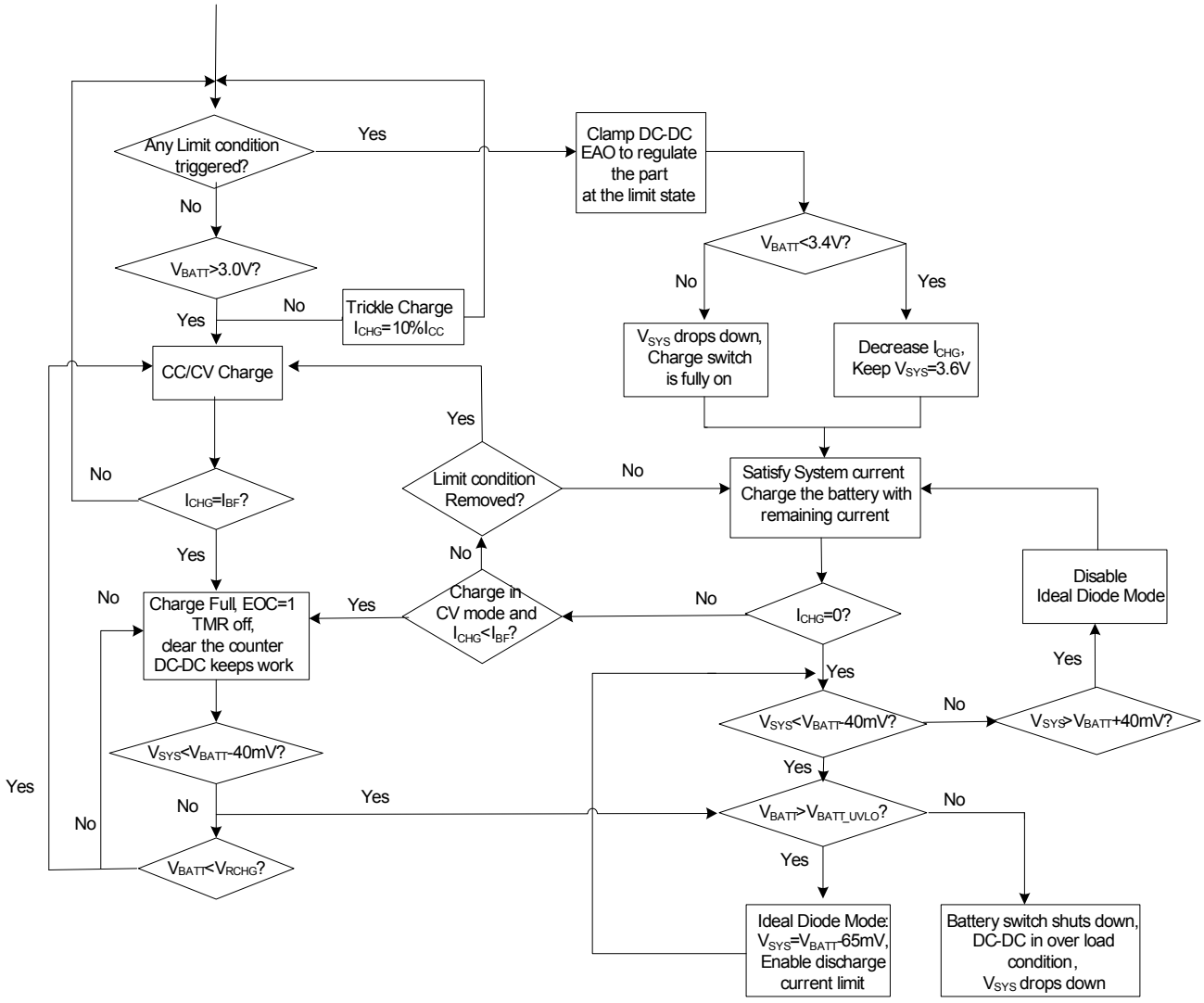


Figure 5: MP2625B Operation Flow Chart under No Fault Condition

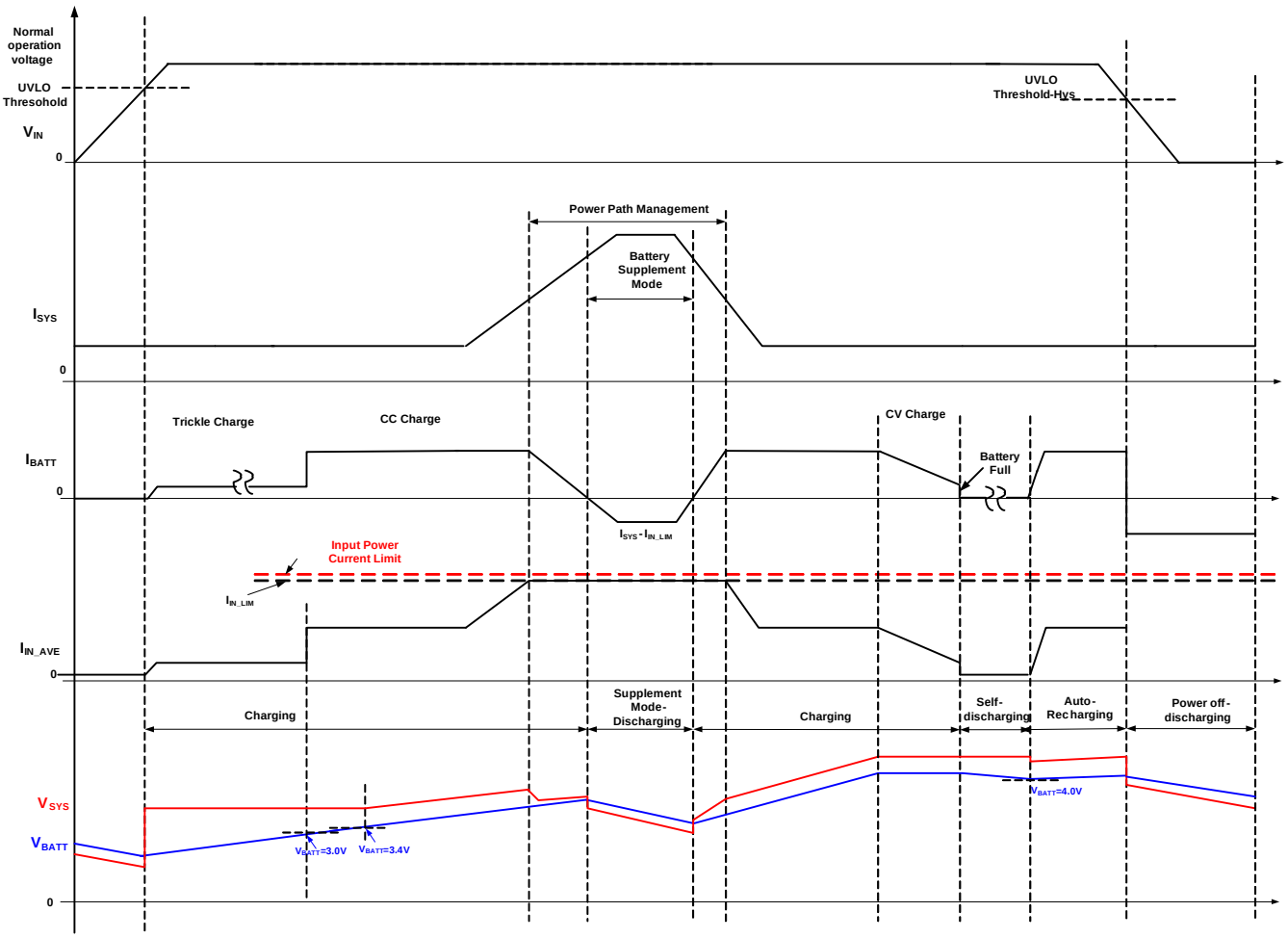


Figure 6: MP2625B Operation Process under No Fault Condition

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Input Current Limit

First the input current limit can be set by the M0 and M1 pins refer to the Table 1, the exact current value in minimum, typical and maximum is listed in the EC table.

Under program mode, connect a resistor from the ILIM pin to AGND to program the input current limit for different input ports. The relationship between the input current limit and setting resistor is as Equation (1) which is shown in following again:

$$I_{IN\_LIM}=1.14\times\frac{40000}{R_{ILIM}(k\Omega)}(mA) \quad (1)$$

For MP2625B, the R_{ILIM} is greater than 22.8k, so that I_{ILIM} is not over 2A.

The tolerance is ±8% of the input current limit setting.

So for a required minimum input current limit value, just calculate its typical value first, then calculate the setting resistor based on Equation (1). Also the maximum value can be calculated according to the tolerance. 1% accuracy resistor is used for this setting. Also, for a given resistor of R_{ILIM}, the input current limit can be calculated. Following table is an example:

Table 3: Example of R_{ILIM} setting

Resistor	R_{ILIM} (kΩ)	I_{IN_LIM} (mA)	8%	-8%
Typ.	54.9	830.601	897.049	764.153
Min.	54.351	838.991	906.11	771.872
Max.	55.449	822.377	888.168	756.587

Therefore, if customer selected a 54.9k in 1% accuracy resistor for the input current limit setting, then the typical input current limit value is 830.6mA, the minimum is 756.6mA and the maximum is 906mA.

Setting the Charge Current

R_{ISET} connecting from the ISET pin to AGND sets the charge current (I_{CHG}). The relationship between the charge current and setting resistor is as Equation (2) which is shown in following again:

$$I_{CHG}=1.15\times\frac{1800}{R_{SET}(k\Omega)}(mA) \quad (2)$$

For example, if the typical I_{CHG} is designed as 2A, then the R_{SET} is calculated at 1.05kΩ. The tolerance of the I_{CHG} setting is ±10%. If the minimum or maximum charge current is required, first the typical value should be calculated according to the tolerance. After that, calculate the resistor according to formula (2). 1% accuracy resistor is used for this setting.

For a given setting resistor, the charge current can be calculated by the same way did in the input current limit setting. Usually in USB mode, the charge current is always set over the USB input limit specification. Then the MP2625 regulates the input current constant at the limitation value. Thus the real CC charge current is not the setting value, it varies with different input and battery voltages.

The maximum CC charge value can be calculated as:

$$I_{CC\_MAX}=\frac{V_{IN}\times I_{ILIM}\times\eta}{V_{TC}}(A) \quad (3)$$

Where V_{TC} is trickle charge threshold (3V) and η is the current charge efficiency. Assume V_{IN}=5.5V, I_{ILIM}=1A, suppose η=83%, thus I_{CC_MAX}=1.52A.

Figure 7 shows a calculating charge current curve by limiting the input current limit.

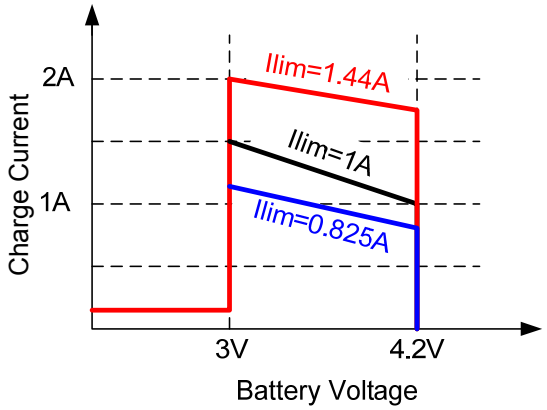


Figure 7: I_{CHG} Variation with Different Input Current Limit

Setting the Input Voltage Limit

The input clamp voltage is set using a resistive voltage divider from the input voltage to VLIM pin. The voltage divider divides the input voltage down to the limit voltage by the ratio:

$$V_{VLIM} = V_{IN\_LIM} \times \frac{R2}{R1+R2}(V) \quad (4)$$

Thus the input voltage is:

$$V_{IN\_LIM} = V_{VLIM} \times \frac{R1+R2}{R2}(V) \quad (5)$$

The voltage clamp reference voltage V_{VLIM} is 1.52V, and a typical value for R2 can be 10kΩ. With this value, R1 can be determined by:

$$R1 = R2 \times \frac{V_{IN\_LIM} - V_{VLIM}}{V_{VLIM}}(V) \quad (6)$$

For example, for a 4.65V input limit voltage, R2 is 10kΩ, and R1 is 20.6kΩ.

The minimum value and the maximum value of the input voltage limit can be calculated according to the accuracy of the resistor and the tolerance of V_{VLIM}. 1% accuracy resistors are used for R1 and R2.

Setting the System Voltage

The system voltage can be regulated to any value between 4.08V to 4.4V by the resistor divider on SYSFB pin as R6 and R7 in Figure 10.

$$V_{SYS} = V_{SYS\_REF} \times \frac{R6+R7}{R7} \quad (7)$$

Where V_{SYS_REF} is 1.152V, the reference voltage of SYS. With a typical value for R7, 10kΩ, R6 can be determined by:

$$R6 = R7 \times \frac{V_{SYS} - V_{SYS\_REF}}{V_{SYS\_REF}}(V) \quad (8)$$

For example, for a 4.2V system voltage, R7 is 10kΩ, and R6 is 26.5kΩ. 1% resistors are selected for the R5 and R6.

Be noted that, the minimum V_{SYS} is limited to be higher than the maximum value of the auto-recharge threshold which is 4.05V.

Selecting the Inductor

Inductor selection trades off among cost, size, and efficiency. A lower inductance value corresponds to a smaller size, but results in higher ripple currents, higher magnetic hysteretic losses, and higher output capacitances. From a practical standpoint, the inductor ripple current does not exceed 30% of the maximum load current under worst cases conditions. For example, if the I_{CHG} is setting to 2A in MP2625B, then, ΔI_L is general set at 0.6A.

However, for the light load condition, the inductor ripple current will be very small which may cause unstable operation due to the peak current mode control of the IC. For stable operation, the experienced minimum limit value for inductor current ripple is 0.5A. Therefore, the inductor current ripple is the maximum one of 30% times I_{CHG} and 0.5A.

And the inductance can be calculated according to Equation (9):

$$L = \frac{V_{IN} - V_{SYS}}{\Delta I_{L\_MAX}} \frac{V_{SYS}}{V_{IN} \times f_S(MHz)}(\mu H) \quad (9)$$

The peak current of the inductor is calculated as Equation (10):

$$I_{PEAK} = I_{LOAD(MAX)} \times (1 + \frac{\%ripple}{2})(mA) \quad (10)$$

Where V_{IN}, V_{SYS}, and f_S are the typical input voltage, the output voltage, and the switching frequency, respectively.

Following Table 4 provides the selection guide of the inductance based on different input voltage.

Table 4: Inductance Selection Guide under different Input Voltage

SPEC	Inductance Selection						
V_{IN}	$L = \frac{V_{IN} - V_{SYS}}{\Delta I_L} \frac{V_{SYS}}{V_{IN} \times f_S(MHz)}$	L_{MIN} (uH)	L_{MAX} (uH)	L (uH)	Saturation Current (A)(6)	DCR (mΩ)	Package
5V		0.55	1.25	1.0	>2.8	<50	Application Required
9V	ΔI_L=max (0.3*I_{CHG},0.5A) ΔI_{LMIN}=0.5A ΔI_{LMAX}=0.6A	2.25	2.8	2.2(5)	>2.8	<50	Application Required

NOTE:

5) Choose the inductor with a value a little lower than the calculated LMIN, makes the ΔI_L increased a little, but the 2.2uH is more regular in the application which will have a lower cost.

6) Saturation Current of the inductor should be higher than the IPEAK, add 0.5A margin here.

Selecting the Input Capacitor

The input capacitor C1 from the typical application circuit absorbs the maximum ripple current from the PWM converter, which is given by

$$I_{RMS\_MAX} = I_{CC\_MAX} \times \frac{\sqrt{V_{TC} \times (V_{IN\_MAX} - V_{TC})}}{V_{IN\_MAX}} (A) \quad (11)$$

For I_{CC_MAX}=2A, V_{TC}=3V, V_{IN_MAX}=10V, the maximum ripple current is 1A. Select the input capacitors so that the temperature rise due to the ripple current does not exceed 10°C. Use ceramic capacitors with X5R or X7R dielectrics because of their low ESR and small temperature coefficients.

For most applications, use a 10μF capacitor. Besides, usually a small cap with at least 1uF (C1) from IN to GND is required to be put as much close as possible to the IC. For the input voltage is high to 10V, consider the spike when input insert, select the input capacitors (both the 22uF and 1uF) in 25V rating.

Selecting the Output Capacitor

The output capacitor C_{SYS} from the typical application circuit is in parallel with the SYS load. C_{SYS} absorbs the high-frequency switching ripple current and smoothes the output voltage. Its impedance must be much less than that of the system load to ensure it properly absorbs the ripple current.

Use a ceramic capacitor because it has lower ESR and smaller size that allows us to ignore the ESR of the output capacitor. Thus, the output voltage ripple is given by:

$$\Delta r = \frac{\Delta V_{SYS}}{V_{SYS}} = \frac{1 - \frac{V_{SYS}}{V_{IN}}}{8 \times C_{SYS} \times f_S^2 \times L} \% \quad (12)$$

In order to guarantee the ±0.5% system voltage accuracy, the maximum output voltage ripple must not exceed 0.5% (e.g. 0.1%). The maximum output voltage ripple occurs at the minimum system voltage and the maximum input voltage.

The output capacitor can be calculated with Equation (13):

$$C_{SYS} = \frac{1 - \frac{V_{SYS\_MIN}}{V_{IN}}}{8 \times f_S^2 \times L \times \Delta r} \quad (13)$$

When SYSFB pin is floating, output voltage ripple is the main concern to select the output capacitor (C_{SYS}), refer to Table 5 for detail selection guide about the SYS capacitance selection under typical inputs.

Table 5: SYS Capacitance Selection Guide

SPEC	SYS Capacitance (C_{SYS}) Selection				
V_{IN}	$C_{SYS} = \frac{1 - \frac{V_{SYS}}{V_{IN}}}{8 \times f_S^2 \times L \times \Delta r}$	C_{SYS_MIN} (uF) [7] When SYSFB is Floating	C_{SYS_MIN} (uF) [7] When SYSFB is Programmed	Temperature Characteristic	Package
5V	Δr=0.1% L=1uH @V_{IN}=5V L=2.2uH @V_{IN}=9V	13.6	20	X5R;X7R	Application Required
9V		13.3	20	X5R;X7R	Application Required

NOTE:

7) For different voltage rating, capacitance will have different DC bias characteristic. Suppose a general condition, capacitance drops 40% under V_{SYS}=4.4V under 10V rating, and 50% at 6.3V rating.

When SYSFB is programmed using external resistors, the control loop function is changed. A zero point is added around the cross over frequency of the DC gain, and this may result in the phase margin varied a lot, which may cause the unstable operation. To avoid this condition, a minimum capacitance requirement should be satisfied to make the pole point to compensate the zero point. This minimum capacitance is 20uF for a general application.

So, for the SYSFB programmed condition, the C_{SYS} should be selected as max (C_{SYS_MIN}, 20uF), C_{SYS_MIN} is calculated from the formula of equation (13), as shown in Table 5. For better stability margin, select a 47uF ceramic capacitor with 6.3V and above voltage rating as the output capacitor in this case.

Resistor Choose for NTC Sensor

Figure 8 shows an internal resistor divider reference circuit to limit the low temperature threshold and high temperature threshold at 65%·VCC and 33.5%·VCC, respectively. For a given NTC thermistor, select appropriate R_{T1} and R_{T2} to set the NTC window:

$$\frac{R_{T2}//R_{NTC\_Cold}}{R_{T1}+R_{T2}//R_{NTC\_Cold}}=\frac{V_{THL}}{VCC}=65\% \quad (14)$$

$$\frac{R_{T2}//R_{NTC\_Hot}}{R_{T1}+R_{T2}//R_{NTC\_Hot}}=\frac{V_{THH}}{VCC}=33.5\% \quad (15)$$

R_{NTC_Hot} is the value of the NTC resistor at high temperature of the required temperature operation range, and R_{NTC_Cold} is the value of the NTC resistor at low temperature.

The two resistors, R_{T1} and R_{T2}, allow the high temperature limit and low temperature limit to be programmed independently. With this feature, the MP2625B can fit most type of NTC resistor and different temperature operation range requirements.

R_{T1} and R_{T2} values depend on the type of the NTC resistor:

$$R_{T2}=\frac{0.3\times R_{NTC\_Cold}\times R_{NTC\_Hot}}{0.1225\times R_{NTC\_Cold}-0.4225\times R_{NTC\_Hot}} \quad (16)$$

$$R_{T1}=\frac{0.3\times R_{NTC\_Hot}\times R_{NTC\_Cold}}{0.2275\times (R_{NTC\_Cold}-R_{NTC\_Hot})} \quad (17)$$

For example, for the thermistor NCP18XH103, it has the following electrical characteristic:

At 0°C, R_{NTC_Cold} = 27.445kΩ;

At 50°C, R_{NTC_Hot} = 4.1601kΩ.

The following equations are derived assuming that the NTC window is between 0°C and 50°C. According to the above equations to calculate R_{T1}=7.15kΩ and R_{T2}=25.5kΩ.

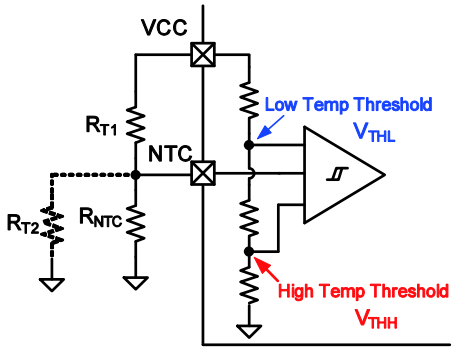


Figure 8: NTC Function Block

PCB Layout Guideline

It is important to pay special attention to the PCB layout to meet specified noise, efficiency and stability requirements. The following design considerations can improve circuit performance:

1) Route the power stage adjacent to their grounds. Aim to minimize the high-side switching node (SW, inductor), trace lengths in the high-current paths and the current sense resistor trace.

Keep the switching node short and away from all small control signals, especially the feedback network.

Place the input capacitor as close as possible to the IN and PGND pins.

Place the output inductor close to the IC and connect the output capacitor between the inductor and PGND of the IC.

2) For high-current applications, the balls for the power pads (IN, SW, SYS, BATT and PGND) should be connected to as much copper in the board as possible. This improves thermal performance because the board conducts heat away from the IC.

3) The PCB should have a ground plane connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, one via

per capacitor for small-signal components). It is also recommended to put vias inside the PGND pads for the IC, if possible. A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With this small layout and a single ground plane, there is no ground-bounce issue, and having the components segregated minimizes coupling between signals.

TYPICAL APPLICATION CIRCUITS

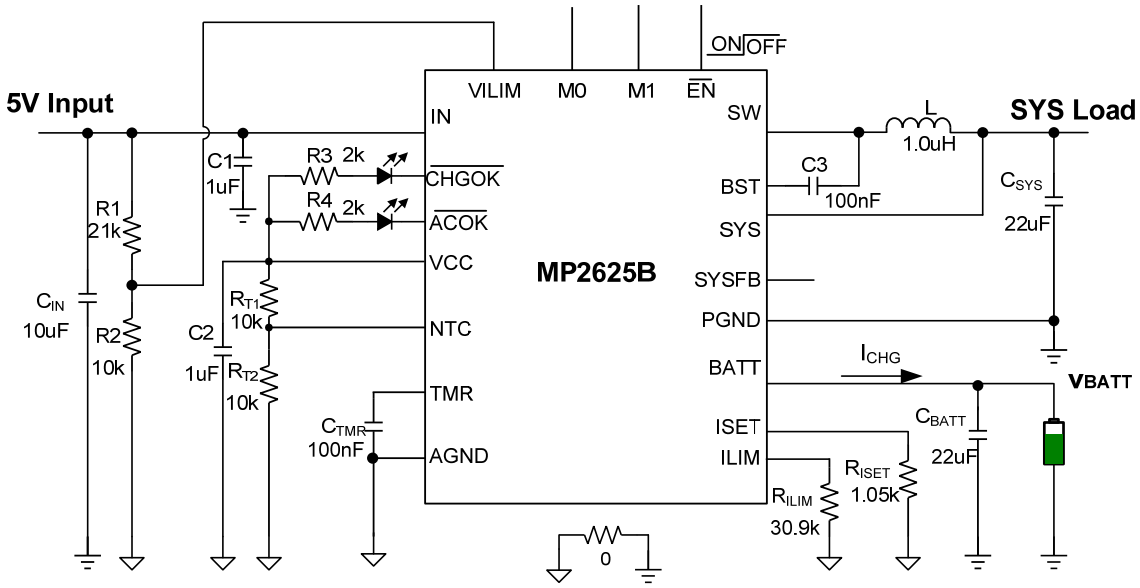


Figure 9: Typical Charge Application Circuit for 5V input with NTC Resistor Fixed

Table 6: The Key BOM of Figure 9.

Qty	Ref	Value	Description	Package	Manufacture
1	C_{IN}	10μF	Ceramic Capacitor;10V; X5R or X7R	1206	Any
1	C1	1μF	Ceramic Capacitor;10V; X5R or X7R	0603	Any
1	C2	1uF	Ceramic Capacitor;6.3V; X5R or X7R	0603	Any
1	C3	100nF	Ceramic Capacitor;16V; X5R or X7R	0603	Any
1	C_{TMR}	100nF	Ceramic Capacitor;6.3V; X5R or X7R	0603	Any
2	C_{SYS},C_{BATT}	22uF	Ceramic Capacitor;10V; X5R or X7R	1206	Any
2	R_{T1},R_{T2}	10k	Film Resistor;1%	0603	Any
1	L1	1.0μH	Inductor;1.0uH;Low DCR;I_{SAT}>2.8A	SMD	Any

TYPICAL APPLICATION CIRCUITS

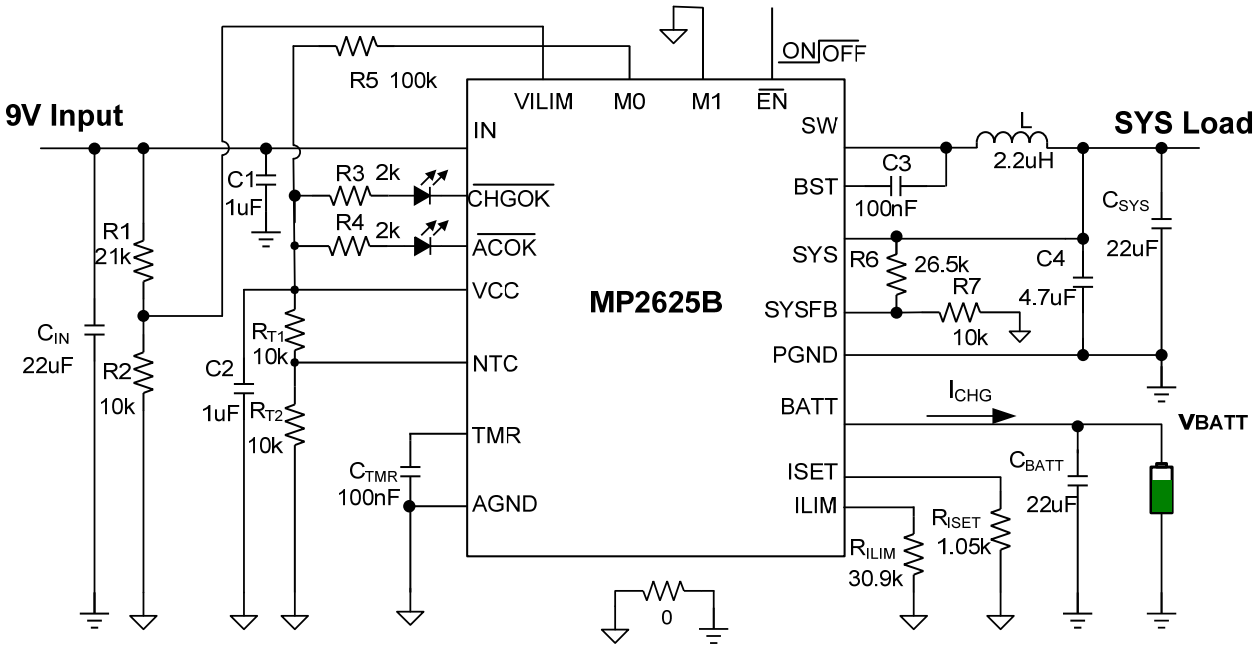


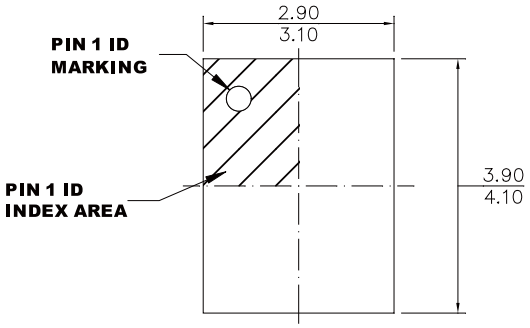
Figure 10: Typical Charge Application Circuit for 9V Input and 1.5A Input Current Limit

Table 7: The Key BOM of Figure 10.

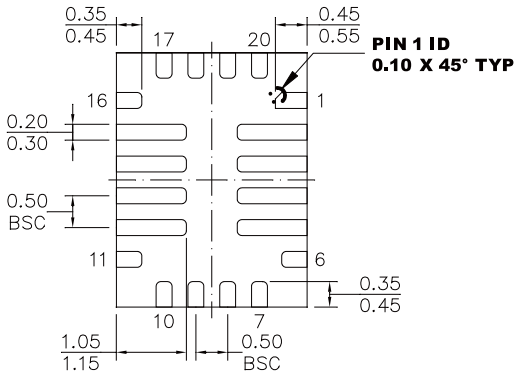
Qty	Ref	Value	Description	Package	Manufacture
1	C_{IN}	22μF	Ceramic Capacitor;16V; X5R or X7R	1206	Any
1	C1	1μF	Ceramic Capacitor;16V; X5R or X7R	0603	Any
1	C2	1uF	Ceramic Capacitor;6.3V; X5R or X7R	0603	Any
1	C3	100nF	Ceramic Capacitor;25V; X5R or X7R	0603	Any
1	C4	4.7uF	Ceramic Capacitor;10V; X5R or X7R	0603	Any
1	C_{TMR}	100nF	Ceramic Capacitor;6.3V; X5R or X7R	0603	Any
2	C_{SYS},C_{BATT}	22uF	Ceramic Capacitor;10V; X5R or X7R	1206	Any
1	R6	26.5k	Film Resistor;1%	0603	Any
3	R_{T1},R_{T2},R7	10k	Film Resistor;1%	0603	Any
1	L1	2.2μH	Inductor;2.2uH;Low DCR;I_{SAT}>6A	SMD	Any

PACKAGE INFORMATION

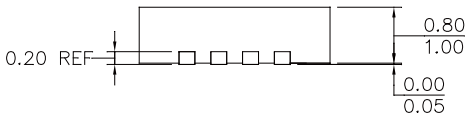
QFN-20 (3mmX4mm)



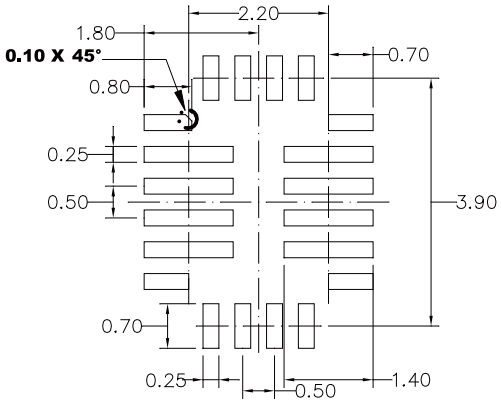
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE