



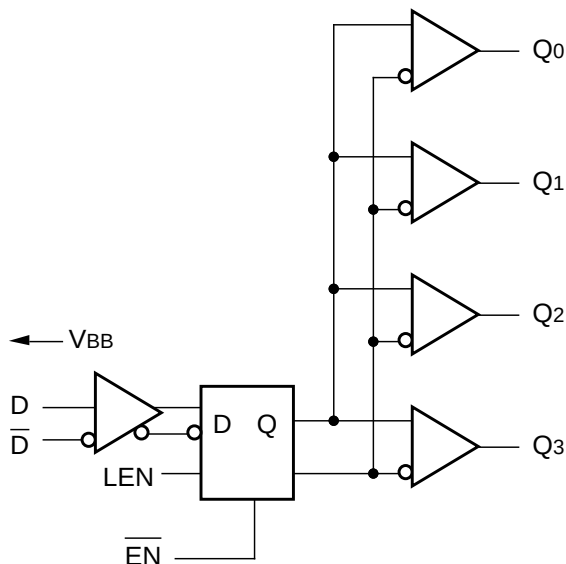
SINGLE SUPPLY QUAD PECL-TO-TTL W/LATCHED OUTPUT ENABLE

Precision Edge®
SY10H841
SY100H841

FEATURES

- Translates positive ECL to TTL (PECL-to-TTL)
- 300ps pin-to-pin skew
- 500ps part-to-part skew
- Differential internal design for increased noise immunity and stable threshold inputs
- V_{BB} reference output
- Single supply
- Enable input
- Latch enable input
- Extra TTL and ECL power/ground pins to reduce cross-talk/noise
- High drive capability: 24mA each output
- Fully compatible with industry standard 10K, 100K I/O levels
- Available in 16-pin SOIC package

BLOCK DIAGRAM



DESCRIPTION

The SY10/100H841 are single supply, low skew translating 1:4 clock drivers.

The devices feature a 24mA TTL output stage, with AC performance specified into a 50pF load capacitance.

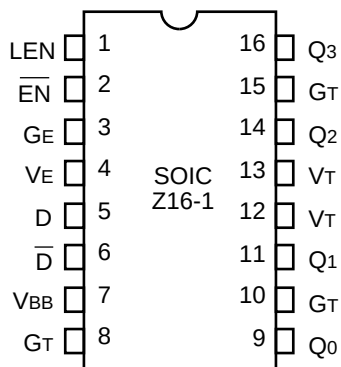
A latch is provided on-chip. When LEN is LOW (or left open, in which case it is pulled low by the internal pull-downs) the latch is transparent. A HIGH on the enable pin ($\overline{EN}$) forces all outputs LOW.

As frequencies increase to 40MHz and above, precise timing and shaping of clock signals becomes extremely important. The H841 solves several clock distribution problems such as minimizing skew (300ps), maximizing clock fanout (24mA drive), and precise duty cycle control through a proprietary differential internal design.

The 10K version is compatible with 10KH ECL logic levels. The 100K version is compatible with 100K levels.

PIN NAMES

Pin	Function
G _T	TTL Ground (0V)
V _T	TTL Vcc (+5.0V)
V _E	ECL Vcc (+5.0V)
G _E	ECL Ground (0V)
D, $\overline{D}$	Signal Input (PECL)
V _{BB}	V _{BB} Reference Output (PECL)
Q ₀ - Q ₃	Signal Outputs (TTL)
$\overline{EN}$	Enable Input (PECL)
LEN	Latch Enable Input

PACKAGE/ORDERING INFORMATION**16-Pin SOIC (Z16-1)****Ordering Information⁽¹⁾**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10H841ZC	Z16-1	Commercial	SY10H841ZC	Sn-Pb
SY10H841ZCTR ⁽²⁾	Z16-1	Commercial	SY10H841ZC	Sn-Pb
SY100H841ZC	Z16-1	Commercial	SY100H841ZC	Sn-Pb
SY100H841ZCTR ⁽²⁾	Z16-1	Commercial	SY100H841ZC	Sn-Pb
SY10H841ZH ⁽³⁾	Z16-1	Commercial	SY10H841ZH with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY10H841ZHTR ^(2, 3)	Z16-1	Commercial	SY10H841ZH with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100H841ZH ⁽³⁾	Z16-1	Commercial	SY100H841ZH with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100H841ZHTR ^(2, 3)	Z16-1	Commercial	SY100H841ZH with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

TRUTH TABLE

D	LEN	EN	Q
L	L	L	L
H	L	L	H
X	X	H	L
X	H	L	Latch

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit
V _E (ECL) V _T (TTL)	Power Supply Voltage	-0.5 to +7.0 -0.5 to +7.0	V
V _I (ECL) V _{OUT} (TTL)	Input Voltage	0.0 to V _{EE} 0.0 to V _T	V
T _{LEAD}	Lead Temperature Range (soldering, 20sec)	+260	°C
T _{store}	Storage Temperature	-65 to +150	°C
T _A	Operating Temperature	0 to +85	°C

NOTE:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN DESCRIPTION

Pin	Symbol	Description
1	LEN	Latch Enable Input
2	EN	Enable Input (PECL)
3	G _E	ECL Ground (0V)
4	V _E	ECL V _{CC} (+5.0V)
5	D	ECL Signal Input (Non-inverting)
6	D̄	ECL Signal Input (Inverting)
7	V _{BB}	V _{BB} Reference Output (PECL)
8	G _T	TTL Ground (0V)
9	Q ₀	Signal Output (TTL)
10	G _T	TTL Ground (0V)
11	Q ₁	Signal Output (TTL)
12	V _T	TTL V _{CC} (+5.0V)
13	V _T	TTL V _{CC} (+5.0V)
14	Q ₂	Signal Output (TTL)
15	G _T	TTL Ground (0V)
16	Q ₃	Signal Output (TTL)

VCC AND CLOAD

Ranges to meet duty cycle requirement: 0°C ≤ T_A ≤ 85°C. Output duty cycle measured relative to 1.5V.

Symbol	Parameter		Min.	Typ.	Max.	Unit	Condition
P _w	Ranges of V _{CC} and C _L to meet min. pulse width (HIGH or LOW) at f _{OUT} ≤ 40MHz	V _{CC} C _L P _w	4.75 10 11	5.0 — —	5.25 50 —	V pF ns	All Outputs
P _w	Ranges of V _{CC} and C _L to meet min. pulse width (HIGH or LOW) at f _{OUT} ≤ 50MHz	V _{CC} C _L P _w	4.875 15 9.0	5.0 — —	5.125 27 —	V pF ns	All Outputs

DC CHARACTERISTICS

V_T = V_E = 5.0V ± 5%

Symbol	Parameter		T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
I _{EE}	Power Supply Current	ECL	—	40	—	40	—	40	mA	V _E Pin
I _{CC} H	Power Supply Current	TTL	—	20	—	20	—	20	mA	Total all V _T pins
I _{CC} L			—	25	—	25	—	25		

TTL DC ELECTRICAL CHARACTERISTICS $V_T = V_E = +5.0V \pm 5\%$

Symbol	Parameter	T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
V _{OH}	Output HIGH Voltage	2.5 2.0	— —	2.5 2.0	— —	2.5 2.0	— —	V	I _{OH} = -3.0mA I _{OH} = -15mA
V _{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	I _{OL} = 24mA
I _{OS}	Output Short Circuit Current	-80	-200	-80	-200	-80	-200	mA	V _{OUT} = 0V

10H ECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾ $V_T = V_E = +5.0V \pm 5\%$

Symbol	Parameter	T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I _{IH}	Input HIGH Current	—	225	—	175	—	175	μA	—
I _{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	μA	—
V _{IH}	Input HIGH Voltage	3.830	4.160	3.870	4.190	3.940	4.280	V	V _E = 5.0V
V _{IL}	Input LOW Voltage	3.050	3.520	3.050	3.520	3.050	3.555	V	V _E = 5.0V
V _{BB}	Output Reference Voltage	3.620	3.730	3.650	3.750	3.690	3.810	V	V _E = 5.0V

Note:

1. ECL V_{IH}, V_{IL} and V_{BB} are referenced to V_{CC}E and will vary 1:1 with the power supply. The levels shown are for I_{VT} = I_{VO} = V_{CC}E = +5.0V.

100H ECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾ $V_T = V_E = +5.0V \pm 5\%$

Symbol	Parameter	T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I _{IH}	Input HIGH Current	—	225	—	175	—	175	μA	—
I _{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	μA	—
V _{IH}	Input HIGH Voltage	3.835	4.120	3.835	4.120	3.835	4.120	V	V _E = 5.0V
V _{IL}	Input LOW Voltage	3.190	3.525	3.190	3.525	3.190	3.525	V	V _E = 5.0V
V _{BB}	Output Reference Voltage	3.620	3.740	3.620	3.740	3.620	3.740	V	V _E = 5.0V

Note:

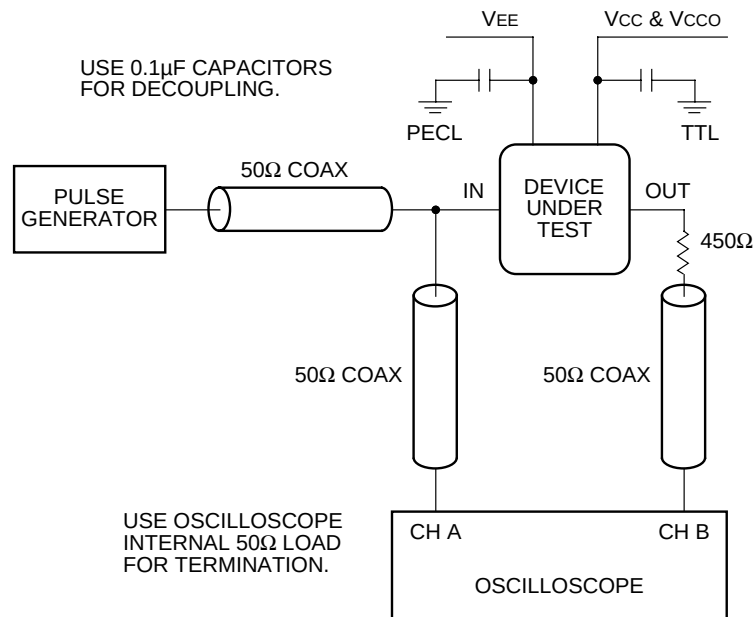
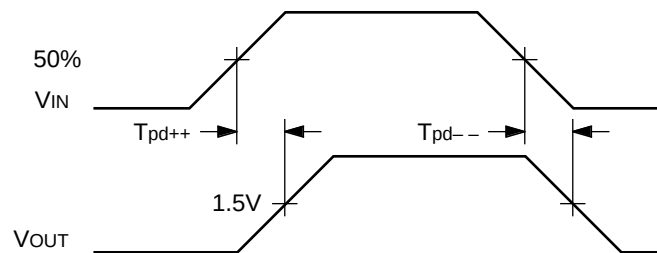
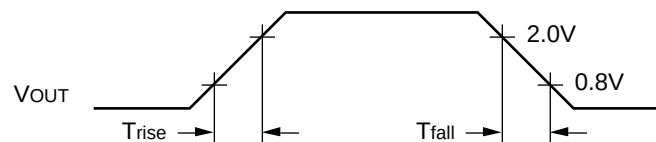
1. ECL V_{IH}, V_{IL} and V_{BB} are referenced to V_{CC}E and will vary 1:1 with the power supply. The levels shown are for I_{VT} = I_{VO} = V_{CC}E = +5.0V.

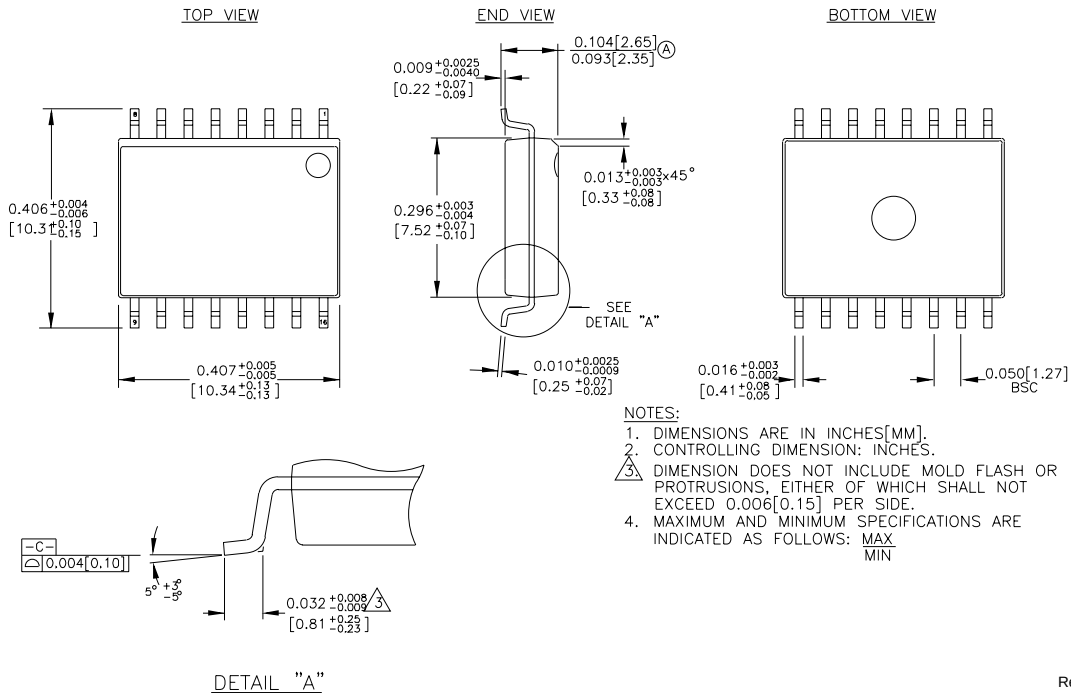
AC CHARACTERISTICS $V_T = V_E = 5.0V \pm 5\%$

Symbol	Parameter		TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay D to Output	Q0–Q3	2.7	3.7	2.7	3.7	2.7	3.7	ns	CL = 50pF
tskpp	Part-to-Part Skew ^(1,4)	Q0–Q3	—	0.5	—	0.5	—	0.5	ns	CL = 50pF
tskew++	Within-Device Skew ^(2,4)	Q0–Q3	—	0.3	—	0.3	—	0.3	ns	CL = 50pF
tskew– –	Within-Device Skew ^(3,4)	Q0–Q3	—	0.3	—	0.3	—	0.3	ns	CL = 50pF
tPLH tPHL	Propagation Delay LEN to Q	Q0–Q3	2.7	3.7	2.7	3.7	2.7	3.7	ns	CL = 50pF
tPLH tPHL	Propagation Delay EN to Output	Q0–Q3	2.7	3.7	2.7	3.7	2.7	3.7	ns	CL = 50pF
tr tf	Output Rise/Fall Time 1.0V to 2.0V	Q0–Q3	—	1.5	—	1.5	—	1.5	ns	CL = 50pF
fMAX	Max. Input Frequency ^(5,6)	Q0–Q3	160	—	160	—	160	—	MHz	CL = 50pF
—	Pulse Width	Q0–Q3	1.5	—	1.5	—	1.5	—	ns	—
—	Recovery Time $\overline{EN}$	Q0–Q3	1.0	—	1.0	—	1.0	—	ns	—
ts	Set-up Time D, $\overline{EN}$	Q0–Q3	0.75	—	0.75	—	0.75	—	ns	—
th	Hold Time D, EN	Q0–Q3	0.75	—	0.75	—	0.75	—	ns	—

Notes:

1. Device-to-Device Skew considering HIGH-to-HIGH transitions at common Vcc level.
2. Within-Device Skew considering HIGH-to-HIGH transitions at common Vcc level.
3. Within-Device Skew considering LOW-to-LOW transitions at common Vcc level.
4. All skew parameters are guaranteed but not tested.
5. Frequency at which output levels will meet at 0.8V to 2.0V minimum swing.
6. The fMAX value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.

TTL SWITCHING CIRCUIT**ECL/TTL PROPAGATION DELAY — SINGLE ENDED****ECL/TTL WAVEFORMS: RISE AND FALL TIMES**

16-PIN SOIC .300" WIDE (Z16-1)

Rev. 03

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