CY2X013
CY2X0137

High-Performance LVDS Oscillator

Features

- Low-jitter crystal oscillator (XO)
- Less than 1 ps typical root mean square (RMS) phase jitter
- Low-voltage differential signaling (LVDS) output
- Output frequency from 50 MHz to 690 MHz
- Factory-configured or field-programmable
- Integrated phase-locked loop (PLL)
- Can be configured as four different devices
- Supply voltage: 3.3 V or 2.5 V
- 5.0 × 3.2 mm Pb-free chip carrier (LCC): CY2X013
- 7.0 × 5.0 mm Pb-free chip carrier (LCC): CY2X0137
- Commercial and industrial temperature ranges

Functional Description

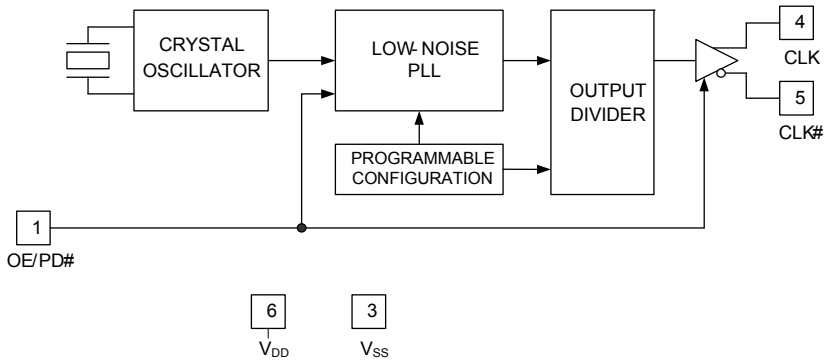
The CY2X013/CY2X0137 device is a high-performance and high-frequency XO. The device uses a Cypress proprietary low-noise PLL to synthesize the frequency from an integrated crystal.

The CY2X013/CY2X0137 device is available as a factory-configured device or as a field-programmable device. Factory-configured devices are configured for general use or they can be customer-specific. The same CY2X013/CY2X0137 device can be configured as four different device types as mentioned in the Logic Block Diagram.

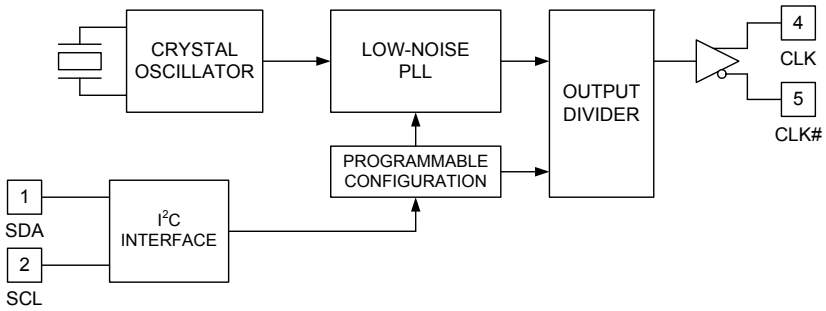
For a complete list of related documentation, click here.

Logic Block Diagram

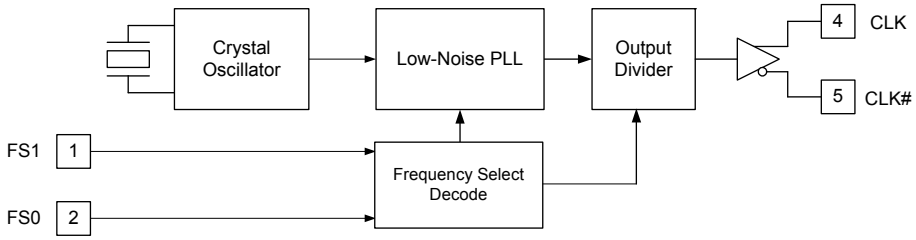
Device Type 1: High-performance LVDS crystal oscillator with Output Enable



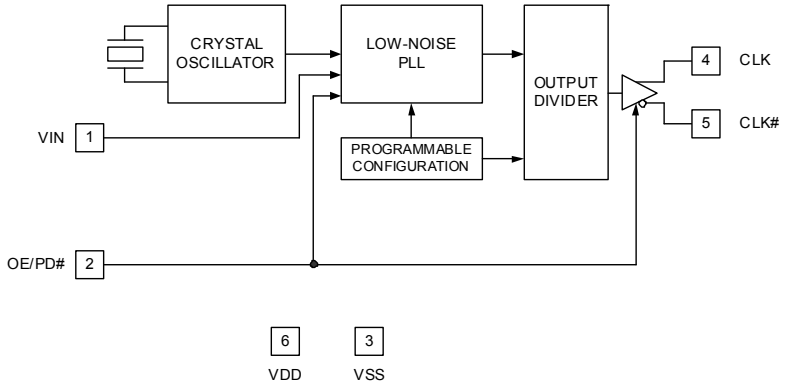
Device Type 2: High-performance LVDS crystal oscillator with Frequency Margining - I^2C control



Device Type 3: High-performance LVDS crystal oscillator with frequency margining - Frequency Select



Device Type 4: High-performance LVDS voltage-controlled crystal oscillator

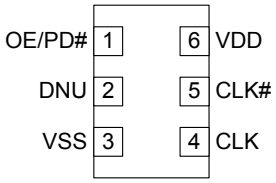


Contents

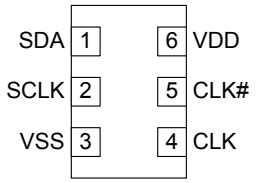
Pinouts

Figure 1. 6-pin Ceramic LCC Pinout

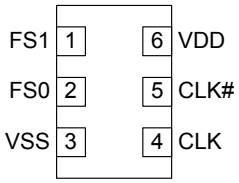
Device Type 1:
High--performance LVDS crystal oscillator with Output Enable:



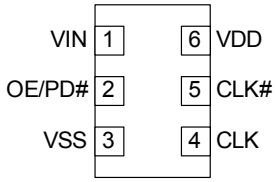
Device Type 2:
High-performance LVDS crystal oscillator with Frequency Margining - I^2C control



Device Type 3:
High-performance LVDS crystal oscillator with Frequency Margining - Frequency Select



Device Type 4:
High-performance LVDS voltage-controlled crystal oscillator



Pin Definitions

6-pin Ceramic LCC

Name	Device Type 1	Device Type 2	Device Type 3	Device Type 4	I/O Type	Description
OE/PD#	1	N/A	N/A	2	CMOS input	Output Enable pin: Active HIGH. If OE = 1, CLK is enabled. Power-down pin: Active LOW. If PD# = 0, the device is powered down and the clock is disabled. The functionality of this pin is programmable
CLK, CLK#	4,5	4,5	4,5	4,5	LVDS output	Differential output clock
DNU	2	N/A	N/A	N/A	–	Do not use: DNU pins are electrically connected, but perform no function
VDD	6	6	6	6	Power	Supply voltage: 2.5 V or 3.3 V
VSS	3	3	3	3	Power	Ground
FS1, FS0	N/A	N/A	1,2	N/A	CMOS input	Frequency Select
SDA	N/A	1	N/A	N/A	I/O	I^2C Serial Data
SCLK	N/A	2	N/A	N/A	CMOS input	I^2C Serial Clock
VIN	N/A	N/A	N/A	1	Analog input	VCXO control voltage, positive slope

Functional Overview

Device Type 1

Device Type 1 is a simple crystal oscillator with one output frequency. Pin 1 can be programmed either as OE or PD#. The OE function is used to enable or disable the CLK output whereas the PD# function places the device in a low-power state,

Device Type 2

Device Type 2 has an I^2C bus serial interface [1], which is used to change the output frequency.

CY2X013/CY2X0137 is configured for four frequencies. At power-on, the four configurations are transparently loaded into an internal volatile memory which, in turn, controls the PLL. The user can switch between the four frequencies through the I^2C bus. The user can also configure CY2X013/CY2X0137 with new output frequencies by shifting new data into the internal memory.

Frequency-margining is a common application for this feature. One frequency is used for the standard operating mode of the device, while additional frequencies are available for margin testing, either during product development or in-system manufacturing test.

Note that all configuration changes made using I^2C are temporary and are lost when power is removed from the device. At power-on, the device returns to its original state.

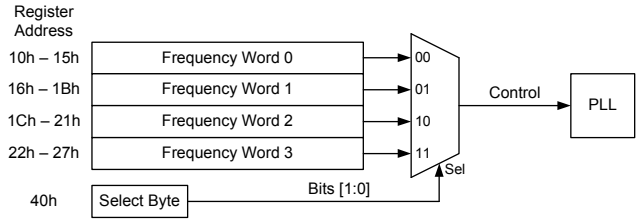
The configuration for a particular frequency is stored in a 6-byte block of memory, known as a word. CY2X013/CY2X0137 has four such words, labeled 'Frequency Word 0' through 'Frequency Word 3'. An additional register byte contains a 2-bit field, which selects one of the four frequency words. By writing to this select byte, the user can switch back and forth between the four programmed frequencies. The select byte can be configured to select any of the four frequency words at power-on.

When changing the output frequency, the frequency transition is not guaranteed to be smooth. There can be frequency excursions beyond the start frequency and the new frequency.Glitches and runt pulses are possible and time must be allowed for the PLL to re-lock.

If more than four frequencies are needed, the I^2C bus can be used to change any of the four frequency words. When writing frequency words through I^2C, the users should not change the currently selected word. Instead, write one of the three unselected words before changing the select byte to select that new word.

Figure 2 shows how the frequency words are arranged and selected.

Figure 2. Frequency Words



Device Type 3

The FS0 and FS1 pins select between four different output frequencies, as shown in Table 1. Frequency margining is a common application for this feature. One frequency is used for the standard operating mode of the device, while the other frequencies are available for margin testing, either during product development or in-system manufacturing test.

Table 1. Frequency Select

FS1	FS0	Output Frequency
0	0	Frequency 0
0	1	Frequency 1
1	0	Frequency 2
1	1	Frequency 3

When changing the output frequency, the frequency transition is not guaranteed to be smooth. There can be frequency excursions beyond the start frequency and the new frequency. Glitches and runt pulses are possible, and time must be allowed for the PLL to relock.

Device Type 4

Device Type 4 is a voltage-controlled crystal oscillator. It has a control voltage pin, VIN, which is an analog input used to adjust the output frequency. The nominal output frequency is defined when VIN = VDD,NOM/2. Increasing the voltage on VIN increases the output frequency, while decreasing the voltage on VIN decreases the output frequency. Any voltage between VSS and VDD is allowed on VIN. The voltage or frequency slope is very linear over most of the control voltage range.

Note
1. The serial interface is I^2C Bus compliant with the following exceptions: SDA input leakage current, SDA input capacitance, SDA and SCLK are clamped to V_{DD}, setup time, and output hold time.

Programming Description

CY2X013/CY2X0137 is a programmable device. Prior to being used in an application, it must be programmed with the output frequency and other variables described in Programming Variables. Two device types are available, each with its own programming flow. They are described in the following sections.

Field-Programmable CY2X013F/CY2X0137F

Field-programmable devices are shipped unprogrammed and must be programmed before being installed on a PCB. Customers use the CyClockWizard™ software to specify the device configuration and generate a joint electron devices engineering council (JEDEC - extension .jed) programming file. Programming of samples and prototype quantities is available using the CyClockWizard software along with a CY3675-CLKMAKER1 CyClockMaker Clock Programmer Kit and CY3675-LCC6B socket adapter. Cypress's value-added distribution partners also provide programming services. Field-programmable devices are designated with an 'F' in the part number. They are intended for quick prototyping and inventory reduction. You can generate JEDEC for these four devices using CyClockWizard 1.0. However, while creating JEDEC or programming different device types, select different MPNs in the CyClockWizard 1.0 software (see Table 2).

You can download the software and programmer kit hardware from www.cypress.com by clicking the hyperlinks in the previous paragraph.

Table 2. MPNs Selection on CyClockWizard 1.0 Software

Device Type	MPN selection on CyClockWizard 1.0
Device Type 1	CY2X013
Device Type 2	CY2XF23
Device Type 3	CY2XF33
Device Type 3	Contact Local Cypress FAE

Factory-Configured CY2X013/CY2X0137

For ready-to-use devices, the preconfigured CY2X013/CY2X0137 device is available for samples or orders, or you can request for a custom configuration. All requests are submitted to the local Cypress field application engineer (FAE) or sales representative. After the request is processed, the user receives a new part number, samples, and datasheet with the programmed values. This part number is used for additional sample requests and production orders. The CY2X013/CY2X0137device is one-time programmable (OTP).

Programming Variables

Output Frequency

CY2X013/CY2X0137 can synthesize a frequency to a resolution of one part per million (ppm), but the actual accuracy of the output frequency is limited by the accuracy of the integrated reference crystal.

The CY2X013/CY2X0137 device has an output frequency range of 50 MHz to 690 MHz, but the range is not continuous. ThisCY2X013CY2X0137cannot generate frequencies in the ranges of 521 MHz to 529 MHz and 596 MHz to 617 MHz.

Pin 1: Output Enable (OE) or Power Down (PD#)

This function is only available in Device Type 1 and 4. Pin 1 (Device Type 1) or Pin 2 (Device type 2) is programmed as either OE or PD#. The OE function is used to enable or disable the CLK output quickly, but it does not reduce core power consumption. The PD# function places the device in a low-power state, but the wake-up takes longer because the PLL must reacquire the lock.

Industrial versus Commercial Device Performance

Industrial and commercial devices have different internal crystals. They have a potentially significant impact on performance levels for applications requiring the lowest possible phase noise. The CyClockWIzard 1.0 software allows the user to select between, and view the expected performance of, both options.

Absolute Pull Range

This is only applicable for Device Type 4. The pull range of VCXO, measured in ppm is programmable. The configuration software allows the user to select one of seven possible absolute pull ranges (APR), ranging up to approximately ±200 ppm. APR is the net pull range of the device, after subtracting frequency variability due to device variation, and temperature, voltage, and aging effects.

Table 3. Device Programming Variables

Variable	Device Type
Output frequency	Device Type 1 and 4
Pin 1 function (OE or PD#)	Device Type 1
Temperature range (commercial or industrial)	Device Type 1, 2, 3 and 4
Output frequency 0	Device Type 2 and 3
Output frequency 1	Device Type 2 and 3
Output frequency 2	Device Type 2 and 3
Output frequency 3	Device Type 2 and 3
Absolute Pull Range	Device Type 4
Pin 2 function (OE or PD#)	Device Type 4

Memory Map

Five fields can be written via the I^2C bus. Four frequency words define the output frequency. As shown in Table 4, each of these words is a 6-byte field. When writing to a frequency word, all six bytes should be written. They may be written either as individual byte writes, or as a block write. The currently selected frequency word should not be written to. All four words are symmetrical, meaning that a 6-byte value that is valid for one word is also valid for any of the other words, and produces the same frequency.

The fifth field is the select byte, located at byte address 40h. The value written into the two least significant bits determines the active frequency word. The other bits of the byte are reserved and must be written with the values indicated in the table. Users should never write to any address other than the 25 bytes described here.

Table 4. Frequency Words

Frequency Word	Byte Addresses (hex)	Word Select (Select Byte 40h)
0	10h to 15h	00
1	16h to 1Bh	01
2	1Ch to 21h	10
3	22h to 27h	11

Table 5. Register 40h: Select Byte

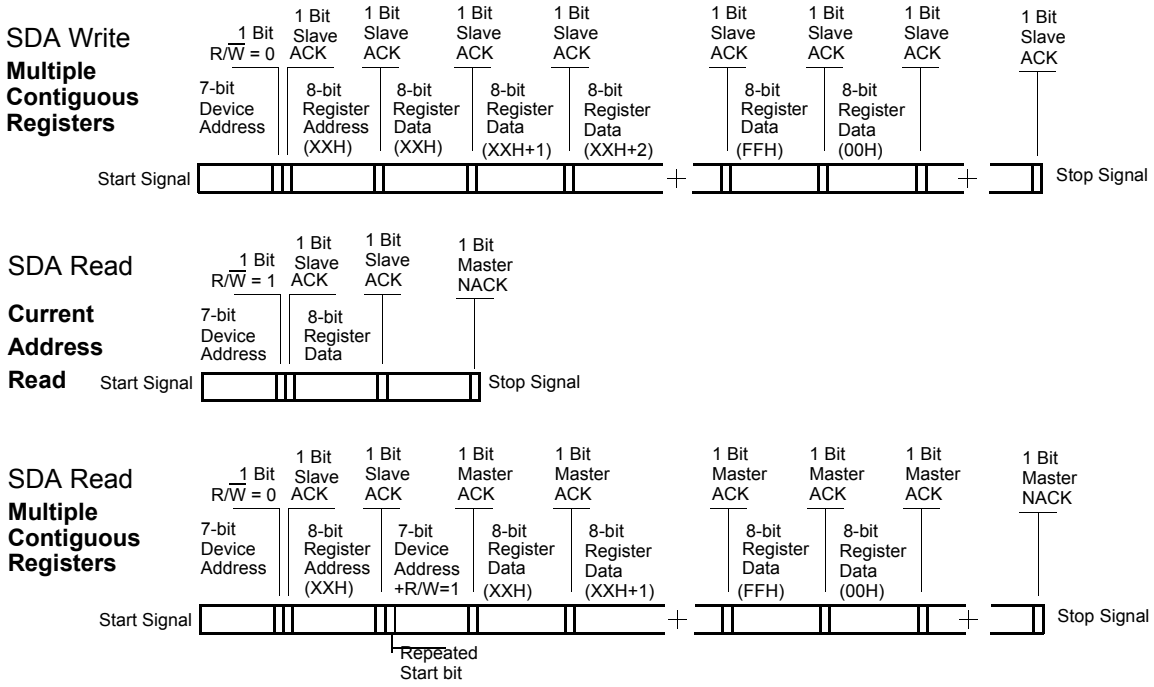
Bits	Default Value (binary)	Name	Description
7:2	000000	Reserved	Reserved. Always write this value.
1:0	User-defined	Word select	Selects the Frequency Word to determine the output frequency. 00 selects Word 0; 01 selects Word 1; 10 selects Word 2; 11 selects Word 3.

Serial Interface Protocol and Timing

The CY2X013 / CY2X0137 device uses the SDA and SCLK pins for an I^2C bus that operates up to 100 kbits/sec in read or write mode. The CY2X013 / CY2X0137 device is always a slave on this bus, meaning that it never initiates a bus transaction. The basic write protocol is as follows:

Start Bit: 7-bit Device Address (DA); R/$\overline{W}$ Bit; Slave Clock Acknowledge (ACK); 8-bit Memory Address (MA); ACK; 8-bit Data; ACK; 8-bit Data in MA+1 if desired; ACK; 8-bit Data in MA+2; ACK; and so on, until STOP Bit. The basic serial format is illustrated in Figure 3.

Figure 3. Data Frame Architecture



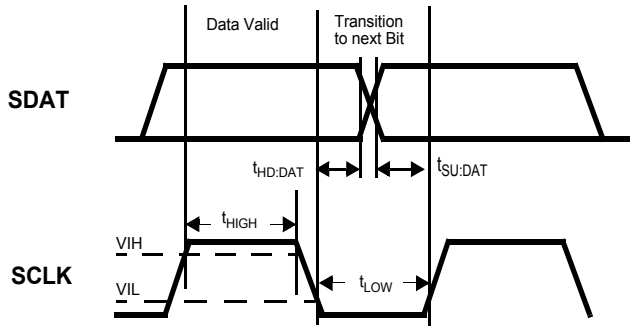
Device Address

The device I²C address is a 7-bit value. The default I²C address, which appears in CyClockWizard is 69H, which can be changed to any other value while generating configuration using CyClockWizard. Note that the default address of the field-programmable (unprogrammed[2]) devices is 69H.

Data Valid

Data is valid when the clock is HIGH and may only be transitioned when the clock is LOW, as illustrated in Figure 4.

Figure 4. Data Valid and Data Transition Periods



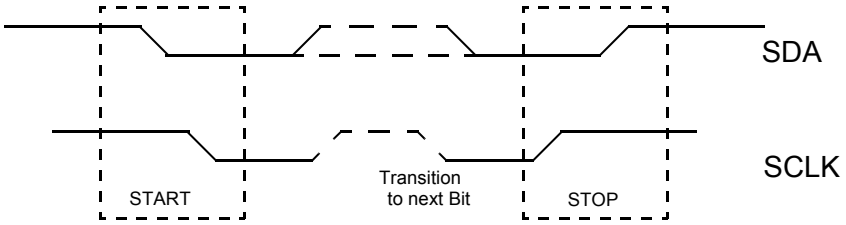
Data Frame

Every new data frame is indicated by a start and stop sequence, as illustrated in Figure 5.

START Sequence - Start frame is indicated by SDA going LOW when SCLK is HIGH. Every time a start signal is given, the next 8-bit data must be the device address (seven bits) and a R/$\overline{W}$ bit, followed by register address (eight bits) and register data (eight bits).

STOP Sequence - Stop frame is indicated by SDA going HIGH when SCLK is HIGH. A stop frame frees the bus for writing to another part on the same bus or writing to another random register address.

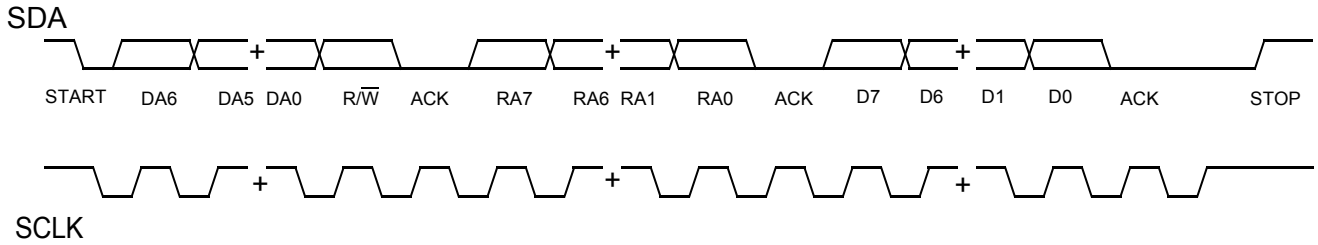
Figure 5. Start and Stop Frame



Acknowledge Pulse

During write mode, the CY2X013/CY2X0137 device responds with an Acknowledge (ACK) pulse after every eight bits. This is accomplished by pulling the SDA line LOW during the N*9th clock cycle as illustrated in Figure 6 (N = the number of bytes transmitted). After the data packet is sent during read mode, the master generates the acknowledge.

Figure 6. Frame Format (Device Address, R/$\overline{W}$, Register Address, Register Data)



Note

2. Field-programmable devices are shipped unprogrammed and must be programmed before being installed on a PCB. An unprogrammed device will output the crystal frequency of the integrated crystal (25 MHz for commercial and 38.8 MHz for industrial).

Write Operations

Writing Individual Bytes

A valid write operation must have a full 8-bit register address after the device address word from the master, which is followed by an acknowledge bit from the slave (SDA = 0/LOW). The next eight bits must contain the data word intended for storage. After the data word is received, the slave responds with another acknowledge bit (SDA = 0/LOW), and the master must end the write sequence with a STOP condition.

Writing Multiple Bytes

To write more than one byte at a time, the master does not end the write sequence with a stop condition. Instead, the master can send multiple contiguous bytes of data to be stored. After each byte, the slave responds with an acknowledge bit, just like after the first byte, and accepts data until the acknowledge bit is responded to by the STOP condition. When receiving multiple bytes, the CY2X013/CY2X0137 device internally increments the register address.

Read Operations

Read operations are initiated the same way as write operations except that the R/W bit of the slave address is set to ‘1’ (HIGH). There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

The CY2X013/CY2X0137 device has an onboard address counter that retains 1 more than the address of the last word access. If the last word written or read was word ‘n’, then a current address read operation returns the value stored in location ‘n+1’. When CY2X0137 receives the slave address with the R/W bit set to a ‘1’, CY2X013/CY2X0137 issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer but does generate a STOP condition, which causes CY2X013/CY2X0137 to stop transmission.

Random Read

Through random read operations, the master may access any memory location. To perform this type of read operation, first the word address must be set. This is accomplished by sending the address to the CY2X013/CY2X0137 as part of a write operation. After the word address is sent, the master generates a START condition following the acknowledge. This terminates the write operation before any data is stored in the address, but not before the internal address pointer is set. Next, the master reissues the control byte with the R/W byte set to ‘1’. The CY2X013/CY2X0137 device then issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer, but does generate a STOP condition, which causes the CY2X013/CY2X0137 to stop transmission.

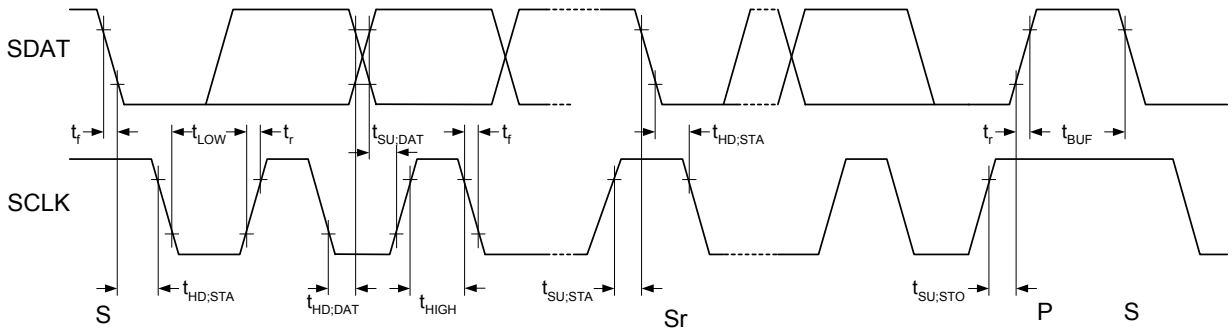
Sequential Read

Sequential read operations follow the same process as random reads except that the master issues an acknowledge instead of a STOP condition after transmission of the first 8-bit data word. This action results in an incrementing of the internal address pointer, and subsequently output of the next 8-bit data word. By continuing to issue acknowledges instead of STOP conditions, the master may serially read the entire contents of the slave device memory. When the internal address pointer points to the FFh register, the pointer will point to the 00h register after the next increment.

Serial Programming Interface Timing Specifications

Parameter	Description	Min	Max	Unit
f_{SCLK}	Frequency of SCLK	–	100	kHz
$t_{HD:STA}$	Hold time START condition	4.0	–	µs
t_{LOW}	Low period of the SCLK clock	4.7	–	µs
t_{HIGH}	High period of the SCLK clock	4.0	–	µs
$t_{SU:STA}$	Setup time for a repeated START condition	4.7	–	µs
$t_{HD:DAT}$	Data hold time	200	–	ns
$t_{SU:DAT}$	Data setup time	1000	–	ns
t_R	Rise time	–	300	ns
t_F	Fall time	–	300	ns
$t_{SU:STO}$	Setup time for STOP condition	4.0	–	µs
t_{BUF}	Bus-free time between STOP and START conditions	4.7	–	µs

Figure 7. Definition for Timing on the Serial bus



Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage		–0.5	4.4	V
V_{IN}[3]	Input voltage, DC	Relative to V_{SS}	–0.5	V_{DD} + 0.5	V
T_S	Temperature, storage	Non operating	–55	135	°C
T_J	Temperature, junction		–40	135	°C
ESD_{HBM}	Electrostatic discharge (ESD) protection human body model (HBM)	JEDEC Std 22-A114-B	2000	–	V
Θ_{JA}[4]	Thermal resistance, junction to ambient	0 m/s airflow	64		°C / W

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	3.3-V supply voltage range	3.0	3.3	3.6	V
	2.5-V supply voltage range	2.375	2.5	2.625	V
T_{PU}	Power-up time for V_{DD} to reach minimum specified voltage (power ramp is monotonic)	0.05	–	500	ms
T_A	Ambient temperature (commercial)	0	–	70	°C
	Ambient temperature (industrial)	–40	–	85	°C

Notes
3. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
4. Simulated. The board is derived from the JEDEC multilayer standard. It measures 76 × 114 × 1.6 mm and has 4 layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.

DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{DD}[5]	Operating supply current	V_{DD} = 3.6 V, OE/PD# = V_{DD}, output terminated, Device Type 1 and 4	–	–	125	mA
		V_{DD} = 2.625 V, OE/PD# = V_{DD}, output terminated, Device Type 1 and 4	–	–	120	mA
		V_{DD} = 3.465 V, CLK = 150 MHz, output terminated, Device Type 2 and 3	–	–	120	mA
		V_{DD} = 2.625 V, CLK = 150 MHz, output terminated, Device Type 2 and 3	–	–	115	mA
I_{SB}	Standby supply current	PD# = V_{SS}	–	–	200	µA
V_{OD}	LVDS differential output voltage	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 100 Ω between CLK and CLK#	247	–	454	mV
ΔV_{OD}	Change in V_{OD} between complementary output states	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 100 Ω between CLK and CLK#	–	–	50	mV
V_{OS}	LVDS offset output voltage	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 100 Ω between CLK and CLK#	1.125	–	1.375	V
ΔV_{OS}	Change in V_{OS} between complementary output states	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 100 Ω between CLK and CLK#	–	–	50	mV
V_{OLS}	Output low voltage (SDA)	I_{OL} = 4 mA	–	–	0.1 × V_{DD}	V
I_{OZ}	LVDS output leakage current	Tristate output, unterminated, measured on one pin while floating the other pin, PD#/OE = V_{SS}	–35	–	35	µA
V_{IH}	Input high voltage		0.7 × V_{DD}	–	–	V
V_{IL}	Input low voltage		–	–	0.3 × V_{DD}	V
I_{IH0}	Input high current, Pin 1	Input = V_{DD}	–	–	115	µA
I_{IH1}	Input high current, Pin 2	Input = V_{DD}	–	–	10	µA
I_{IL0}	Input low current, Pin 1	Input = V_{SS}	–50	–		µA
I_{IL1}	Input low current, Pin 2	Input = V_{SS}	–20	–	–	µA
C_{IN0}[6]	Input capacitance, Pin 1		–	15	–	pF
C_{IN1}[6]	Input capacitance, Pin 2		–	4	–	pF
V_{VIN}	V_{IN} input voltage (Device Type 4)		0	–	V_{DD}	V
I_{VIN}	V_{IN} input current (Device Type 4)	$V_{SS} \le V_{IN} \le V_{DD}$	–50	–	115	µA
INL_{VIN}[6, 7]	V_{IN} to F_{OUT} Integral Nonlinearity (Device Type 4)	$V_{SS} \le V_{IN} \le V_{DD}$	–	1	–	%

Notes
5. I_{DD} includes ~4 mA of current that is dissipated externally in the output termination resistors.
6. Not 100% tested, guaranteed by design and characterization.
7. Integral nonlinearity is defined in IEEE Standard 1241-2000.

AC Electrical Characteristics

The following table lists the AC electrical specifications for this device. [8]

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{OUT}	Output frequency [9]		50	–	690	MHz
FSC	Frequency stability, commercial devices [10]	V_{DD} = min to max, T_A = 0 °C to 70 °C	–	–	±35	ppm
FSI	Frequency stability, industrial devices [10]	V_{DD} = min to max, T_A = –40 °C to 85 °C	–	–	±55	ppm
AG	Aging, 10 years		–	–	±15	ppm
T_{DC}	Output duty cycle	F ≤ 450 MHz, measured at zero crossing	45	50	55	%
		F > 450 MHz, measured at zero crossing	40	50	60	%
T_R, T_F	Output rise and fall time	20% and 80% of full output swing	–	0.35	1.0	ns
T_{OHZ}	Output disable time	Time from falling edge on OE to stopped outputs (asynchronous)	–	–	100	ns
T_{OE}	Output enable time	Time from rising edge on OE to outputs at a valid frequency (asynchronous)	–	–	120	ns
T_{LOCK}	Startup time	Time for CLK to reach valid frequency measured from the time V_{DD} = V_{DD}(min) or from PD# rising edge	–	–	5	ms
T_{LSER}	Relock time	Time for CLK to reach valid frequency from serial bus change to select bits in register 40h, measured from I^2C STOP (Device Type 2) or Time for CLK to reach valid frequency from FS0 or FS1 pin change (Device Type 3)	–	–	1	ms
$T_{Jitter(\phi)}$	RMS phase jitter (random)	F_{OUT} = 106.25 MHz (12 kHz to 20 MHz)	–	1	–	ps

Notes
8. Not 100% tested, guaranteed by design and characterization.
9. This parameter is specified in the CyClockWizard 1.0 software.
10. Frequency stability is the maximum variation in frequency from F_0. It includes initial accuracy, and variation from temperature and supply voltage.

Switching Waveforms

Figure 8. Output Voltage Swing

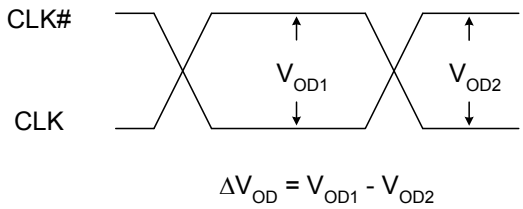


Figure 9. Output Offset Voltage

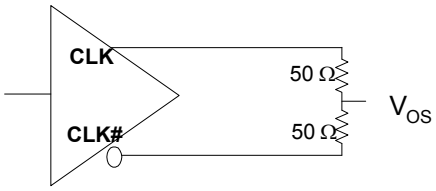


Figure 10. Duty Cycle Timing

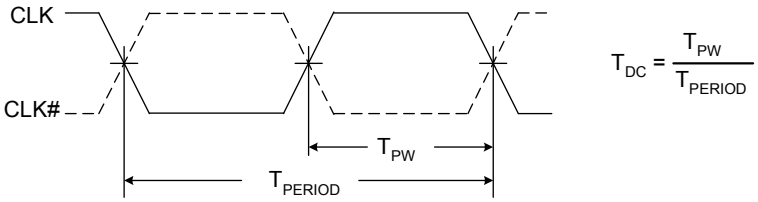


Figure 11. Output Rise and Fall Time

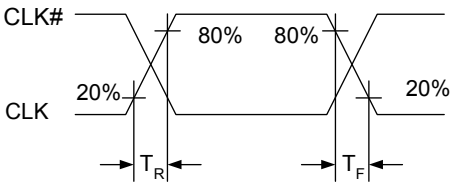
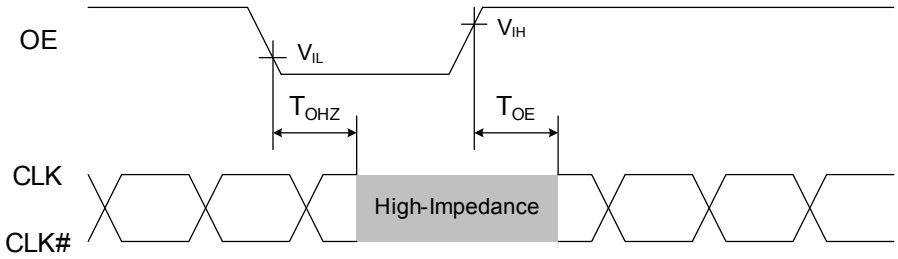
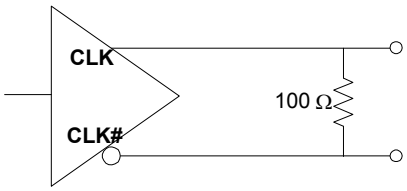


Figure 12. Output Enable and Disable Timing



Termination Circuits

Figure 13. LVDS Termination



Ordering Information

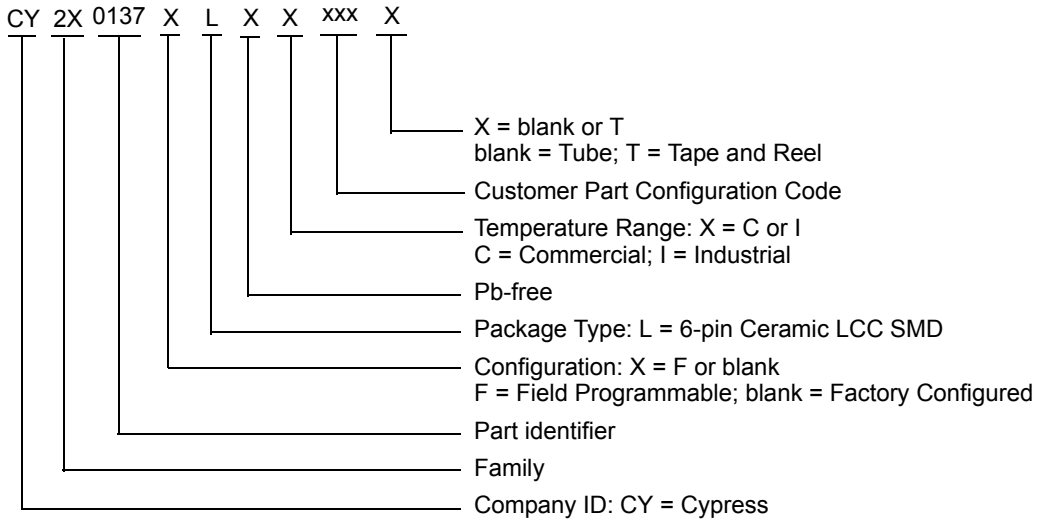
Part Number	Configuration	Package Description	Product Flow
Pb-free			
CY2X013FLXCT	Field-programmable	6-pin ceramic LCC SMD - Tape and Reel	Commercial, 0 °C to 70 °C
CY2X013FLXIT	Field-programmable	6-pin ceramic LCC SMD - Tape and Reel	Industrial, –40 °C to 85 °C
CY2X0137FLXCT	Field-programmable	6-pin ceramic LCC SMD - Tape and Reel	Commercial, 0 °C to 70 °C
CY2X0137FLXIT	Field-programmable	6-pin ceramic LCC SMD - Tape and Reel	Industrial, –40 °C to 85 °C

Some product offerings are factory-programmed, customer-specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or sales representative for more information.

Possible Configurations

Part Number [11]	Configuration	Package Description	Product Flow
Pb-free			
CY2X013LXCxxx	Factory-configured	6-pin ceramic LCC SMD	Commercial, 0 °C to 70 °C
CY2X013LXCxxxT	Factory-configured	6-pin ceramic LCC SMD - Tape and Reel	Commercial, 0 °C to 70 °C
CY2X013LXIxxx	Factory-configured	6-pin ceramic LCC SMD	Industrial, –40 °C to 85 °C
CY2X013LXIxxxT	Factory-configured	6-pin ceramic LCC SMD - Tape and Reel	Industrial, –40 °C to 85 °C
CY2X0137LXCxxx	Factory-configured	6-pin ceramic LCC SMD	Commercial, 0 °C to 70 °C
CY2X0137LXCxxxT	Factory-configured	6-pin ceramic LCC SMD - Tape and Reel	Commercial, 0 °C to 70 °C
CY2X0137LXIxxx	Factory-configured	6-pin ceramic LCC SMD	Industrial, –40 °C to 85 °C
CY2X0137LXIxxxT	Factory-configured	6-pin ceramic LCC SMD - Tape and Reel	Industrial, –40 °C to 85 °C

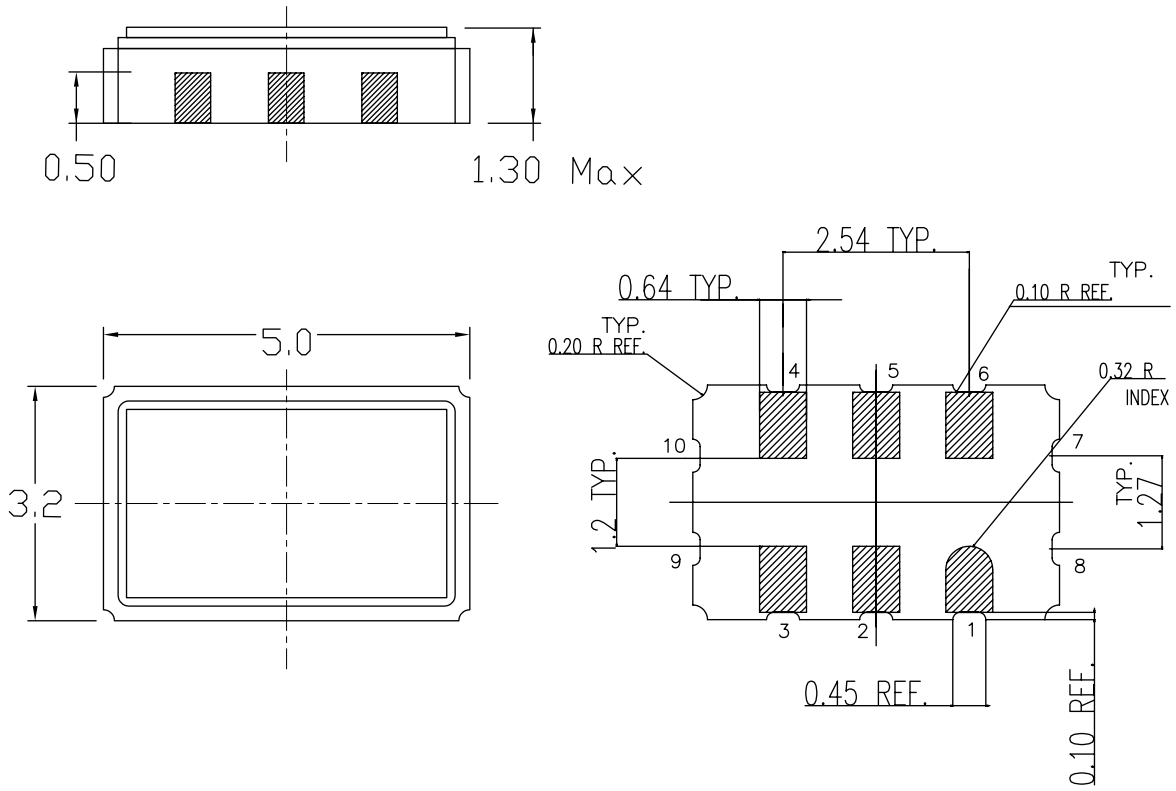
Ordering Code Definitions



Note
11. “xxx” indicates factory programmed parts based on customer specific configuration. For more details, contact your local Cypress FAE or a sales representative.

Package Diagrams

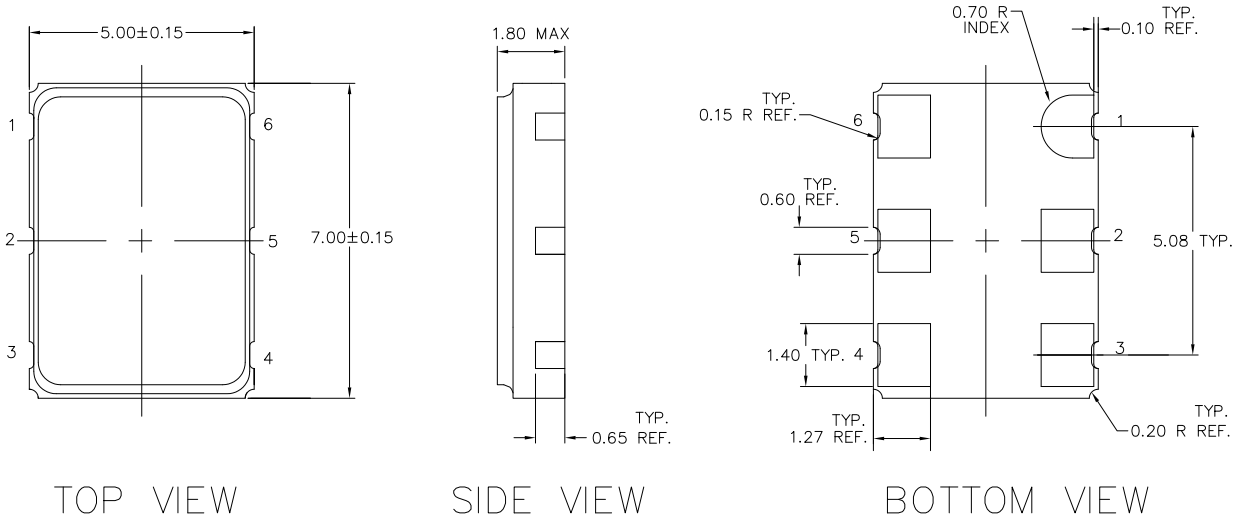
Figure 14. 6-pin Ceramic LCC (5.0 × 3.2 × 1.30 mm) LZ06B Package Outline, 001-10044



001-10044 *C

Package Diagrams (continued)

Figure 15. 6-pin Ceramic LCC (5.0 × 7.0 × 1.80 mm) LZ06B Package Outline, 001-85862



NOTES:

1. Dimensions are in mm
2. Kyocera Ref. Drawing No. KD−VA1806

001-85862 *A

Acronyms

Acronym	Description
ESD	Electrostatic Discharge
FAE	Field Application Engineer
HBM	Human Body Model
JEDEC	Joint Electron Devices Engineering Council
LCC	Leadless Chip Carrier
LVDS	Low-Voltage Differential Signaling
OE	Output Enable
OTP	One-Time Programmable
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
RMS	Root Mean Square
XO	Crystal Oscillator

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mV	millivolt
ms	millisecond
ns	nanosecond
Ω	ohm
ppm	parts per million
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY2X013/CY2X0137, High-Performance LVDS Oscillator Document Number: 001-86061				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3944886	PURU	06/21/2013	New data sheet.
*A	4178429	CINM	10/30/2013	Changed status from Preliminary to Final. Updated Ordering Information: Updated part numbers. Updated to new template.
*B	4587303	CINM	12/05/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Memory Map: Updated Serial Interface Protocol and Timing: Updated Figure 3 (Updated the last ACK in SDA Read to “NACK”).
*C	4756544	XHT	05/06/2015	Updated Document Title to read as “CY2X013/CY2X0137, High-Performance LVDS Oscillator”. Added CY2X013 part related information in all instances across the document. Added Serial Programming Interface Timing Specifications. Updated Ordering Information: Updated part numbers. Updated Package Diagrams: Added spec 001-10044 *C.
*D	5832001	XHT	07/25/2017	Updated to new template. Completing Sunset Review.

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