17 Ω, +12 V / ± 5 V / +5 V / +3 V, 8-Ch / Dual 4-Ch High Performance Analog Multiplexers

DESCRIPTION

The DG408LE, DG409LE are monolithic analog multiplexers / demultiplexers designed to operate on single and dual supplies. Single supply voltage ranges from 3 V to 16 V while dual supply operation is recommended with ± 3 V to ± 8 V.

The DG408LE is an 8 channel single-ended analog multiplexer designed to connect one of eight inputs to a common output as determined by a 3 bit binary address (A_0, A_1, A_2). The DG409LE is a dual 4 channel differential analog multiplexer designed to connect one of four differential inputs to a common dual output as determined by its 2 bit binary address (A_0, A_1). Break-before-make switching action to protect against momentary crosstalk between adjacent channels.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer / demultiplexer to all switches off for stacking several devices. All control inputs, address (Ax) and enable (EN) are TTL compatible over the full specified operating temperature range.

The DG408LE, DG409LE feature low on-resistance, fast switching time, and low leakage. They are ideal for data acquisition, control and automation, test instrument, and healthcare products. The DG408LE, DG409LE has an internal regulator powers the logic circuit. Such design reduces device power consumption and makes them ideal for battery operated applications.

The DG408LE, DG409LE are available in TSSOP16, SOIC16, and QFN16 packages.

FEATURES

- Pin-for-pin compatibility with DG408, DG409, and DG508, DG509
- 3 V to 16 V single supply or ± 3 V to ± 8 V dual supply operation
- Low power consumption: 6 µA/max., EN = Vx = 5 V
- Lower on-resistance: $R_{DS(on)}$ - 17 Ω typ.
- Fast switching: t_{ON} - 55 ns, t_{OFF} - 36 ns
- Break-before-make guaranteed
- Low leakage: $I_{S(OFF)}$ - 1 nA max.
- TTL, CMOS, LV logic (3 V) compatible
- -99 dB off-isolation and -98 dB crosstalk at 100 kHz
- Low parasitic capacitances: $C_{S(OFF)}$ = 5.5 pF, $C_{D(ON)}$ = 35 pF (DG408LE)
- ESD Protection:
  - ± 2.5 kV human body model
  - ± 100 V machine model
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free Available

RoHS* Available

HALOGEN FREE Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

BENEFITS

- High accuracy
- Single and dual power rail capacity
- Wide operating voltage range
- Simple logic interface

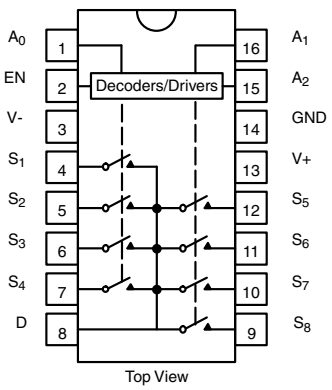
APPLICATIONS

- Automatic test equipment
- Data acquisition systems
- Meters and instruments
- Medical and healthcare systems
- Communication systems
- Audio and video signal routing
- Relay replacement
- Battery powered systems
- Computer peripherals
- Audio and video signal routing

FUNCTIONAL BLOCK DIAGRAMS AND PIN CONFIGURATIONS

DG408LE

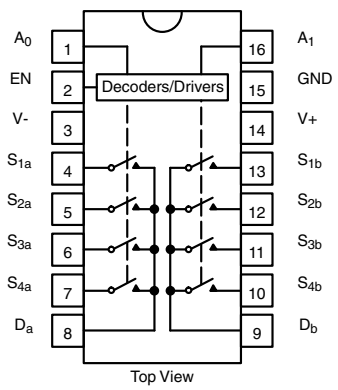
Dual-In- Line, SOIC and TSSOP



Top View

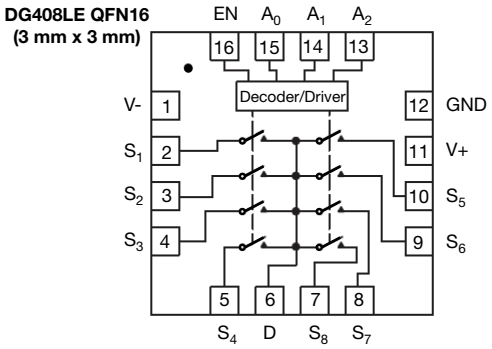
DG409LE

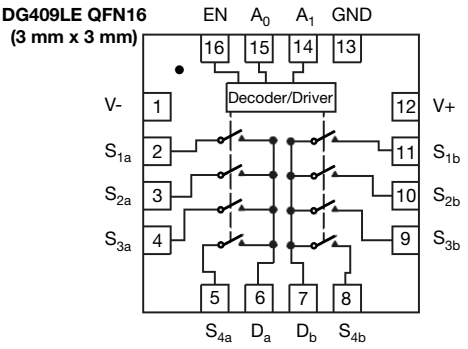
Dual-In- Line, SOIC and TSSOP



Top View

QFN OUTLINE





TRUTH TABLE (DG408LE)				
A_2	**A_1**	**A_0**	**EN**	**ON SWITCH**
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE (DG409LE)			
A_1	**A_0**	**EN**	**ON SWITCH**
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Note

- For low and high voltage levels for V_{AX} and V_{EN} consult “Digital Control” parameters for specific V+ operation.

ORDERING INFORMATION				
TEMP. RANGE	**CONFIGURATION**	**PACKAGE**	**PART NUMBER**	**MIN. ORDER / PACK. QUANTITY**
-40 °C to +85 °C Lead-free	8 Channel Single Ended DG408LE	16-pin TSSOP	DG408LEDQ-GE3	Tube 360 units
			DG408LEDQ-T1-GE3	Tape and reel, 3000 units
		16-pin SOIC	DG408LEDY-GE3	Tube 500 units
			DG408LEDY-T1-GE3	Tape and reel, 2500 units
		16-pin QFN (3 mm x 3 mm) Variation 2	DG408LEDN-T1-GE4	Tape and reel, 2500 units
	Dual 4 Channel Differential DG409LE	16-pin TSSOP	DG409LEDQ-GE3	Tube 360 units
			DG409LEDQ-T1-GE3	Tape and reel, 3000 units
		16-pin SOIC	DG409LEDY-GE3	Tube 500 units
			DG409LEDY-T1-GE3	Tape and reel, 2500 units
		16-pin QFN (3 mm x 3 mm) Variation 2	DG409LEDN-T1-GE4	Tape and reel, 2500 units

Note

- -T1 indicates tape and reel, -GE3 indicates lead (Pb)-free and RoHS-compliant, NO -GE3 indicates standard tin/lead finish.
- Exposed pad of QFN package can be connected to GND, V-, or left floating.

ABSOLUTE MAXIMUM RATINGS			
PARAMETER		**LIMIT**	**UNIT**
V+ to V- [e]		18	V
GND to V-		-18	
Digital Inputs [a], V_S, V_D		(V-) - 0.3 to (V) + 0.3	
Current (any terminal)		30	mA
Peak Current, S or D (pulsed at 1 ms, 10 % duty cycle max.)		100	
Storage Temperature	(D suffix)	-65 to +125	°C
Power Dissipation (package) [b]	16-pin plastic TSSOP [c]	600	mW
	16-pin narrow SOIC [c]	600	
	16-pin miniQFN [d]	1385	
ESD Human Body Model (HBM); per ANSI / ESDA / JEDEC® JS-001		2500	V
Latch Up Current, per JESD78D		300	mA

Notes

a. Signals on S_X, D_X, A_X, or EN exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 8 mW/°C above 75 °C.
d. Derate 17.3 mW/°C above 70 °C
e. Also applies when V- = GND

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (Single Supply 12 V)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 12 V, ± 10 %, V- = 0 V V_{EN} = 0.8 V or 2.4 V [f]**	**TEMP. [b]**	**TYP. [d]**	**D SUFFIX -40 °C to +85 °C**		**UNIT**
					MIN. [c]	**MAX. [c]**	
Analog Switch							
Analog Signal Range [e]	V_{ANALOG}		Full	-	0	12	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_D = 10.8 V, V_D = 2 V or 9 V, I_S = 10 mA sequence each switch on	Room	17	-	23	Ω
			Full	-	-	27	
$R_{DS(on)}$ Matching Between Channels [g]	ΔR_{DS}	V_D = 10.8 V, V_D = 2 V or 9 V I_S = 10 mA	Room	1	-	3	
On-Resistance Flatness	$R_{FLAT(on)}$		Room	3		6.5	
Switch Off Leakage Current [a]	$I_{S(off)}$	V_{EN} = 0 V, V_D = 11 V or 1 V V_S = 1 V or 11 V	Room	-	-1	1	nA
			Full	-	-5	5	
	$I_{D(on)}$		Room	-	-1	1	
			Full	-	-5	5	
Channel On Leakage Current [a]	$I_{D(on)}$	V_S = V_D = 1 V or 11 V	Room	-	-1	1	
			Full	-	-5	5	
Digital Control							
Logic High Input Voltage	V_{INH}		Full	-	2.4	-	V
Logic Low Input Voltage	V_{INL}		Full	-	-	0.8	
Input Current [a]	I_{IN}	V_{AX} = V_{EN} = 2.4 V or 0.8 V	Full	-	-1	1	µA
Dynamic Characteristics							
Transition Time	t_{TRANS}	V_{S1} = 8 V, V_{S8} = 0 V, (DG408LE) V_{S1b} = 8 V, V_{S4b} = 0 V, (DG409LE) see figure 2	Room	85	-	100	ns
			Full	-	-	110	
Break-Before-Make Time	t_{OPEN}	$V_{S(all)}$ = V_{DA} = 5 V see figure 4	Room	34	1	-	
			Full	-	-	-	
Enable Turn-On Time	$t_{ON(EN)}$	V_{AX} = 0 V, V_{S1} = 5 V (DG408LE) V_{AX} = 0 V, V_{S1b} = 5 V (DG409LE) see figure 3	Room	55	-	72	
			Full	-	-	82	
Enable Turn-Off Time	$t_{OFF(EN)}$		Room	36	-	47	
			Full	-	-	50	
Charge Injection [e] (DG408LE)	Q	C_L = 1 nF, V_{GEN} = 6 V, R_{GEN} = 0 Ω	Room	-11	-	-	pC
Charge Injection [e] (DG409LE)			Room	-10	-	-	
Off Isolation [e, h] (DG408LE)	OIRR	f = 100 kHz, R_L = 50 Ω	Room	-99	-	-	dB
Off Isolation [e, h] (DG409LE)			Room	-87	-	-	
Crosstalk [e] (DG408LE)	X_{TALK}		Room	-98	-	-	
Crosstalk [e] (DG409LE)			Room	-109	-	-	
Source Off Capacitance [e] (DG408LE)	$C_{S(off)}$	f = 1 MHz, V_S = 0 V, V_{EN} = 0 V	Room	5.5	-	-	pF
Source Off Capacitance [e] (DG409LE)			Room	5.5	-	-	
Drain Off Capacitance [e] (DG408LE)	$C_{D(off)}$	f = 1 MHz, V_D = 2.4 V, V_{EN} = 0 V	Room	25	-	-	
Drain Off Capacitance [e] (DG409LE)			Room	13.5	-	-	
Drain On Capacitance (DG408LE)	$C_{D(on)}$	f = 1 MHz, V_D = 0 V, V_{EN} = 2.4 V (DG409LE only)	Room	35	-	-	
Drain On Capacitance [e] (DG409LE)			Room	23.5	-	-	
Power Supplies							
Power Supply Range	V+			-	3	12	V
Power Supply Current	I+	V_{EN} = V_A = 0 V or 5 V	Room	3.5		6	µA

Notes

a. Leakage parameters are guaranteed by worst case test condition and not subject to production test.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta R_{DS(on)}$ = $R_{DS(on)}$ max. - $R_{DS(on)}$ min.
h. Worst case isolation occurs on Channel 4 do to proximity to the drain pin.

SPECIFICATIONS (Dual Supply V+ = 5 V, V - = -5 V)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 5 V, ± 10 %, V- = -5 V V_{EN} = 0.6 V or 2.4 V [f]**	**TEMP. [b]**	**TYP. [d]**	**D SUFFIX -40 °C to +85 °C**		**UNIT**
					MIN. [c]	**MAX. [c]**	
Analog Switch							
Analog Signal Range [e]	V_{ANALOG}		Full	-	-5	5	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_D = ± 3.5 V, I_S = 10 mA sequence each switch on	Room	15	-	25	Ω
			Full	-	-	30	
Switch Off Leakage Current [a]	$I_{S(off)}$	V+ = 5.5, V- = 5.5 V V_{EN} = 0 V, V_D = ± 4.5 V, V_S = ± 4.5 V	Room	-	-1	1	nA
			Full	-	-5	5	
	$I_{D(off)}$		Room	-	-1	1	
			Full	-	-5	5	
Channel On Leakage Current [a]	$I_{D(on)}$	V+ = 5.5 V, V- = -5.5 V V_{EN} = 2.4 V, V_D = ± 4.5 V, V_S = ± 4.5 V	Room	-	-1	1	
			Full	-	-5	5	
Digital Control							
Logic High Input Voltage	V_{INH}		Full	-	2.4	-	V
Logic Low Input Voltage	V_{INL}		Full	-	-	0.6	
Input Current [a]	I_{IN}	V_{AX} = V_{EN} = 2.4 V or 0.6 V	Full	-	-1	1	µA
Dynamic Characteristics							
Transition Time	t_{TRANS}	V_{S1} = 3.5 V, V_{S8} = -3.5 V, (DG408LE) V_{S1b} = 3.5 V, V_{S4b} = -3.5 V, (DG409LE) see figure 2	Room	87	-	100	ns
			Full	-	-	120	
Break-Before-Make Time	t_{OPEN}	$V_{S(all)}$ = V_{DA} = 3.5 V see figure 4	Room	84	1	-	
			Full	-	-	-	
Enable Turn-On Time	$t_{ON(EN)}$	V_{AX} = 0 V, V_{S1} = 3.5 V (DG408LE) V_{AX} = 0 V, V_{S1b} = 3.5 V (DG409LE) see figure 3	Room	58	-	73	
			Full	-	-	80	
Enable Turn-Off Time	$t_{OFF(EN)}$		Room	31	-	46	
			Full	-	-	51	
Source Off Capacitance [e] (DG408LE)	$C_{S(off)}$	f = 1 MHz, V_S = 0 V, V_{EN} = 0 V	Room	6	-	-	pF
Source Off Capacitance [e] (DG409LE)			Room	5.5	-	-	
Drain Off Capacitance [e] (DG408LE)	$C_{D(off)}$	f = 1 MHz, V_D = 0 V, V_{EN} = 0 V	Room	26	-	-	
Drain Off Capacitance [e] (DG409LE)			Room	14	-	-	
Drain On Capacitance [e] (DG408LE)	$C_{D(on)}$	f = 1 MHz, V_D = 0 V, V_{EN} = 2.4 V	Room	36	-	-	
Drain On Capacitance [e] (DG409LE)			Room	24	-	-	

Notes

a. Leakage parameters are guaranteed by worst case test condition and not subject to production test.
b. Room = 25 °C, full = as determined by the operating temperature suffix.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta R_{DS(on)} = R_{DS(on)}$ max. - $R_{DS(on)}$ min.
h. Worst case isolation occurs on channel 4 do to proximity to the drain pin.

SPECIFICATIONS (Single Supply 5 V)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 5 V, ± 10 %, V- = 0 V V_{EN} = 0.6 V or 2.4 V [f]**	**TEMP. [b]**	**TYP. [d]**	**D SUFFIX -40 °C to +85 °C**		**UNIT**
					MIN. [c]	**MAX. [c]**	
Analog Switch							
Analog Signal Range [e]	V_{ANALOG}		Full	-	0	5	V
Drain-Source On-Resistance	$R_{DS(on)}$	V+ = 4.5 V, V_D or V_S = 1 V or 3.5 V, I_S = 5 mA	Room	28	-	36	Ω
			Full	-	-	41	
$R_{DS(on)}$ Matching Between Channels [g]	ΔR_{DS}	V+ = 4.5 V, V_D = 1 V or 3.5 V, I_S = 5 mA	Room	1	-	3	
On-Resistance Flatness	$R_{FLAT(on)}$		Room	-	-	4	
Switch Off Leakage Current [a]	$I_{S(off)}$	V+ = 5.5 V, V_S = 1 V or 4 V V_D = 4 V or 1 V	Room	-	-1	1	nA
			Full	-	-5	5	
	$I_{D(off)}$		Room	-	-1	1	
			Full	-	-5	5	
Channel On Leakage Current [a]	$I_{D(on)}$	V+ = 5.5 V, V_D = V_S = 1 V or 4 V sequence each switch on	Room	-	-1	1	
			Full	-	-5	5	
Digital Control							
Logic High Input Voltage	V_{INH}	V+ = 5 V	Full	-	2.4	-	V
Logic Low Input Voltage	V_{INL}		Full	-	-	0.6	
Input Current [a]	I_{IN}	V_{AX} = V_{EN} = 2.4 V or 0.6 V	Full	-	-1	1	µA
Dynamic Characteristics							
Transition Time	t_{TRANS}	V_{S1} = 3.5 V, V_{S8} = 0 V, (DG408LE) V_{S1b} = 3.5 V, V_{S4b} = 0 V, (DG409LE) see figure 2	Room	113	-	135	ns
			Full	-	-	165	
Break-Before-Make Time	t_{OPEN}	$V_{S(all)}$ = V_{DA} = 3.5 V, see figure 4	Room	75	1	-	
			Full	-	-	-	
Enable Turn-On Time	$t_{ON(EN)}$	V_{AX} = 0 V, V_{S1} = 3.5 V (DG408LE) V_{AX} = 0 V, V_{S1b} = 3.5 V (DG409LE) see figure 3	Room	77	-	89	
			Full	-	-	110	
Enable Turn-Off Time	$t_{OFF(EN)}$		Room	43	-	50	
			Full	-	-	53	
Charge Injection [e] (DG408LE)	Q	C_L = 1 nF, R_{GEN} = 0 Ω, V_{GEN} = 2.5 V	Room	-2	-	-	pC
Charge Injection [e] (DG409LE)			Room	-2	-	-	
Off Isolation [e, h] (DG408LE)	OIRR	f = 100 kHz, R_L = 50 Ω	Room	-100	-	-	dB
Off Isolation [e, h] (DG409LE)			Room	-83	-	-	
Crosstalk [e] (DG408LE)	X_{TALK}		Room	-101	-	-	
Crosstalk [e] (DG409LE)			Room	-108	-	-	
Source Off Capacitance [e] (DG408LE)	$C_{S(off)}$	f = 1 MHz, V_S = 0 V, V_{EN} = 0 V	Room	6.5	-	-	pF
Source Off Capacitance [e] (DG409LE)			Room	6.5	-	-	
Drain Off Capacitance [e] (DG408LE)	$C_{D(off)}$	f = 1 MHz, V_D = 0 V, V_{EN} = 0 V	Room	30	-	-	
Drain Off Capacitance [e] (DG409LE)			Room	16	-	-	
Drain On Capacitance [e] (DG408LE)	$C_{D(on)}$	f = 1 MHz, V_D = 0 V, V_{EN} = 2.4 V	Room	40	-	-	
Drain On Capacitance [e] (DG409LE)			Room	26.5	-	-	

Notes

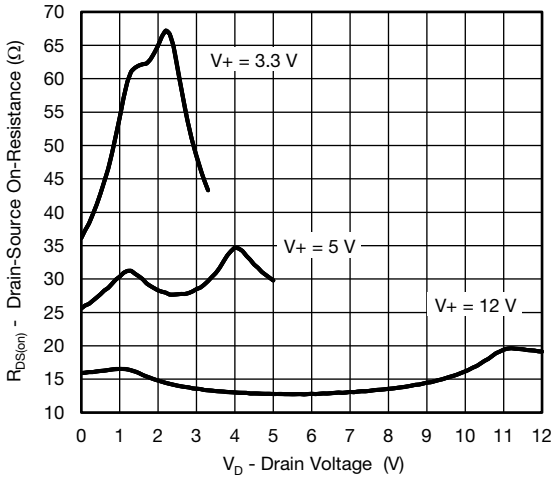
a. Leakage parameters are guaranteed by worst case test condition and not subject to production test.
b. Room = 25 °C, full = as determined by the operating temperature suffix.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta R_{DS(on)}$ = $R_{DS(on)}$ max. - $R_{DS(on)}$ min.
h. Worst case isolation occurs on channel 4 do to proximity to the drain pin.

SPECIFICATIONS (Single Supply 3 V)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 3 V, ± 10 %, V- = 0 V V_{EN} = 0.4 V or 2 V [f]**	**TEMP. [b]**	**TYP. [d]**	**D SUFFIX -40 °C to +85 °C**		**UNIT**
					MIN. [c]	**MAX. [c]**	
Analog Switch							
Analog Signal Range [e]	V_{ANALOG}		Full	-	0	3	V
Drain-Source On-Resistance	$R_{DS(on)}$	V+ = 2.7 V, V_D = 0.5 or 2.2 V, I_S = 5 mA	Room	63	-	80	Ω
			Full	-	-	92	
Switch Off Leakage Current [a]	$I_{S(off)}$	V+ = 3.3 V, V_S = 2 or 1 V, V_D = 1 or 2 V	Room	-	-1	1	nA
			Full	-	-5	5	
	$I_{D(off)}$		Room	-	-1	1	
			Full	-	-5	5	
Channel On Leakage Current [a]	$I_{D(on)}$	V+ = 3.3 V, V_D = V_S = 1 V or 2 V sequence each switch on	Room	-	-1	1	
			Full	-	-5	5	
Digital Control							
Logic High Input Voltage	V_{INH}		Full	-	2	-	V
Logic Low Input Voltage	V_{INL}		Full	-	-	0.4	
Input Current [a]	I_{IN}	V_{AX} = V_{EN} = 2.4 V or 0.4 V	Full	-	-1	1	µA
Dynamic Characteristics							
Transition Time	t_{TRANS}	V_{S1} = 1.5 V, V_{S8} = 0 V, (DG408LE) V_{S1b} = 1.5 V, V_{S4b} = 0 V, (DG409LE) see figure 2	Room	211	-	275	ns
			Full	-	-	300	
Break-Before-Make Time	t_{OPEN}	$V_{S(all)}$ = V_{DA} = 1.5 V, see figure 4	Room	209	1	-	
			Full	-	-	-	
Enable Turn-On Time	$t_{ON(EN)}$	V_{AX} = 0 V, V_{S1} = 1.5 V (DG408LE) V_{AX} = 0 V, V_{S1b} = 1.5 V (DG409LE) see figure 3	Room	125	-	150	
			Full	-	-	180	
Enable Turn-Off Time	$t_{OFF(EN)}$		Room	45	-	75	
			Full	-	-	95	
Charge Injection [e] (DG408LE)	Q	C_L = 1 nF, R_{GEN} = 0 Ω, V_{GEN} = 1.5 V	Room	0	-	-	pC
Charge Injection [e] (DG409LE)			Room	-0.4	-	-	
Off Isolation [e, h] (DG408LE)	OIRR	f = 100 kHz, R_L = 50 Ω	Room	-90	-	-	dB
Off Isolation [e, h] (DG409LE)			Room	-95	-	-	
Crosstalk [e] (DG408LE)	X_{TALK}		Room	-95	-	-	
Crosstalk [e] (DG409LE)			Room	-93	-	-	
Source Off Capacitance [e] (DG408LE)	$C_{S(off)}$	f = 1 MHz, V_S = 0 V, V_{EN} = 0 V	Room	7	-	-	pF
Source Off Capacitance [e] (DG409LE)			Room	7	-	-	
Drain Off Capacitance [e] (DG408LE)	$C_{D(off)}$	f = 1 MHz, V_D = 0 V, V_{EN} = 0 V	Room	33	-	-	
Drain Off Capacitance [e] (DG409LE)			Room	18	-	-	
Drain On Capacitance [e] (DG408LE)	$C_{D(on)}$	f = 1 MHz, V_D = 0 V, V_{EN} = 2 V	Room	43	-	-	
Drain On Capacitance [e] (DG409LE)			Room	28	-	-	

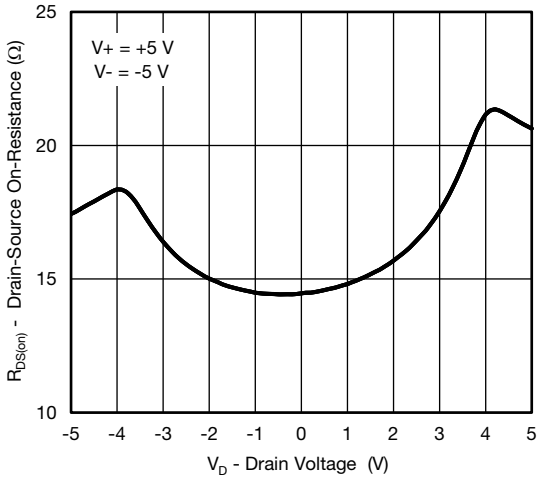
Notes

a. Leakage parameters are guaranteed by worst case test condition and not subject to production test.
b. Room = 25 °C, full = as determined by the operating temperature suffix.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta R_{DS(on)} = R_{DS(on)}$ max. - $R_{DS(on)}$ min.
h. Worst case isolation occurs on channel 4 do to proximity to the drain pin.

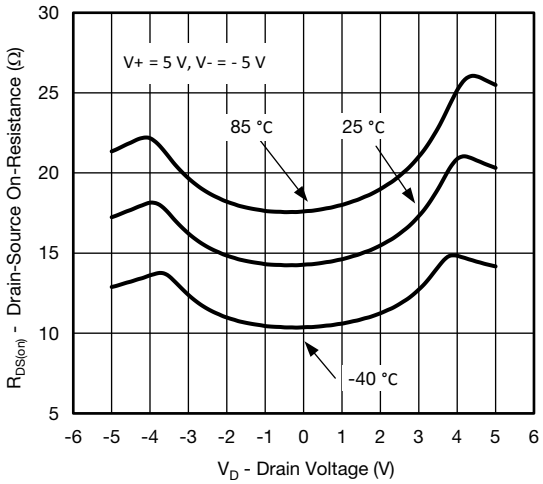
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



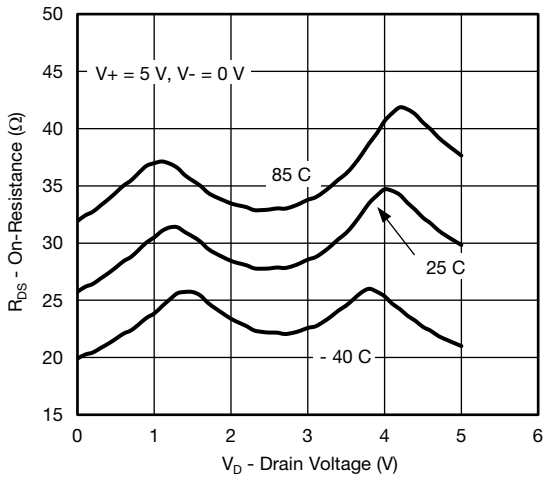
$R_{DS(on)}$ vs. V_D and Power Supply



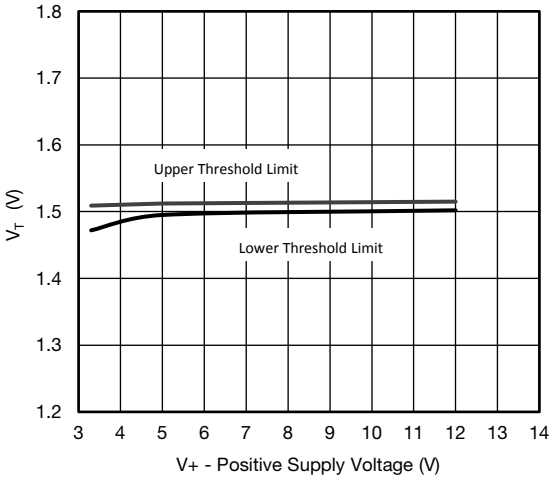
$R_{DS(on)}$ vs. V_D and Power Supply



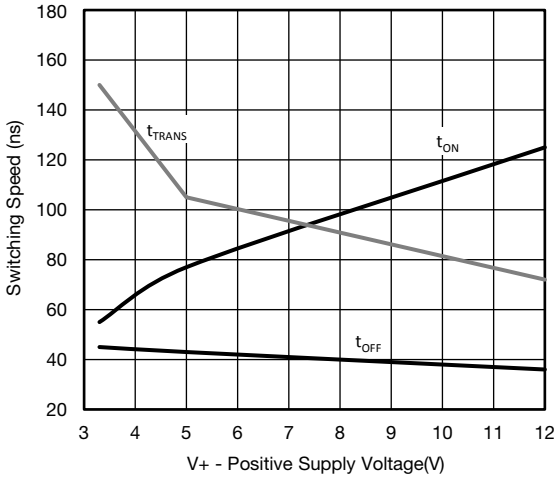
$R_{DS(on)}$ vs. V_D and Temperature (Dual Supply)



$R_{DS(on)}$ vs. V_D and Temperature

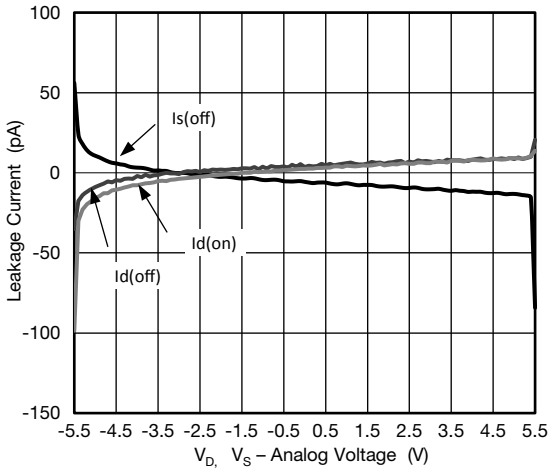


Input Threshold vs. V+ Supply Voltage

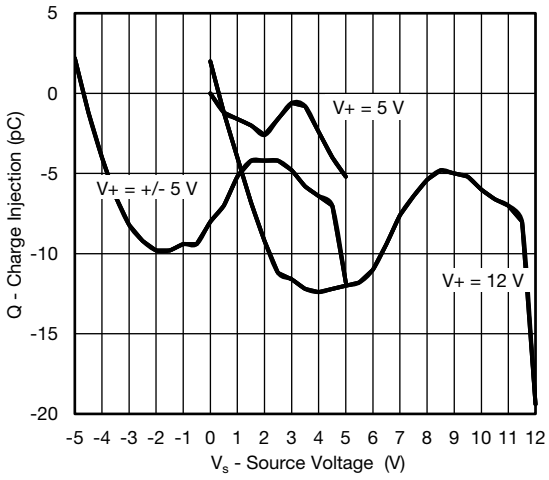


Switching Time vs. Supply Voltage

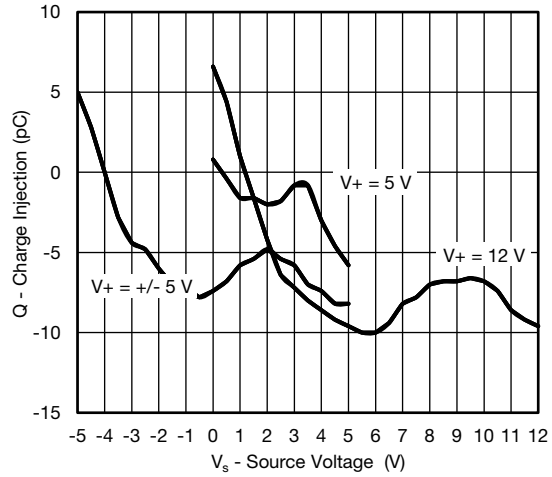
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



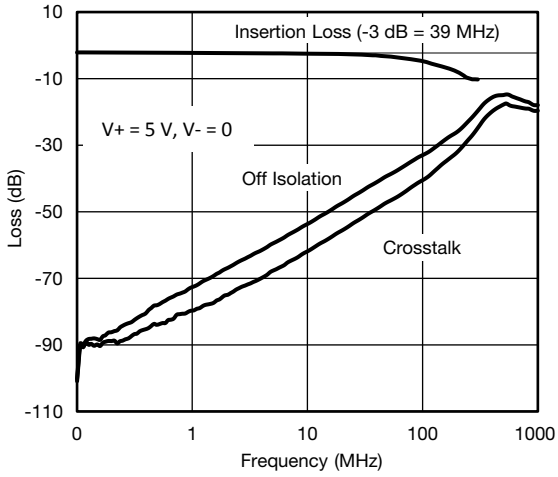
Leakage Current vs. Analog Voltage



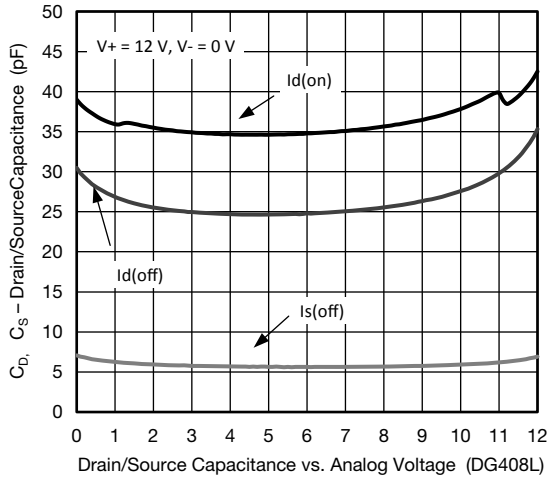
Charge Injection vs. Analog Voltage (DG408LE)



Charge Injection vs. Analog Voltage (DG409LE)



Insertion Loss, Off Isolation, and Crosstalk vs. Frequency



Drain/Source Capacitance vs. Analog Voltage (DG408LE)

SCHEMATIC DIAGRAM (Typical Channel)

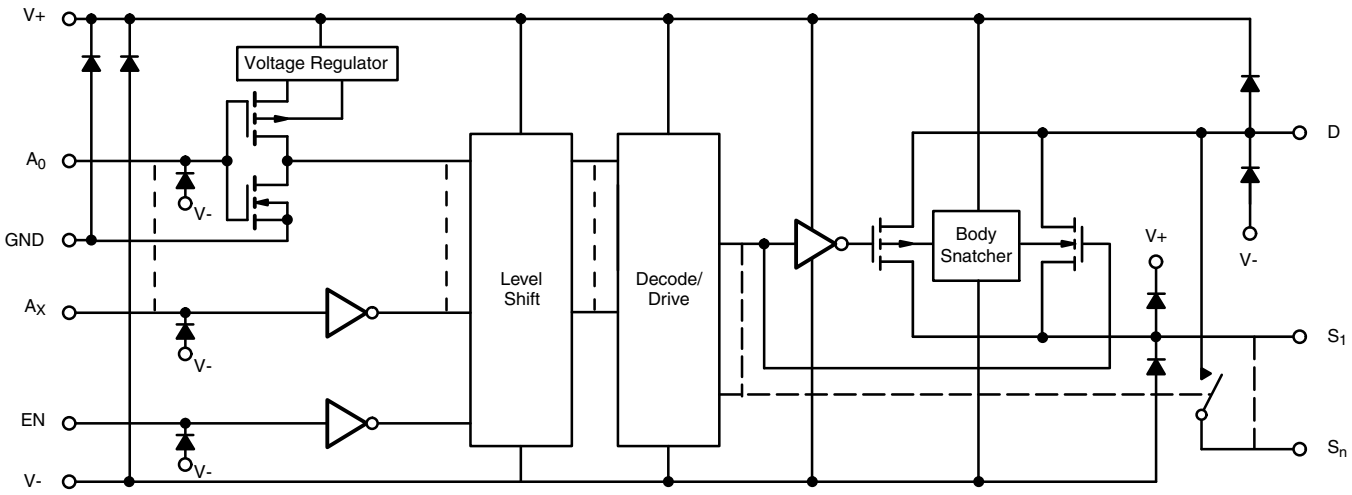
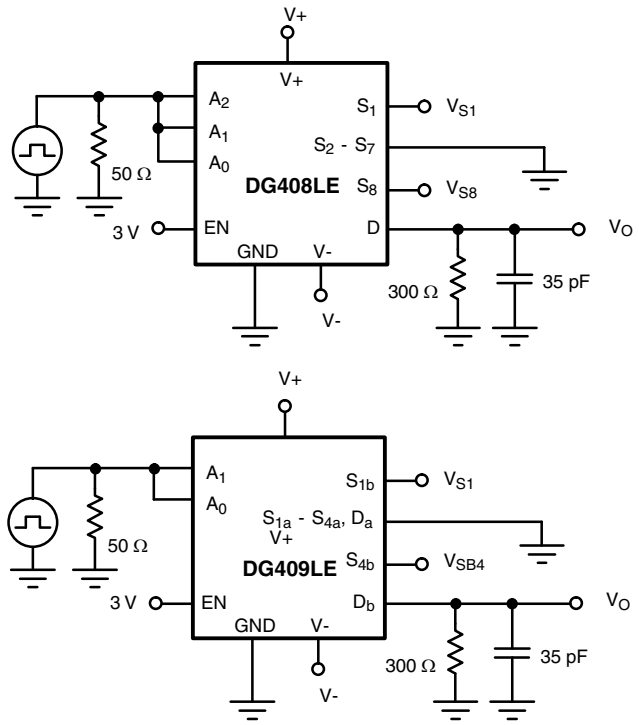


Fig. 1

TEST CIRCUITS



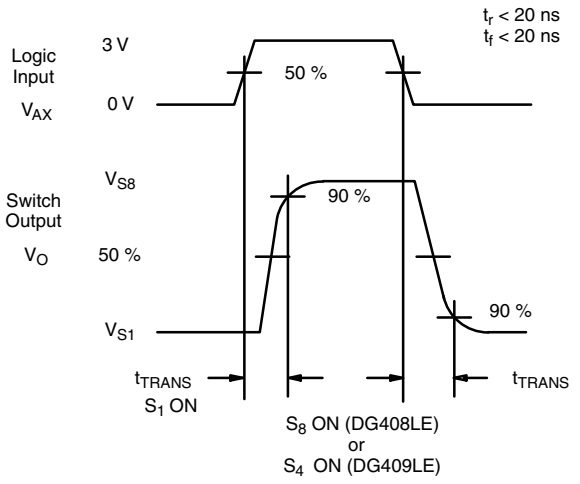


Fig. 2 - Transition Time

TEST CIRCUITS

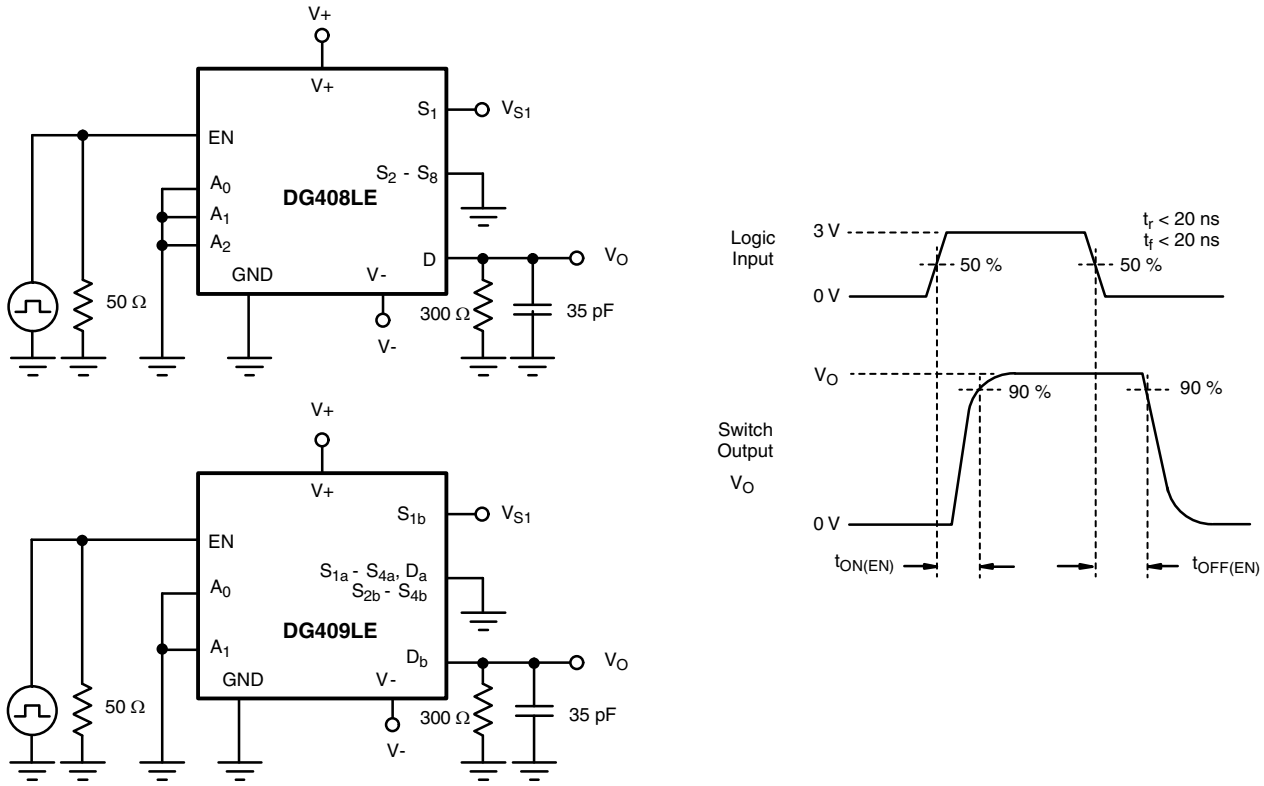


Fig. 3 - Enable Switching Time

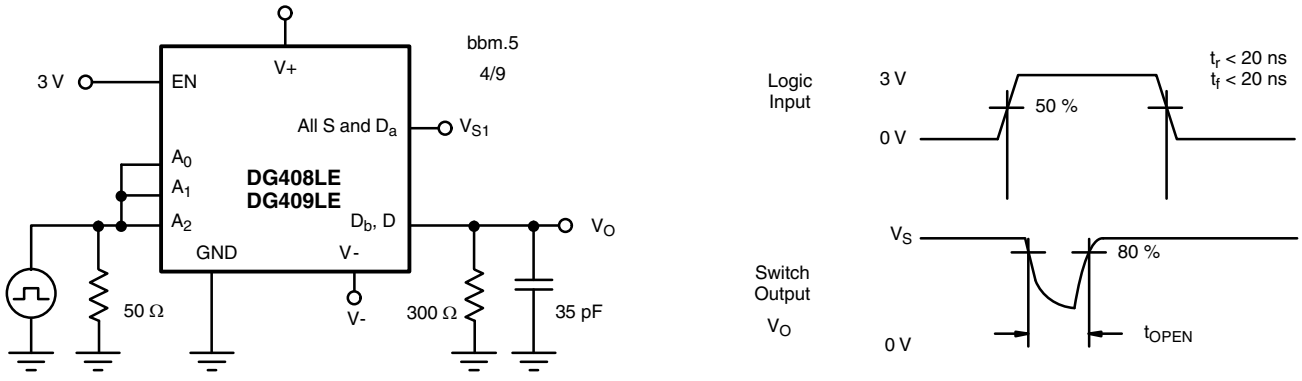


Fig. 4 - Break-Before-Make Interval

TEST CIRCUITS

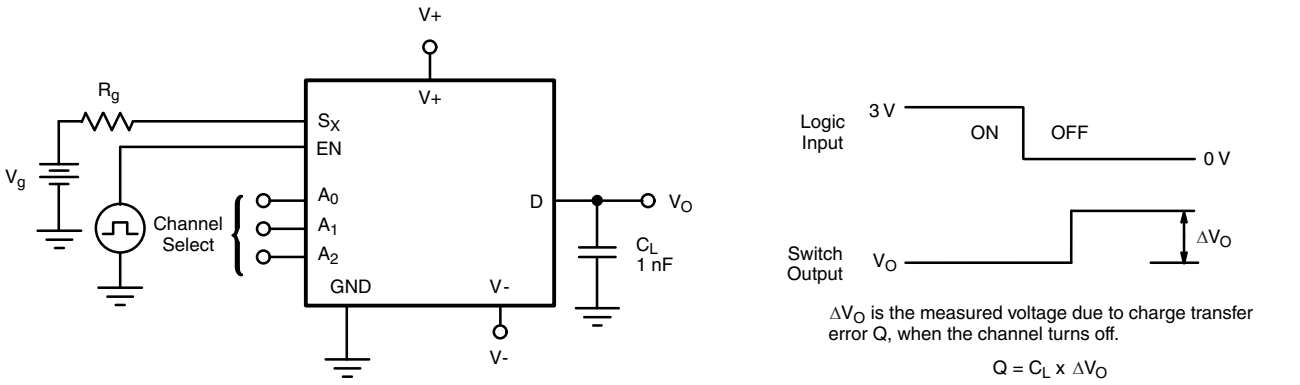


Fig. 5 - Charge Injection

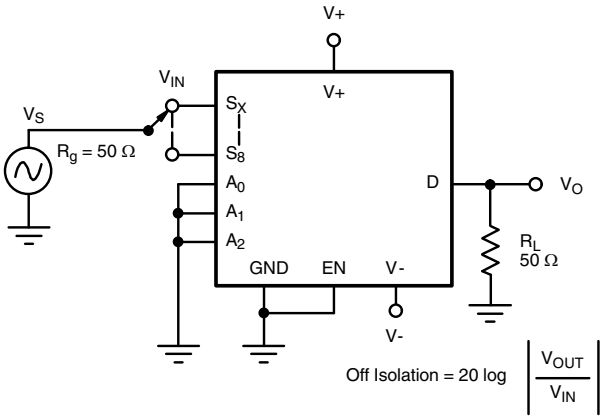


Fig. 6 - Off Isolation

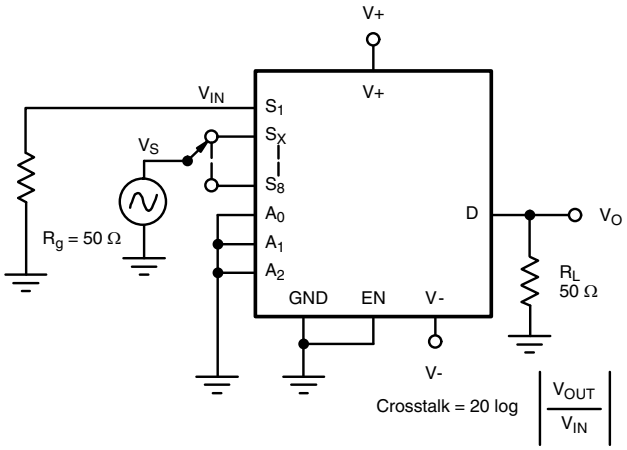


Fig. 7 - Crosstalk

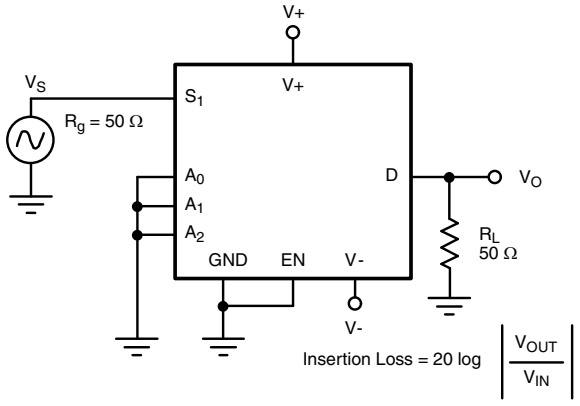


Fig. 8 - Insertion Loss

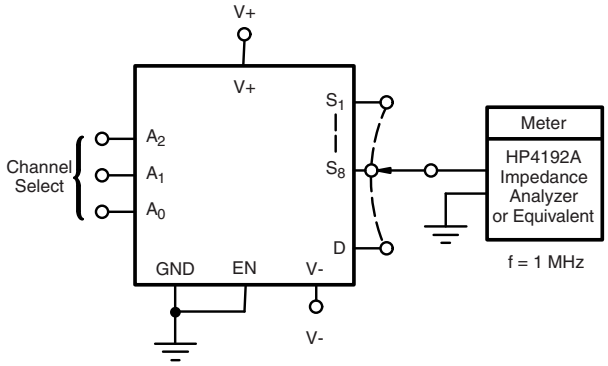


Fig. 9 - Source Drain Capacitance

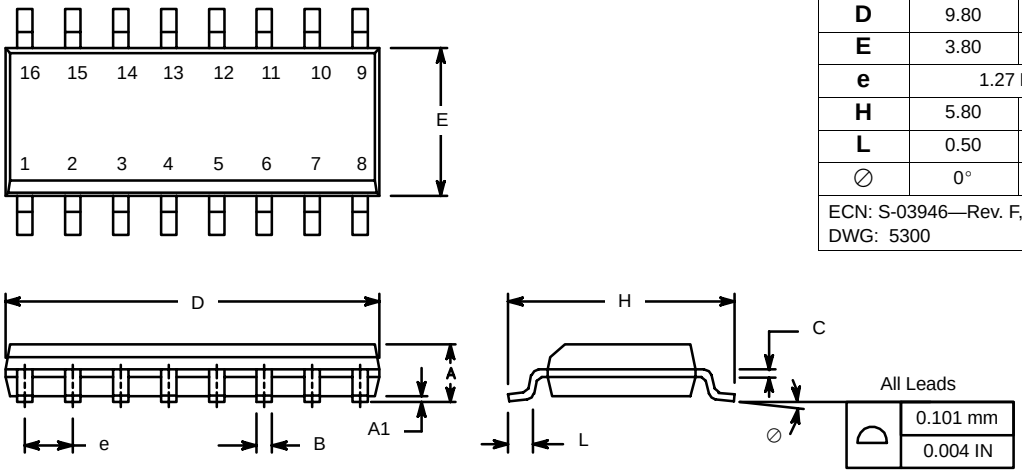
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?78084.

SOIC (NARROW): 16-LEAD

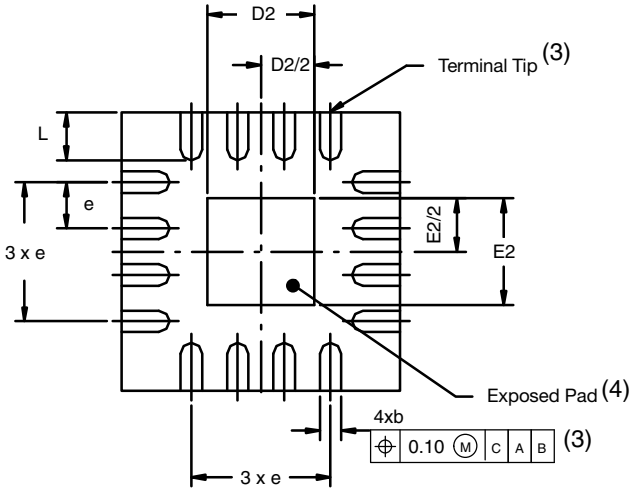
JEDEC Part Number: MS-012

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
⊘	0°	8°	0°	8°

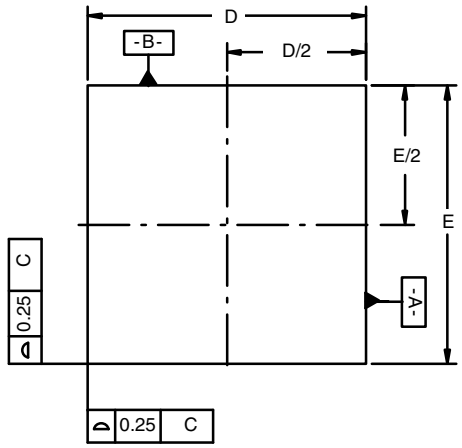
ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300



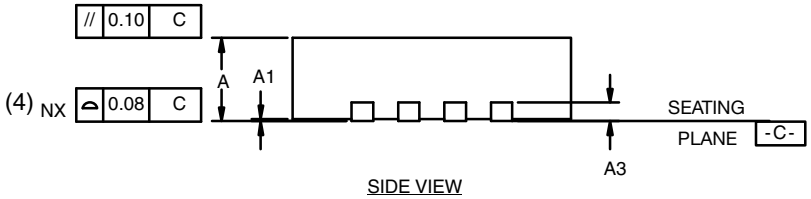
QFN-16 Lead (3 x 3)



BOTTOM VIEW



TOP VIEW



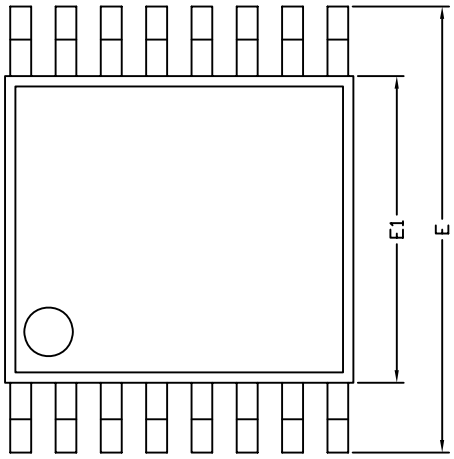
SIDE VIEW

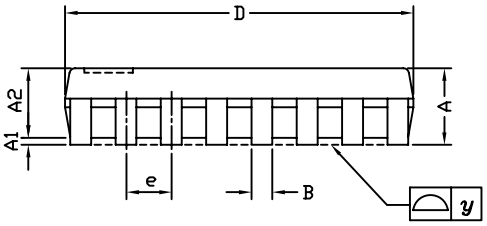
Notes

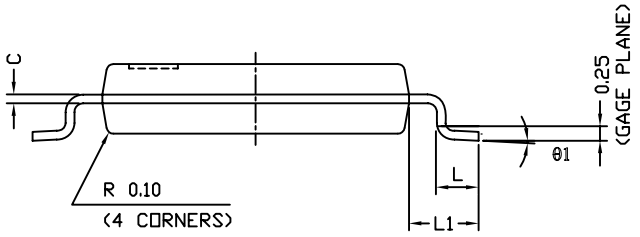
(1) All dimensions are in millimeters.
(2) N is the total number of terminals.
(3) Dimension b applies to metallized terminal and is measured between 0.25 and 0.30 mm from terminal tip.
(4) Coplanarity applies to the exposed heat sink slug as well as the terminal.
(5) The pin #1 identifier may be either a mold or marked feature, it must be located within the zone indicated.

DIM.	VARIATION 1						VARIATION 2					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	0.80	0.90	1.00	0.031	0.035	0.039	0.80	0.90	1.00	0.031	0.035	0.039
b	0.18	0.23	0.30	0.007	0.009	0.012	0.18	0.25	0.30	0.007	0.010	0.012
D	2.90	3.00	3.10	0.114	0.118	0.122	2.90	3.00	3.10	0.114	0.118	0.122
D2	1.00	1.15	1.25	0.039	0.045	0.049	1.50	1.70	1.80	0.059	0.067	0.071
E	2.90	3.00	3.10	0.114	0.118	0.122	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.00	1.15	1.25	0.039	0.045	0.049	1.50	1.70	1.80	0.059	0.067	0.071
e	0.50 BSC			0.020 BSC			0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020	0.30	0.40	0.50	0.012	0.016	0.020
ECN: T16-0233-Rev. D, 09-May-16 DWG: 5899												

TSSOP: 16-LEAD

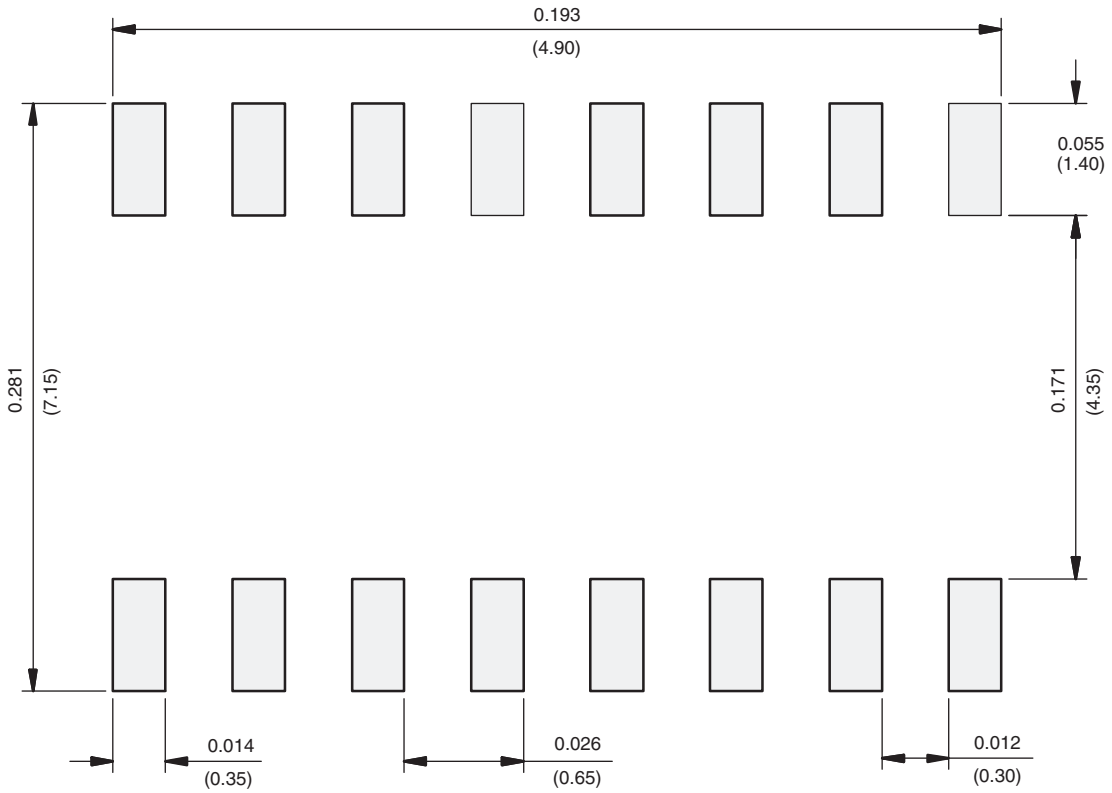






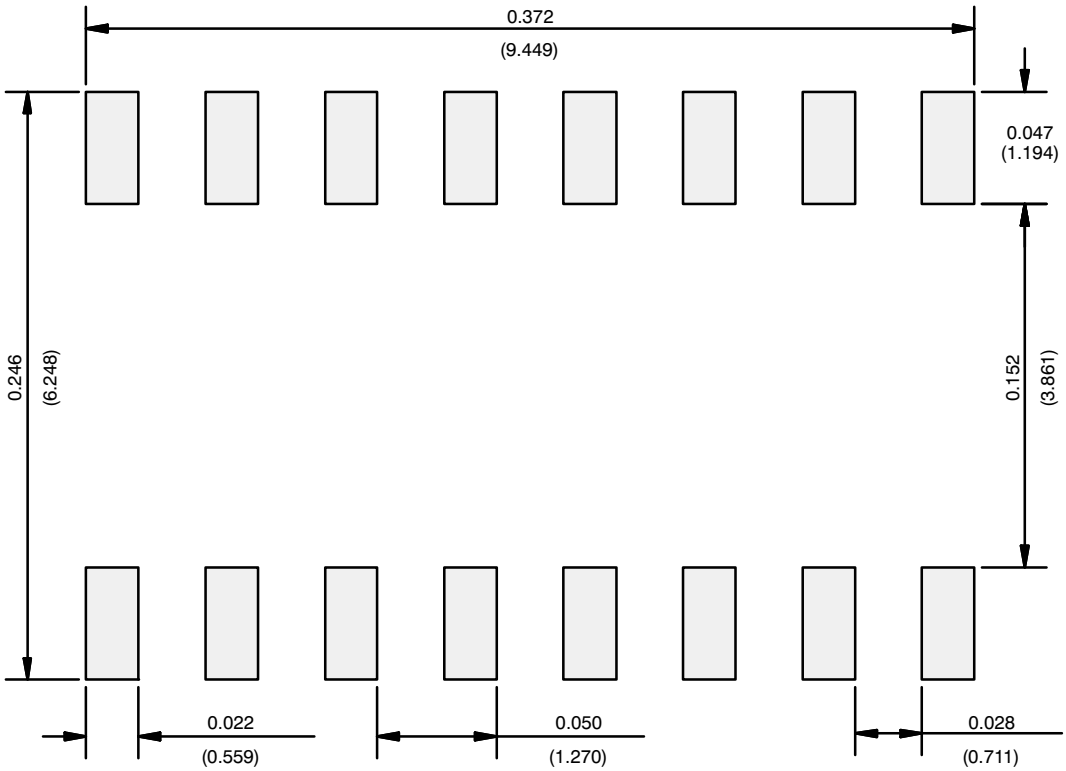
Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06 DWG: 5624			

RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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