



PRMH11

50 V, 100 mA NPN/NPN Resistor-Equipped double Transistors (RET)

14 September 2018

Product data sheet

1. General description

NPN/NPN Resistor-Equipped double Transistors (RET) in an ultra small DFN1412-6 (SOT1268) leadless Surface-Mounted Device (SMD) plastic package.

PNP/PNP complement: PRMB11.

NPN/PNP complement: PRMD3.

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Low package height of 0.5 mm
- AEC-Q101 qualified

3. Applications

- Digital applications
- Cost-saving alternative to BC847/BC857 series in digital applications
- Control of IC inputs
- Switching loads

4. Quick reference data

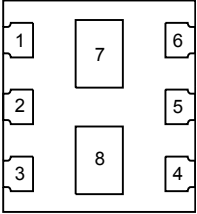
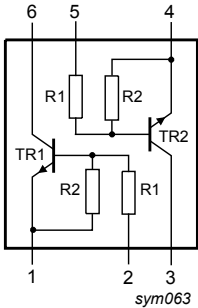
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
I_O	output current		-	-	100	mA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 5\text{ mA}; T_{amb} = 25\text{ °C}$	30	-	-	
R1	bias resistor 1	$T_{amb} = 25\text{ °C}$	[1]	7	10	13 kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	1.2

[1] See section "Test information" for resistor calculation and test conditions.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 Transparent top view DFN1412-6 (SOT1268)	 sym063
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		
7	O1	output (collector) TR1		
8	O2	output (collector) TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PRMH11	DFN1412-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body: 1.4 mm x 1.2 mm x 0.47 mm	SOT1268

7. Marking

Table 4. Marking codes

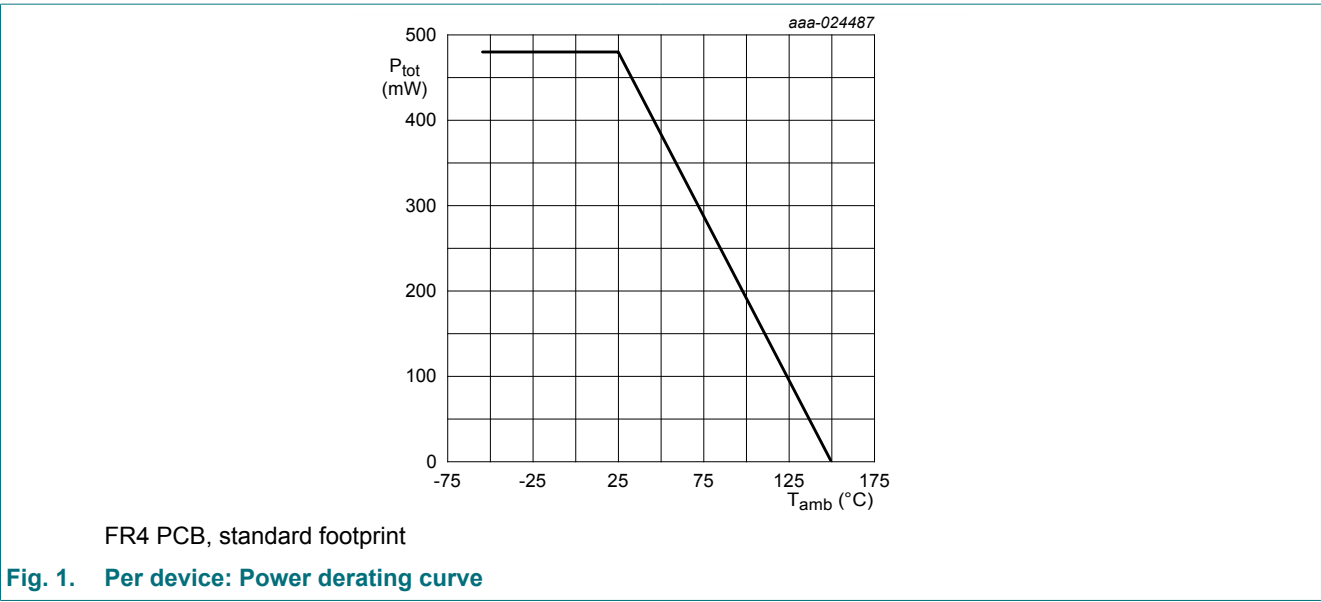
Type number	Marking code
PRMH11	B9

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	10	V
V _I	input voltage	positive		-	40	V
		negative		-	-10	V
I _O	output current			-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	325	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	480	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

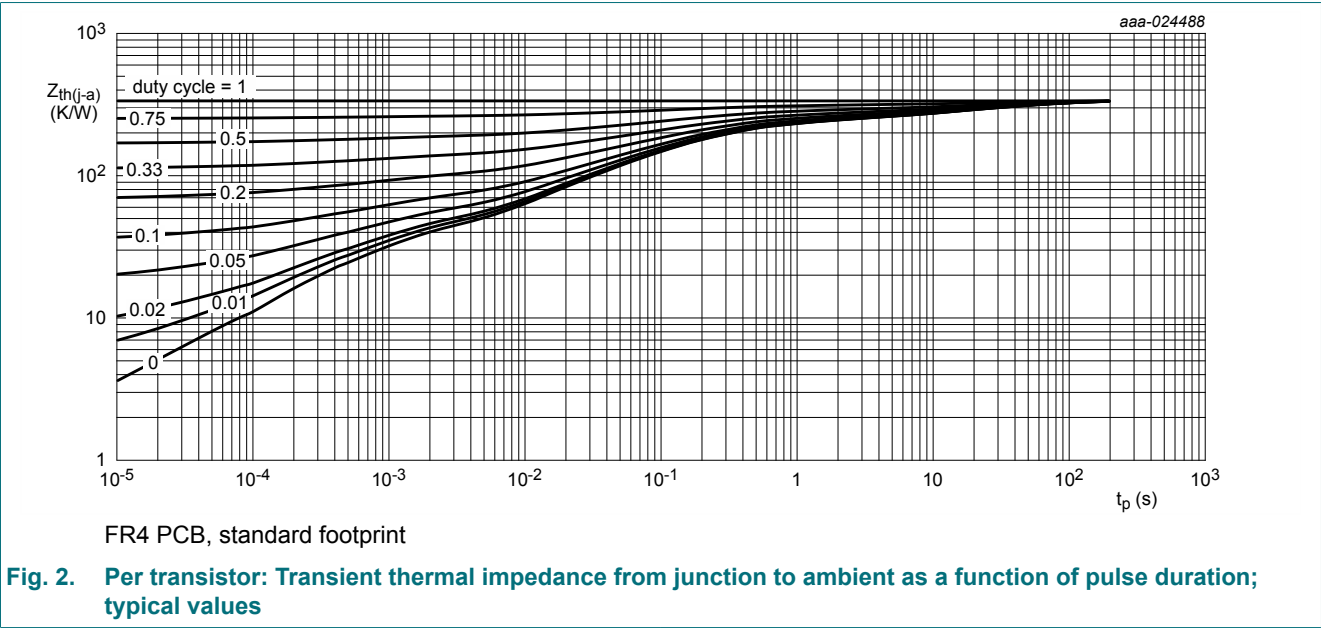


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	385	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	261	K/W

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



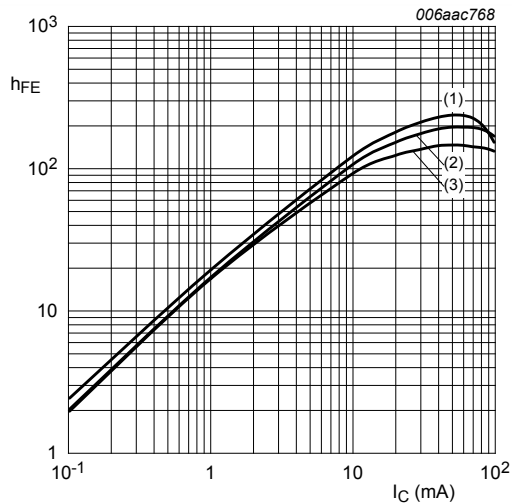
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30 \text{ V}; I_B = 0 \text{ A}; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	-	1	μA
		$V_{CE} = 30 \text{ V}; I_B = 0 \text{ A}; T_j = 150 \text{ }^{\circ}\text{C}$		-	-	5	μA
I_{CBO}	collector-base cut-off current	$V_{CB} = 50 \text{ V}; I_E = 0 \text{ A}; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	-	100	nA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_C = 0 \text{ A}; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	-	400	μA
h_{FE}	DC current gain	$V_{CE} = 5 \text{ V}; I_C = 5 \text{ mA}; T_{amb} = 25 \text{ }^{\circ}\text{C}$		30	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10 \text{ mA}; I_B = 0.5 \text{ mA}; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	-	150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5 \text{ V}; I_C = 100 \text{ } \mu\text{A}; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	1.1	0.8	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3 \text{ V}; I_C = 10 \text{ mA}; T_{amb} = 25 \text{ }^{\circ}\text{C}$		2.5	1.8	-	V
R1	bias resistor 1	$T_{amb} = 25 \text{ }^{\circ}\text{C}$	[1]	7	10	13	k Ω
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	
C_C	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = 0 \text{ A}; i_e = 0 \text{ A}; f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^{\circ}\text{C}$		-	-	2.5	pF
f_T	transition frequency	$V_{CE} = 5 \text{ V}; I_C = 10 \text{ mA}; f = 100 \text{ MHz}; T_{amb} = 25 \text{ }^{\circ}\text{C}$	[2]	-	230	-	MHz

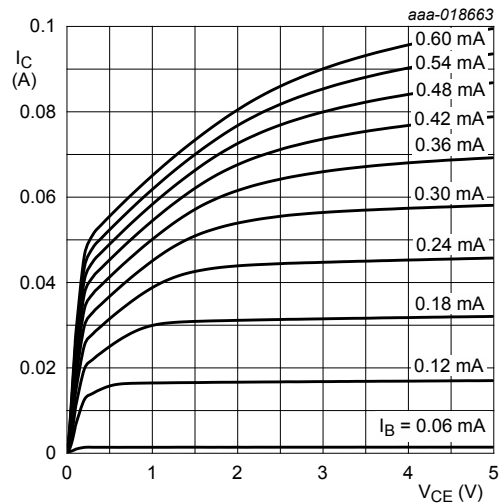
[1] See section "Test information" for resistor calculation and test conditions.

[2] Characteristics of built-in transistor



$V_{CE} = 5 \text{ V}$
 (1) $T_{amb} = 100 \text{ }^{\circ}\text{C}$
 (2) $T_{amb} = 25 \text{ }^{\circ}\text{C}$
 (3) $T_{amb} = -40 \text{ }^{\circ}\text{C}$

Fig. 3. DC current gain as a function of collector current; typical values



$T_{amb} = 25 \text{ }^{\circ}\text{C}$

Fig. 4. Collector current as a function of collector-emitter voltage; typical values

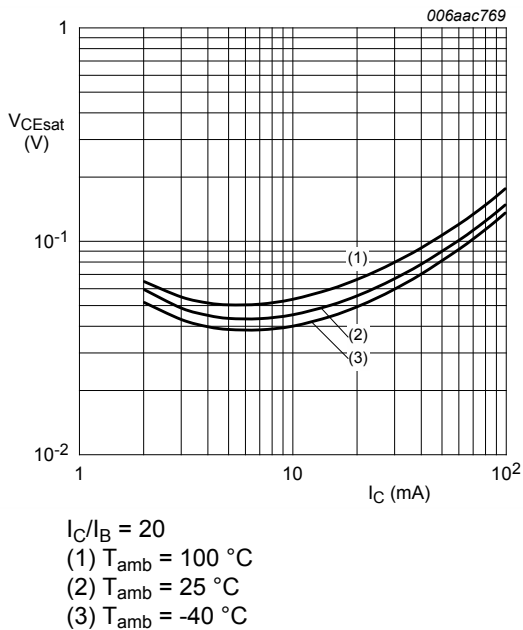


Fig. 5. Collector-emitter saturation voltage as a function of collector current; typical values

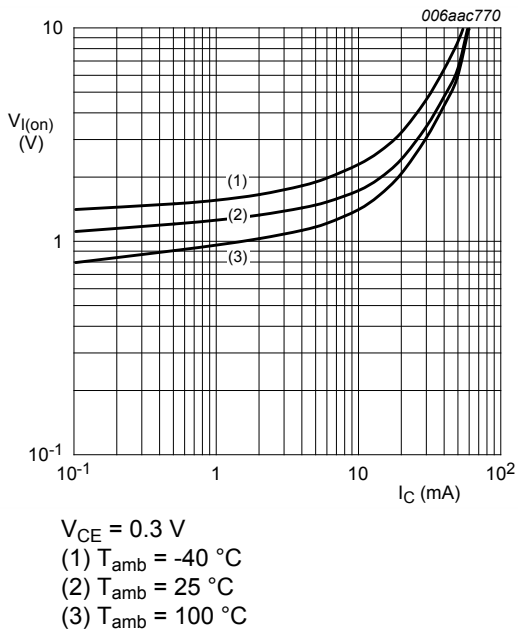


Fig. 6. On-state input voltage as a function of collector current; typical values

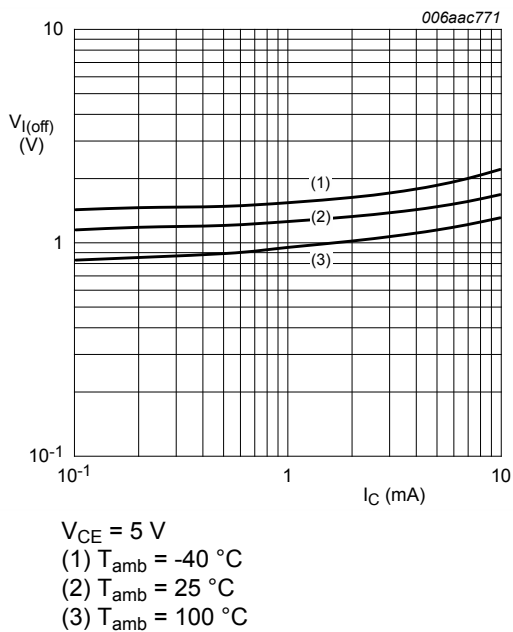


Fig. 7. Off-state input voltage as a function of collector current; typical values

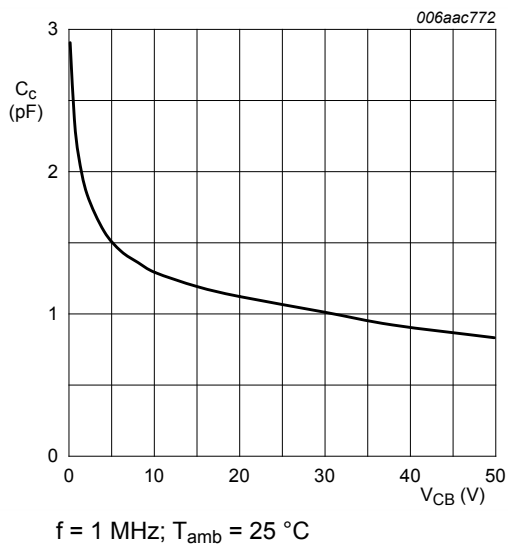
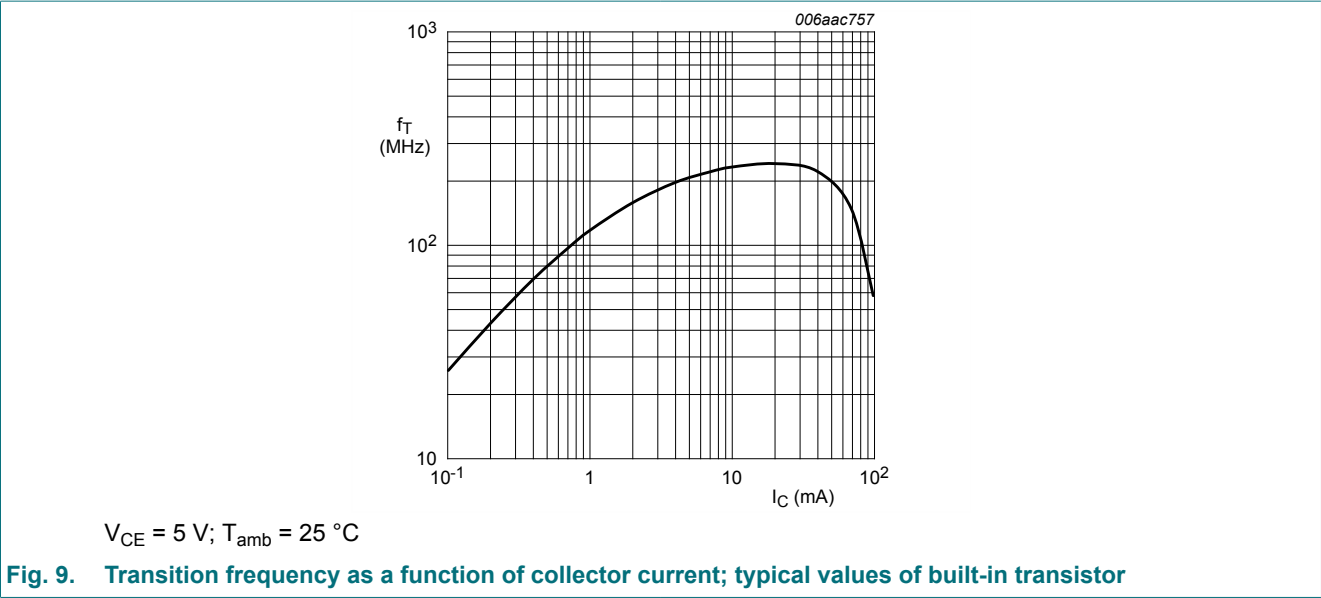


Fig. 8. Collector capacitance as a function of collector-base voltage; typical values

50 V, 100 mA NPN/NPN Resistor-Equipped double Transistors (RET)



11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

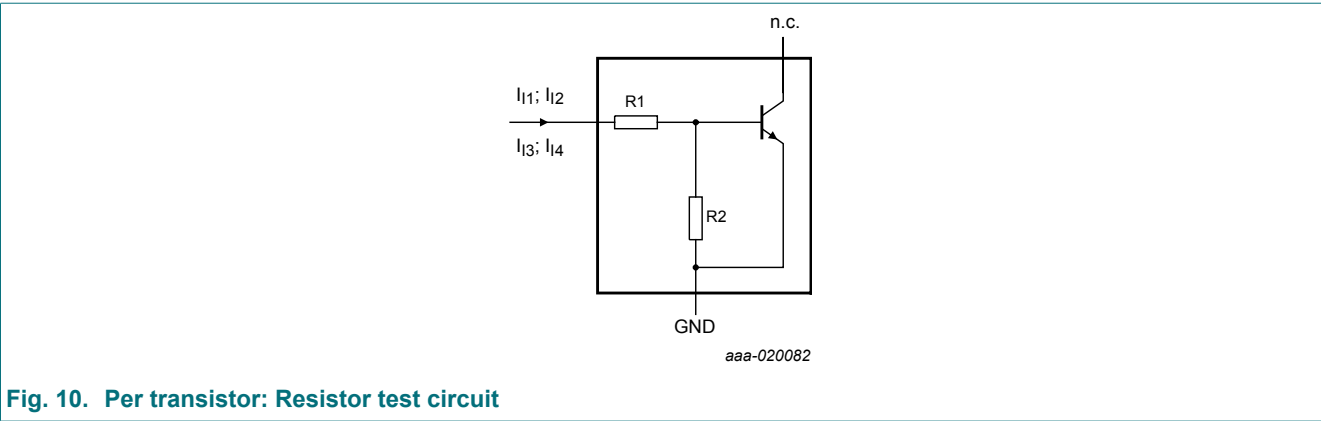
Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R1 = \frac{V(I12) - V(I11)}{I12 - I11}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I14) - V(I13)}{R1 \cdot (I14 - I13)} - 1$$



Resistor test conditions

Table 8. Resistor test conditions

R1 (kΩ)	R2 (kΩ)	Test conditions			
		I11	I12	I13	I14
10	10	350 μA	450 μA	-350 μA	-450 μA

12. Package outline

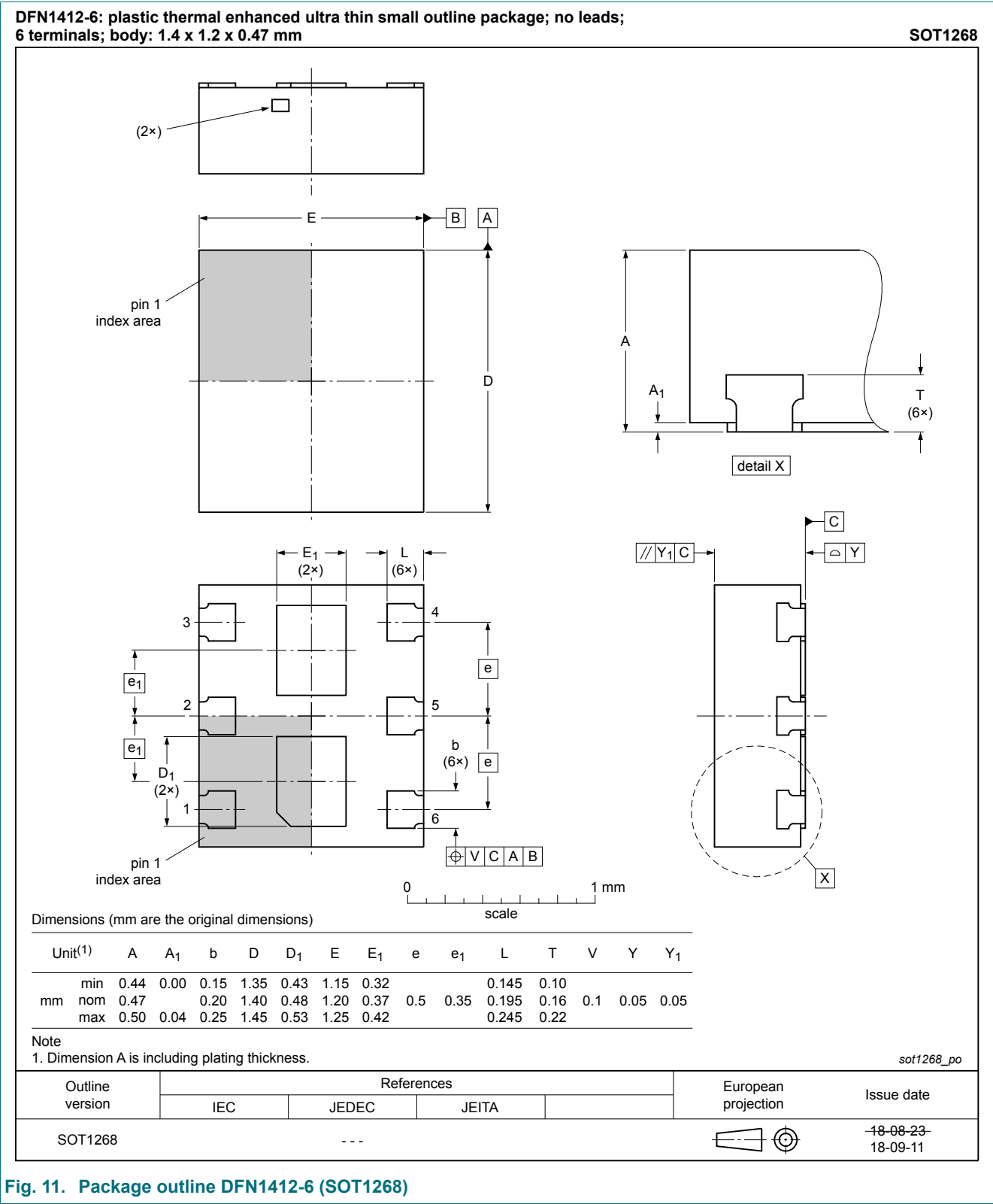


Fig. 11. Package outline DFN1412-6 (SOT1268)

13. Soldering

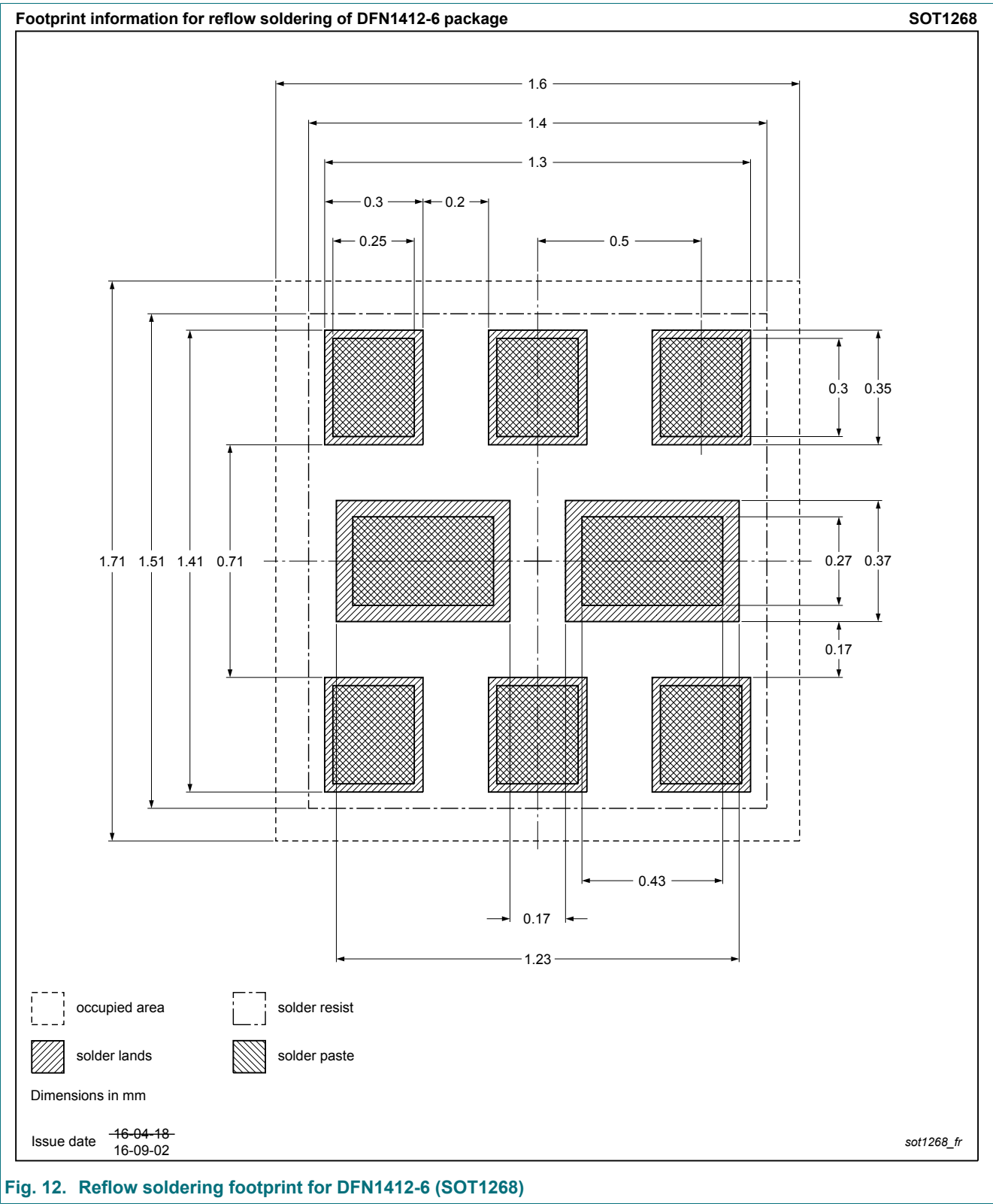


Fig. 12. Reflow soldering footprint for DFN1412-6 (SOT1268)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PRMH11 v.2	20180914	Product data sheet	-	PRMH11 v.1
Modifications:	• Package outline drawing updated: Unit T added			
PRMH11 v.1	20170814	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Applications..... 1

4. Quick reference data..... 1

5. Pinning information.....2

6. Ordering information.....2

7. Marking.....2

8. Limiting values..... 3

9. Thermal characteristics..... 4

10. Characteristics..... 5

11. Test information..... 8

12. Package outline..... 9

13. Soldering..... 10

14. Revision history..... 11

15. Legal information..... 12

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