30 A VRPower® Integrated Power Stage

DESCRIPTION

The SiC521 and SiC521A are integrated power stage solutions optimized for synchronous buck applications to offer high current, high efficiency, and high power density performance. Packaged in Vishay's proprietary 4.5 mm x 3.5 mm MLP package, SiC521 and SiC521A enable voltage regulator designs to deliver up to 30 A continuous current per phase.

The internal power MOSFETs utilize Vishay's state-of-the-art Gen IV TrenchFET technology that delivers industry benchmark performance to significantly reduce switching and conduction losses.

The SiC521 and SiC521A incorporate an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, an integrated bootstrap Schottky diode, and zero current detect to improve light load efficiency. The drivers are also compatible with a wide range of PWM controllers, support tri-state PWM, and 3.3 V (SiC521A) / 5 V (SiC521) PWM logic.

FEATURES

RoHS COMPLIANT HALOGEN FREE

- Thermally enhanced PowerPAK® MLP4535-22L package
- Vishay's Gen IV MOSFET technology and a low-side MOSFET with integrated Schottky diode
- Delivers up to 30 A continuous current, 40 A at 10 ms peak current
- 95 % peak efficiency
- High frequency operation up to 1.5 MHz
- Power MOSFETs optimized for 12 V input stage
- 3.3 V (SiC521A) / 5 V (SiC521) PWM logic with tri-state and hold-off
- Zero current detect control for light load efficiency improvement
- Low PWM propagation delay (< 20 ns)
- Under voltage lockout for V_{CIN}
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Multi-phase VRDs for CPU, GPU, and memory
- Synchronous buck converters
- DC/DC VR modules

TYPICAL APPLICATION DIAGRAM

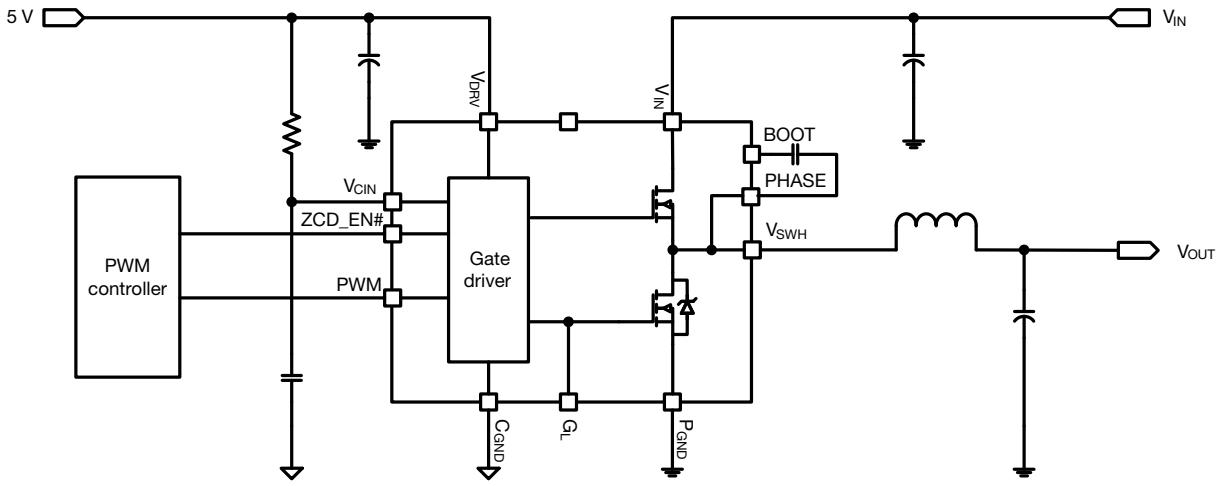

Fig. 1 - SiC521 and SiC521A Typical Application Diagram

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PINOUT CONFIGURATION

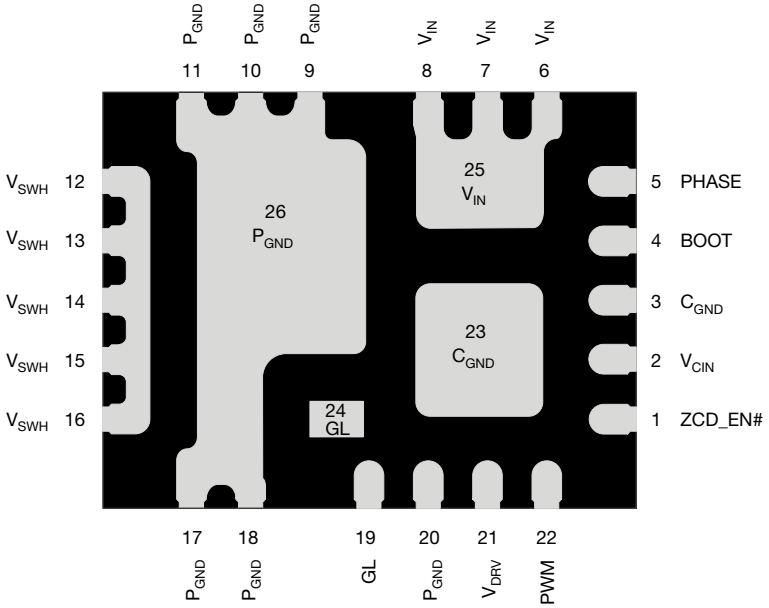

Fig. 2 - SiC521 and SiC521A Pin Configuration

PIN DESCRIPTION		
PIN NUMBER	**NAME**	**FUNCTION**
1	ZCD_EN#	ZCD control. Active low
2	V_{CIN}	Supply voltage for internal logic circuitry
3, 23	C_{GND}	Analog ground for the driver IC
4	BOOT	High-side driver bootstrap voltage
5	PHASE	Return path of high-side gate driver
6 to 8, 25	V_{IN}	Power stage input voltage. Drain of high-side MOSFET
9 to 11, 17, 18, 20, 26	P_{GND}	Power ground
12 to 16	V_{SWH}	Switch node of the power stage
19, 24	GL	Low-side gate signal
21	V_{DRV}	Supply voltage for internal gate driver
22	PWM	PWM control input

ORDERING INFORMATION			
PART NUMBER	**PACKAGE**	**MARKING CODE**	
SiC521CD-T1-GE3	PowerPAK® MLP4535-22L	SiC521	5 V PWM optimized
SiC521ACD-T1-GE3		SiC521A	3.3 V PWM optimized
SiC521ADB and SiC521DB	Reference board		

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ABSOLUTE MAXIMUM RATINGS			
ELECTRICAL PARAMETER	**CONDITIONS**	**LIMIT**	**UNIT**
Input Voltage	V_{IN}	-0.3 to +25	V
Control Logic Supply Voltage	V_{CIN}	-0.3 to +7	
Drive Supply Voltage	V_{DRV}	-0.3 to +7	
Switch Node (DC voltage)	V_{SWH}	-0.3 to +25	
Switch Node (AC voltage) (1)		-8 to +30	
BOOT Voltage (DC voltage)	V_{BOOT}	32	
BOOT Voltage (AC voltage) (2)		38	
BOOT to PHASE (DC voltage)	$V_{BOOT- PHASE}$	-0.3 to +7	
BOOT to PHASE (AC voltage) (3)		-0.3 to +8	
All Logic Inputs and Outputs (PWM and ZCD_EN#)		-0.3 to V_{CIN} + 0.3	
Output Current, $I_{OUT(AV)}$ (4)	f_S = 300 kHz, V_{IN} = 12 V, V_{OUT} = 1.8 V	30	A
	f_S = 1 MHz, V_{IN} = 12 V, V_{OUT} = 1.8 V	25	
Max. Operating Junction Temperature	T_J	150	°C
Ambient Temperature	T_A	-40 to +125	
Storage Temperature	T_{stg}	-65 to +150	
Electrostatic Discharge Protection	Human body model, JESD22-A114	3000	V
	Charged device model, JESD22-C101	1000	

Note

(1) The specification values indicated "AC" is V_{SWH} to P_{GND}, -8 V (< 20 ns, 10 µJ), min. and 30 V (< 50 ns), max.

(2) The specification value indicates "AC voltage" is V_{BOOT} to P_{GND}, 36 V (< 50 ns) max.

(3) The specification value indicates "AC voltage" is V_{BOOT} to V_{PHASE}, 8 V (< 20 ns) max.

(4) Output current rated with testing evaluation board at T_A = 25 °C with natural convection cooling. The rating is limited by the peak evaluation board temperature, T_J = 150 °C, and varies depending on the operating conditions and PCB layout. This rating may be changed with different application settings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE				
ELECTRICAL PARAMETER	**MINIMUM**	**TYPICAL**	**MAXIMUM**	**UNIT**
Input Voltage (V_{IN})	4.5	-	18	V
Drive Supply Voltage (V_{DRV})	4.5	5	5.5	
Control Logic Supply Voltage (V_{CIN})	4.5	5	5.5	
BOOT to PHASE ($V_{BOOT-PHASE}$, DC voltage)	4	4.5	5.5	
Thermal Resistance from Junction to PCB	-	5	-	°C/W
Thermal Resistance from Junction to Case	-	2.5	-	

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ELECTRICAL SPECIFICATIONS

(ZCD_EN# = 5 V, V_{IN} = 12 V, V_{DRV} and V_{CIN} = 5 V, T_A = 25 °C)

PARAMETER	SYMBOL	TEST CONDITION	LIMITS			UNIT
			MIN.	TYP.	MAX.	
POWER SUPPLY						
Control Logic Supply Current	I_{VCIN}	no switching, V_{PWM} = FLOAT	-	300	-	µA
		f_S = 300 kHz, D = 0.1	-	300	-	
Drive Supply Current	I_{VDRV}	f_S = 300 kHz, D = 0.1	-	8	15	mA
		f_S = 1 MHz, D = 0.1	-	30	-	
		no switching, V_{PWM} = FLOAT	-	50	-	µA
BOOTSTRAP SUPPLY						
Bootstrap Diode Forward Voltage	V_F	I_F = 2 mA	-	-	0.4	V
PWM CONTROL INPUT (SiC521)						
Rising Threshold	$V_{TH_PWM_R}$		3.4	3.7	4.0	V
Falling Threshold	$V_{TH_PWM_F}$		0.72	0.9	1.1	
Tri-state Voltage	V_{TRI}	V_{PWM} = FLOAT	-	2.3	-	
Tri-state Rising Threshold	$V_{TRI_TH_R}$		0.9	1.15	1.38	
Tri-state Falling Threshold	$V_{TRI_TH_F}$		3.1	3.35	3.6	
Tri-state Rising Threshold Hysteresis	$V_{HYS_TRI_R}$		-	225	-	mV
Tri-state Falling Threshold Hysteresis	$V_{HYS_TRI_F}$		-	325	-	
PWM Input Current	I_{PWM}	V_{PWM} = 5 V	-	-	350	µA
		V_{PWM} = 0 V	-	-	-350	
PWM CONTROL INPUT (SiC521A)						
Rising Threshold	$V_{TH_PWM_R}$		2.2	2.45	2.7	V
Falling Threshold	$V_{TH_PWM_F}$		0.72	0.9	1.1	
Tri-state Voltage	V_{TRI}	V_{PWM} = FLOAT	-	1.8	-	
Tri-state Rising Threshold	$V_{TRI_TH_R}$		0.9	1.15	1.38	
Tri-state Falling Threshold	$V_{TRI_TH_F}$		1.95	2.2	2.45	
Tri-state Rising Threshold Hysteresis	$V_{HYS_TRI_R}$		-	225	-	mV
Tri-state Falling Threshold Hysteresis	$V_{HYS_TRI_F}$		-	275	-	
PWM Input Current	I_{PWM}	V_{PWM} = 3.3 V	-	-	225	µA
		V_{PWM} = 0 V	-	-	-225	
TIMING SPECIFICATIONS						
Tri-State to GH/GL Rising Propagation Delay	$t_{PD_TRI_R}$	No load, see fig. 4	-	20	-	ns
Tri-state Hold-Off Time	t_{TSHO}		-	150	-	
GH - Turn Off Propagation Delay	$t_{PD_OFF_GH}$		-	20	-	
GH - Turn On Propagation Delay (Dead time rising)	$t_{PD_ON_GH}$		-	10	-	
GL - Turn Off Propagation Delay	$t_{PD_OFF_GL}$		-	20	-	
GL - Turn On Propagation Delay (Dead time falling)	$t_{PD_ON_GL}$		-	10	-	
PWM Minimum On-Time	$t_{PWM_ON_MIN}$		30	-	-	
ZCD_EN# INPUT						
ZCD_EN# Logic Input Voltage	$V_{IH_ZCD_EN\#}$	Input logic high	2	-	-	V
	$V_{IL_ZCD_EN\#}$	Input logic low	-	-	0.8	
PROTECTION						
Under Voltage Lockout	V_{UVLO}	V_{CIN} rising, on threshold	-	3.7	4.1	V
		V_{CIN} falling, off threshold	2.7	3.1	-	
Under Voltage Lockout Hysteresis	V_{UVLO_HYST}		-	575	-	mV

Notes

(1) Typical limits are established by characterization and are not production tested.

(2) Guaranteed by design.

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DETAILED OPERATIONAL DESCRIPTION

PWM Input with Tri-state Function

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate tri-state logic (H, L and tri-state) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is driven above $V_{PWM_TH_R}$ the low-side is turned OFF and the high-side is turned ON. When PWM input is driven below $V_{PWM_TH_F}$ the high-side is turned OFF and the low-side is turned ON. For tri-state logic, the PWM input operates as previously stated for driving the MOSFETs when PWM is logic high and logic low. However, there is a third state that is entered as the PWM output of tri-state compatible controller enters its high impedance state during shut-down. The high impedance state of the controller's PWM output allows the SiC521 and SiC521A to pull the PWM input into the tri-state region (see definition of PWM logic and Tri-State, fig. 4). If the PWM input stays in this region for the Tri-state Hold-Off Period, t_{TSHO}, both high-side and low-side MOSFETs are turned OFF. The function allows the VR phase to be disabled without negative output voltage swing caused by inductor ringing and saves a Schottky diode clamp. The PWM and tri-state regions are separated by hysteresis to prevent false triggering. The SiC521A incorporates PWM voltage thresholds that are compatible with 3.3 V logic and the SiC521 thresholds are compatible with 5 V logic.

Diode Emulation Mode (ZCD_EN#)

When ZCD_EN# pin is logic low and PWM signal switches low, GL is forced ON (after normal BBM time). During this time, it is under control of the ZCD (zero crossing detect) comparator. If, after the internal blanking delay, the inductor current becomes zero, the low-side is turned OFF. This improves light load efficiency by avoiding discharge of output capacitors. If PWM enters tri-state, then device will go into normal tri-state mode after tri-state delay. The GL output will be turned OFF regardless of Inductor current, this is an alternative method of improving light load efficiency by reducing switching losses.

Voltage Input (V_{IN})

This is the power input to the drain of the high-side power MOSFET. This pin is connected to the high power intermediate BUS rail.

Switch Node (V_{SWH} and PHASE)

The switch node, V_{SWH}, is the circuit power stage output. This is the output applied to the power inductor and output filter to deliver the output for the buck converter. The PHASE pin is internally connected to the switch node, V_{SWH}. This pin is to be used exclusively as the return pin for the BOOT capacitor. A 20 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET in the event that V_{CIN} goes to zero while V_{IN} is still applied.

Ground Connections (C_{GND} and P_{GND})

P_{GND} (power ground) should be externally connected to C_{GND} (control signal ground). The layout of the printed circuit board should be such that the inductance separating C_{GND} and P_{GND} is minimized. Transient differences due to inductance effects between these two pins should not exceed 0.5 V.

Control and Drive Supply Voltage Input (V_{DRV}, V_{CIN})

V_{CIN} is the bias supply for the gate drive control IC. V_{DRV} is the bias supply for the gate drivers. It is recommended to separate these pins through a resistor. This creates a low pass filtering effect to avoid coupling of high frequency gate drive noise into the IC.

Bootstrap Circuit (BOOT)

The internal bootstrap diode and an external bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap diode is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a boot strap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin.

Shoot-Through Protection and Adaptive Dead Time

The SiC521 and SiC521A have an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high-side and low-side MOSFETs are not turned ON at the same time. The adaptive dead time control operates as follows. The high-side and low-side gate voltages are monitored to prevent the MOSFET turning ON from tuning ON until the other MOSFET's gate voltage is sufficiently low (< 1 V). Built in delays also ensure that one power MOSFET is completely OFF, before the other can be turned ON. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.

Under Voltage Lockout (UVLO)

During the start up cycle, the UVLO disables the gate drive, holding high-side and low-side MOSFET gates low, until the supply voltage rail has reached a point at which the logic circuitry can be safely activated. The SiC521 and SiC521A also incorporate logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device. As an added precaution, a 20 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET.

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FUNCTIONAL BLOCK DIAGRAM

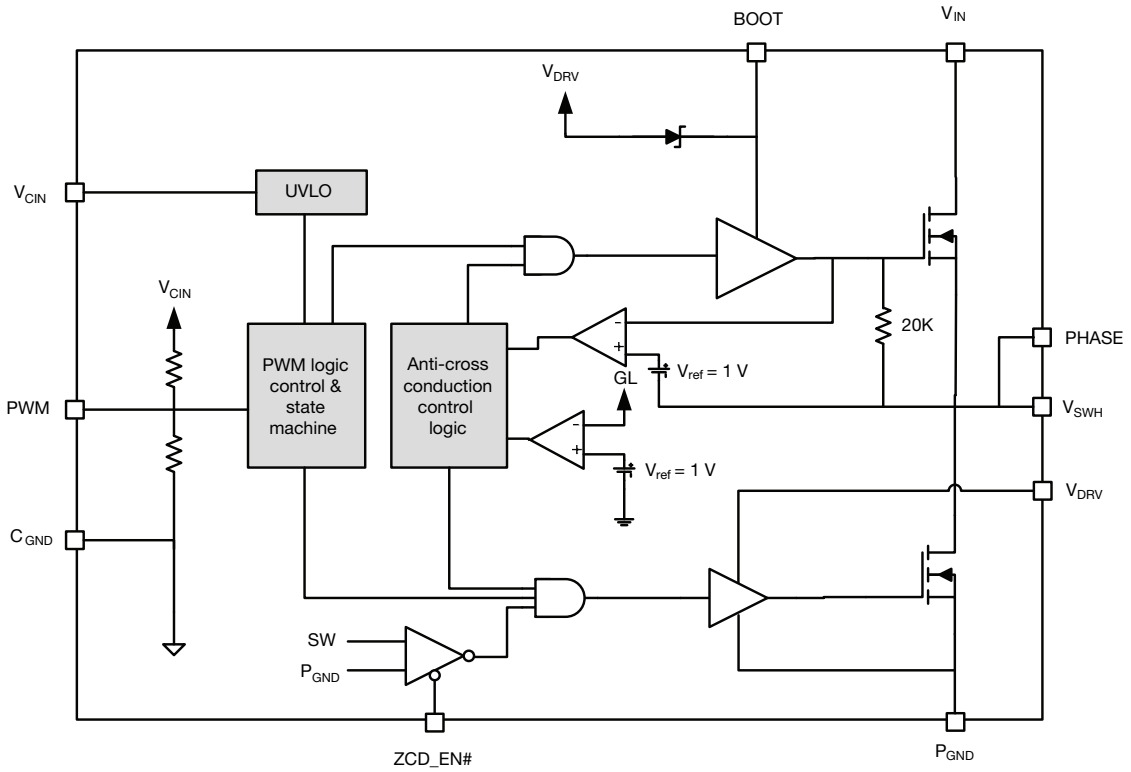

Fig. 3 - SiC521 and SiC521A Functional Block Diagram

DEVICE TRUTH TABLE			
ZCD_EN#	**PWM**	**GH**	**GL**
L	L	L	H, I_L > 0A L, I_L < 0A
L	H	H	L
L	Tri-state	L	L
H	L	L	H
H	H	H	L
H	Tri-state	L	L

PWM TIMING DIAGRAM

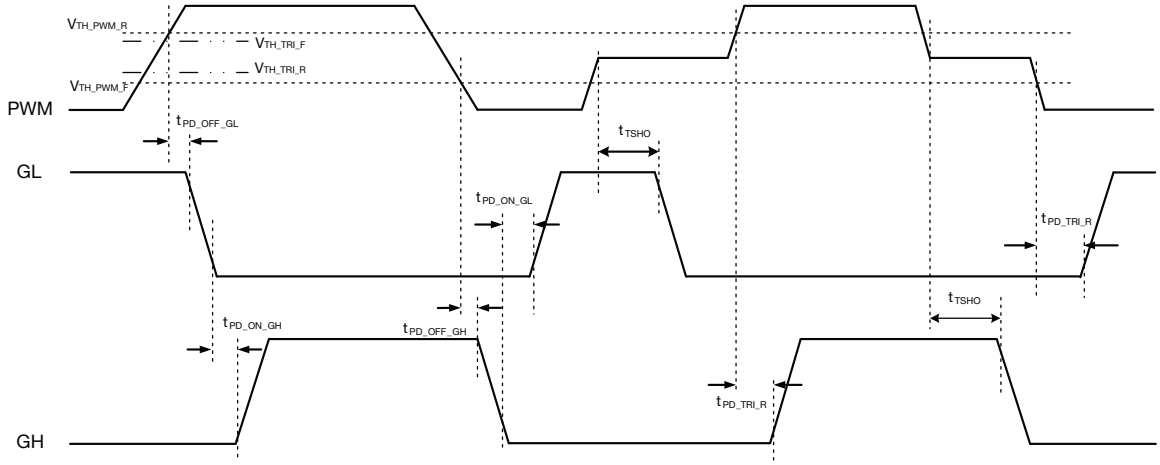

Fig. 4 - Definition of PWM Logic and Tri-State

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ELECTRICAL CHARACTERISTICS

Test condition: V_{IN} = 12 V, V_{DRV} = V_{CIN} = 5 V, ZCD_EN# = 5 V, V_{OUT} = 1 V, L_{OUT} = 360 nH, (DCR = 0.32 mΩ), T_A = 25 °C
(All power loss and normalized power loss curves show SiC521 and SiC521A losses only unless otherwise stated)

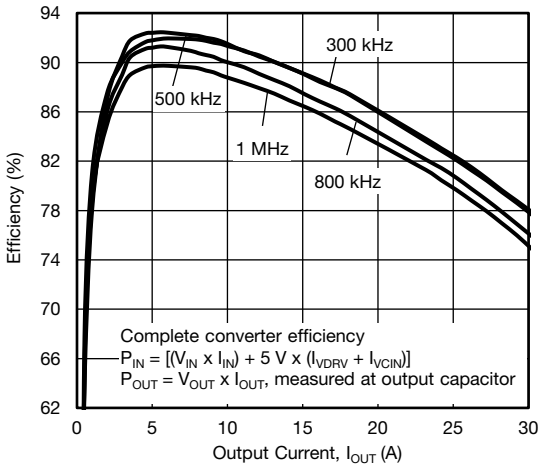

Fig. 5 - Efficiency vs. Output Current

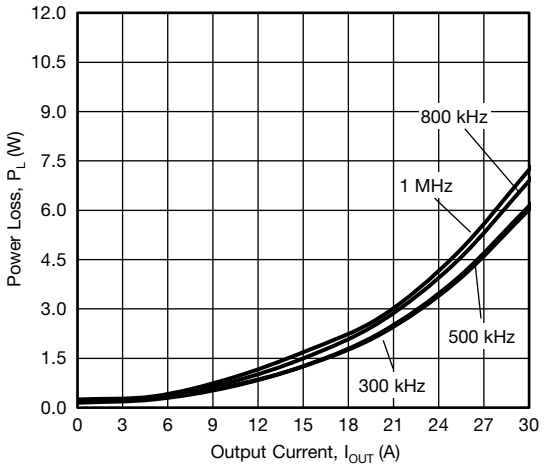

Fig. 8 - Power Loss vs. Output Current

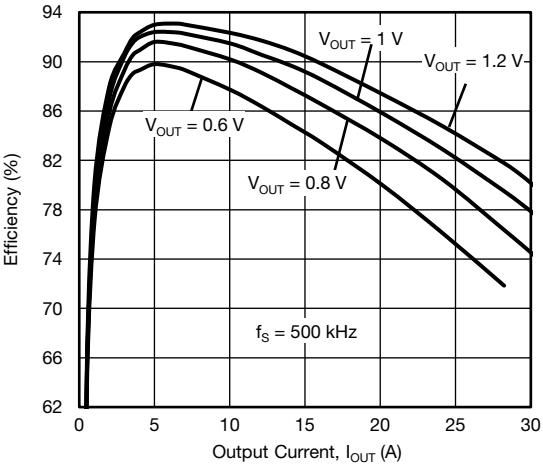

Fig. 6 - Efficiency vs. Output Current

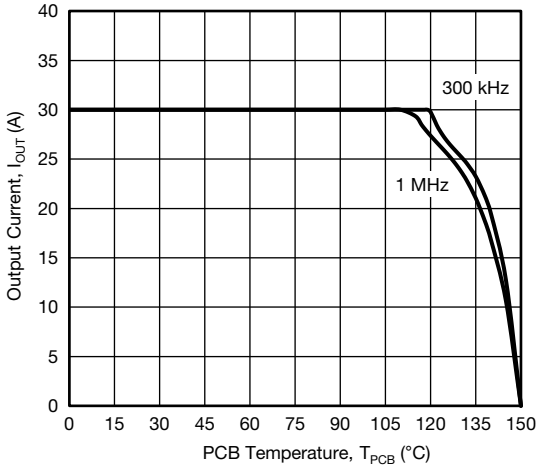

Fig. 9 - Safe Operating Area

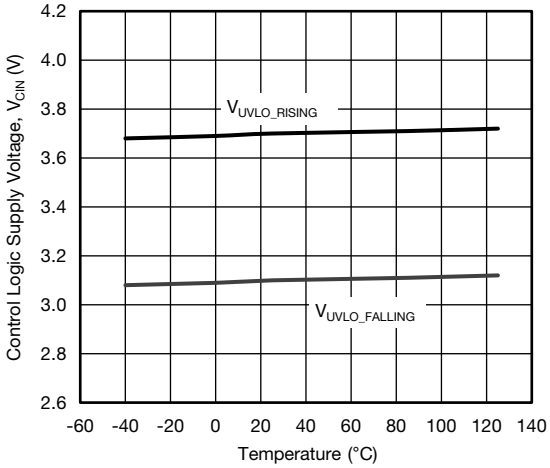

Fig. 7 - UVLO Threshold vs. Temperature

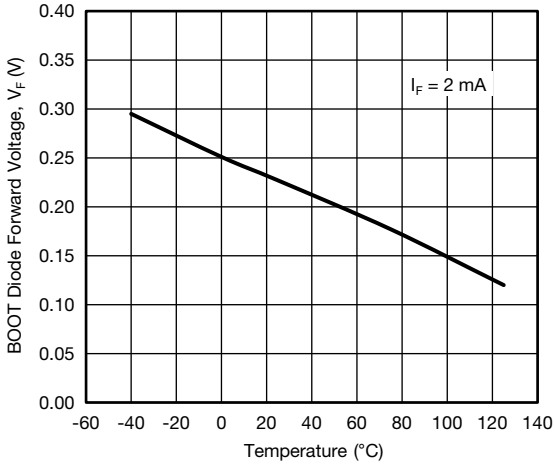

Fig. 10 - BOOT Diode Forward Voltage vs. Temperature

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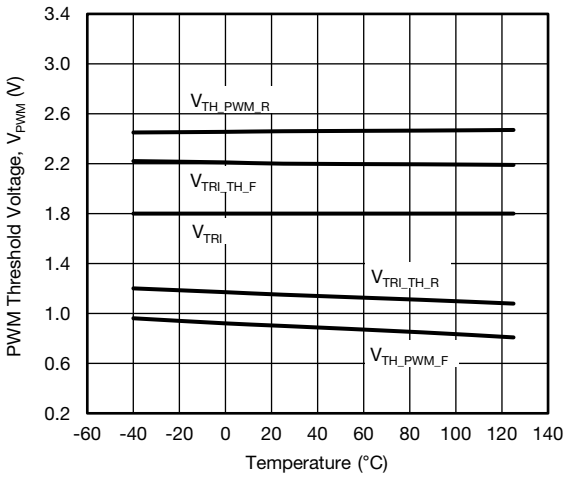

Fig. 11 - PWM Threshold vs. Temperature (SiC521A)

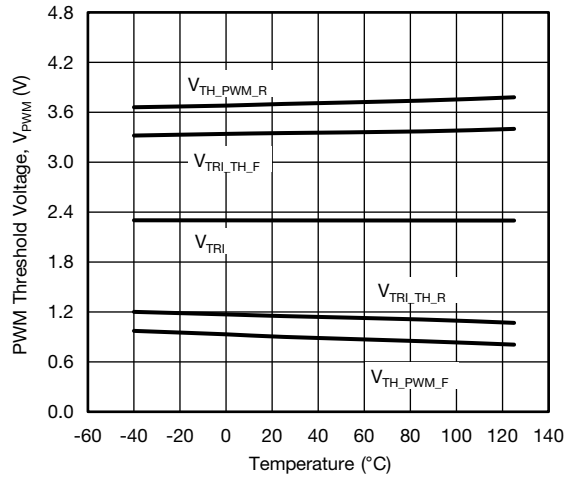

Fig. 12 - PWM Threshold vs. Temperature (SiC521)

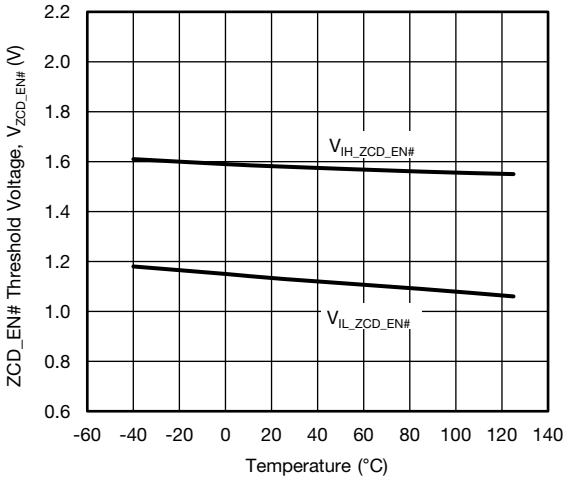

Fig. 13 - ZCD_EN# Threshold vs. Temperature

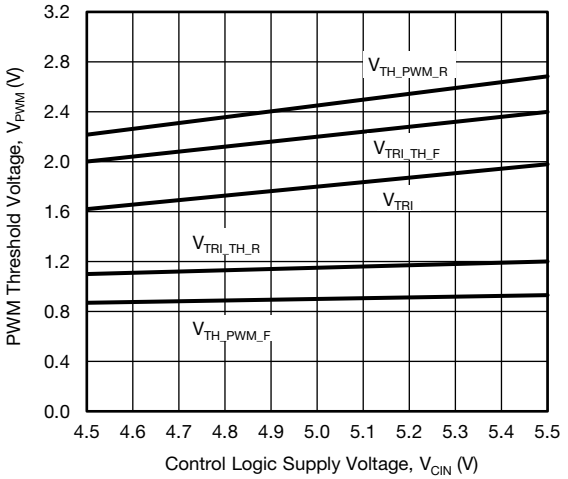

Fig. 14 - PWM Threshold vs. Driver Supply Voltage (SiC521A)

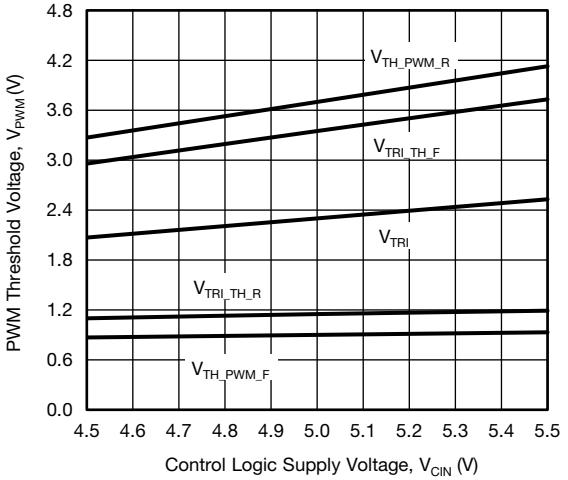

Fig. 15 - PWM Threshold vs. Driver Supply Voltage (SiC521)

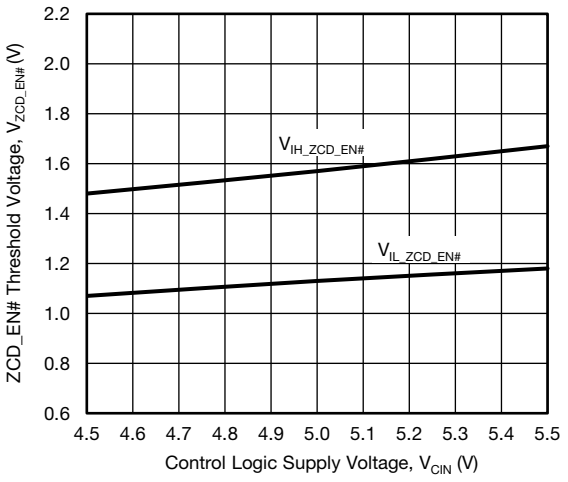

Fig. 16 - ZCD_EN# Threshold vs. Driver Supply Voltage

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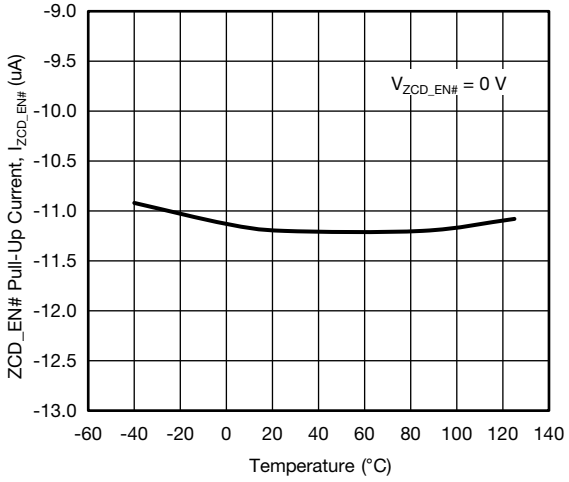


Fig. 17 - ZCD_EN# Pull-Up Current vs. Temperature

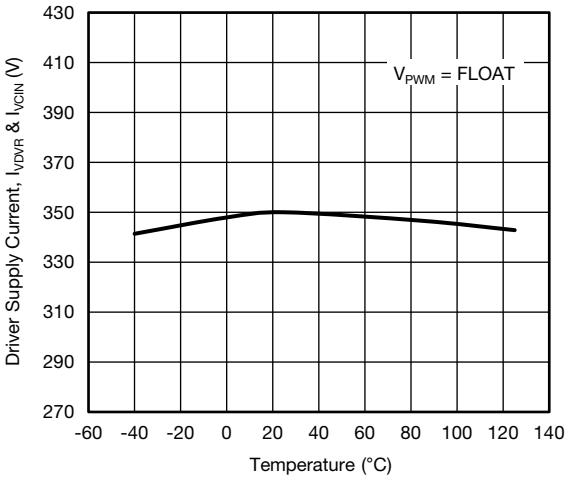
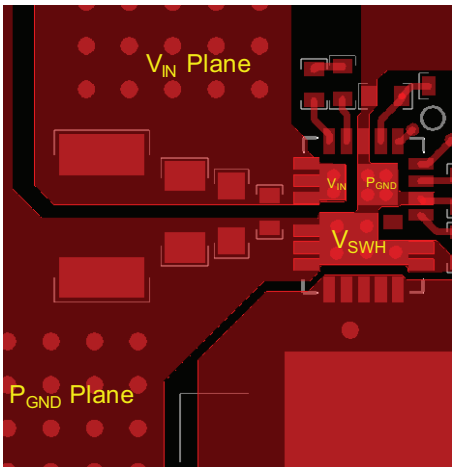


Fig. 18 - Driver Quiescent Current vs. Temperature

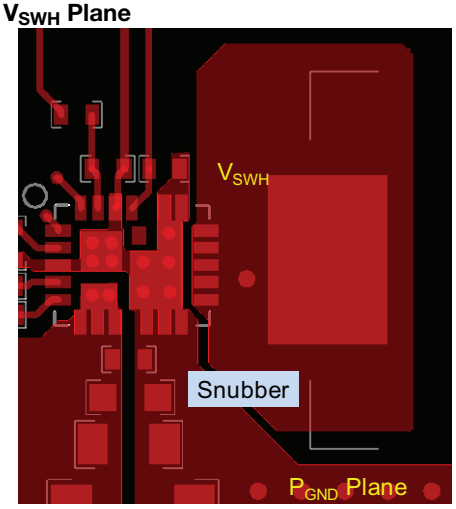
PCB LAYOUT RECOMMENDATIONS

Step 1: V_{IN} / P_{GND} Planes and Decoupling



1. Layout V_{IN} and P_{GND} planes as shown above.
2. Ceramic capacitors should be placed directly between V_{IN} and P_{GND}, and very close to the device for best decoupling effect.
3. Different values / packages of ceramic capacitors should be used to cover entire decoupling spectrum e.g. 1210, 0805, 0603, 0402.
4. Smaller capacitance values, placed closer to the devices, V_{IN} pin(s), results in better high frequency noise absorbing.

Step 2: V_{SWH} Plane



1. Connect output inductor to IC with large plane to lower resistance.
2. V_{SWH} plane also serves as a heat-sink for low-side MOSFET. Make the plane wide and short to achieve the best thermal path.
3. If any snubber network is required, place the components as shown above and the network can be placed at bottom.

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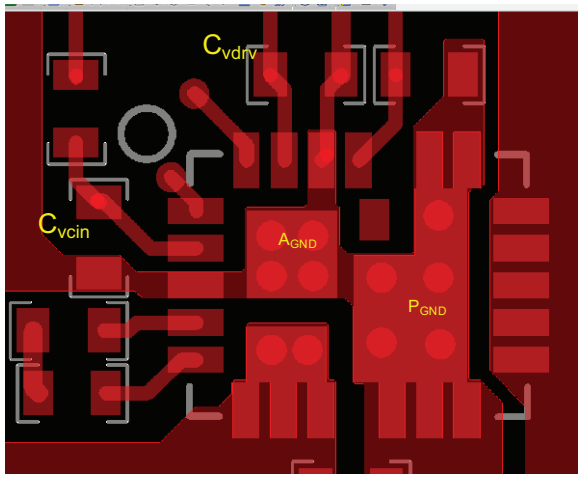
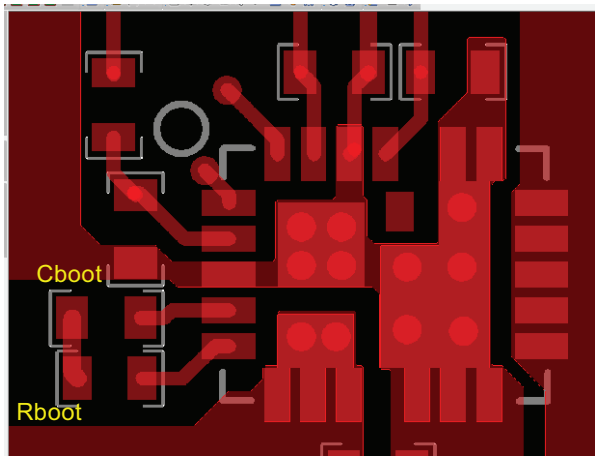
Step 3: V_{CIN} / V_{DRV} Input Filter



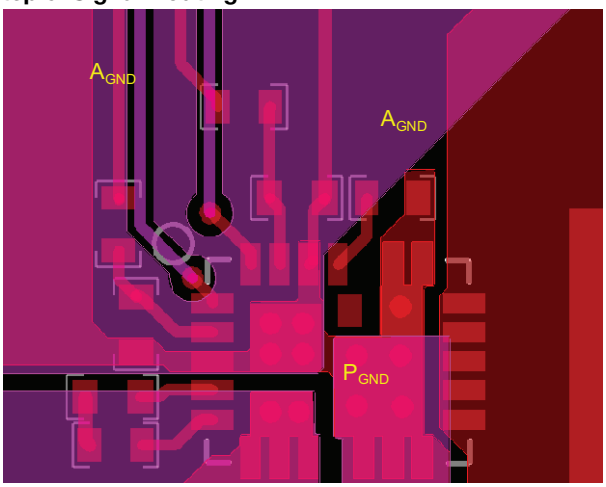
1. The V_{CIN} / V_{DRV} input filter ceramic cap should be placed as close as possible to the IC. It is recommended to connect two capacitors separately.
2. V_{CIN} capacitor should be placed between pin 2 and pin 3 (A_{GND} of driver IC) to achieve best noise filtering.
3. V_{DRV} capacitor should be placed between pin 20 (P_{GND} of driver IC) and pin 21 to provide maximum instantaneous driver current for low side MOSFET during switching cycle.
4. For connecting V_{CIN} to A_{GND}, it is recommended to use a large plane to reduce parasitic inductance.

Step 4: BOOT Resistor and Capacitor Placement



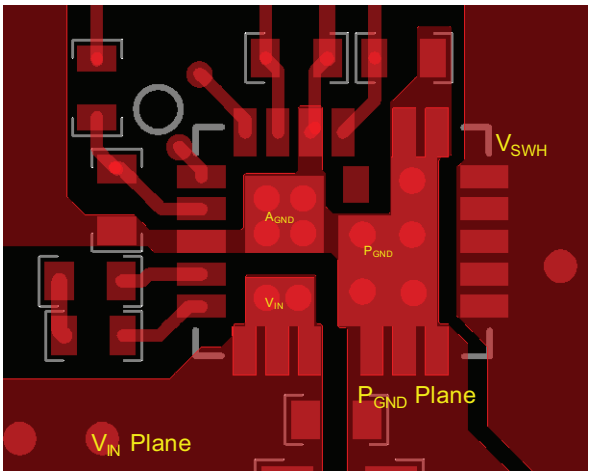
1. The components need to be placed as close as possible to IC, directly between PHASE (pin 5) and BOOT (pin 4).
2. To reduce parasitic inductance, chip size 0402 can be used.

Step 5: Signal Routing



1. Route the PWM and ZCD_EN# signal traces out of the top left corner next to pin 1.
2. The PWM signal is an important signal, both signal and return traces should not cross any power nodes on any layer.
3. It is best to “shield” these traces from power switching nodes, e.g. V_{SWH}, with a GND island to improve signal integrity.
4. GL (pin 19) has been connected with GL pad (pin 24) internally.

Step 6: Adding Thermal Relief Vias



1. Thermal relief vias can be added on the V_{IN} and A_{GND} pads to utilize inner layers for high-current and thermal dissipation.
2. To achieve better thermal performance, additional vias can be placed on V_{IN} plane and P_{GND} plane.
3. V_{SWH} pad is a noise source, it is not recommended to place vias on this pad.
4. 8 mil vias for pads and 10 mils vias for planes are the optimal via sizes. Vias on pad may drain solder during assembly and cause assembly issues. Consult with the assembly house for guidelines.

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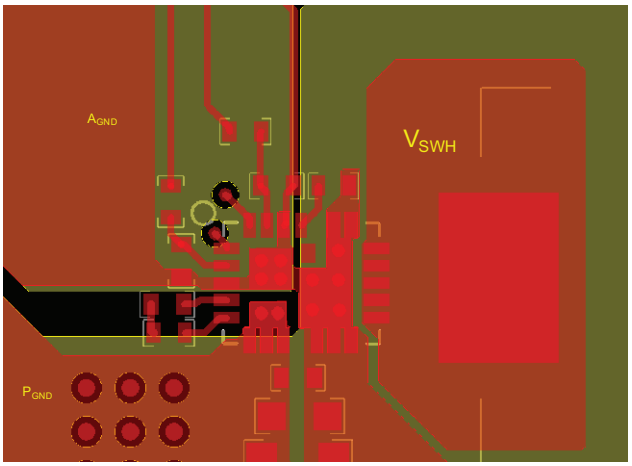
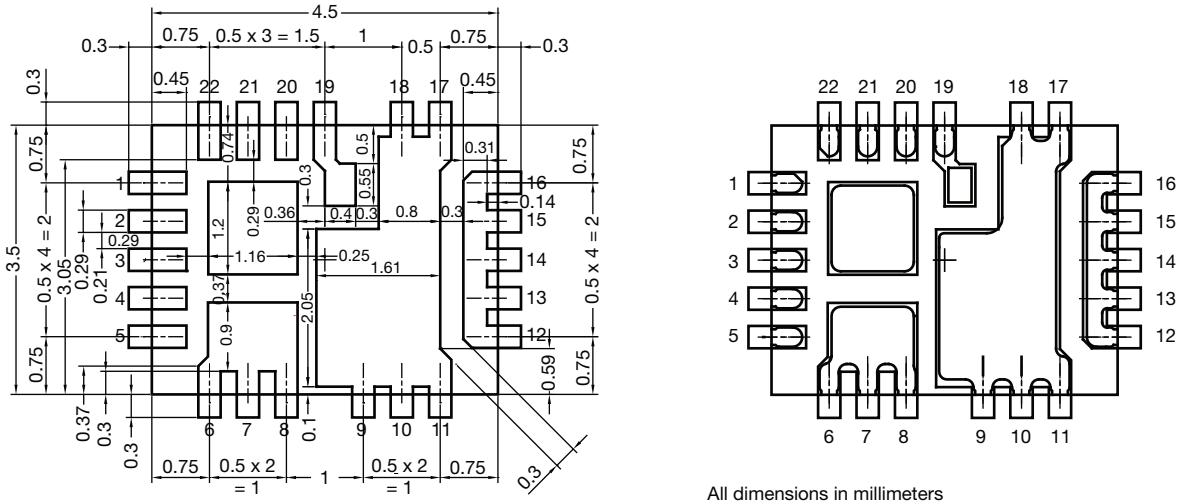
Step 7: Ground Connection



1. It is recommended to make a single connection between A_{GND} and P_{GND} which can be made on the top layer.
2. It is recommended to make the entire first inner layer (below top layer) the ground plane and separate them into A_{GND} and P_{GND} planes.
3. These ground planes provide shielding between noise sources on top layer and signal traces on bottom layer.

RECOMMENDED LAND PATTERN POWERPAK® MLP4535-22L



All dimensions in millimeters

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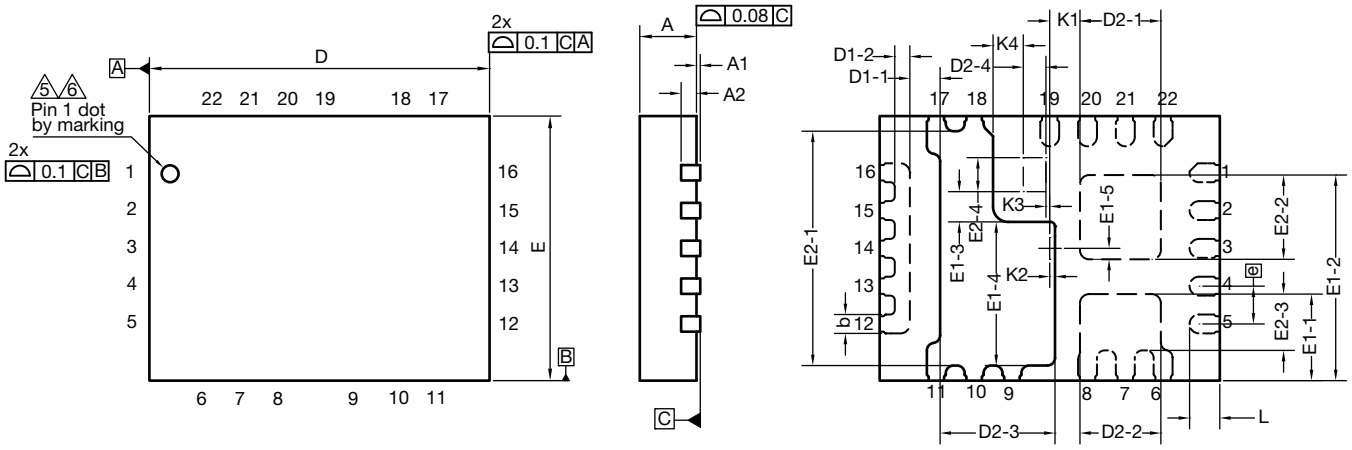
PACKAGE OUTLINE DRAWING MLP4535-22L



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A (8)	0.70	0.75	0.80	0.027	0.0029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 ref.			0.008 ref.	
b (4)	0.20	0.25	0.30	0.0078	0.0098	0.0110
D		4.50 BSC			0.177 BSC	
e		0.50 BSC			0.019 BSC	
E		3.50 BSC			0.137 BSC	
L	0.35	0.40	0.45	0.013	0.015	0.017
N (3)		22			22	
Nd (3)		6			6	
Ne (3)		5			5	
D1-1	0.35	0.40	0.45	0.013	0.015	0.017
D1-2	0.15	0.20	0.25	0.005	0.007	0.009
D2-1	1.02	1.07	1.12	0.040	0.042	0.044
D2-2	1.02	1.07	1.12	0.040	0.042	0.044
D2-3	1.47	1.52	1.57	0.057	0.059	0.061
D2-4	0.25	0.30	0.35	0.009	0.011	0.013
E1-1	1.095	1.145	1.195	0.043	0.045	0.047
E1-2	2.67	2.72	2.77	0.105	0.107	0.109
E1-3	0.35	0.40	0.45	0.013	0.015	0.017
E1-4	1.85	1.90	1.95	0.072	0.074	0.076
E1-5	0.095	0.145	0.195	0.0037	0.0057	0.0076
E2-1	3.05	3.10	3.15	0.120	0.122	0.124
E2-2	1.065	1.115	1.165	0.0419	0.0438	0.0458
E2-3	0.695	0.745	0.795	0.027	0.029	0.031
E2-4	0.40	0.45	0.50	0.015	0.017	0.019
K1		0.40 BSC			0.015 BSC	
K2		0.07 BSC			0.002 BSC	
K3		0.05 BSC			0.001 BSC	
K4		0.40 BSC			0.015 BSC	

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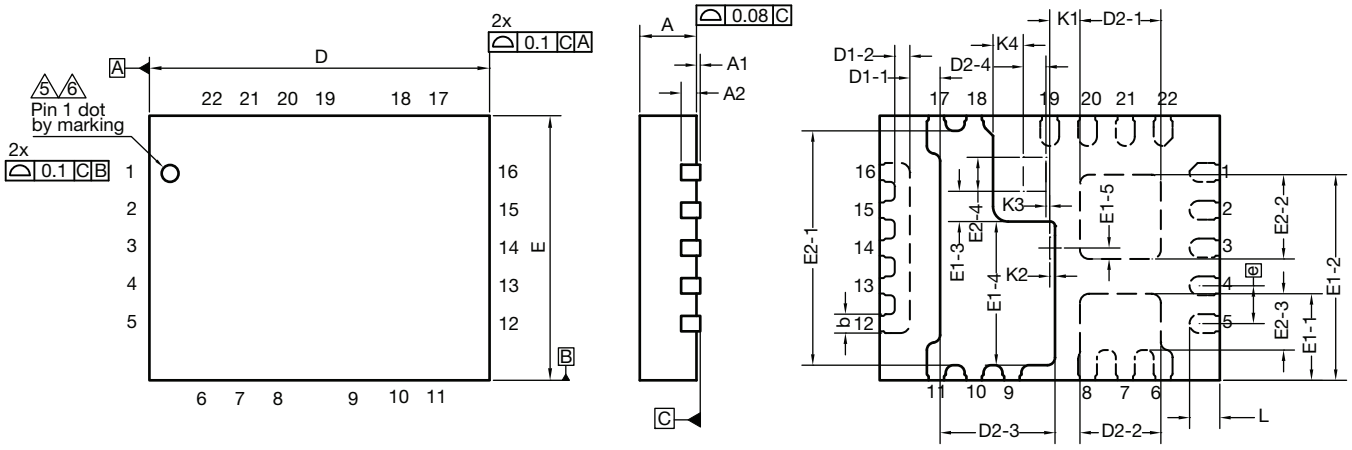
MLP 4.5 x 3.5-22L BWL Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A [8]	0.70	0.75	0.80	0.027	0.0029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 ref.			0.008 ref.	
b [4]	0.20	0.25	0.30	0.0078	0.0098	0.0110
D		4.50 BSC			0.177 BSC	
e		0.50 BSC			0.019 BSC	
E		3.50 BSC			0.137 BSC	
L	0.35	0.40	0.45	0.013	0.015	0.017
N [3]		22			22	
Nd [3]		6			6	
Ne [3]		5			5	
D1-1	0.35	0.40	0.45	0.013	0.015	0.017
D1-2	0.15	0.20	0.25	0.005	0.007	0.009
D2-1	1.02	1.07	1.12	0.040	0.042	0.044
D2-2	1.02	1.07	1.12	0.040	0.042	0.044
D2-3	1.47	1.52	1.57	0.057	0.059	0.061
D2-4	0.25	0.30	0.35	0.009	0.011	0.013
E1-1	1.095	1.145	1.195	0.043	0.045	0.047
E1-2	2.67	2.72	2.77	0.105	0.107	0.109
E1-3	0.35	0.40	0.45	0.013	0.015	0.017
E1-4	1.85	1.90	1.95	0.072	0.074	0.076
E1-5	0.095	0.145	0.195	0.0037	0.0057	0.0076
E2-1	3.05	3.10	3.15	0.120	0.122	0.124
E2-2	1.065	1.115	1.165	0.0419	0.0438	0.0458
E2-3	0.695	0.745	0.795	0.027	0.029	0.031
E2-4	0.40	0.45	0.50	0.015	0.017	0.019
K1		0.40 BSC			0.015 BSC	
K2		0.07 BSC			0.002 BSC	
K3		0.05 BSC			0.001 BSC	
K4		0.40 BSC			0.015 BSC	

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Notes

1. Use millimeters as the primary measurement
2. Dimensioning and tolerances conform to ASME Y14.5M. - 1994
3. N is the number of terminals,
   Nd is the number of terminals in X-direction and
   Ne is the number of terminals in Y-direction.
4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
5. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
6. Exact shape and size of this feature is optional
7. Package warpage max. 0.08 mm
8. Applied only for terminals

T14-0626-Rev. A, 20-Oct-14 DWG: 6028

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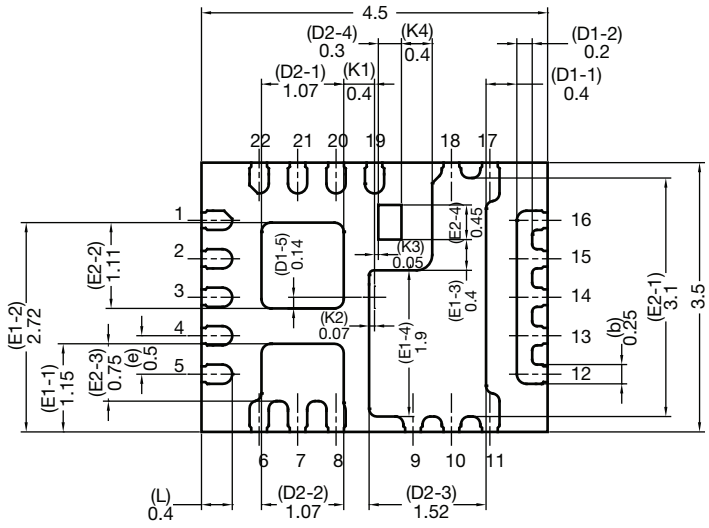
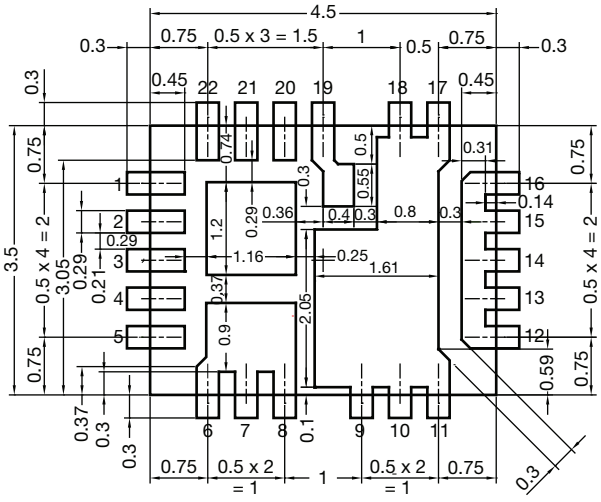
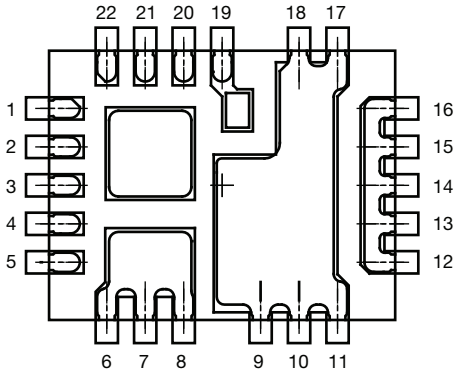
Recommended Land Pattern PowerPAK® MLP4535-22L

Package outline top view, transparent
(not bottom view)



Land pattern





All dimensions in millimeters

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