

## Triple Output Power Supply for TFT-LCD

## ■ GENERAL DESCRIPTION

☆GreenOperation Compatible

The XC9516 series can offer three different power supplies to TFT-LCD panels. These power supplies consist of a step-up DC/DC converter for a source driver, positive and negative charge pumps for a gate driver.

This IC has power-on sequences to keep inrush current as small when output voltage rises. The step-up DC/DC output can be used as power-on sequences with adding a P-channel FET as external component. Also, the FET can shut down a path to the power input line when CE pin is low.

## ■ APPLICATIONS

- TFT-LCD panels
- LCD monitors

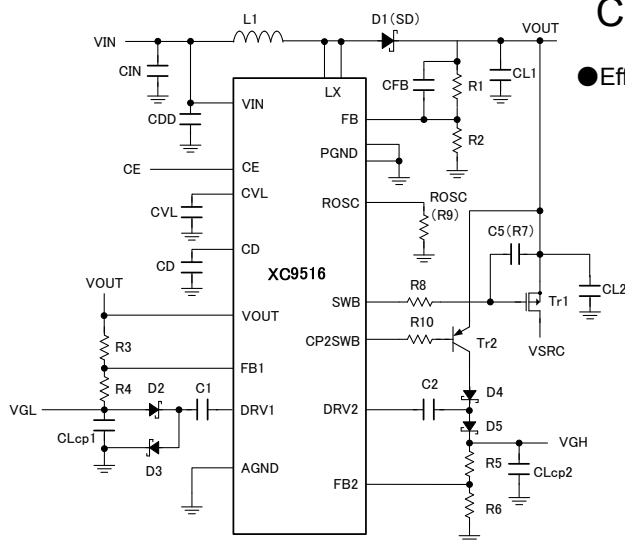
## ■ FEATURES

## A Step-up DC/DC Converter and 2 of Charge Pumps (Positive/Negative)

<b>Input Voltage Range</b>	: 2.5V ~ 5.5V
<b>Maximum Output Voltage</b>	: 19V (DC/DC output)
<b>Output Voltage Accuracy</b>	: ±1.5%
<b>Oscillation Frequency</b>	: 300kHz ~ 1.2MHz (Adjustable)
<b>External MOSFET Gate Signal Output</b>	: N-Channel Open Drain
<b>Switch Over-Current Protection</b>	: 1.3A
<b>Soft-Start Time</b>	: Internally fixed
<b>Protection</b>	: Over Voltage Protection (Step-up DC/DC 21V) Short-Circuit Protection (Step-up DC/DC) Short-Circuit Protection (Positive and Negative Charge Pump) Thermal Shutdown (150°C) UVLO (1.87V)
<b>Operating Ambient Temperature</b>	: -40°C~+85°C
<b>Package</b>	: QFN-20
<b>Environmentally Friendly</b>	: EU RoHS Compliant, Pb Free

## ■ TYPICAL APPLICATION CIRCUITS

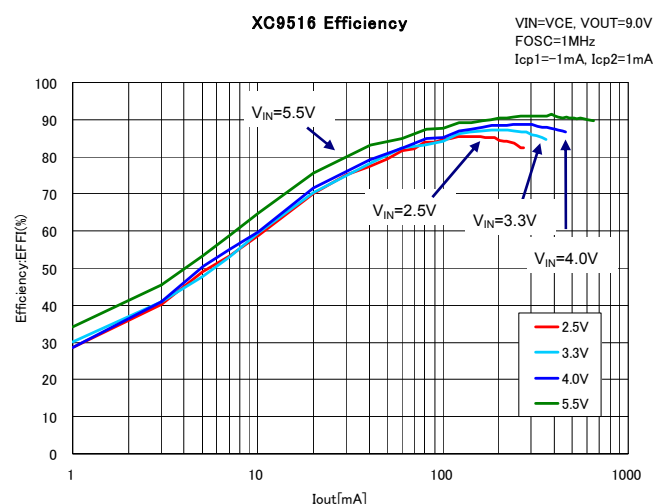
## ■ TYPICAL PERFORMANCE CHARACTERISTICS



## e.g) Components List

$V_{OUT} = 9.2V$ , $V_{GL} = -5.3V$ , $V_{GH} = 12V$	$R_1 = 820\text{ k}\Omega$
$C_{IN} = 4.7\text{ }\mu\text{F}$	$R_2 = 100\text{ k}\Omega$
$C_{L1}, C_{L2} = 4.7\text{ }\mu\text{F}$	$R_3 = 390\text{ k}\Omega$
$C_1, C_2 = 0.01\text{ }\mu\text{F}$	$R_4 = 300\text{ k}\Omega$
$C_{VL}, C_D = 0.1\text{ }\mu\text{F}$	$R_5 = 820\text{ k}\Omega$
$C_{DD} = 1\text{ }\mu\text{F}$	$R_6 = 75\text{ k}\Omega$
$C_{Lcp1}, C_{Lcp2} = 1\text{ }\mu\text{F}$	$R_8 = 300\text{ k}\Omega$
$C_{FB} = 22\text{ pF}$	$R_{OSC} (R_9) = 130\text{ k}\Omega$
$C_5 = 0.01\text{ }\mu\text{F}$	$R_{10} = 51\text{ k}\Omega$

## ● Efficiency vs. Output Current



## PIN CONFIGURATION



\*1 The dissipation pad : AGND Level

(If the pad needs to be connected to other pins, it should be considered about the level of pad voltage.)

## PIN ASSIGNMENT

PIN NUMBER	PIN NAME	FUNCTIONS
1	DRV1	Negative Charge Pump Driver Output
2	CP2SWB	Positive Charge Pump for Output Control
3	FB1	FB Pin for Negative Charge Pump
4	CE	Chip Enable Pin
5	FB	FB Pin for Step-Up DC/DC Converter
6	ROSC	Frequency Setting
7	NC	No Connection
8	V <sub>IN</sub>	Power
9	CD	Short Protection Delay Capacitor Connection
10	AGND	Analog Ground
11	FB2	FB Input for Positive Charge Pump
12	CVL	Internal Power Capacitor Connection
13	SWB	Step-Up DC/DC Converter Output Control
14	V <sub>OUT</sub>	Step-Up DC/DC Converter Output Voltage
15	DRV2	Positive Charge Pump Driver Output
16	L <sub>X</sub>	Driver Output Pin for Step-Up DC/DC Converter
17	L <sub>X</sub>	Driver Output Pin for Step-Up DC/DC Converter
18	NC	No Connection
19	PGND	Power Ground Pin for Driver
20	PGND	Power Ground Pin for Driver

## LOGIC CONDITION

PIN NAME	LOGIC	CONDITION
CE PIN	L	$GND \leq V_{CE} \leq 0.4V$
	H	$1.2V \leq V_{CE} \leq V_{IN}$

Voltage is based on V<sub>SS</sub> (GND=AGND=PGND)

## FUNCTION CHART

CONDITIONS	IC OPERATION
L	OFF(Stand-by)
H	ON

IC operation is unstable when CE opens so that these pins shall not be left open outside.

## PRODUCT CLASSIFICATION

### Ordering Information

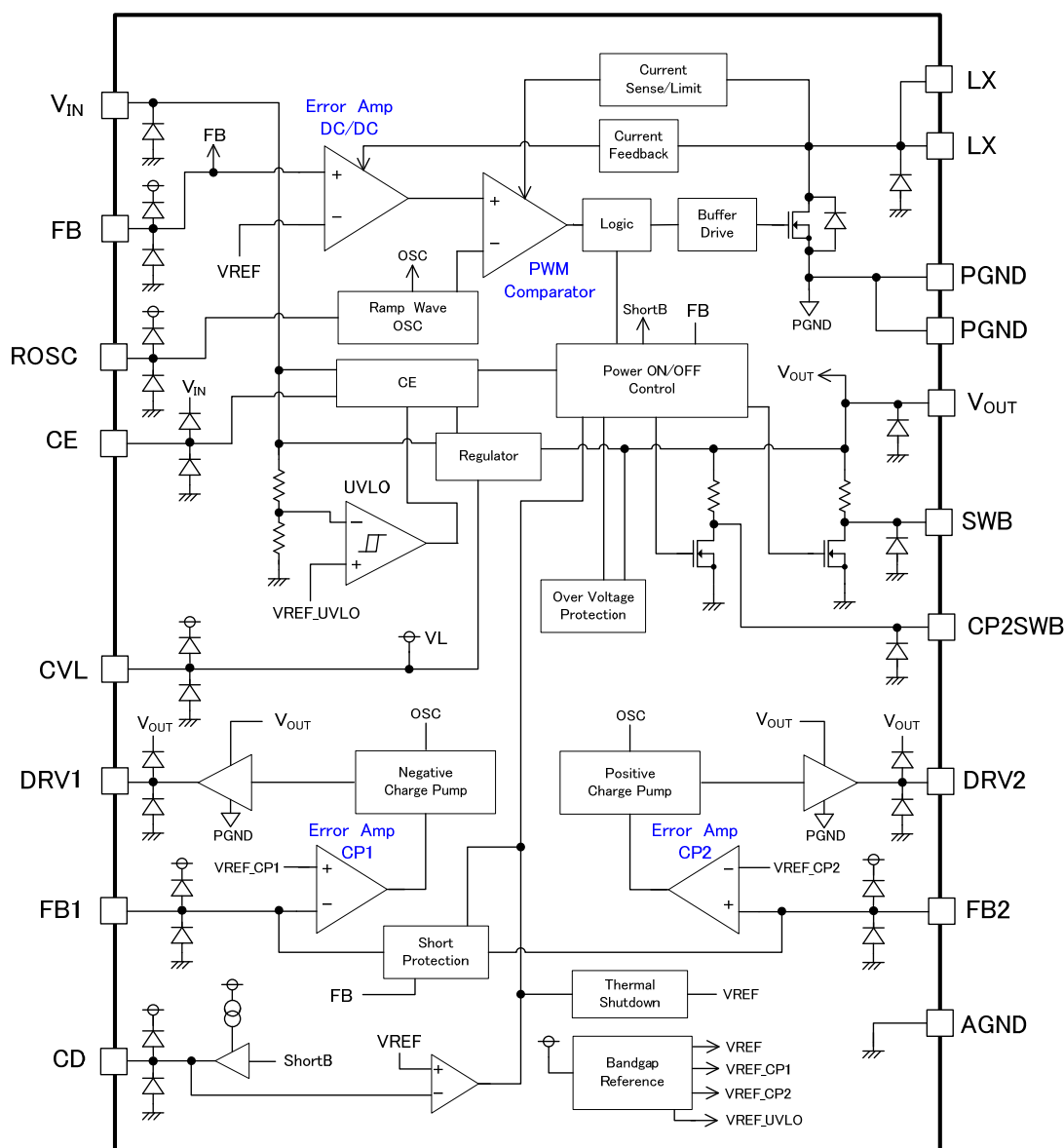
XC9516①②③④⑤⑥-⑦<sup>(\*)</sup> ⇒ XC9516A21AZR-G

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	UVLO Detect Voltage	A	Detect Voltage: 1.87V, Hysteresis Width 0.44V
②③	Over Voltage Limit	21	Over Voltage Detect Voltage: 21V
④	Over Current Limit	A	Over Current Detect Voltage: 1.3A
⑤⑥-⑦ <sup>(*)</sup>	Package (Order Unit)	ZR-G	QFN-20 (1,000/Reel) <sup>(**)</sup>

(\*1) The "-G" suffix denotes Halogen and Antimony free as well as being fully RoHS compliant.

(\*2) The XC9516 reels are shipped in a moisture-proof packing.

## BLOCK DIAGRAM



PGND and AGND are externally connected to the same potential.

## ■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNITS
V <sub>IN</sub> Voltage	V <sub>IN</sub>	-0.3~6.0	V
CE Pin Voltage	V <sub>CE</sub>	-0.3~V <sub>IN</sub> +0.3 or 6.0 <sup>(*)1</sup>	V
FB Pin Voltage	V <sub>FB</sub>	-0.3~V <sub>CVL</sub> +0.3 or 6.0 <sup>(*)2</sup>	V
FB1 Pin Voltage	V <sub>FB1</sub>	-0.3~V <sub>CVL</sub> +0.3 or 6.0 <sup>(*)2</sup>	V
FB2 Pin Voltage	V <sub>FB2</sub>	-0.3~V <sub>CVL</sub> +0.3 or 6.0 <sup>(*)2</sup>	V
ROSC Pin Voltage	V <sub>ROSC</sub>	-0.3~V <sub>CVL</sub> +0.3 or 6.0 <sup>(*)2</sup>	V
CD Pin Voltage	V <sub>CD</sub>	-0.3~V <sub>CVL</sub> +0.3 or 6.0 <sup>(*)2</sup>	V
CVL Pin Voltage	V <sub>VL</sub>	-0.3~6.0	V
SWB Pin Voltage	V <sub>SWB</sub>	-0.3~22	V
CP2SWB Pin Voltage	V <sub>CP2SWB</sub>	-0.3~22	V
V <sub>OUT</sub> Pin Voltage	V <sub>OUT</sub>	-0.3~22	V
L <sub>X</sub> Pin Voltage	V <sub>LX</sub>	-0.3~22	V
DR1 Pin Voltage	V <sub>DRV1</sub>	-0.3~V <sub>OUT</sub> +0.3 or 22 <sup>(*)3</sup>	V
DR2 Pin Voltage	V <sub>DRV2</sub>	-0.3~V <sub>OUT</sub> +0.3 or 22 <sup>(*)3</sup>	V
L <sub>X</sub> Pin Current	I <sub>LX</sub>	1650	mA
Power Dissipation	P <sub>d</sub>	300	mW
Operating Ambient Temperature	Topr	-40 ~ +85	°C
Storage Temperature	Tstg	-55 ~ +125	°C

\* All voltages are described based on GND. (GND=AGND=PGND)

(\*)1 The maximum value should be either V<sub>IN</sub>+0.3 or +6.0 in the lowest.

(\*)2 The maximum value should be either V<sub>CVL</sub>+0.3 or +6.0 in the lowest.

(\*)3 The maximum value should be either V<sub>OUT</sub>+0.3 or +22.0 in the lowest.

## ■ ELECTRICAL CHARACTERISTICS

Unless otherwise stated,  $V_{IN}=V_{CE}=3.3V$ ,  $V_{OUT}=9.0V$ ,  $f_{OSC}=300kHz$ ,  $T_a=25^{\circ}C$

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Power Input Voltage Range	$V_{IN}$		2.5	-	5.5	V	-
Input Voltage Rise Time	$t_{VIN}$	$V_{IN}=V_{CE}=0.2V \rightarrow 2.5V$ (*1)	-	-	15	ms	⑳
Supply Current	$I_{DD1}$	$V_{FB}=V_{FB2}=0.8V$ , $V_{FB1}=1.2V$ , $V_{CD}=0V$	0.8	2.0	4.0	$\mu A$	①
Stand-by Current	$I_{STB}$	$V_{CE}=0V$	-	0.1	8.0	$\mu A$	②
Oscillation Frequency	$f_{OSC}$	$V_{FB}=V_{FB2}=0.8V$ , $V_{FB1}=1.2V$ , $V_{CD}=0V$ , $R_{OSC}$ Open	255	300	345	kHz	③
UVLO Detect Voltage ( $V_{IN}$ falls down)	$V_{UVLO1}$	$V_{IN}=V_{CE}$ , $V_{FB}=V_{FB2}=0.8V$ , $V_{FB1}=1.2V$ , $V_{CD}=0V$	1.77	1.87	1.97	V	④
UVLO Feedback Voltage ( $V_{IN}$ rises)	$V_{UVLO2}$	$V_{IN}=V_{CE}$ , $V_{FB}=V_{FB2}=0.8V$ , $V_{FB1}=1.2V$ , $V_{CD}=0V$	2.22	2.31	2.40	V	④
CE "High" Voltage	$V_{CEH}$	$V_{FB}=V_{FB2}=0.8V$ , $V_{FB1}=1.2V$ , $V_{CD}=0V$	1.2	-	$V_{IN}$	V	⑤
CE "Low" Voltage	$V_{CEL}$	$V_{FB}=V_{FB2}=0.8V$ , $V_{FB1}=1.2V$ , $V_{CD}=0V$	AGND	-	0.4	V	⑤
CE Input Current	$I_{CE}$	$V_{IN}=5.5V$ , $V_{CE}=0V$ or $5.5V$	-0.1	-	0.1	$\mu A$	⑥
CD Pin Charge Current	$I_{CD1}$	$V_{FB}=0.9V \rightarrow 0.4V$ , $V_{FB1}=V_{FB2}=0.9V$	2.6	5.5	8.4	$\mu A$	⑦
CD Pin Discharge Current	$I_{CD2}$	$V_{FB}=V_{FB1}=V_{FB2}=0.9V$ , $V_{CD}=0.1V$	0.20	0.38	0.56	mA	⑧
CD Pin Detect Voltage	$V_{CD}$	$V_{FB}=V_{FB1}=V_{FB2}=0V$	0.95	1.0	1.05	V	⑨
CP2SWB "L" Output Voltage	$V_{SWB2}$	Input Current=1mA	0.55	0.65	0.80	V	⑩
SWB "L" Output Voltage	$V_{SWB}$	Input Current=1mA	0.26	0.33	0.40	V	⑩
CP2SWB Pull up Resistance	$R_{CP2}$	$V_{CE}=0V$ , $V_{OUT}=5.5V$ , $CP2SWB=1.0V$	350	800	2500	k $\Omega$	⑪
SWB Pull up Resistance	$R_{SWB}$	$V_{CE}=0V$ , $V_{OUT}=5.5V$ , $SWB=1.0V$	350	800	2500	k $\Omega$	⑪
Thermal Shutdown Temperature	$T_{TSD}$		-	150	-	$^{\circ}C$	-
Hysteresis Width	$T_{HYS}$		-	20	-	$^{\circ}C$	-
<b>● Step-Up DC/DC Converter Block</b>							
FB Voltage	$V_{FB}$	$V_{FB1}=1.2V$ , $V_{FB2}=0.8V$ , $V_{CD}=0V$	0.985	1	1.015	V	⑫
Setting Output Voltage Range	$V_{OUTSET}$		5.5	-	19	V	-
Maximum Duty Cycle	$D_{MAX}$	$V_{FB}=V_{FB1}=V_{FB2}=0V$ , $V_{CD}=0V$ , $R_{OSC}$ Open	92	95	98	%	⑬
Soft-Start Time	$t_{SS}$		2.0	4.0	5.0	ms	⑲
$L_x$ "N-ch" ON Resistance	$R_{LXN}$		100	190	400	m $\Omega$	-
$L_x$ Current Limit	$I_{LIM}$	$f_{OSC}=1.0MHz$	1.1	1.3	1.5	A	⑱
$V_{OUT}$ Over Voltage Limit	$V_{OVP}$		19.5	21	22	V	⑰
Short Protection Voltage	$V_{SHORT}$	$V_{FB1}=V_{FB2}=0.9V$ , $C_D=0.1 \mu F$	0.40	0.48	0.55	V	⑮
FB Input Current	$I_{FB}$	$V_{IN}=5.5V$ , $V_{CE}=0V$ , $V_{FB}=0V$ , $5.5V$	-0.1	-	0.1	$\mu A$	⑭
<b>● Negative Charge Pump Block</b>							
FB1 Voltage	$V_{FB1}$	$V_{FB}=V_{FB2}=0.8V$ , $V_{CD}=0V$	0.985	1	1.015	V	⑫
Output Impedance 1	$R_{OUT1}$	$V_{FB1}=1.2V$ , $I_{DRV1}=20mA$	-	15	45	$\Omega$	⑰
Short Protection Voltage 1	$V_{SHORT1}$	$V_{FB}=V_{FB2}=0.9V$ , $C_D=0.1 \mu F$	1.2	2.4	2.8	V	⑮
FB1 Input Current	$I_{FB1}$	$V_{IN}=5.5V$ , $V_{CE}=0V$ , $V_{FB1}=0V$ , $5.5V$	-0.1	-	0.1	$\mu A$	⑭
<b>● Positive Charge Pump Block</b>							
FB2 Voltage	$V_{FB2}$	$V_{FB}=0.8V$ , $V_{FB1}=1.2V$ , $V_{CD}=0V$	0.985	1.0	1.015	V	⑫
Output Impedance 2	$R_{OUT2}$	$V_{FB2}=0.8V$ , $I_{DRV2}=20mA$	-	15	45	$\Omega$	⑰
Short Protection Voltage 2	$V_{SHORT2}$	$V_{FB}=V_{FB1}=0.9V$ , $C_D=0.1 \mu F$	0.40	0.48	0.55	V	⑮
FB2 Input Current	$I_{FB2}$	$V_{IN}=5.5V$ , $V_{CE}=0V$ , $V_{FB2}=0V$ , $5.5V$	-0.1	-	0.1	$\mu A$	⑭

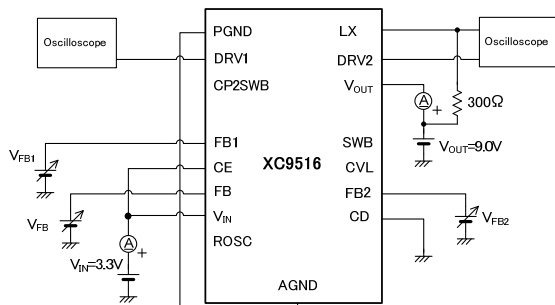
(\*1) Test Condition for input voltage rise time

When used at  $V_{IN}=V_{CE}$ , input voltage should rise from 0.2V to 2.5V within 15ms.

Please also note input voltage before rise should be less than 0.2V. Please see test circuit 20 for test condition, and for the detail of recommended input wave form, please see NOTES ON USE.

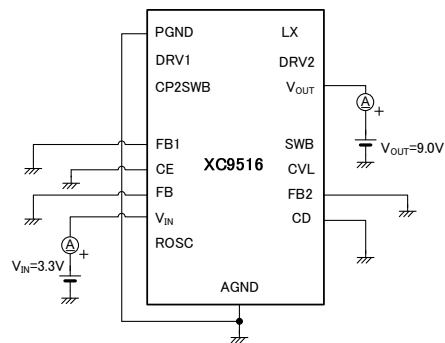
## TEST CIRCUITS

<Circuit1 Supply Current>



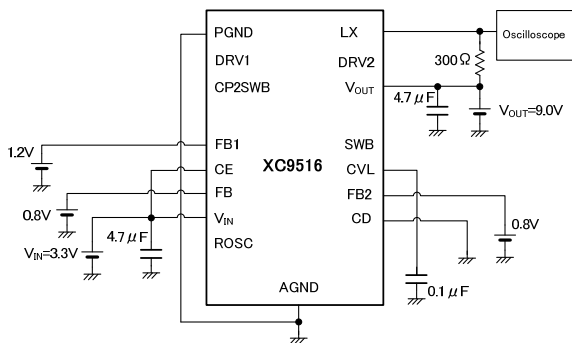
- ①  $V_{FB}=0.8V \rightarrow 1.2V \rightarrow 0.8V$  L<sub>x</sub> oscillation is checked
  - ②  $V_{FB1}=1.2V \rightarrow 0.8V \rightarrow 1.2V$  DRV1 Oscillation is checked.
  - ③  $V_{FB2}=0.8V \rightarrow 1.2V \rightarrow 0.8V$  DRV2 Oscillation is checked.
- After ①~③, supply current is measured at both V<sub>IN</sub> and V<sub>OUT</sub>.

<Circuit2 Stand-by Current>



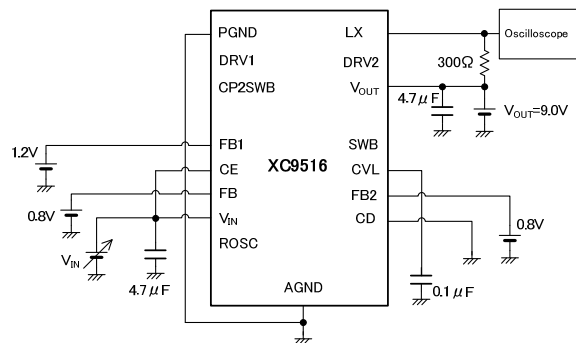
$V_{CE}=0V$ , supply current is measured at both V<sub>IN</sub> and V<sub>OUT</sub>.

<Circuit3 Oscillation Frequency>



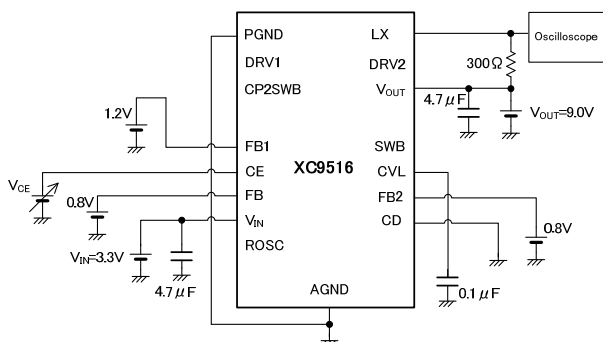
L<sub>x</sub> Oscillation period is measured.

<Circuit4 UVLO Detect/Release Voltage>



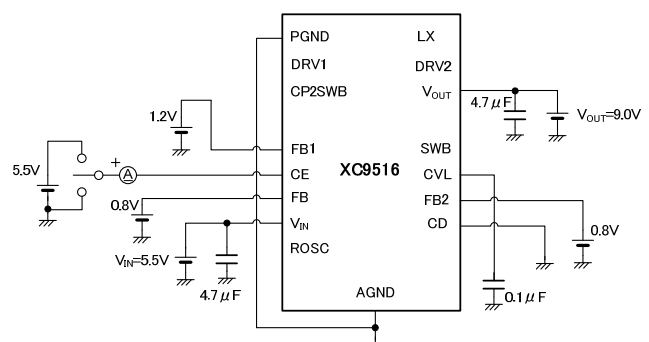
UVLO Detect Voltage Measurement: V<sub>IN</sub> is decreased (2.5V→1.5V), V<sub>IN</sub> is 測定 則定  
measured when L<sub>x</sub> oscillation stopped.  
UVLO Release Voltage Measurement: V<sub>IN</sub> is increased (1.5V→2.5V) when  
L<sub>x</sub> oscillation started,

<Circuit5 CE H/L Voltage>



CE H Voltage Measurement: V<sub>CE</sub> is increased (0.4V→1.2V), V<sub>CE</sub> is measured  
when L<sub>x</sub> oscillation started.  
CE L Voltage Measurement: V<sub>CE</sub> is decreased (1.2V→0.4V), V<sub>CE</sub> is measured  
when L<sub>x</sub> oscillation stopped.

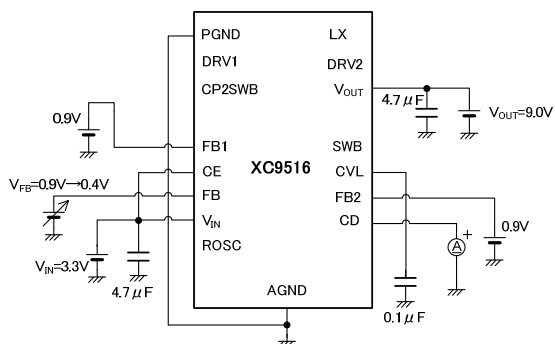
<Circuit6 CE H/L Input Current>



CE H Input Current: Current is measured when CE pin Voltage is 5.5V.  
CE L Input Current: Current is measured when CE pin Voltage is 0V.

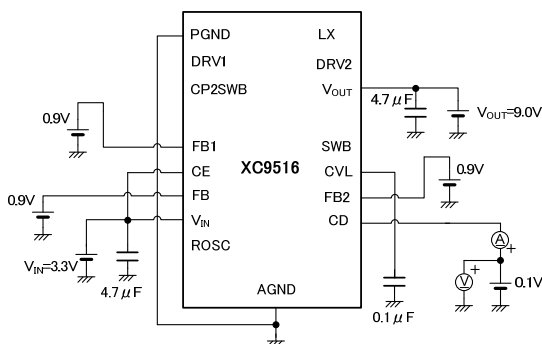
## ■ TEST CIRCUITS (Continued)

< Circuit7 C<sub>D</sub> pin Charge Current >



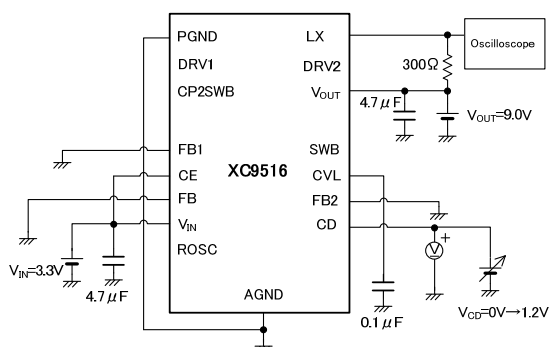
After  $V_{FB}=0.9V \rightarrow 0.4V$ , CD pin output current is measured.

< Circuit8 C<sub>D</sub> pin Discharge Current >



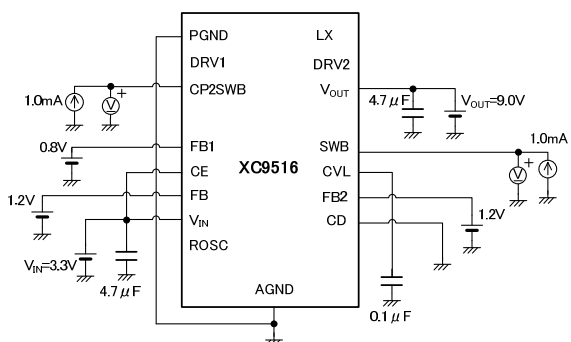
Input current is measured when C<sub>D</sub> pin Voltage is 0.1V.

< Circuit9 C<sub>D</sub> pin Detect Voltage >



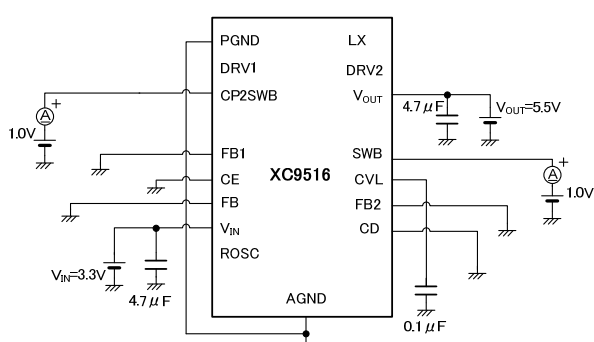
$V_{CD}=0.1V \rightarrow 0.2V$   $V_{CD}$  is measured when L<sub>x</sub> oscillation stopped.

< Circuit10 CP2SWB/SWB L Output Voltage >



CP2SWB L Output Voltage: Voltage is measured when 1.0mA is flow in CP2SWB pin.  
SWB L Output Voltage Voltage is measured when 1.0mA is flow in SWB pin.

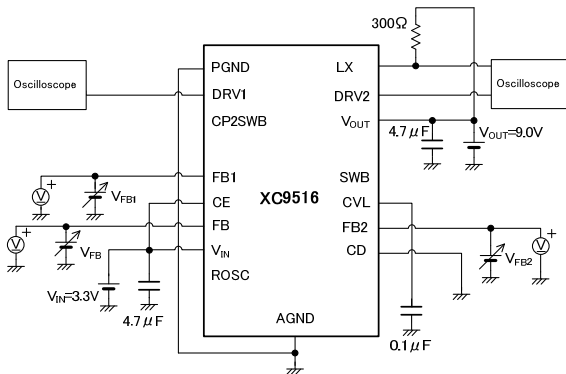
< Circuit11 CP2SWB/SWB pins Pull-up Resistance >



CP2SWB Pull-up Resistance Measurement: Output current is measured when CP2SWB pin is 1.0V.  $R=(5.5-1.0)/I$   
CP2SWB and SWB pins are internally pulled-up to  $V_{OUT}$   
SWB Pull-up Resistance Measurement: Output Current is measured when SWB pin voltage is 1.0V.  $R=(5.5-1.0)/I$   
\*CP2SWB and SWB pins are internally pulled-up to  $V_{OUT}$

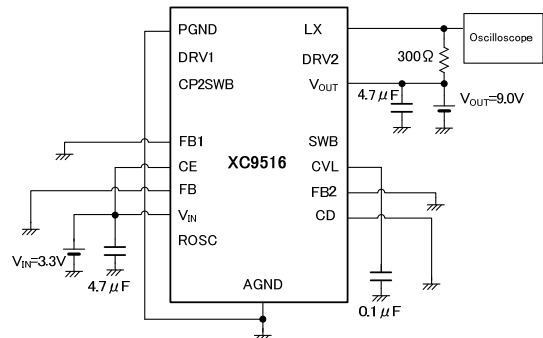
## TEST CIRCUITS (Continued)

< Circuit12 FB/FB1/FB2 Voltage Test >



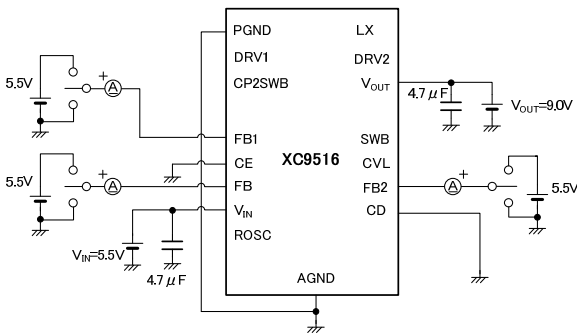
FB Voltage Measurement:  $V_{FB}=1.1V \rightarrow 0.9V$ ,  $V_{FB}$  is measured when  $L_x$  oscillation started.  
 FB1 Voltage Measurement:  $V_{FB1}=0.9V \rightarrow 1.1V$ ,  $V_{FB1}$  is measured when DRV1 oscillation started.  
 FB2 Voltage Measurement:  $V_{FB2}=1.1V \rightarrow 0.9V$ ,  $V_{FB2}$  is measured when DRV2 oscillation started.

< Circuit13 Maximum Duty Cycle >



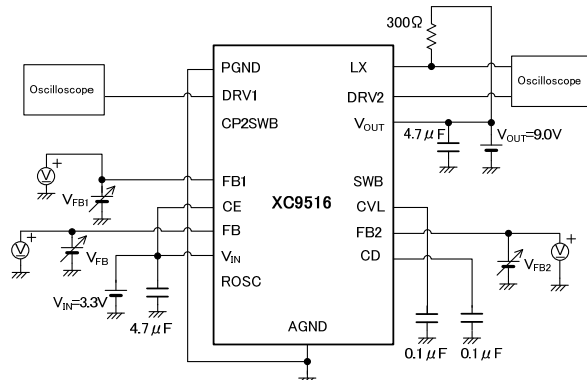
Duty cycle of  $L_x$  oscillation is measured.

< Circuit14 FB/FB1/FB2 H/L Input Current >



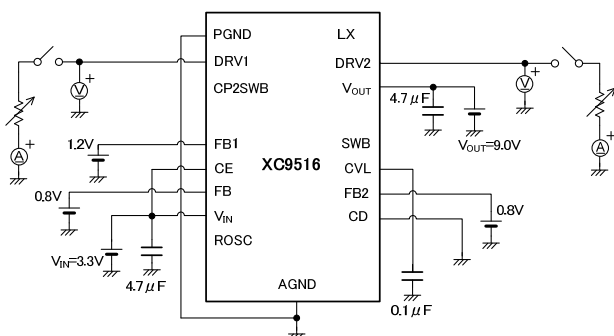
FB Input Current Measurement: Input Current is measured when FB Voltage is 5.5V/0V.  
 FB1 Input Current Measurement: Input Current is measured when FB1 Voltage is 5.5V/0V.  
 FB2 Input Current Measurement: Input Current is measured when FB2 Voltage is 5.5V/0V.

< Circuit15 FB/FB1/FB2 Short Circuit Protection >



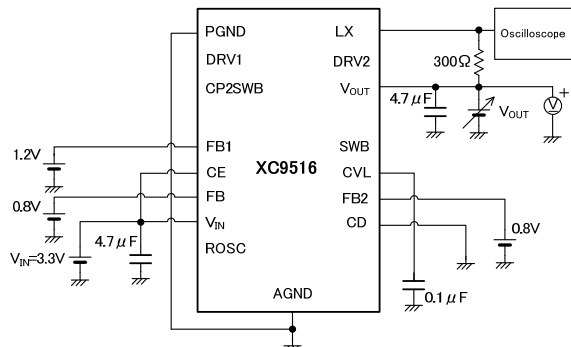
FB Short Protection Measurement:  $V_{FB}=0.9V \rightarrow 0.4V$ ,  $V_{FB}$  is measured when  $V_{FB}$  oscillation stopped.  
 FB1 Short Protection Measurement:  $V_{FB1}=1.2V \rightarrow 2.8V$ ,  $V_{FB1}$  is measured when DRV1 oscillation stopped.  
 FB2 Short Protection Measurement:  $V_{FB2}=0.9V \rightarrow 0.4V$ ,  $V_{FB2}$  is measured when DRV2 oscillation stopped.

< Circuit16 Output Impedance 1/2 >



Output Impedance1: A load current of 20mA is applied to DRV1,  
 DRV1 voltage is measured when a load is applied or not applied  $R=V/I \cdot 0.02$ .  
 Output Impedance2: A load current of 20mA is applied to DRV2,  
 DRV2 voltage is measured when a load is applied or not applied  $R=V/I \cdot 0.02$ .

< Circuit17 VOUT Over Voltage Limit Measurement >



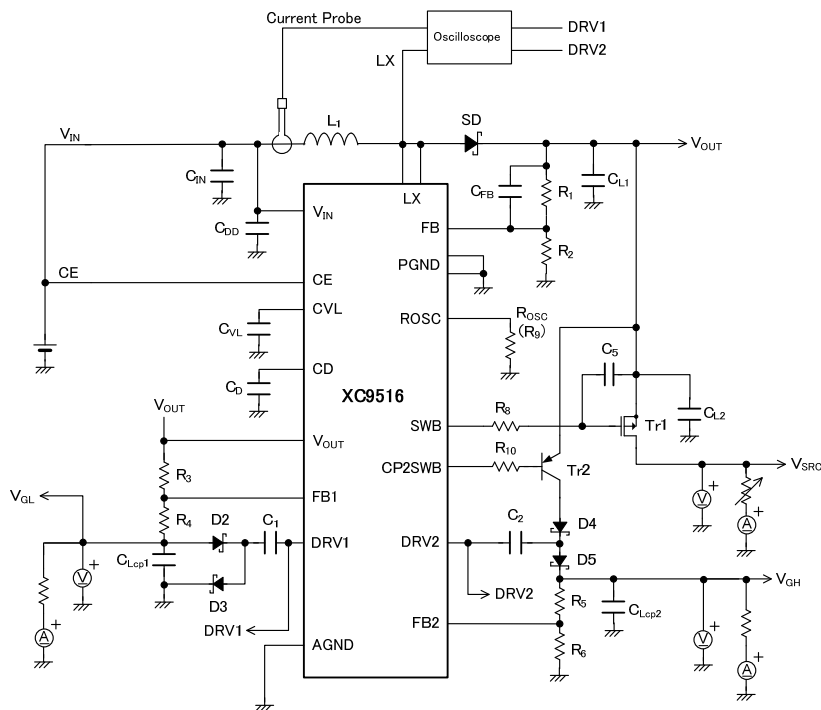
$V_{OUT}=18V \rightarrow 22V$ ,  $V_{OUT}$  is measured when  $L_x$  oscillation stopped.



## TEST CIRCUITS (Continued)

### < Circuit18 L<sub>x</sub> Current Limit >

- A load current (Variable Resistor) is connected to V<sub>SR</sub>C.  
 Coil peak current at V<sub>IN</sub>-L<sub>1</sub> is monitored by the current probe. A coil peak current is measured.



### < Circuit18 L<sub>x</sub> External Components List >

NAME	MODEL NAME	CHARACTERISTIC	MANUFACTURER
L <sub>1</sub>	LTF5022T-4R7N2R0	Coil, 4.7 μH	TDK
SD	XBS204S17	Schottky diode, 2A/40V	TOREX
D2-5	XBS104S13	Schottky diode, 1A/40V	TOREX
Tr1	XP152A11E5MR	Pch MOSFET	TOREX
Tr2	CPH3109	PNP transistor	SANYO
C <sub>IN</sub>	LMK212BJ475KG	ceramic condenser, 4.7 μF/10V	TAIYO YUDEN
C <sub>D</sub> , C <sub>VL</sub>	TMK107BJ104KA	ceramic condenser, 0.1 μF/25V	TAIYO YUDEN
C <sub>OD</sub>	TMK107BJ105KA	ceramic condenser, 1 μF/25V	TAIYO YUDEN
C <sub>L1</sub> , C <sub>L2</sub>	C3216X5R1E475M	ceramic condenser, 4.7 μF/25V	TDK
C <sub>Lcp1</sub> , C <sub>Lcp2</sub>	TMK107BJ105KA	ceramic condenser, 1 μF/25V	TAIYO YUDEN
C <sub>FB</sub>	C1608JB1H220J	ceramic condenser, 22pF/50V	TDK
C <sub>1</sub> , C <sub>2</sub>	C1608JB1H103K	ceramic condenser, 0.01 μF/50V	TDK
R <sub>1</sub>	RMC1/16K824FTP	chip resistance, 820k Ω	KAMAYA
R <sub>2</sub>	RMC1/16K104FTP	chip resistance, 100k Ω	KAMAYA
R <sub>3</sub>	RMC1/16K394FTP	chip resistance, 390k Ω	KAMAYA
R <sub>4</sub>	RMC1/16K304FTP	chip resistance, 300k Ω	KAMAYA
R <sub>5</sub>	RMC1/16K824FTP	chip resistance, 820k Ω	KAMAYA
R <sub>6</sub>	RMC1/16K753FTP	chip resistance, 75k Ω	KAMAYA
C <sub>5</sub>	C1608JB1H103K	ceramic condenser, 0.01 μF/50V	TDK
R <sub>8</sub>	RMC1/16K304FTP	chip resistance, 300k Ω	KAMAYA
R <sub>9</sub>	RMC1/16K134FTP	chip resistance, 130k Ω	KAMAYA
R <sub>10</sub>	RMC1/16K513FTP	chip resistance, 51k Ω	KAMAYA

### < Setting values when the above parts are used >

V<sub>OUT</sub>=V<sub>SR</sub>C=9.2V  
 V<sub>GL</sub>=-5.3V  
 V<sub>GH</sub>=12.0V  
 f<sub>OSC</sub>=1.0MHz

## TEST CIRCUITS (Continued)

### < Circuit19 Soft start/Start-up Sequence >

• Soft start Measurement

CE voltage is triggered on rising edge ( $0V \rightarrow V_{IN}$ ).

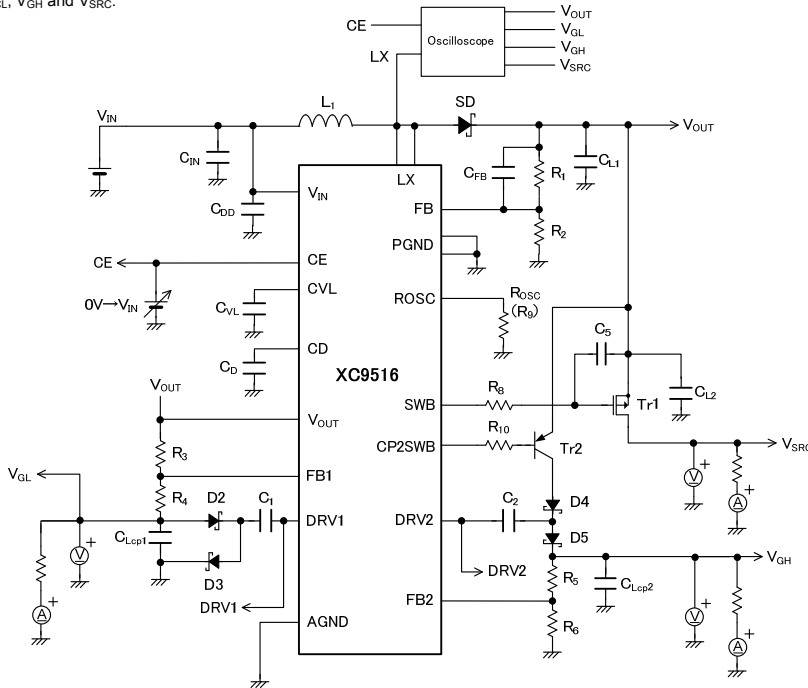
$L_x$  oscillation start from  $1.0V \leq V_{CE}$ .

$V_{OUT}$  rising time is measured.

• Start-up Sequence Measurement

Trigger on CE start-up. Sequence is checked in

the order of  $V_{OUT}$ ,  $V_{CL}$ ,  $V_{GH}$  and  $V_{SRC}$ .



### < Circuit19 $L_x$ External Components List >

NAME	MODEL NAME	CHARACTERISTIC	MANUFACTURER
$L_1$	LTF5022T-4R7N2R0	Coil, 4.7 $\mu$ H	TDK
SD	XBS204S17	Schottky diode, 2A/40V	TOREX
D2-5	XBS104S13	Schottky diode, 1A/40V	TOREX
Tr1	XP152A11E5MR	Pch MOSFET	TOREX
Tr2	GPH3109	PNP transistor	SANYO
$C_{IN}$	LMK212BJ475KG	ceramic condenser, 4.7 $\mu$ F/10V	TAIYO YUDEN
$C_D, C_{VL}$	TMK107BJ104KA	ceramic condenser, 0.1 $\mu$ F/25V	TAIYO YUDEN
$C_{DD}$	TMK107BJ105KA	ceramic condenser, 1 $\mu$ F/25V	TAIYO YUDEN
$C_{L1}, C_{L2}$	C3216X5R1E475M	ceramic condenser, 4.7 $\mu$ F/25V	TDK
$C_{Lcp1}, C_{Lcp2}$	TMK107BJ105KA	ceramic condenser, 1 $\mu$ F/25V	TAIYO YUDEN
$C_{FB}$	C1608JB1H220J	ceramic condenser, 22pF/50V	TDK
$C_1, C_2$	C1608JB1H103K	ceramic condenser, 0.01 $\mu$ F/50V	TDK
$R_1$	RMC1/16K824FTP	chip resistance, 820k $\Omega$	KAMAYA
$R_2$	RMC1/16K104FTP	chip resistance, 100k $\Omega$	KAMAYA
$R_3$	RMC1/16K394FTP	chip resistance, 390k $\Omega$	KAMAYA
$R_4$	RMC1/16K304FTP	chip resistance, 300k $\Omega$	KAMAYA
$R_5$	RMC1/16K824FTP	chip resistance, 820k $\Omega$	KAMAYA
$R_6$	RMC1/16K753FTP	chip resistance, 75k $\Omega$	KAMAYA
$C_5$	C1608JB1H103K	ceramic condenser, 0.01 $\mu$ F/50V	TDK
$R_8$	RMC1/16K304FTP	chip resistance, 300k $\Omega$	KAMAYA
$R_9$	RMC1/16K134FTP	chip resistance, 130k $\Omega$	KAMAYA
$R_{10}$	RMC1/16K513FTP	chip resistance, 51k $\Omega$	KAMAYA

### < Setting values when the above parts are used >

$$V_{OUT} = V_{SRC} = 9.2V$$

$$V_{GL} = -5.3V$$

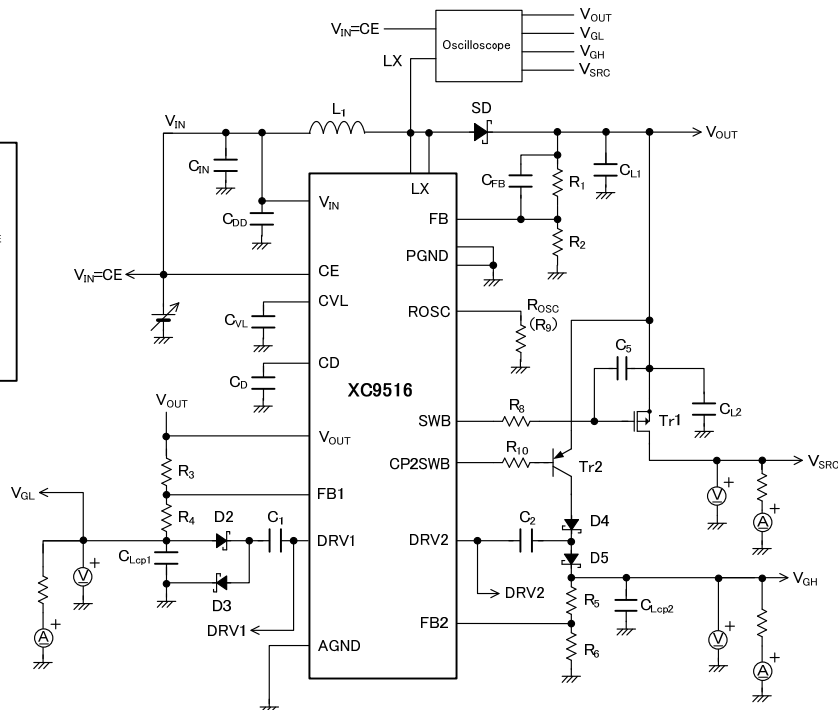
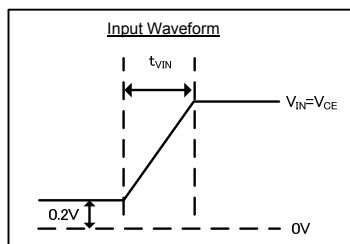
$$V_{GH} = 12.0V$$

$$f_{OSC} = 1.0MHz$$

## TEST CIRCUITS (Continued)

### < Circuit20 Input Voltage Start-up Time >

- Input Voltage Start-up Time
- $V_{SRC}$  is measured after rising  $V_{IN}$  and  $V_{CE}$  within less than 15ms.  
 $V_{IN}=V_{CE}=0.2V \rightarrow 2.5V, t_{VIN} \leq 15ms$
- Recommended Input Waveform  
Start-up with  $V_{IN}=V_{CE} \leq 0.2V$   
Start-up time  $t_{VIN} \leq 15ms$



### < Circuit20 $L_x$ External Components List >

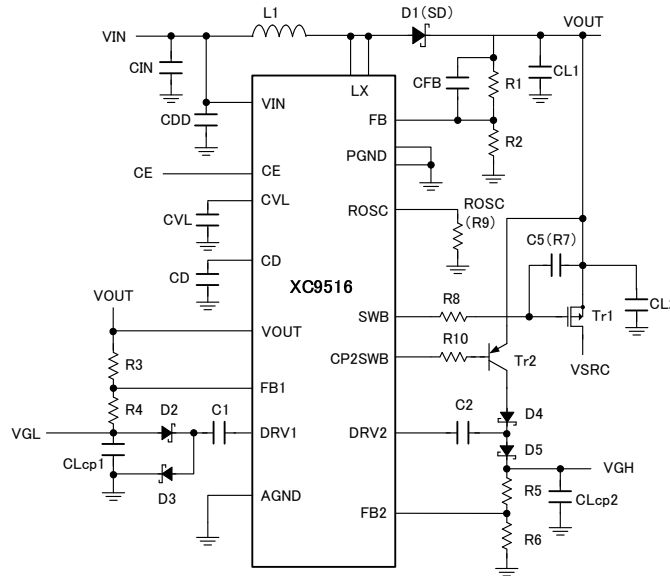
NAME	MODEL NAME	CHARACTERISTIC	MANUFACTURER
$L_1$	LTF5022T-4R7N2R0	Coil, 4.7 $\mu$ H	TDK
SD	XBS204S17	Schottky diode, 2A/40V	TOREX
D2-5	XBS104S13	Schottky diode, 1A/40V	TOREX
$Tr1$	XP152A11E5MR	Pch MOSFET	TOREX
$Tr2$	CPH3109	PNP transistor	SANYO
$C_{IN}$	LMK212BJ475KG	ceramic condenser, 4.7 $\mu$ F/10V	TAIYO YUDEN
$C_D, C_{VL}$	TMK107BJ104KA	ceramic condenser, 0.1 $\mu$ F/25V	TAIYO YUDEN
$C_{DD}$	TMK107BJ105KA	ceramic condenser, 1 $\mu$ F/25V	TAIYO YUDEN
$C_{L1}, C_{L2}$	C3216X5R1E475M	ceramic condenser, 4.7 $\mu$ F/25V	TDK
$C_{Lcp1}, C_{Lcp2}$	TMK107BJ105KA	ceramic condenser, 1 $\mu$ F/25V	TAIYO YUDEN
$C_{FB}$	C1608JB1H220J	ceramic condenser, 22pF/50V	TDK
$C_1, C_2$	C1608JB1H103K	ceramic condenser, 0.01 $\mu$ F/50V	TDK
$R_1$	RMC1/16K824FTP	chip resistance, 820k $\Omega$	KAMAYA
$R_2$	RMC1/16K104FTP	chip resistance, 100k $\Omega$	KAMAYA
$R_3$	RMC1/16K394FTP	chip resistance, 390k $\Omega$	KAMAYA
$R_4$	RMC1/16K304FTP	chip resistance, 300k $\Omega$	KAMAYA
$R_5$	RMC1/16K824FTP	chip resistance, 820k $\Omega$	KAMAYA
$R_6$	RMC1/16K753FTP	chip resistance, 75k $\Omega$	KAMAYA
$C_5$	C1608JB1H103K	ceramic condenser, 0.01 $\mu$ F/50V	TDK
$R_8$	RMC1/16K304FTP	chip resistance, 300k $\Omega$	KAMAYA
$R_9$	RMC1/16K134FTP	chip resistance, 130k $\Omega$	KAMAYA
$R_{10}$	RMC1/16K513FTP	chip resistance, 51k $\Omega$	KAMAYA

### < Setting values when the above parts are used >

$V_{OUT}=V_{SRC}=9.2V$   
 $V_{GL}=-5.3V$   
 $V_{GH}=12.0V$   
 $f_{OSC}=1.0MHz$

## OPERATIONAL EXPLANATION

XC9516 series includes following blocks which are a reference voltage source, an oscillation circuit connecting to an external  $R_{OSC}$  register, a UVLO circuit to prevent malfunction in low voltage operation, internal power supply regulator connecting external  $C_{VL}$  capacitor, a step-up DC/DC converter, step-up charge pump and inverting charge pump, a short circuit protection circuit, an over current sensing circuit, an over voltage sensing circuit and a thermal shutdown circuit.



The step-up DC/DC converter consists of a ramp wave circuit created from the above mentioned oscillation circuit, an error amplifier to compare feedback voltage through external resistor network from  $V_{OUT}$  output voltage and internal reference voltage, a PWM comparator to decide duty cycle by comparing ramp wave form created by the above mentioned ramp wave circuit and error amplifier output, a phase compensation circuit and current feedback circuit for output voltage stabilization, a N-channel MOS driver transistor to provide duty cycle on-time from  $L_X$  pin, a current limit circuit to limit the current to flow the N-channel MOS driver transistor, a over-voltage protection circuit operated at 1.3 typical to protect the devices connecting to the  $V_{OUT}$  output voltage pin.

A multi-loop feedback control by feedback voltage and N-channel MOS driver transistor provides stable output voltage operation so that low ESR ceramic capacitor can be used.

The inverting voltage charge pump consists of an error amplifier to compare internal voltage reference and the feedback voltage through external resistor network from  $V_{OUT}$  output voltage, output impedance control circuit to adjust output impedance by output level of the error amplifier, driver circuit for charge pump operation.

The step-up charge pump consists of an error amplifier to compare internal voltage reference and the feedback voltage through external resistor network from  $V_{OUT}$  output voltage, output impedance control circuit to adjust output impedance by output level of the error amplifier, driver circuit for charge pump operation.

### <Reference Voltage Source>

The reference voltage source provides the reference voltage to ensure stable output voltage of the IC.

### <Oscillation Circuit >

The oscillation circuit determines switching frequency. The frequency can be changed by external resistance  $R_{OSC}$  in a range of 300 kHz to 1.2MHz. When  $R_{OSC}$  pin is left open, the frequency is fixed at 300kHz.

When the frequency is low, efficiency is high at light load. When the frequency is high, "L" value of coil will be low and makes space saving.

The oscillation frequency is calculated by the following formula (Equation 1).

$$R_{OSC} = 95 \times 10^9 / (f_{OSC} - 300 \times 10^3) \cdot \cdot \cdot \text{ (Equation 1)}$$

where  $f_{OSC}$  denotes a setting frequency.

### < Ramp Wave Circuit >

This circuit is used to produce ramp waveforms needed for PWM operation.

### < Error Amplifier for DC/DC>

The error amplifier is designed to monitor output voltage. The error amplifier compares the reference voltage with the feedback voltage through the external divider resistors. When a feedback voltage is lower than the reference voltage, the output voltage of the error amplifier is increased.

## OPERATIONAL EXPLANATION (Continued)

### <External Resistors for setting Output Voltages>

A setting output voltage  $V_{OUT}$  for the step-up DC/DC is calculated by the following formula (Equation 2).

$$V_{OUT} = V_{FB} \times (R1 + R2) / R2 \dots \dots \text{(Equation 2)}$$

$$V_{FB1}=1.0V, R1 + R2 < 1000k\Omega$$

A setting output voltage  $V_{GL}$  for the negative charge pump is calculated by the following formula (Equation 3).

$$V_{GL} = V_{FB1} - (V_{OUT} - V_{FB1}) \times R4 / R3 \dots \dots \text{(Equation 3)}$$

$$V_{FB1}=1.0V, R3 + R4 < 1000k\Omega$$

A setting output voltage  $V_{GH}$  for the step-up charge pump is calculated by the following formula (Equation 4).

$$V_{GH} = V_{FB2} \times (R5 + R6) / R6 \dots \dots \text{(Equation 4)}$$

$$V_{FB2}=1.0V, R5 + R6 < 1000k\Omega$$

### <Regulator for Internal Power Circuit >

The XC9516 series includes a regulator for internal power circuit in order to stabilize operation. Its power source is taken from  $V_{IN}$  and  $V_{OUT}$ . An external capacitor  $C_{VL}=0.1 \mu F$  is required to stabilize this internal power supply.

### <UVLO Circuit >

When the input voltage  $V_{IN}$  falls below a threshold voltage 1.87V (TYP.), all driver transistors will be forced off to prevent malfunction. When the  $V_{IN}$  voltage becomes 2.31V (TYP.) or higher, the UVLO function is released and the IC performs the soft-start function to initiate startup operation.

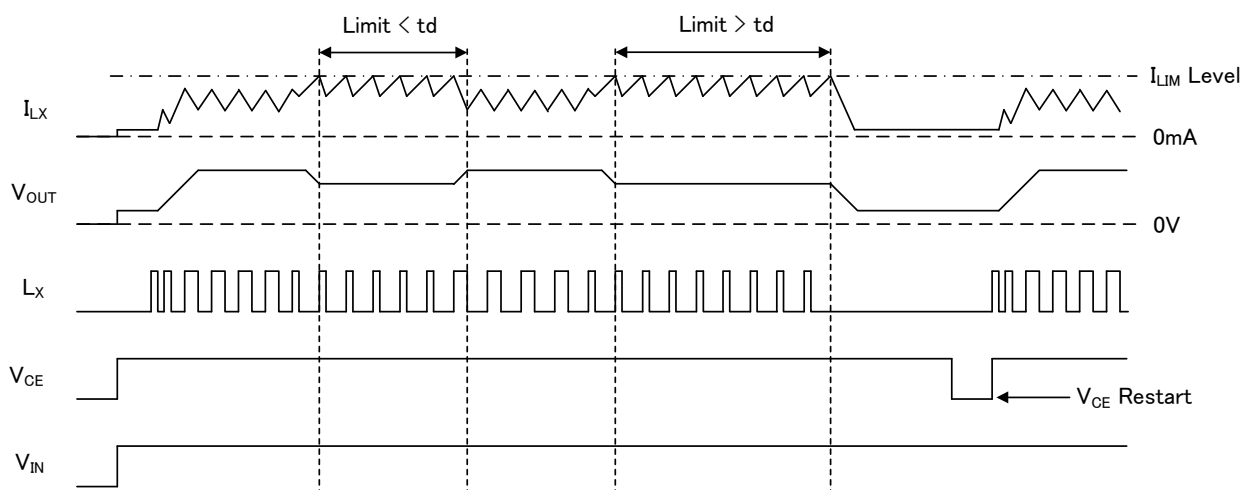
### < Current Limit >

The current limiter monitors the current flowing through the N-channel MOS driver transistor connected to the Lx pin, and features a combination of the current limit and latch function.

- ①When the driver current is greater than a specific level (a peak current of inductor), the constant-current type current limit function operates to turn off the pulses from the Lx pin at any given timing.
- ②When the driver transistor is turned off, the limiter circuit is then released from the current limit detection state.
- ③At the next pulse, the driver transistor is turned on. However, the transistor is immediately turned off in the case of an over-current state.
- ④When the over-current state is eliminated, the IC resumes its normal operation.

The IC waits for the over-current state to end by repeating the steps ①~③. During a latch delay time which was set by an external capacitor with CD pin, if the ①~③ over-current state is repeated, all driver transistors in the step-up DC/DC converter, the step-up charge pump and the voltage inverting charge pump will be maintained to turn off. Once the IC is in suspension mode, operations can be resumed by either turning the IC off via the CE pin, or by restoring power to the  $V_{IN}$  pin.

Depending on the state of a substrate, it may result in the case where the latch delay time may become longer or the operation may not be latched. Please locate an input capacitor to the  $C_D$  pin as close as possible.



Current Limit Timing Chart

## ■ OPERATIONAL EXPLANATION (Continued)

### <Short-circuit Detection Circuit >

When either output voltage falls below the set voltage while monitoring each feedback voltage of a step-up DC/DC converter, step-up charge pump and inverting charge pump it is allowed as short-circuit so that latch delay circuit starts operation. If the output voltage goes back in the range of the set voltage within the latch delay time, the start of the latch delay circuit will be released. When output voltage is not recovered, all of the driver transistors will be turned off and latched after the latch delay time.

### <Latch Delay Circuit >

Where each short-circuit detection circuit detects output voltage short-circuit or when the over-current detection circuit detects over-current of the L<sub>X</sub> pin, All driver transistors in a step-up DC/DC converter, step-up charge pump and inverting charge pump will be turned off and latched after the delay time which was set by an external capacitor to the C<sub>D</sub> pin. In order to release the latch, either turning the IC off and on via the CE pin or restoring power supply (V<sub>IN</sub> pin) should be selected. A setting delay time t<sub>D</sub> is calculated by the following formula (Equation 5).

$$C_D = t_d \times 5.5 \times 10^{-6} / 1.0 \cdot \cdot \cdot \text{(Equation 5)}$$

5.5 x 10<sup>-6</sup> (C<sub>D</sub> Pin Charge Current, Typical)  
1.0 (C<sub>D</sub> Pin Detect Voltage, TYP.)

### <Thermal Shutdown>

For protection against heat damage of the ICs, thermal shutdown function monitors chip temperature. The thermal shutdown circuit starts operating and all of the driver transistors will be turned off when the chip's temperature reaches 150°C. When the temperature drops to 130°C or less after shutting of the current flow, the IC performs the soft start function to initiate output startup operation.

### <Over-voltage Protection>

The over-voltage limit monitors the voltage of V<sub>OUT</sub> pin. All of the driver transistors will be turned off when the voltage of V<sub>OUT</sub> pin elevates and beyond 21V (TYP.). In order to release the latch, either turning the IC off and on via the CE pin or restoring power supply (V<sub>IN</sub> pin) should be selected.

## ■ OPERATIONAL EXPLANATION (Continued)

### <Start-up Sequence>

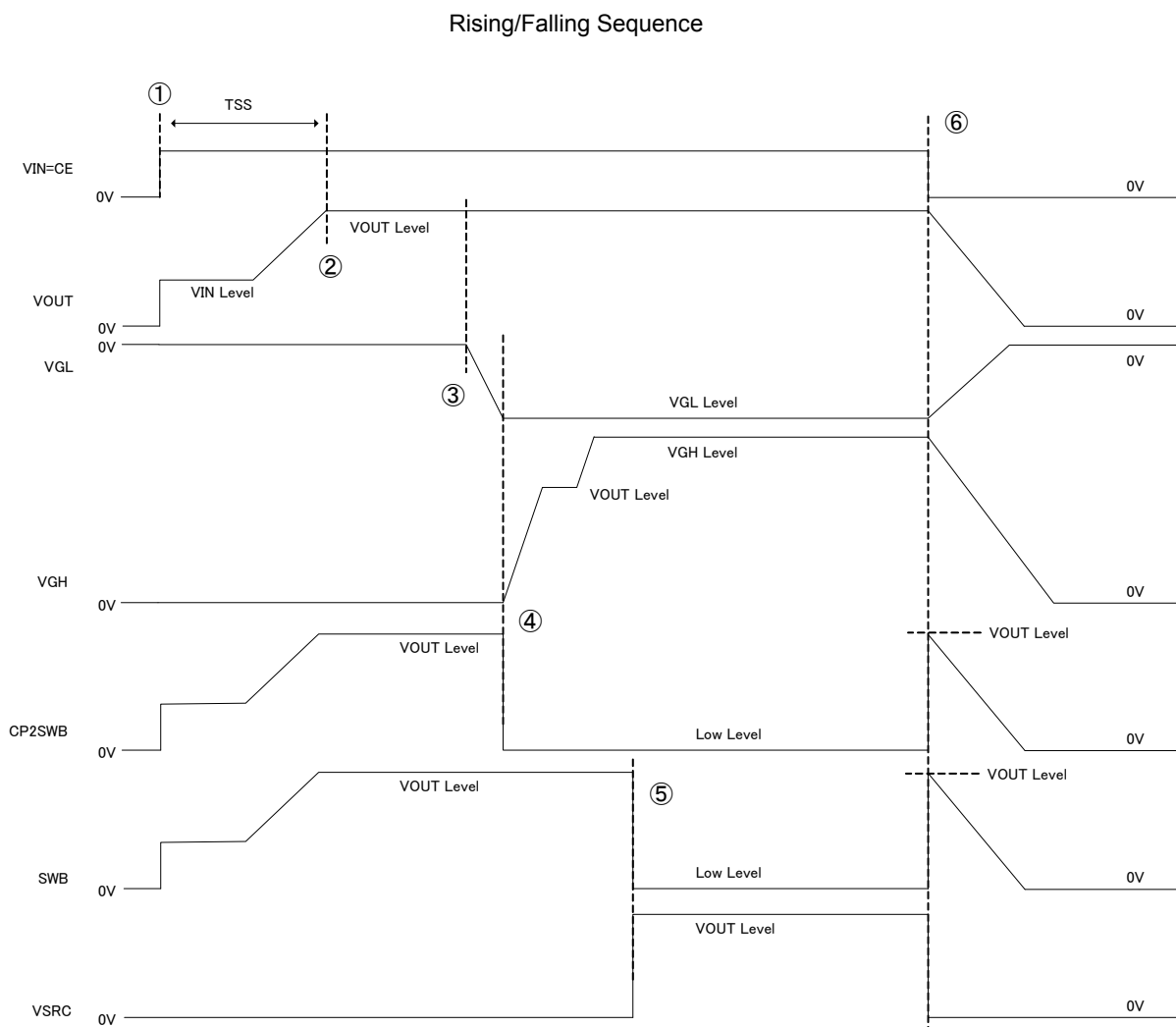
After  $V_{IN}$  input with CE same time, the DC/DC starts to operate to set  $V_{OUT}$  voltage. After the DC/DC start-up, a negative inverting charge pump starts to operate to see  $V_{GL}$  voltage. After the negative charge pump, CP2SWB low signal output turns Tr2 on to make a positive charge pump starts to operate to see  $V_{GH}$  voltage. After  $V_{GH}$  output, SWB low signal output turn Tr1 on for  $V_{SRC}$  output. The CP2SWB and SWB pins are internally pulled up to  $V_{OUT}$ , therefore, this  $V_{OUT}$  level is kept until a low signal come out. When falling,  $V_{OUT}$ ,  $V_{GL}$ , and  $V_{GH}$  outputs go off after  $V_{IN}$  and  $V_{CE}$  goes to ground. The  $V_{SRC}$  output will be turned off when the Tr2 goes off.

### When Rising

- ①  $V_{IN}=V_{CE}$  input
- ②  $V_{OUT}$  Rising completed
- ③  $V_{GL}$  Operation started
- ④ CP2SWB Low output,  $V_{GH}$  rising started
- ⑤ SWB Low output,  $V_{SRC}$  output

### When Falling

- ⑥  $V_{IN}=V_{CE}=0V$ ,  $V_{OUT}$ ,  $V_{GL}$ ,  $V_{GH}$ ,  $V_{SRC}$  output is OFF



## NOTES ON USE

- For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.
- Switching regulators like step-up DC/DC converters may cause spike noise and/or ripple voltage. These amounts are greatly affected by peripheral components (coil inductance values, capacitor value and substrate layout of peripheral circuit). Test and inspect the actual circuits thoroughly before use.
- An input capacitor should be placed near the IC  $V_{IN}$  pin as much as possible.
- As for power-on, when CE pin is used with connecting to  $V_{IN}$  pin,  $V_{IN}-V_{CE}$  voltage should begin rising from below 2.0V. Rise time should be less than 15ms. (Please refer to Figure 1.)  
On the other hand, when CE pin is used independently from  $V_{IN}$  pin, CE pin voltage should be started to rise after  $V_{IN}$  pin voltage rising. (Please refer to Figure 2.)
- GND pattern should be layouted to get a same level of voltage for AGND pin, PGND pin, and package heatsink.
- When current over limited value (peak current) flows for a specified period, current limit circuit will turn off a built-in driver transistor (integral latch circuit). Until the circuit detects the latch delay time and turns off the build-in driver transistor, current of limited level continues to flow, so please take full care of rating of coils.
- In case of  $V_{GL}$  voltage,  $V_{GH}$  voltage may overshoots or undershoots when power supply rise, please put speed-up capacitor (CFB1, CFB2) between FB1 pin and  $V_{GL}$ , FB2 pin and  $V_{GH}$ . (Please refer to figure 3 and 4.)
- When load of inverting charge pump and step-up charge pump are with no load and load current of step-up DC/DC converter is large, the output of the each charge pump may become unstable by switch of step-up DC/DC converter. In case of that, please put a ferrite bead (L2) into a driver output (DRV1 pin and DRV2 pin) of the each charge pump. (Please refer to figure 4.)
- Torex places an importance on improving our products and its reliability.  
However, by any possibility, we would request user fail-safe design and post-aging treatment on system or equipment.

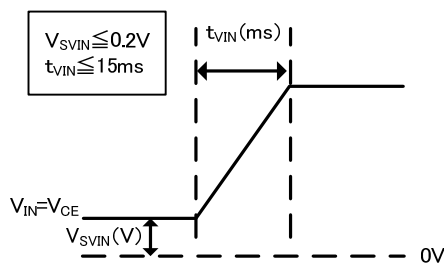


Figure 1. (Recommended for input wave form for  $V_{IN}=V_{CE}$ )

Rising is recommended from less than 0.2V.

Rise time should be within 15ms.

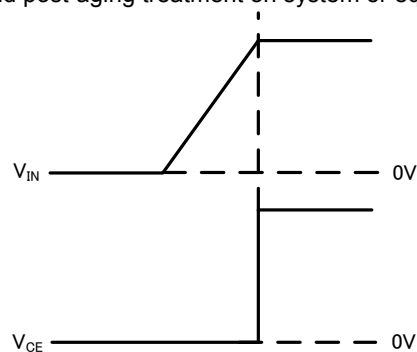


Figure 2. (Recommended for input wave form for  $V_{IN}$  pin and CE pin are input separately.)

CE should be rising after  $V_{IN}$  rising.

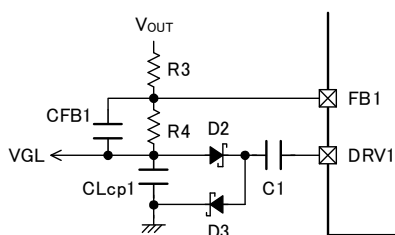


Figure 3.

Connection diagram for speed-up capacitor (CFB1)

CFB1 is connected to between FB1 pin and  $V_{GL}$

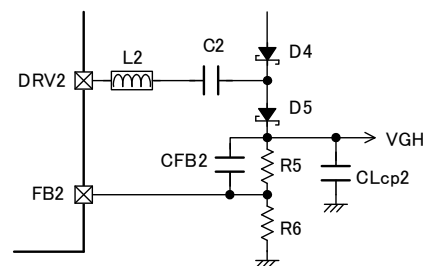


Figure 4.

Connection diagram for a ferrite bead / speed-up capacitor (CFB2)

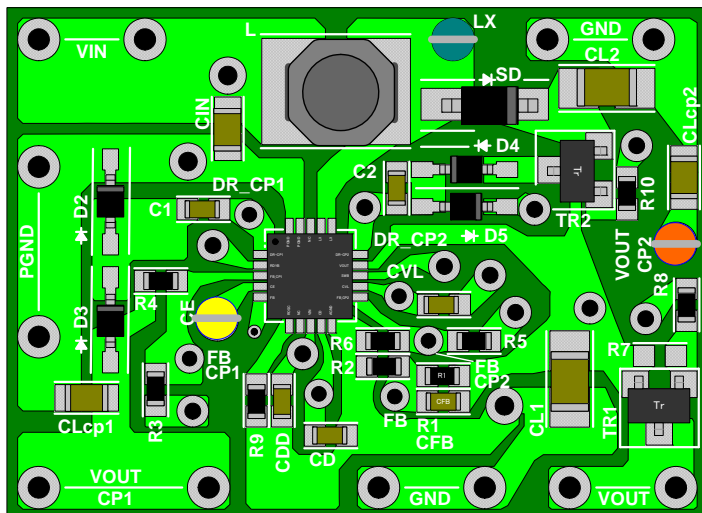
L2 (ferrite bead) is connected to between DRV2 pin and C2.

CFB2 is connected to between FB2 pin and  $V_{GH}$ .



**NOTES ON USE (Continued)**

TOP VIEW (Layout example)



\*Notes for Board

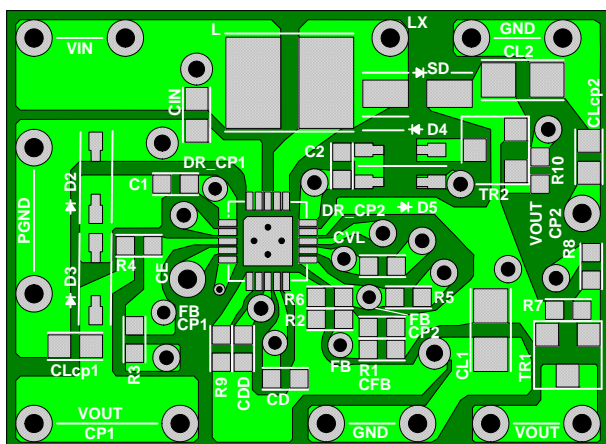
VOUTCP1=V<sub>GL</sub>

VOUTCP2=V<sub>GH</sub>

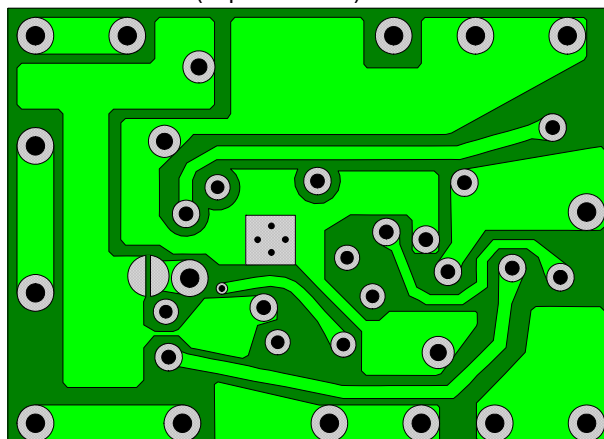
**Components List**

DESIGNATOR	PRODUCT	NOTE	MAKER	QTY
IC	XC9516A21AZR-G		TOREX	1
L	LTF5022T-4R7N2R0	Coil, 4.7 $\mu$ H	TDK	1
SD	XBS204S17	Schottky Barrie Diodes, 2A/40V	TOREX	1
D2, D3, D4, D5	XBS104S13	Schottky Barrie Diodes, 1A/40V	TOREX	4
Tr1	XP152A11E5MR	P-ch MOS FET	TOREX	1
Tr2	CPH3109	PNP Transistor	SANYO	1
CIN	LMK212BJ475KG	Ceramic Capacitor, 4.7 $\mu$ F/10V	TAIYO UDEN	1
CD, CVL	TMK107BJ104KA	Ceramic Capacitor, 0.1 $\mu$ F/25V	TAIYO UDEN	2
CDD	TMK107BJ105KA	Ceramic Capacitor, 1 $\mu$ F/25V	TAIYO UDEN	1
CL1, CL2	C3216X5R1E475M	Ceramic Capacitor, 4.7 $\mu$ F/25V	TDK	2
CLcp1, CLcp2	TMK107BJ105KA	Ceramic Capacitor, 1 $\mu$ F/25V	TAIYO UDEN	2
CFB	C1608JB1H220J	Ceramic Capacitor, 22pF/50V	TDK	1
C1, C2	C1608JB1H103K	Ceramic Capacitor, 0.01 $\mu$ F/50V	TDK	2
R1	RMC1/16K824FTP	Chip Resistor, 820k $\Omega$	KAMAYA ELECTRIC	1
R2	RMC1/16K104FTP	Chip Resistor, 100k $\Omega$	KAMAYA ELECTRIC	1
R3	RMC1/16K394FTP	Chip Resistor, 390k $\Omega$	KAMAYA ELECTRIC	1
R4	RMC1/16K304FTP	Chip Resistor, 300k $\Omega$	KAMAYA ELECTRIC	1
R5	RMC1/16K824FTP	Chip Resistor, 820k $\Omega$	KAMAYA ELECTRIC	1
R6	RMC1/16K753FTP	Chip Resistor, 75k $\Omega$	KAMAYA ELECTRIC	1
R7	C1608JB1H103K	Ceramic Capacitor, 0.01 $\mu$ F/50V	TDK	1
R8	RMC1/16K304FTP	Chip Resistor, 300k $\Omega$	KAMAYA ELECTRIC	1
R9	RMC1/16K134FTP	Chip Resistor, 130k $\Omega$	KAMAYA ELECTRIC	1
R10	RMC1/16K513FTP	Chip Resistor, 51k $\Omega$	KAMAYA ELECTRIC	1
L2	MMZ1608S400A	Ferrite bead, 40 $\Omega$ @100MHz	TDK	1

TOP VIEW

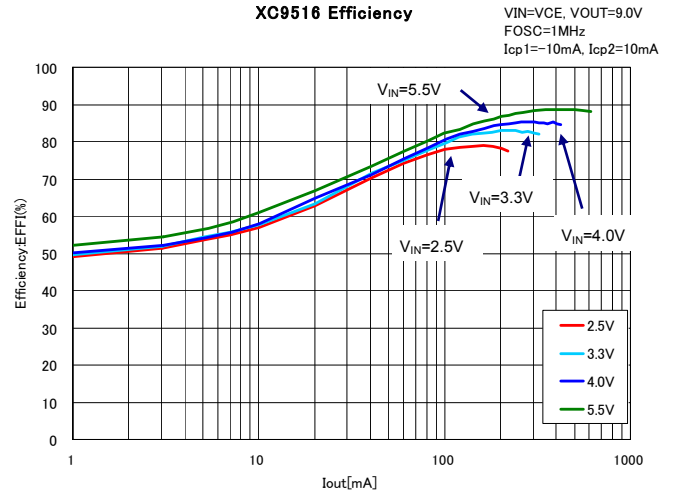
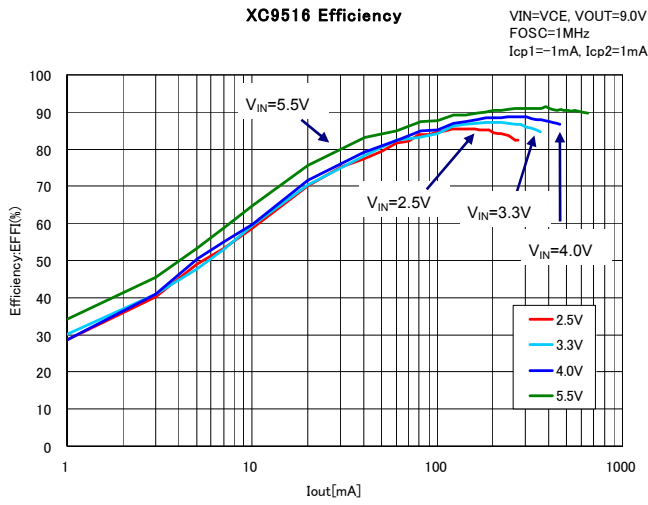


BOTTOM VIEW (Flip horizontal)

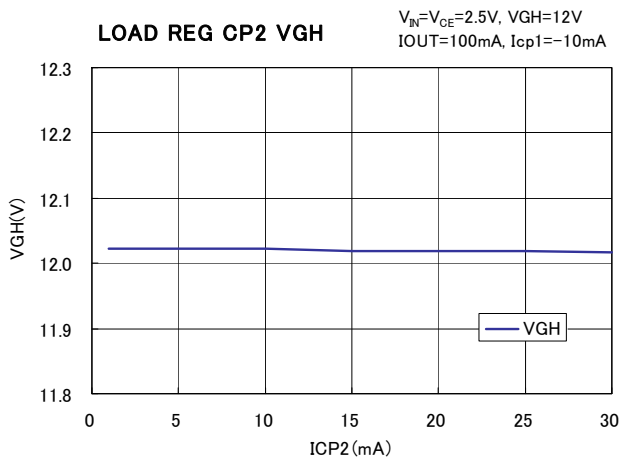
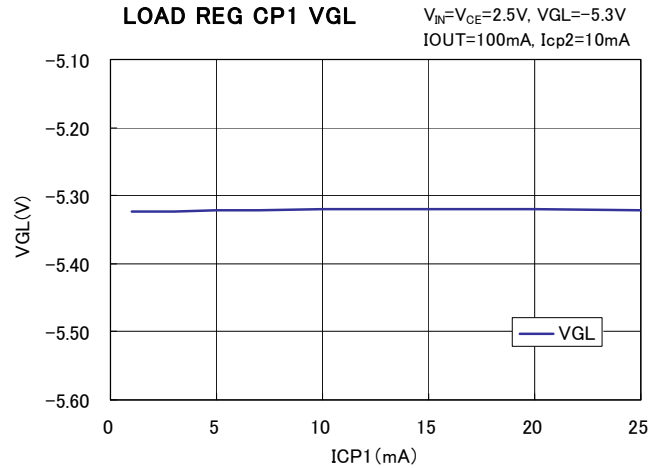
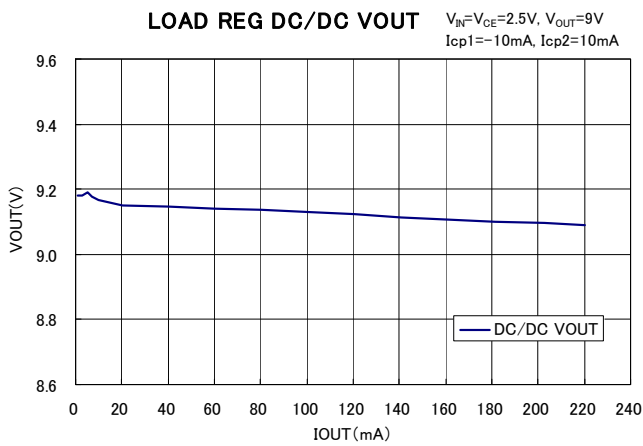


## TYPICAL PERFORMANCE CHARACTERISTICS

### (1) Efficiency vs. Output Current

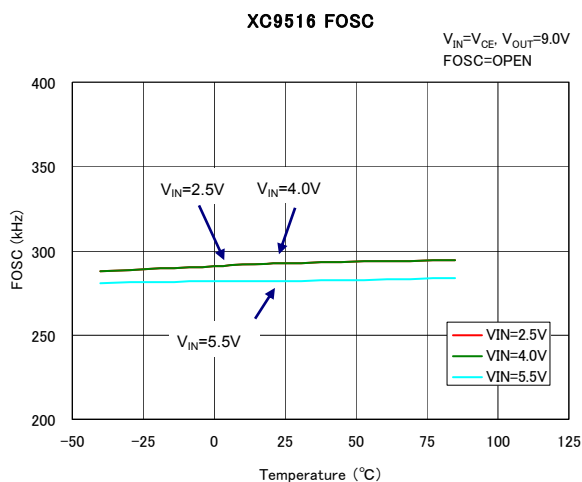


### (2) Output Voltage vs. Output Current

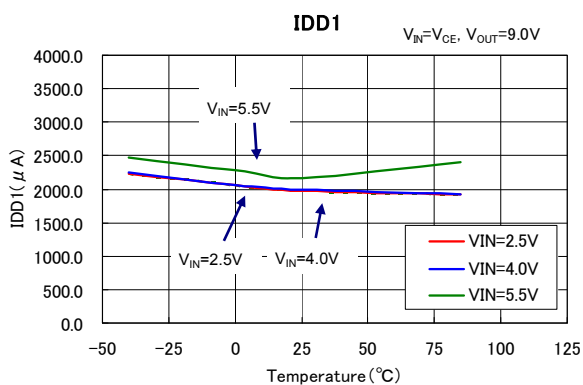


## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

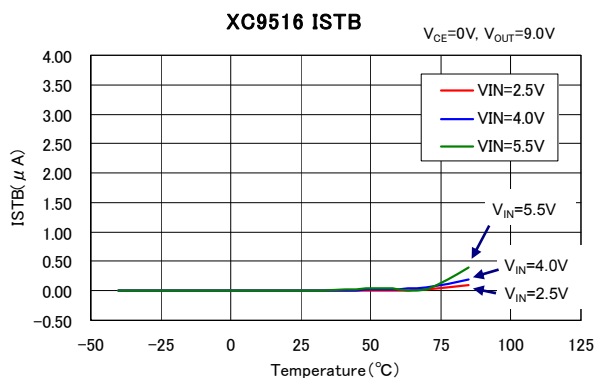
(3) Frequency vs. Ambient Temperature



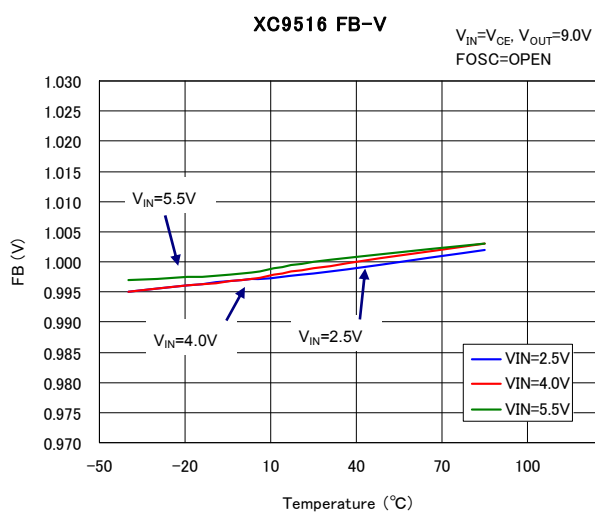
(4) Supply Current vs. Ambient Temperature



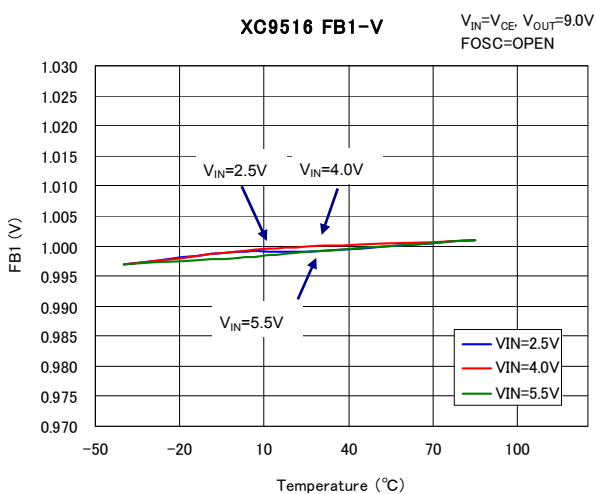
(5) Stand-by Current vs. Ambient Temperature



(6) FB Voltage vs. Ambient Temperature

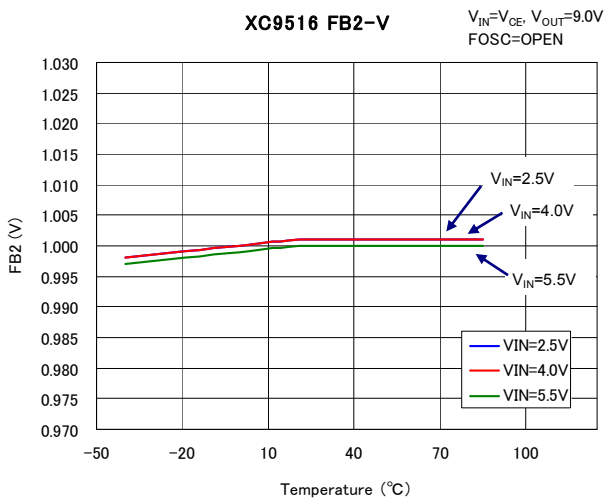


(7) FB1 Voltage vs. Ambient Temperature

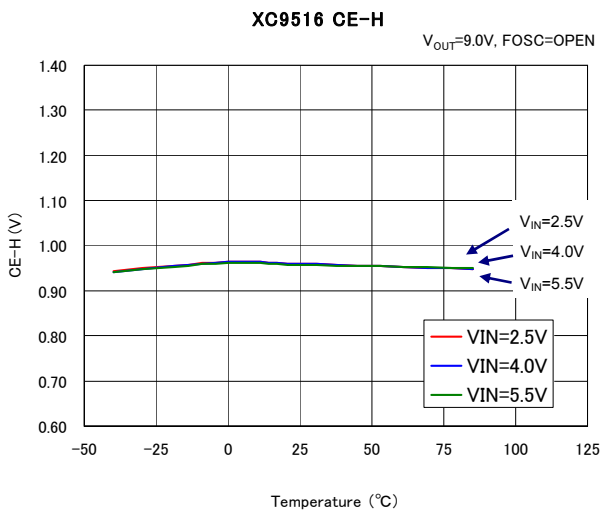


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

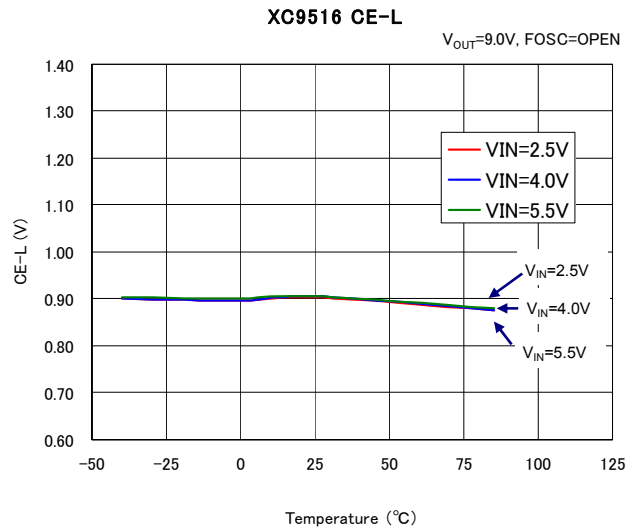
(8) FB2 Voltage vs. Ambient Temperature



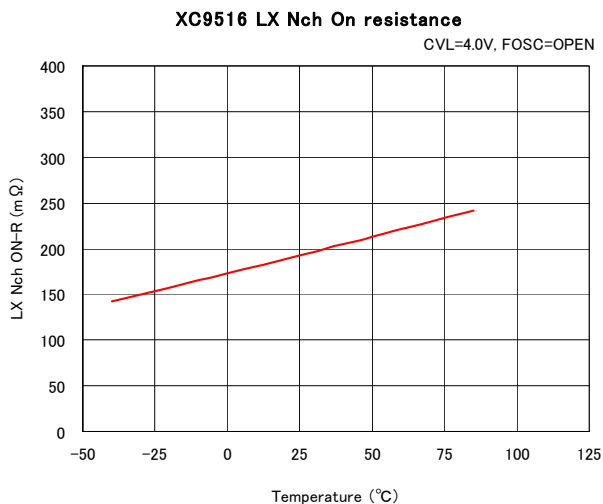
(9) CE "H" Voltage vs. Ambient Temperature



(10) CE "L" Voltage vs. Ambient Temperature

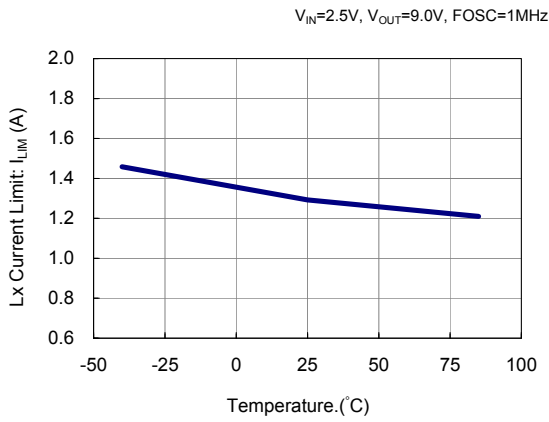


(11) LX Pin N-ch Driver ON Resistance vs. Ambient Temperature

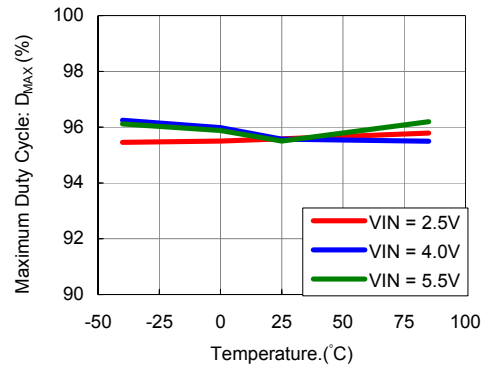


## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

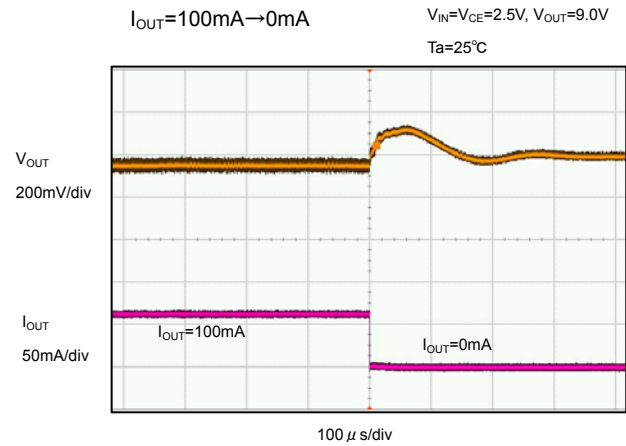
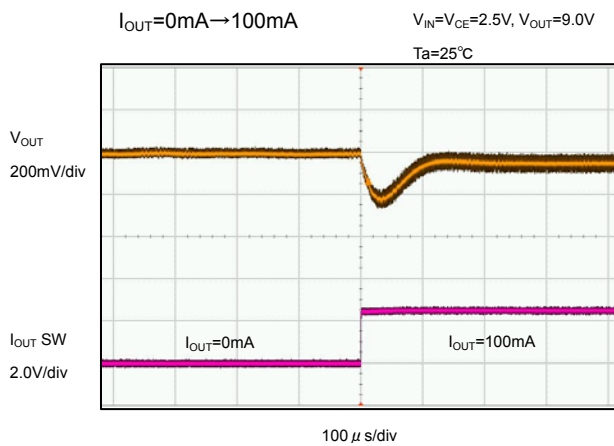
(12) LX Current Limit vs. Ambient Temperature



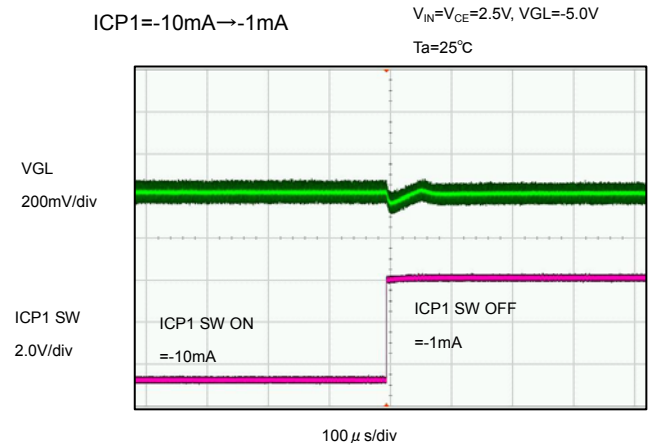
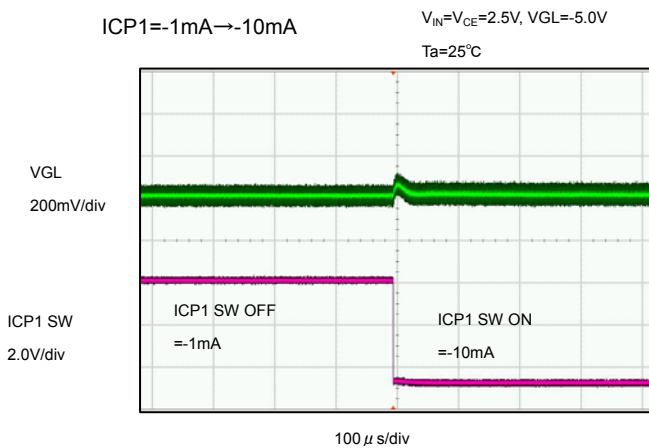
(13) Maximum Duty Cycle vs. Ambient Temperature



(14) Load Transient Response 1 vs. DC/DC Output ( $V_{OUT}$ )

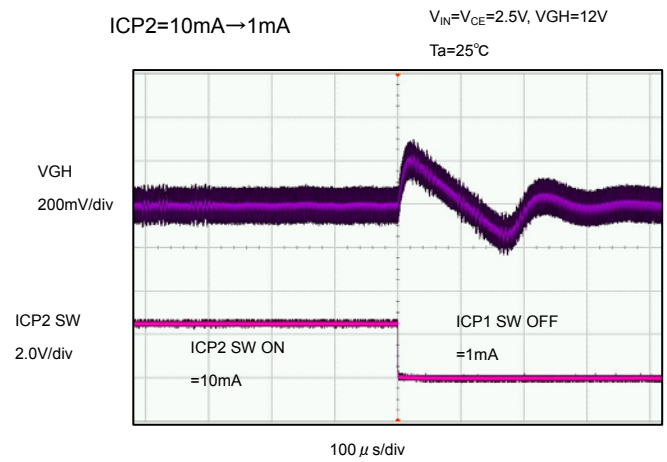
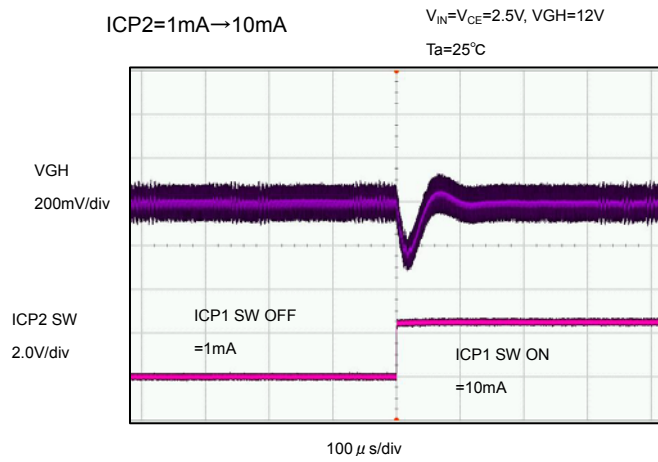


(15) Load Transient Response 2 vs. CP1 Output (VGL)

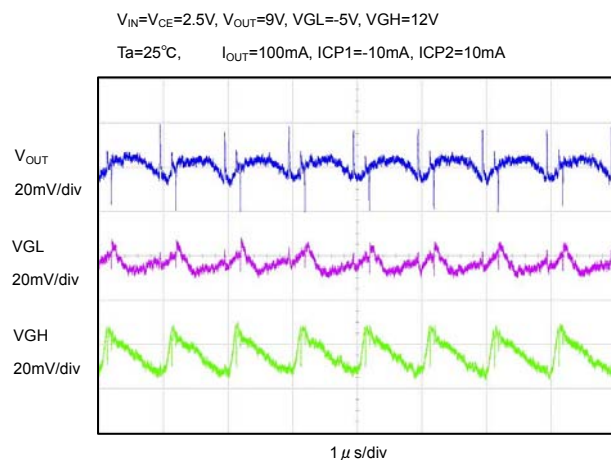
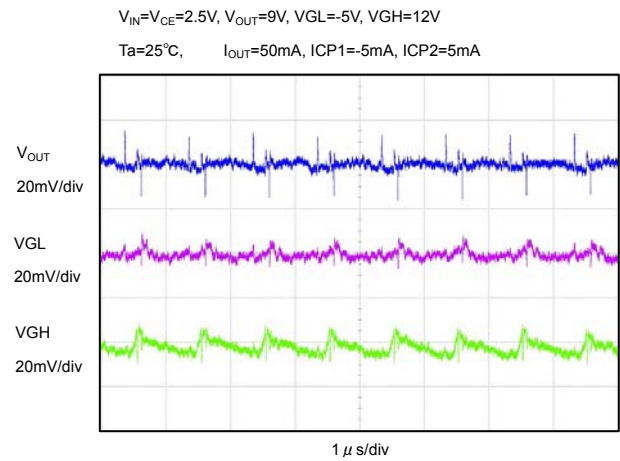
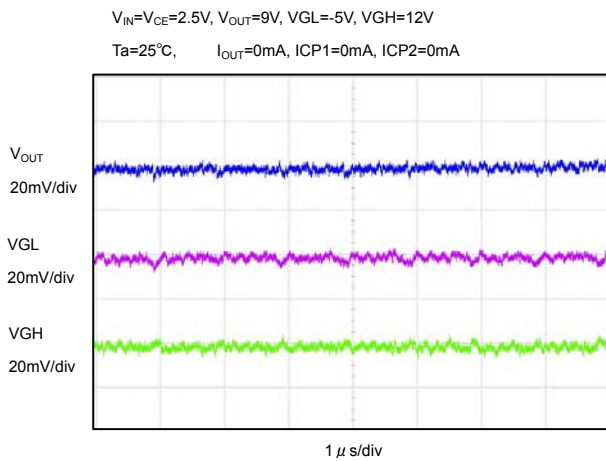


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(16) Load Transient Response 3 vs. CP2 Output (VGH)

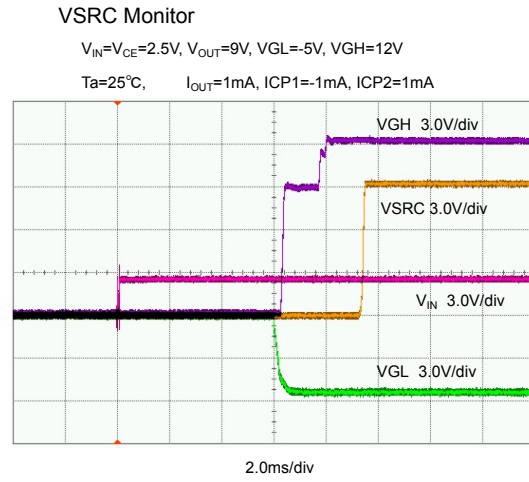
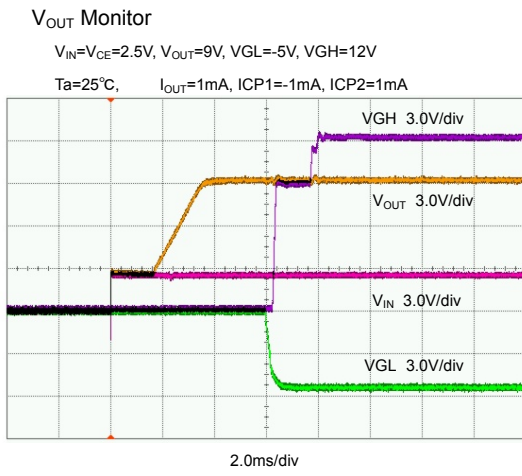


(17) Ripple Rejection Rat vs. Output Current



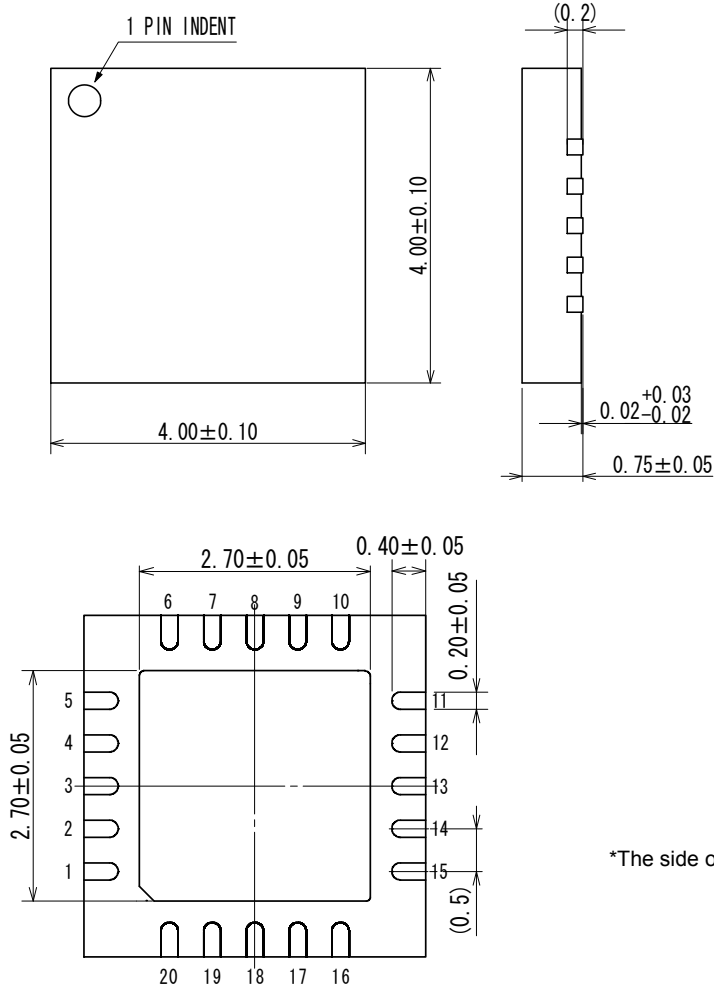
## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (18) Start-up Sequence



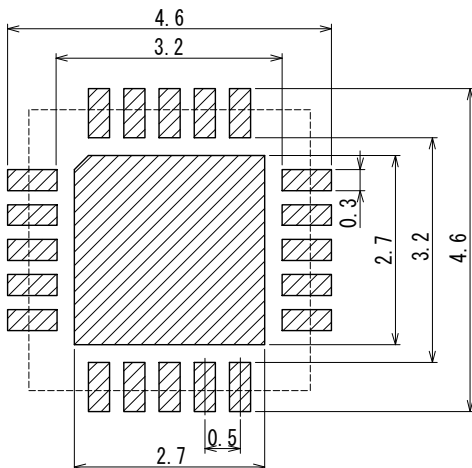
## PACKAGING INFORMATION

### ●QFN-20 (Unit: mm)

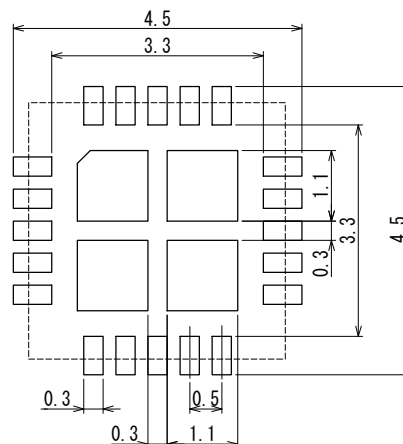


\*The side of pins are not gilded, but nickel is used.

### ●QFN-20 Reference Pattern Layout (Unit: mm)



### ●QFN-20 Reference Metal Mask Design (Unit: mm)

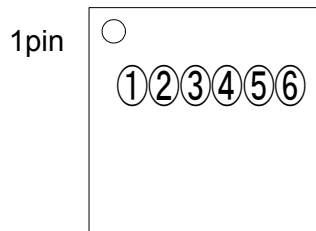


Solder Thickness : 120 μm (reference)



## MARKING RULE

QFN20



① represents product series

MARK	PRODUCT SERIES
0	XC9516*****-G

② represents UVLO setting voltage and LX detect over current

MARK	UVLO VOLTAGE	LX DETECT OVER CURRENT	PRODUCT SERIES
A	Detect : 1.87V, Hysteresis Width : 0.44V	1.3A	XC9516A**A**-G

③④ represents  $V_{OUT}$  detect over voltage

MARK		$V_{OUT}$ DETECT OVER VOLTAGE (e.g.)	PRODUCT SERIES
③	④		
2	1	21V	XC9516*21***-G

⑤⑥ represents production lot number

01~09, 0A~0Z, 11···9Z, A1~A9, AA~Z9, ZA~ZZ repeated

(G, I, J, O, Q, W excluded)

\*No character inversion used.

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