

# NVMFS5C680NL

## Power MOSFET

60 V, 27.5 mΩ, 21 A, Single N-Channel

### Features

- Small Footprint (5 x 6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVMFS5C680NLWF – Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter                                                                     | Symbol                                            | Value                     | Unit             |
|-------------------------------------------------------------------------------|---------------------------------------------------|---------------------------|------------------|
| Drain-to-Source Voltage                                                       | $V_{DS}$                                          | 60                        | V                |
| Gate-to-Source Voltage                                                        | $V_{GS}$                                          | $\pm 20$                  | V                |
| Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3, 4)                   | Steady State                                      | $T_C = 25^\circ\text{C}$  | $I_D$ 21 A       |
|                                                                               |                                                   | $T_C = 100^\circ\text{C}$ | 15               |
| Power Dissipation $R_{\theta JC}$ (Notes 1, 2, 3)                             | Steady State                                      | $T_C = 25^\circ\text{C}$  | $P_D$ 24 W       |
|                                                                               |                                                   | $T_C = 100^\circ\text{C}$ | 12               |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1 & 3, 4)                     | Steady State                                      | $T_A = 25^\circ\text{C}$  | $I_D$ 8.1 A      |
|                                                                               |                                                   | $T_A = 100^\circ\text{C}$ | 5.7              |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 3)                                | Steady State                                      | $T_A = 25^\circ\text{C}$  | $P_D$ 3.4 W      |
|                                                                               |                                                   | $T_A = 100^\circ\text{C}$ | 1.7              |
| Pulsed Drain Current                                                          | $T_A = 25^\circ\text{C}$ , $t_p = 10 \mu\text{s}$ | $I_{DM}$ 87               | A                |
| Operating Junction and Storage Temperature                                    | $T_J$ , $T_{stg}$                                 | -55 to +175               | $^\circ\text{C}$ |
| Source Current (Body Diode)                                                   | $I_S$                                             | 20                        | A                |
| Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 1.5 \text{ A}$ ) | $E_{AS}$                                          | 44.6                      | mJ               |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s)             | $T_L$                                             | 260                       | $^\circ\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

| Parameter                                   | Symbol          | Value | Unit               |
|---------------------------------------------|-----------------|-------|--------------------|
| Junction-to-Case – Steady State (Note 3)    | $R_{\theta JC}$ | 6.3   | $^\circ\text{C/W}$ |
| Junction-to-Ambient – Steady State (Note 3) | $R_{\theta JA}$ | 44    |                    |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi ( $\Psi$ ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

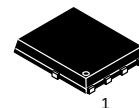
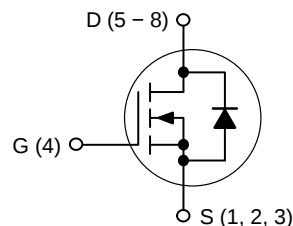


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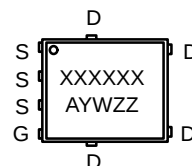
| $V_{(BR)DSS}$ | $R_{DS(on)}$ MAX | $I_D$ MAX |
|---------------|------------------|-----------|
| 60 V          | 27.5 mΩ @ 10 V   | 21 A      |
|               | 43.0 mΩ @ 4.5 V  |           |

### N-Channel



DFN5  
(SO-8FL)  
CASE 488AA  
STYLE 1

### MARKING DIAGRAM



XXXXXX = 5C680L (NVMFS5C680NL) or  
680LWF (NVMFS5C680NLWF)

A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# NVMFS5C680NL

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

### OFF CHARACTERISTICS

|                                   |                      |                                                  |                        |  |     |    |
|-----------------------------------|----------------------|--------------------------------------------------|------------------------|--|-----|----|
| Drain-to-Source Breakdown Voltage | V <sub>(BR)DSS</sub> | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA   | 60                     |  |     | V  |
| Zero Gate Voltage Drain Current   | I <sub>DSS</sub>     | V <sub>GS</sub> = 0 V,<br>V <sub>DS</sub> = 60 V | T <sub>J</sub> = 25°C  |  | 10  | μA |
|                                   |                      |                                                  | T <sub>J</sub> = 125°C |  | 250 |    |
| Gate-to-Source Leakage Current    | I <sub>GSS</sub>     | V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V    |                        |  | 100 | nA |

### ON CHARACTERISTICS (Note 5)

|                               |                     |                                                            |     |      |      |    |
|-------------------------------|---------------------|------------------------------------------------------------|-----|------|------|----|
| Gate Threshold Voltage        | V <sub>GS(TH)</sub> | V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 13 μA | 1.2 |      | 2.2  | V  |
| Drain-to-Source On Resistance | R <sub>DS(on)</sub> | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.5 A             |     | 22.9 | 27.5 | mΩ |
|                               |                     | V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 7.5 A            |     | 35.8 | 43.0 |    |
| Forward Transconductance      | g <sub>FS</sub>     | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A              |     | 20   |      | S  |

### CHARGES AND CAPACITANCES

|                              |                     |                                                                         |  |     |  |    |
|------------------------------|---------------------|-------------------------------------------------------------------------|--|-----|--|----|
| Input Capacitance            | C <sub>iss</sub>    | V <sub>GS</sub> = 0 V, f = 1.0 MHz,<br>V <sub>DS</sub> = 25 V           |  | 330 |  | pF |
| Output Capacitance           | C <sub>oss</sub>    |                                                                         |  | 172 |  |    |
| Reverse Transfer Capacitance | C <sub>rss</sub>    |                                                                         |  | 5   |  |    |
| Total Gate Charge            | Q <sub>G(TOT)</sub> | V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 48 V, I <sub>D</sub> = 7.5 A  |  | 5.8 |  | nC |
| Threshold Gate Charge        | Q <sub>G(TH)</sub>  |                                                                         |  | 0.8 |  |    |
| Gate-to-Source Charge        | Q <sub>GS</sub>     |                                                                         |  | 1.3 |  |    |
| Gate-to-Drain Charge         | Q <sub>GD</sub>     |                                                                         |  | 0.6 |  |    |
| Total Gate Charge            | Q <sub>G(TOT)</sub> | V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 48 V, I <sub>D</sub> = 7.5 A |  | 2.7 |  | nC |

### SWITCHING CHARACTERISTICS (Note 6)

|                     |                     |                                                                                                   |  |      |  |    |
|---------------------|---------------------|---------------------------------------------------------------------------------------------------|--|------|--|----|
| Turn-On Delay Time  | t <sub>d(on)</sub>  | V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 48 V,<br>I <sub>D</sub> = 7.5 A, R <sub>G</sub> = 1.0 Ω |  | 5    |  | ns |
| Rise Time           | t <sub>r</sub>      |                                                                                                   |  | 12.5 |  |    |
| Turn-Off Delay Time | t <sub>d(off)</sub> |                                                                                                   |  | 14   |  |    |
| Fall Time           | t <sub>f</sub>      |                                                                                                   |  | 2.5  |  |    |

### DRAIN-SOURCE DIODE CHARACTERISTICS

|                         |                 |                                                                                  |                        |     |      |     |    |
|-------------------------|-----------------|----------------------------------------------------------------------------------|------------------------|-----|------|-----|----|
| Forward Diode Voltage   | V <sub>SD</sub> | V <sub>GS</sub> = 0 V,<br>I <sub>S</sub> = 7.5 A                                 | T <sub>J</sub> = 25°C  |     | 0.87 | 1.2 | V  |
|                         |                 |                                                                                  | T <sub>J</sub> = 125°C |     | 0.76 |     |    |
| Reverse Recovery Time   | t <sub>RR</sub> | V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs,<br>I <sub>S</sub> = 7.5 A |                        | 18  |      | ns  |    |
| Charge Time             | t <sub>a</sub>  |                                                                                  |                        | 8.3 |      |     |    |
| Discharge Time          | t <sub>b</sub>  |                                                                                  |                        | 9.7 |      |     |    |
| Reverse Recovery Charge | Q <sub>RR</sub> |                                                                                  |                        | 7.5 |      |     | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

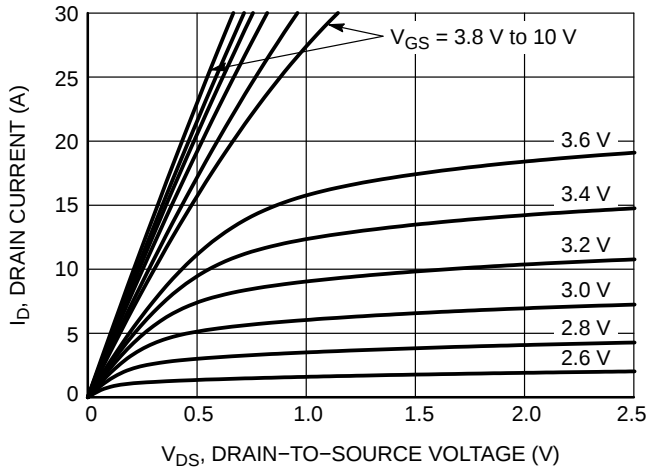


Figure 1. On-Region Characteristics

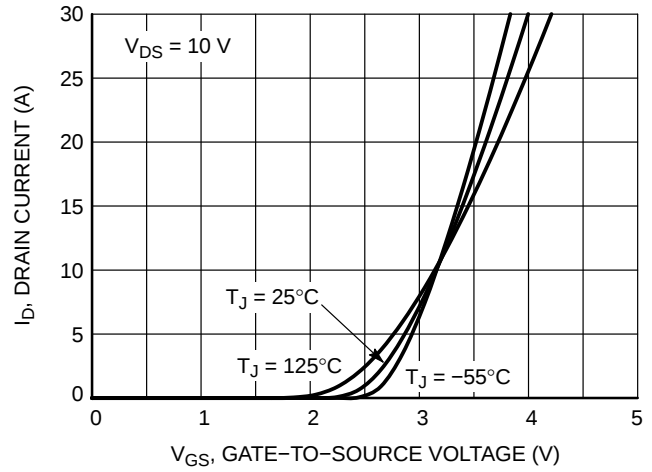


Figure 2. Transfer Characteristics

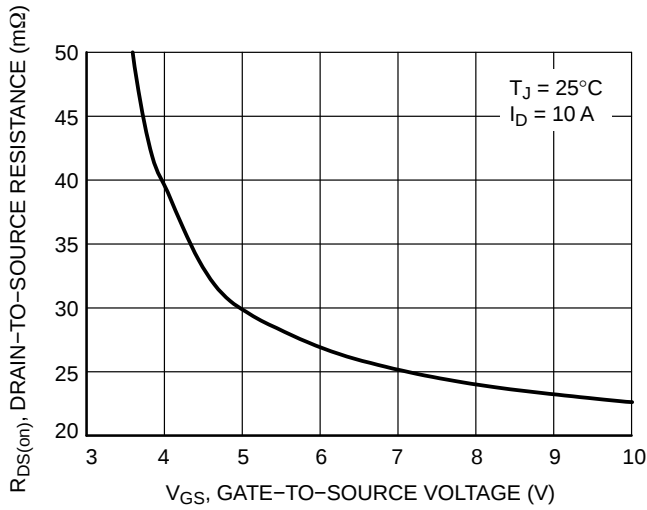


Figure 3. On-Resistance vs. Gate-to-Source Voltage

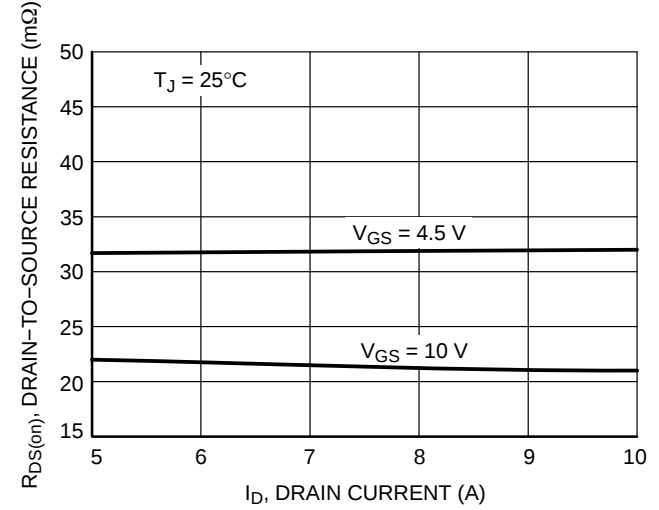


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

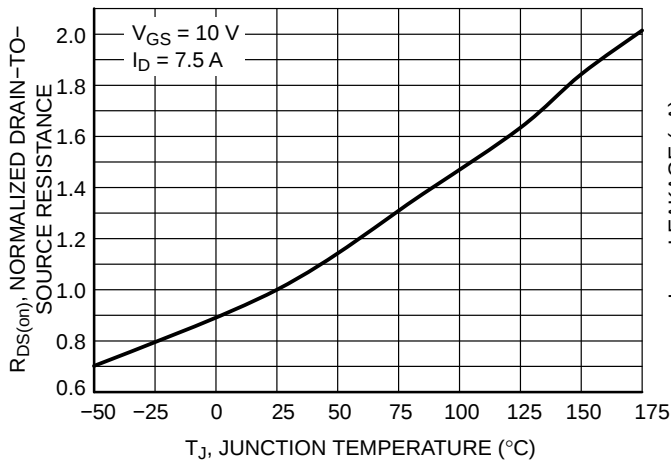


Figure 5. On-Resistance Variation with Temperature

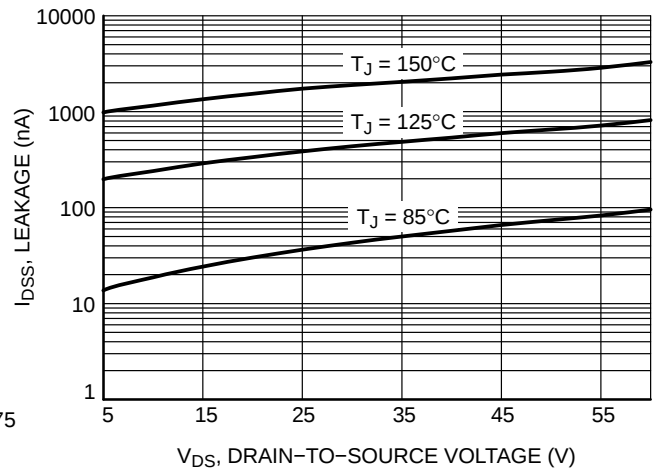


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

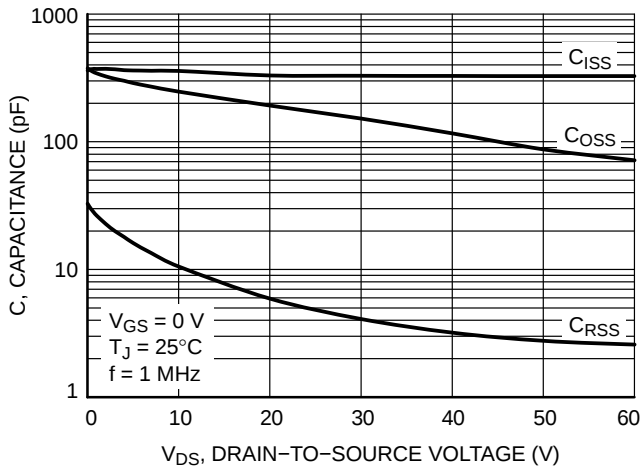


Figure 7. Capacitance Variation

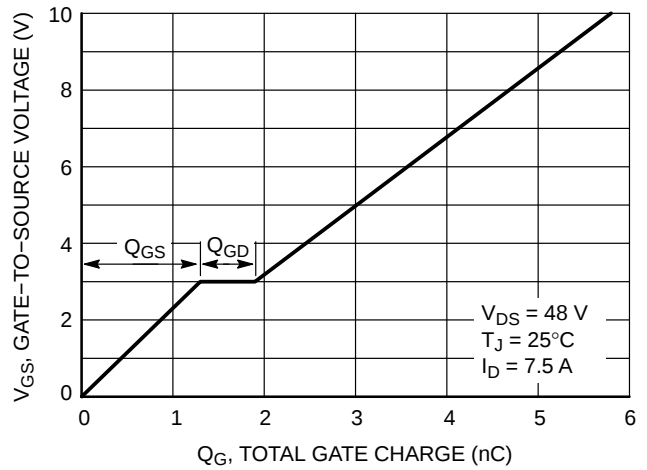


Figure 8. Gate-to-Source vs. Total Charge

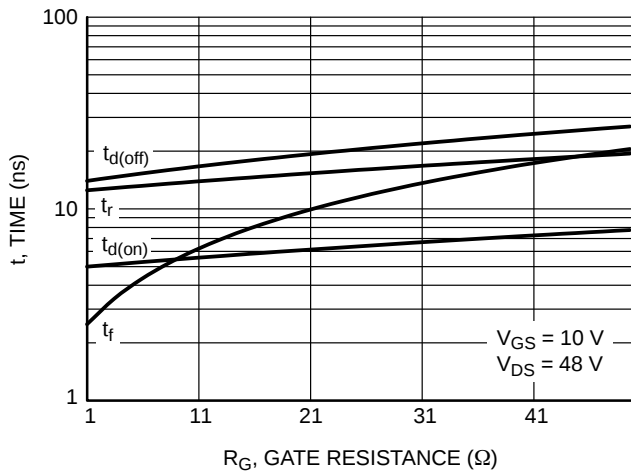


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

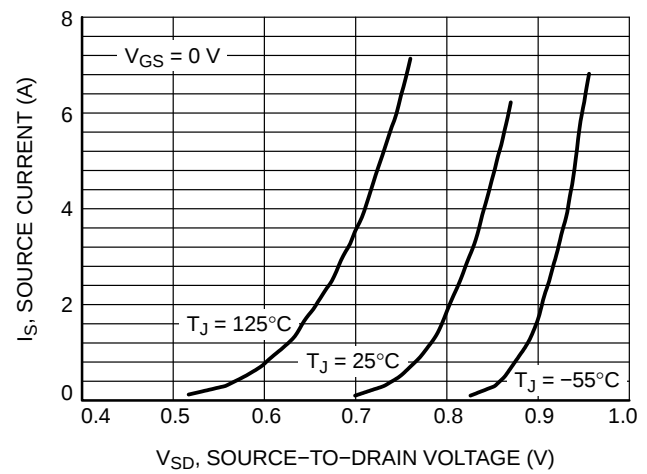


Figure 10. Diode Forward Voltage vs. Current

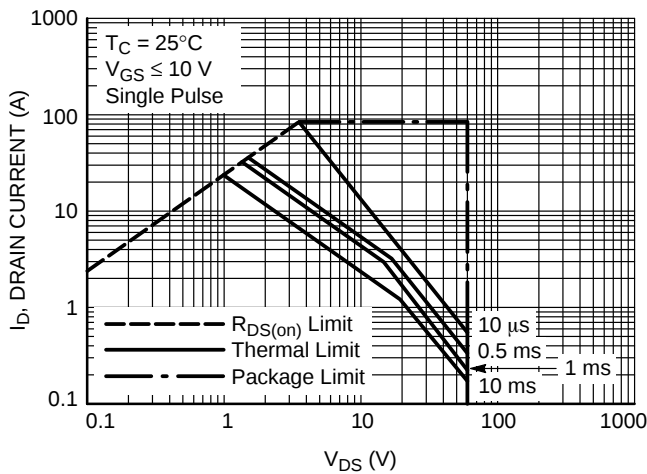


Figure 11. Maximum Rated Forward Biased Safe Operating Area

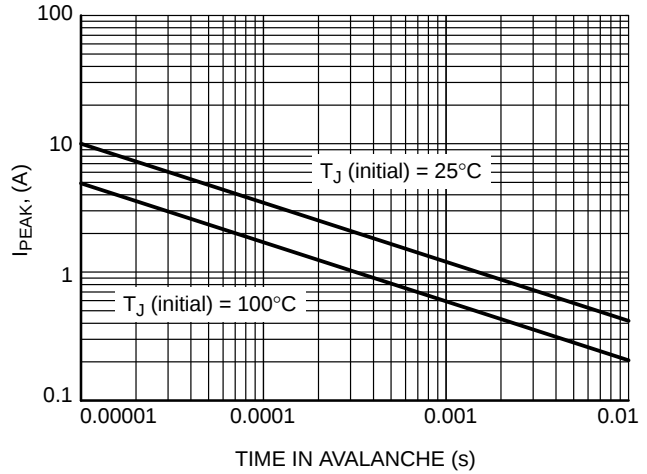


Figure 12.  $I_{PEAK}$  vs. Time in Avalanche

# NVMFS5C680NL

## TYPICAL CHARACTERISTICS

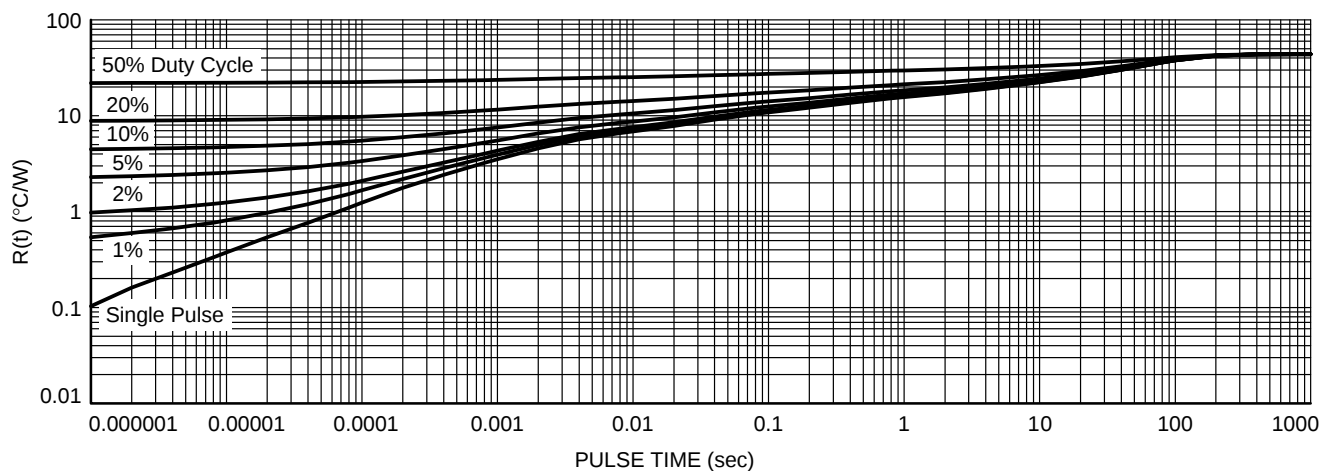


Figure 13. Thermal Characteristics

### DEVICE ORDERING INFORMATION

| Device            | Marking | Package           | Shipping <sup>†</sup> |
|-------------------|---------|-------------------|-----------------------|
| NVMFS5C680NLT1G   | 5C680L  | DFN5<br>(Pb-Free) | 1500 / Tape & Reel    |
| NVMFS5C680NLWFT1G | 680LWF  | DFN5<br>(Pb-Free) | 1500 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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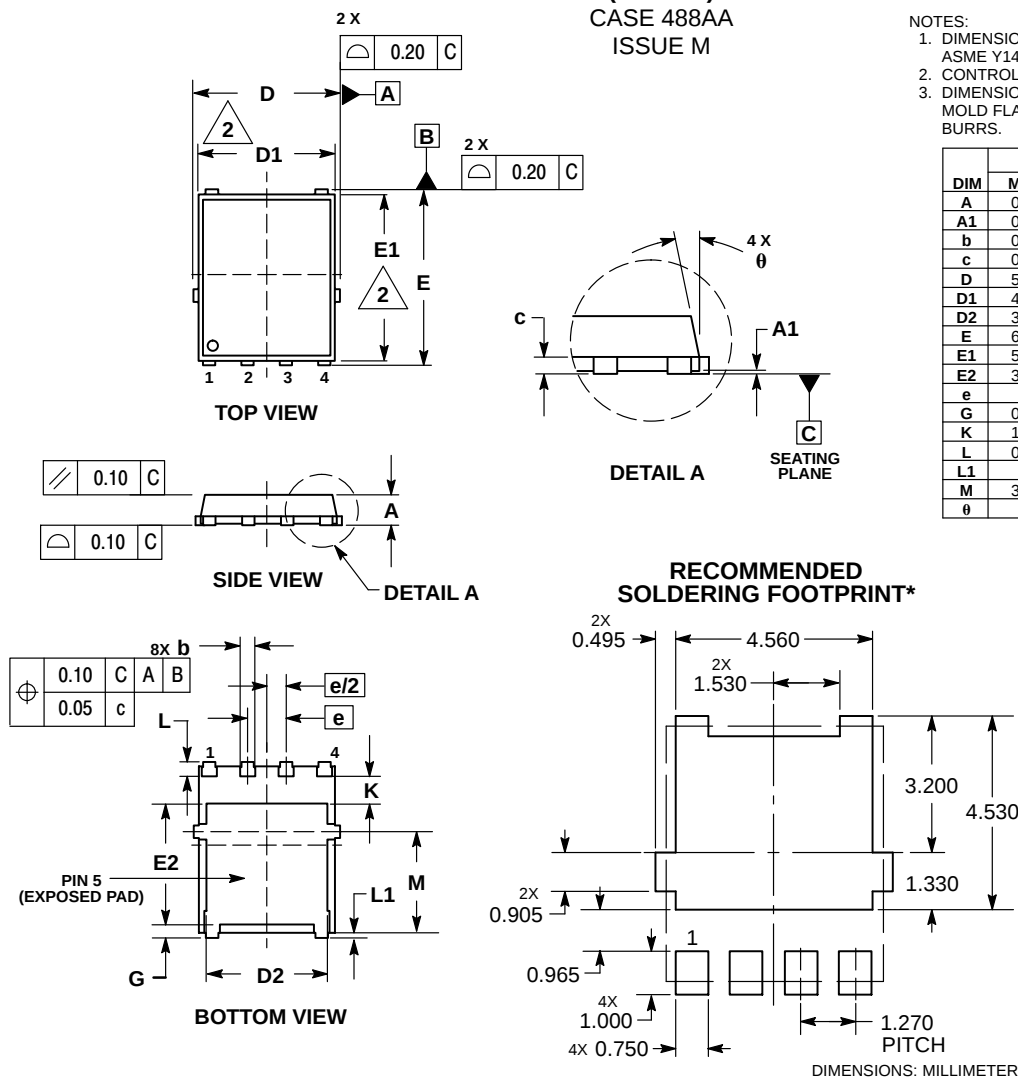
## PACKAGE DIMENSIONS

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE M

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

| DIM | MILLIMETERS |       |      |
|-----|-------------|-------|------|
|     | MIN         | NOM   | MAX  |
| A   | 0.90        | 1.00  | 1.10 |
| A1  | 0.00        | ---   | 0.05 |
| b   | 0.33        | 0.41  | 0.51 |
| c   | 0.23        | 0.28  | 0.33 |
| D   | 5.00        | 5.15  | 5.30 |
| D1  | 4.70        | 4.90  | 5.10 |
| D2  | 3.80        | 4.00  | 4.20 |
| E   | 6.00        | 6.15  | 6.30 |
| E1  | 5.70        | 5.90  | 6.10 |
| E2  | 3.45        | 3.65  | 3.85 |
| e   | 1.27 BSC    |       |      |
| G   | 0.51        | 0.575 | 0.71 |
| K   | 1.20        | 1.35  | 1.50 |
| L   | 0.51        | 0.575 | 0.71 |
| L1  | 0.125 REF   |       |      |
| M   | 3.00        | 3.40  | 3.80 |
| θ   | 0°          | ---   | 12°  |

STYLE 1:  
PIN 1. SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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