High- or Low-Side, Bidirectional Current Power Monitor with 2-Wire Interface

Check for Samples: INA220B-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified with the following results:**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C3B**
- **High- or Low-Side Sensing**
- **Senses Bus Voltages From 0 V to 26 V**
- **Reports Current, Voltage, and Power**
- **16 Programmable Addresses**
- **High Accuracy: 0.5% (Max) Over Temperature (INA220B-Q1)**
- **User-Programmable Calibration**
- **Fast (3.4 MHz) 2-Wire Mode**
- **MSOP-10 Package**

APPLICATIONS

- **Automotive**
- **Servers**
- **Telecom Equipment**
- **Notebook Computers**
- **Power Management**
- **Battery Chargers**
- **Power Supplies**
- **Test Equipment**

DESCRIPTION

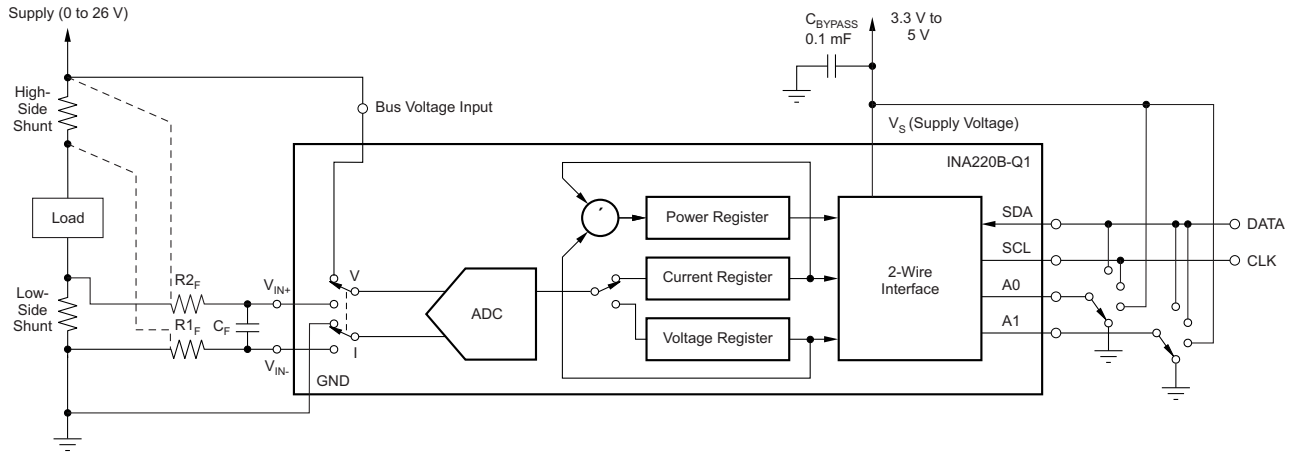
The INA220B-Q1 device is a current shunt and power monitor with an 2-wire interface. The INA220B-Q1 device monitors both shunt drop and supply voltage. A programmable calibration value, combined with an internal multiplier, enables direct readouts in amperes. An additional multiplying register calculates power in watts. The 2-wire interface features 16 programmable addresses. The separate shunt input on the INA220B-Q1 device allows it to be used in systems with low-side sensing.

The INA220B-Q1 device is available in two grades: A and B. The B grade version has higher accuracy and higher precision specifications.

The INA220B-Q1 device senses across shunts on buses that can vary from 0 V to 26 V, useful for low-side sensing or CPU power supplies. The device uses a single 3 V to 5.5 V supply, drawing a maximum of 1 mA of supply current. The INA220B-Q1 device operates from –40°C to 125°C.

RELATED PRODUCTS

DESCRIPTION	DEVICE
Current/Power Monitor with Watchdog, Peak-Hold, and Fast Comparator Functions	INA209
Zero-Drift, Low-Cost, Analog Current Shunt Monitor Series in Small Package	INA210, INA211, INA212, INA213, INA214
Zero-Drift, Bidirectional Current Power Monitor with 2-Wire Interface	INA219



General Load, Low- or High-Side Sensing

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION (1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	VSSOP-DGS	Reel of 2500	INA220BQDGSRQ1	IPUQ

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the INA220B-Q1 product folder at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		INA220B-Q1	UNIT
Supply Voltage, V_S		6	V
Analog Inputs, V_{IN+}, $V_{IN–}$	Differential (V_{IN+}) – ($V_{IN–}$)(2)	–26 to 26	V
	Common-Mode	–0.3 to 26	V
V_{BUS}		–0.3 to 26	V
SDA		GND – 0.3 to 6	V
SCL		GND – 0.3 to V_S 0.3	V
Input Current Into Any Pin		5	mA
Open-Drain Digital Output Current		10	mA
Operating Temperature		–40 to 125	°C
Storage Temperature		–65 to 150	°C
Junction Temperature		150	°C
ESD Ratings	Human Body Model (HBM) AEC-Q100 Classification Level H2	2	kV
	Charged Device Model (CDM) AEC-Q100 Classification Level C3B	750	V

(1) Stresses above *Absolute Maximum Ratings* may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) V_{IN+} and $V_{IN–}$ may have a differential voltage of –26 V to 26 V; however, the voltage at these pins must not exceed the range –0.3 V to 26 V.

RECOMMENDED OPERATING CONDITIONS

Boldface limits apply over the specified temperature range, T_A = –40°C to 125°C
At T_A = 25°C, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 32 mV, V_{BUS} = 12 V, PGA = ÷ 1, and BRNG(1) = 1, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
DIGITAL INPUTS (SDA as Input, SCL, A0, A1)					
Input Capacitance			3		pF
Leakage Input Current	0 ≤ V_{IN} ≤ V_S		0.1	1	µA
Input Logic Levels:					
V_{IH}		0.7 (V_S)		6	V
V_{IL}		–0.3		0.3 (V_S)	V
Hysteresis			500		mV
OPEN-DRAIN DIGITAL OUTPUTS (SDA)					
Logic '0' Output Level	I_{SINK} = 3mA		0.15	0.4	V
High-Level Output Leakage Current	V_{OUT} = VS		0.1	1	µA
POWER SUPPLY					
Operating Supply Range		3		5.5	V
Quiescent Current			0.7	1	mA
Quiescent Current, Power-Down Mode			6	15	µA
Power-On Reset (POR) Threshold			2		V
TEMPERATURE RANGE					
Specified Temperature Range		–40		85	°C
Operating Temperature Range		–40		125	°C
Thermal Resistance(2) θJA					
MSOP-10			200		°C/W

(1) BRNG is bit 13 of the Configuration Register.
(2) θ_{JA} value is based on JEDEC low-K board.

THERMAL INFORMATION

THERMAL METRIC(1)		INA220B-Q1 DGS (10 PINS)	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	165.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	53.2	
θ_{JB}	Junction-to-board thermal resistance	86.6	
ψ_{JT}	Junction-to-top characterization parameter	6.4	
ψ_{JB}	Junction-to-board characterization parameter	84.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS: V_S = 3.3V

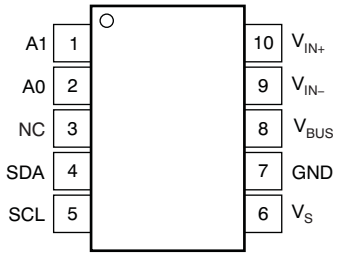
Boldface limits apply over the specified temperature range, **T_A = –40°C to 125°C.**
At T_A = 25°C, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 32 mV, V_{BUS} = 12 V, PGA = ÷ 1, and BRNG(1) = 1, unless otherwise noted.

PARAMETER		TEST CONDITIONS	INA220B-Q1 MIN	INA220B-Q1 TYP	INA220B-Q1 MAX	UNIT
INPUT						
Full-Scale Current Sense (Input) Voltage Range		PGA = ÷ 1	0		±40	mV
		PGA = ÷ 2	0		±80	mV
		PGA = ÷ 4	0		±160	mV
		PGA = ÷ 8	0		±320	mV
Bus Voltage (Input Voltage) Range(2)		BRNG = 1	0		32	V
		BRNG = 0	0		16	V
Common-Mode Rejection	CMRR	V_{IN+} = 0 V to 26 V	100	120		dB
Offset Voltage, RTI(3)	V_{OS}	PGA = ÷ 1		±10	±50(4)	µV
		PGA = ÷ 2		±20	±75	µV
		PGA = ÷ 4		±30	±75	µV
		PGA = ÷ 8		±40	±100	µV
versus Temperature				**0.16**		**µV/°C**
versus Power Supply	PSRR	V_S = 3 V to 5.5 V		10		µV/V
Current Sense Gain Error				±40		m%
versus Temperature, MSOP-10				**1**		**m%/°C**
Input Impedance		Active Mode				
V_{IN+} Pin				20		µA
$V_{IN–}$ Pin				20		µA
V_{BUS} Pin(5)				320		kΩ
Input Leakage(6)		Power-Down Mode				
V_{IN+} Pin				0.1	±0.5	µA
$V_{IN–}$ Pin				0.1	±0.5	µA
DC ACCURACY						
ADC Basic Resolution				12		Bits
1LSB Step Size						
Shunt Voltage				10		µV
Bus Voltage				4		mV
Current Measurement Error				±0.2	±0.3	%
over Temperature					**±0.5**	**%**
Bus Voltage Measurement Error		V_{BUS} = 12 V		±0.2	±0.5	%
over Temperature					**±1**	**%**
Differential Nonlinearity				±0.1		LSB
ADC TIMING						
ADC Conversion Time		12-Bit		532	586	µs
		11-Bit		276	304	µs
		10-Bit		148	163	µs
		9-Bit		84	93	µs
Minimum Convert Input Low Time			4			µs
SMBus						
SMBus Timeout(7)				28	35	ms

(1) BRNG is bit 13 of the Configuration Register.
(2) This parameter only expresses the full-scale range of the analog-to-digital converter (ADC) scaling. In no event should more than 26 V be applied to this device.
(3) Referred-to-input (RTI).
(4) Shaded cells indicate improved specifications of the INA220B-Q1.
(5) The input impedance of this pin may vary approximately ±15%.
(6) Input leakage is positive (current flowing into the pin) for the conditions shown at the top of the table. Negative leakage currents can occur under different input conditions.
(7) System management bus (SMBus) timeout in the INA220B-Q1 resets the interface any time SCL or SDA is low for over 28 ms.

PIN CONFIGURATIONS

DGS PACKAGE
MSOP-10
(Top View)



PIN DESCRIPTIONS: MSOP-10

MSOP-10 (DGS)		DESCRIPTION
PIN NO	NAME	
1	A1	Address pin. Connect to GND, SCL, SDA, or V_S. Table 1 shows pin settings and corresponding addresses.
2	A0	Address pin. Connect to GND, SCL, SDA, or V_S. Table 1 shows pin settings and corresponding addresses.
3	NC	No internal connection
4	SDA	Serial bus data line.
5	SCL	Serial bus clock line.
6	V_S	Power supply, 3 V to 5.5 V.
7	GND	Ground.
8	V_{BUS}	Bus voltage input.
9	V_{IN-}	Negative differential shunt voltage. Connect to negative side of shunt resistor. Bus voltage is measured from this pin to ground.
10	V_{IN+}	Positive differential shunt voltage. Connect to positive side of shunt resistor.

TYPICAL CHARACTERISTICS

At T_A = 25°C, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 32 mV, PGA = ÷ 1, and BRNG = 1, unless otherwise noted.

FREQUENCY RESPONSE

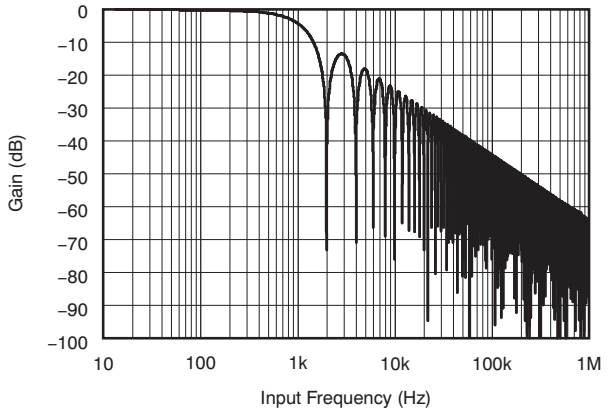


Figure 1.

ADC SHUNT OFFSET vs TEMPERATURE

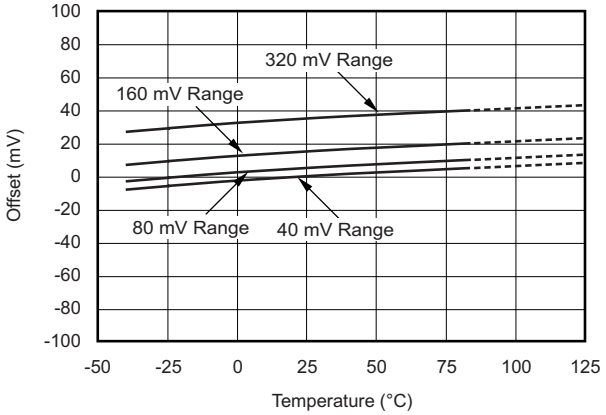


Figure 2.

ADC SHUNT GAIN ERROR vs TEMPERATURE

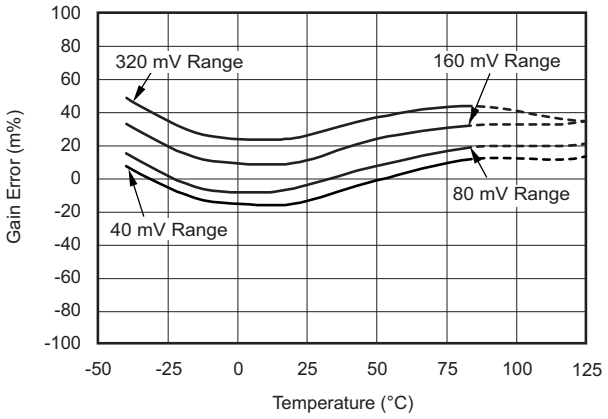


Figure 3.

ADC BUS VOLTAGE OFFSET vs TEMPERATURE

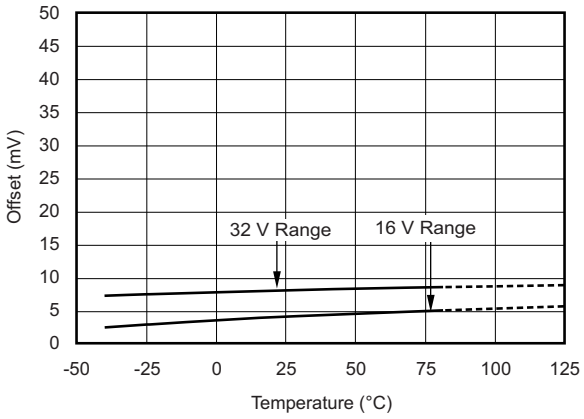


Figure 4.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 32 mV, PGA = ÷ 1, and BRNG = 1, unless otherwise noted.

ADC BUS GAIN ERROR vs TEMPERATURE

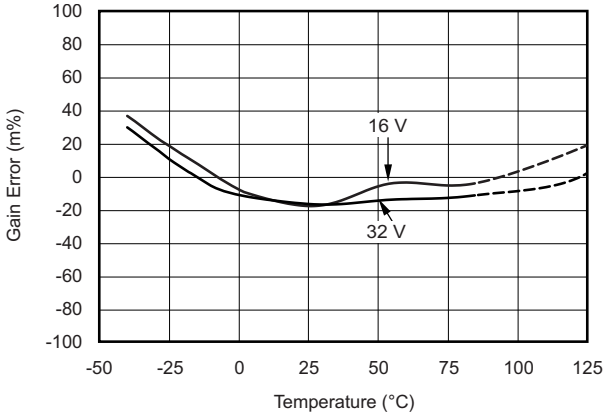


Figure 5.

INTEGRAL NONLINEARITY vs INPUT VOLTAGE

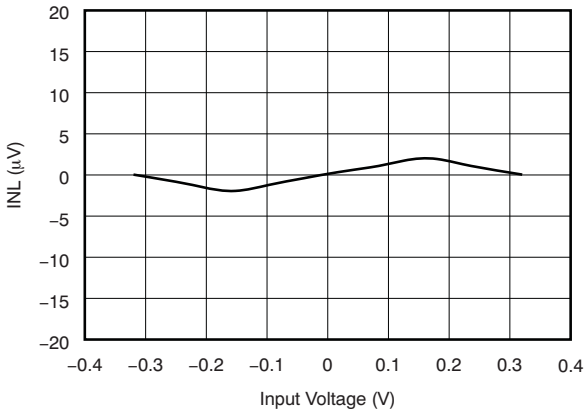


Figure 6.

INPUT CURRENTS WITH LARGE DIFFERENTIAL VOLTAGES (V_{IN+} at 12 V, Sweep of $V_{IN–}$)

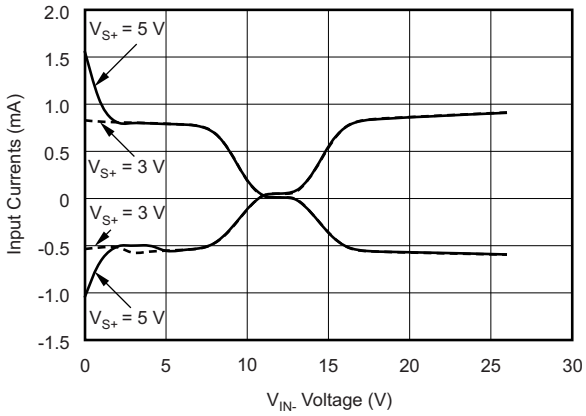


Figure 7.

ACTIVE I_Q vs TEMPERATURE

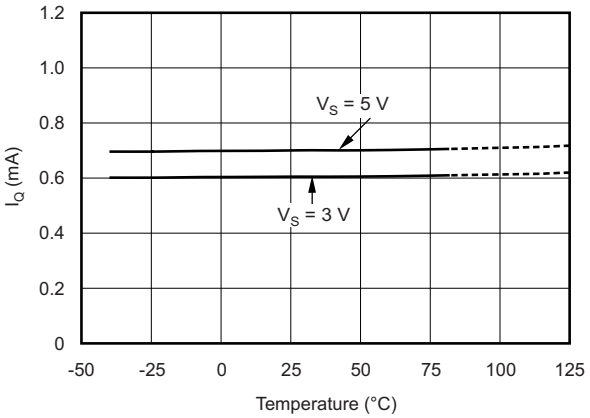


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 32 mV, PGA = ÷ 1, and BRNG = 1, unless otherwise noted.

SHUTDOWN I_Q vs TEMPERATURE

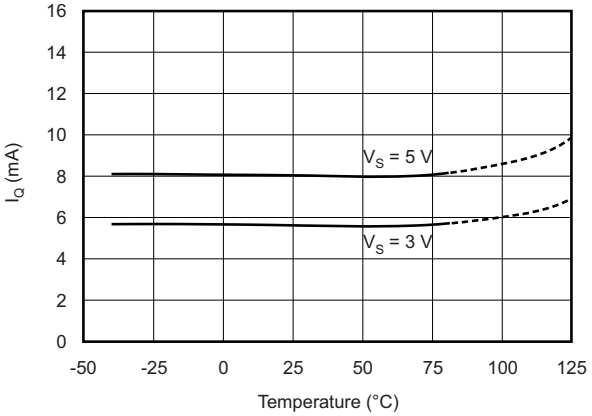


Figure 9.

ACTIVE I_Q vs 2-WIRE CLOCK FREQUENCY

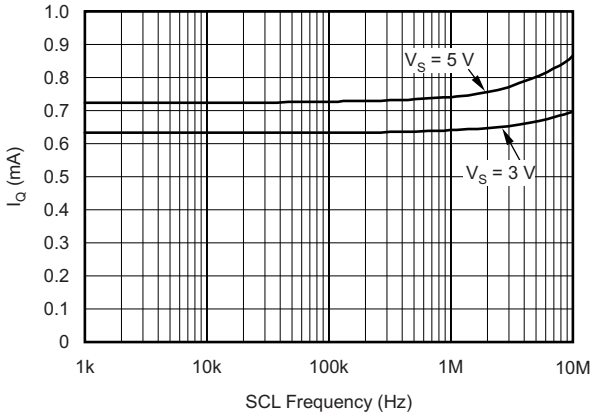


Figure 10.

TOTAL PERCENT BUS VOLTAGE ERROR vs SUPPLY VOLTAGE

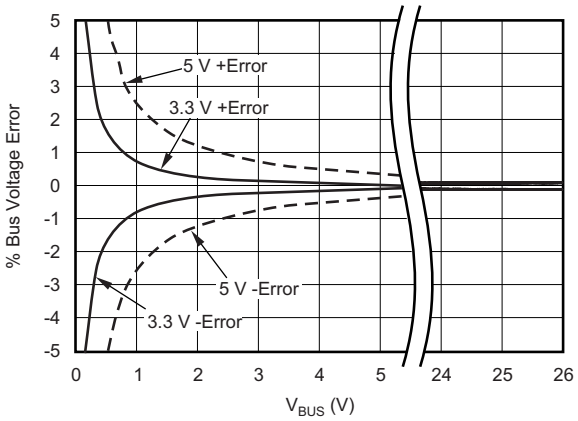


Figure 11.

SHUTDOWN I_Q vs 2-WIRE CLOCK FREQUENCY

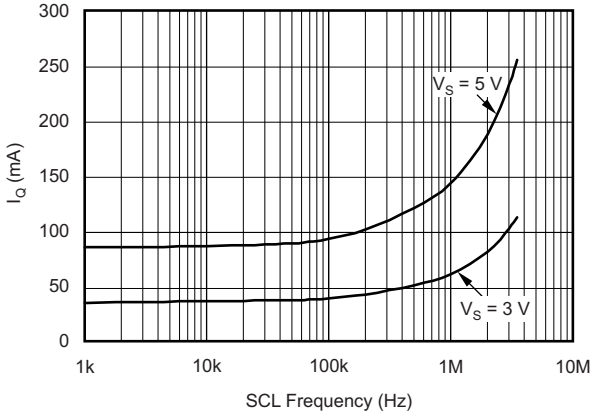
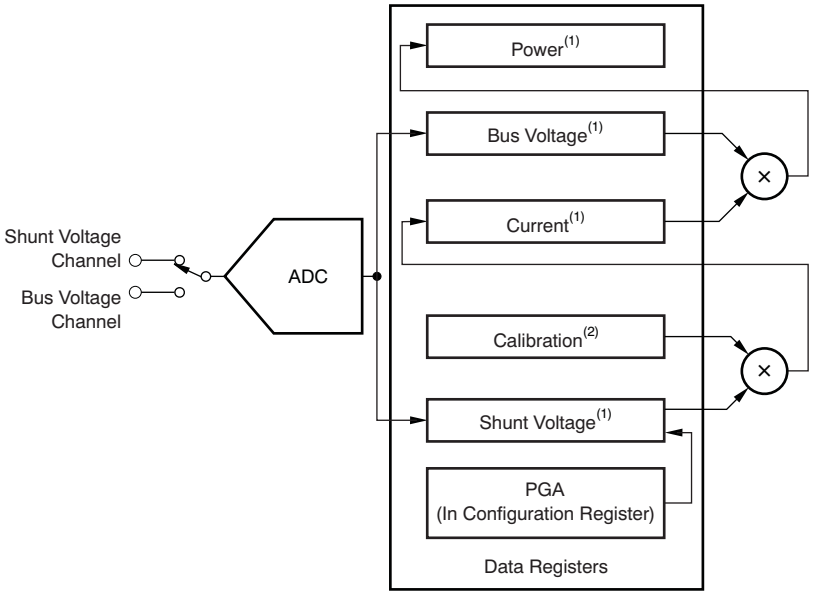


Figure 12.

REGISTER BLOCK DIAGRAM



(1) Read-only.

(2) Write-only.

Figure 13. INA220B-Q1 Register Block Diagram

APPLICATION INFORMATION

The INA220B-Q1 device is a digital current shunt monitor with an 2-wire and SMBus compatible interface. It provides digital current, voltage, and power readings necessary for accurate decision making in precisely controlled systems. Programmable registers allow flexible configuration for measurement resolution, and continuous versus triggered operation. Detailed register information appears at the end of this data sheet, beginning with Table 3. See the Register Block Diagram for a block diagram of the INA220B-Q1 device.

INA220B-Q1 TYPICAL APPLICATION

The figure on the front page shows a typical application circuit for the INA220B-Q1 device. Use a 0.1 µF ceramic capacitor for power-supply bypassing, placed as closely as possible to the supply and ground pins.

The input filter circuit consisting of R_{F1}, R_{F2}, and C_F is not necessary in most applications. If the need for filtering is unknown, reserve board space for the components and install 0 Ω resistors unless a filter is needed. See the *Filtering and Input Considerations* section.

BUS OVERVIEW

The INA220B-Q1 device offers compatibility with both 2-wire and SMBus interfaces. The 2-wire and SMBus protocols are essentially compatible with one another.

The 2-wire interface is used throughout this data sheet as the primary example, with SMBus protocol specified only when a difference between the two systems is being addressed. Two bidirectional lines, serial bus clock line (SCL) and serial bus data line (SDA), connect the INA220B-Q1 to the bus. Both SCL and SDA are open-drain connections.

The device that initiates the transfer is called a master, and the devices controlled by the master are slaves. The bus must be controlled by a master device that generates the SCL, controls the bus access, and generates START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling the SDA from a HIGH to a LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and eight bits of data are sent, followed by an Acknowledge bit. During data transfer, SDA must remain stable while SCL is HIGH. Any change in SDA while SCL is HIGH is interpreted as a START or STOP condition.

Once all data have been transferred, the master generates a STOP condition, indicated by pulling SDA from LOW to HIGH while SCL is HIGH. The INA220B-Q1 device includes a 28 ms timeout on its interface to prevent locking up an SMBus.

Serial Bus Address

To communicate with the INA220B-Q1 device, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation.

The INA220B-Q1 device has two address pins, A0 and A1. Table 1 describes the pin logic levels for each of the 16 possible addresses. The state of pins A0 and A1 is sampled on every bus communication and should be set before any activity on the interface occurs. The address pins are read at the start of each communication event.

Table 1. INA220B-Q1 Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	V_{S+}	1000001
GND	SDA	1000010
GND	SCL	1000011
V_{S+}	GND	1000100
V_{S+}	V_{S+}	1000101
V_{S+}	SDA	1000110
V_{S+}	SCL	1000111
SDA	GND	1001000
SDA	V_{S+}	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V_{S+}	1001101
SCL	SDA	1001110
SCL	SCL	1001111

Serial Interface

The INA220B-Q1 device operates only as a slave device on the 2-wire bus and SMBus. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The INA220B-Q1 device supports the transmission protocol for fast (1 kHz to 400 kHz) and high-speed (HS) (1 kHz to 3.4 MHz) modes. All data bytes are transmitted most significant byte first.

WRITING TO AND READING FROM THE INA220B-Q1 DEVICE

Accessing a particular register on the INA220B-Q1 device is accomplished by writing the appropriate value to the register pointer. Refer to Table 3 for a complete list of registers and corresponding addresses. The value for the register pointer as shown in Figure 17 is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit LOW. Every write operation to the INA220B-Q1 device requires a value for the register pointer.

Writing to a register begins with the first byte transmitted by the master. This byte is the slave address, with the R/$\overline{W}$ bit LOW. The INA220B-Q1 device then acknowledges receipt of a valid address. The next byte transmitted by the master is the address of the register to which data will be written. This register address value updates the register pointer to the desired register. The next two bytes are written to the register addressed by the register pointer. The INA220B-Q1 device acknowledges receipt of each data byte. The master may terminate data transfer by generating a START or STOP condition.

When reading from the INA220B-Q1 device, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit LOW, followed by the register pointer byte. No additional data are required. The master then generates a START condition and sends the slave address byte with the R/$\overline{W}$ bit HIGH to initiate the read command. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register pointer. This byte is followed by an Acknowledge from the master; then the slave transmits the least significant byte. The master acknowledges receipt of the data byte. The master may terminate data transfer by generating a Not-Acknowledge after receiving any data byte, or generating a START or STOP condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the INA220B-Q1 device retains the register pointer value until it is changed by the next write operation.

Figure 14 and Figure 15 show read and write operation timing diagrams, respectively. Note that register bytes are sent most significant byte first, followed by the least significant byte. Figure 16 shows the timing diagram for the SMBus ALERT response operation. Figure 17 illustrates a typical register pointer configuration.

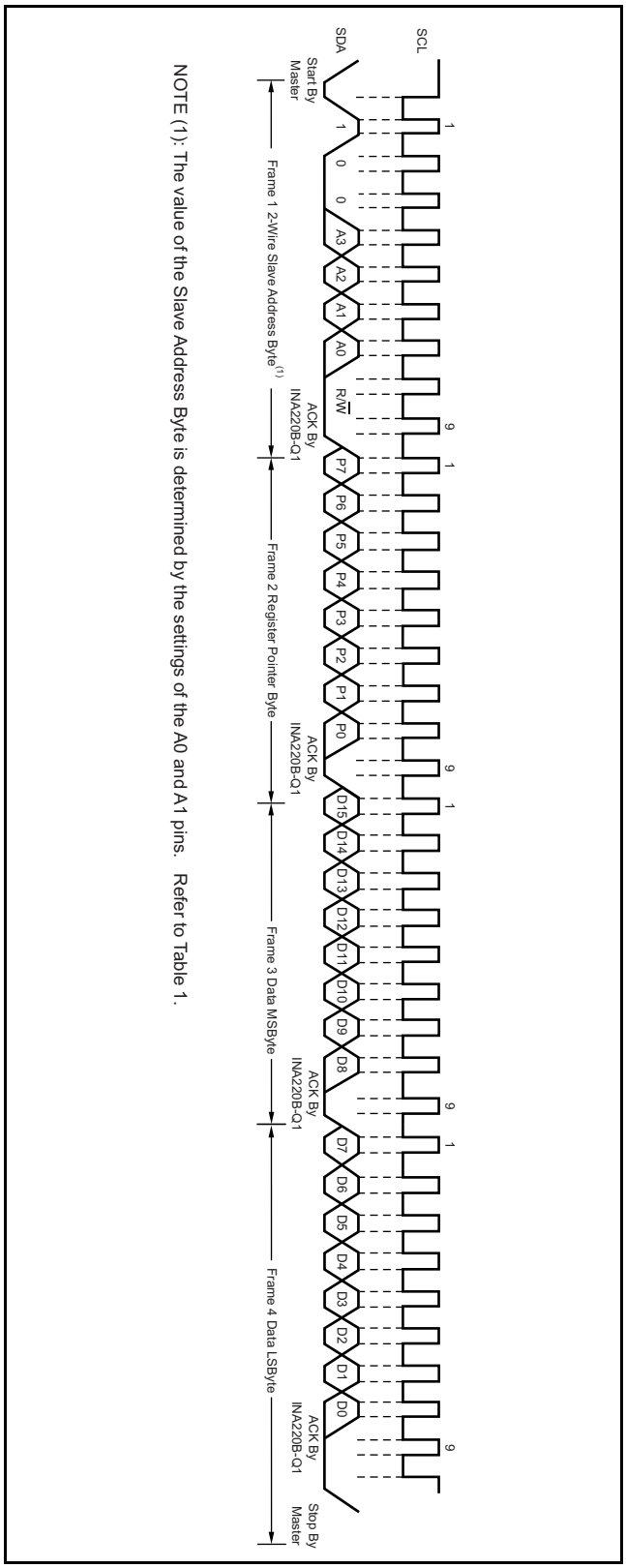


Figure 14. Timing Diagram for Write Word Format

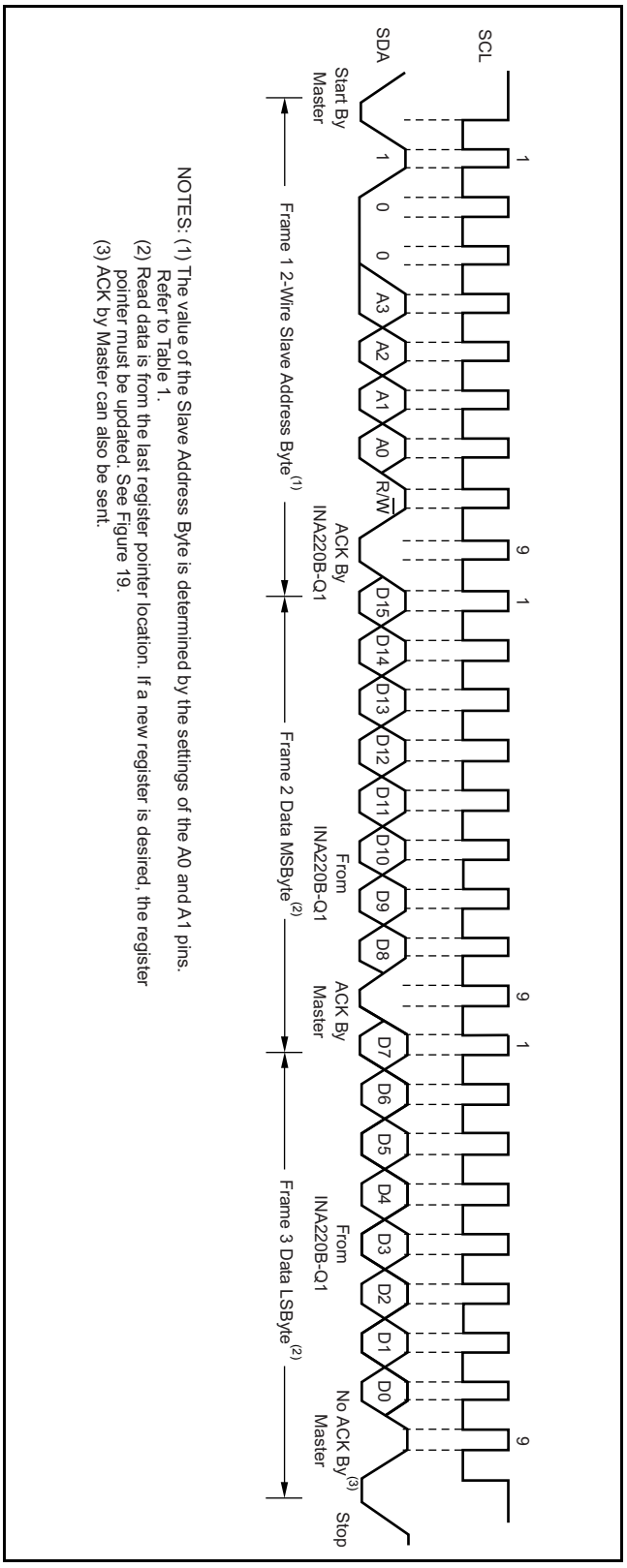
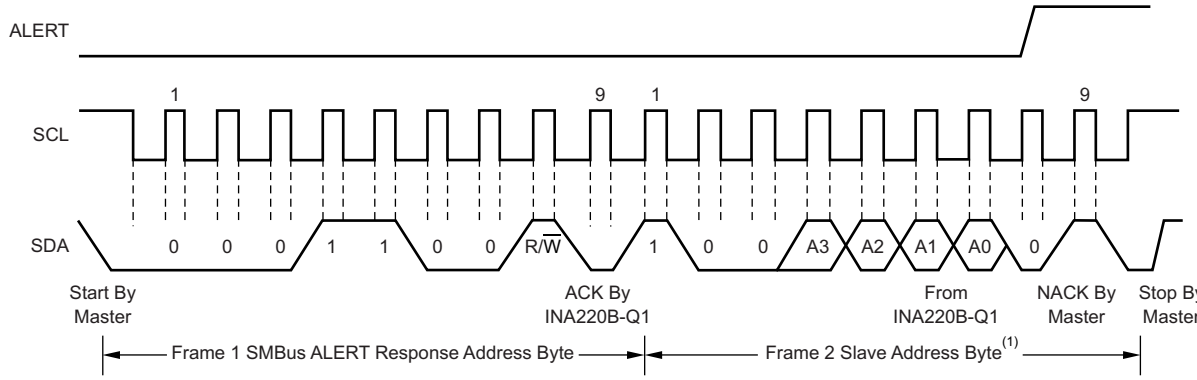
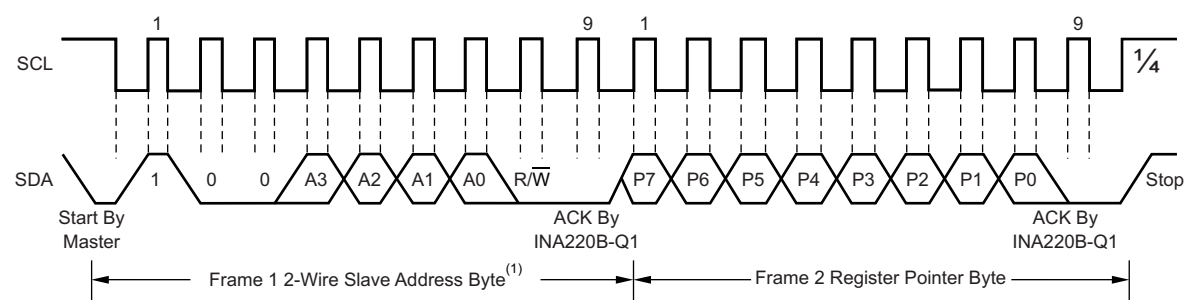


Figure 15. Timing Diagram for Read Word Format



NOTE (1): The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.

Figure 16. Timing Diagram for SMBus ALERT



NOTE (1): The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.

Figure 17. Typical Register Pointer Set

HS 2-Wire Mode

When the bus is idle, both the SDA and SCL lines are pulled HIGH by the pull-up devices. The master generates a START condition followed by a valid serial byte containing the HS master code 00001XXX. This transmission is made in fast (400 kbps) or standard (100 kbps) (F/S) mode at no more than 400 kbps. The INA220B-Q1 device does not acknowledge the HS master code, but does recognize it and switches its internal filters to support 3.4 Mbps operation.

The master then generates a repeated START condition (a repeated START condition has the same timing as the START condition). After this repeated START condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4 Mbps are allowed. Instead of using a STOP condition, repeated START conditions should be used to secure the bus in HS mode. A STOP condition ends the HS mode and switches all the internal filters of the INA220B-Q1 device to support the F/S mode.

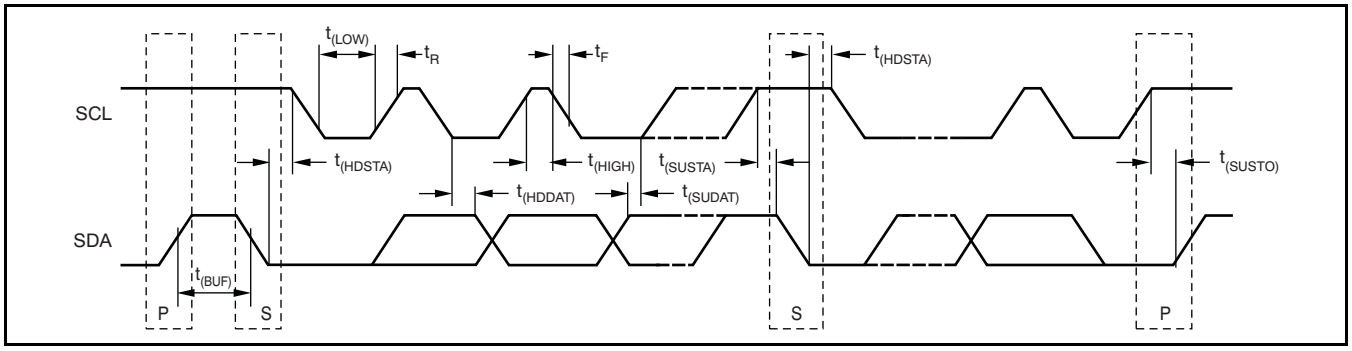


Figure 18. Bus Timing Diagram

Bus Timing Diagram Definitions

PARAMETER		FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	
SCL Operating Frequency	$f_{(SCL)}$	0.001	0.4	0.001	3.4	MHz
Bus Free Time Between STOP and START Condition	$t_{(BUF)}$	600		160		ns
Hold time after repeated START condition. After this period, the first clock is generated.	$t_{(HDSTA)}$	100		100		ns
Repeated START Condition Setup Time	$t_{(SUSTA)}$	100		100		ns
STOP Condition Setup Time	$t_{(SUSTO)}$	100		100		ns
Data Hold Time	$t_{(HDDAT)}$	0		0		ns
Data Setup Time	$t_{(SUDAT)}$	100		10		ns
SCL Clock LOW Period	$t_{(LOW)}$	1300		160		ns
SCL Clock HIGH Period	$t_{(HIGH)}$	600		60		ns
Clock/Data Fall Time	t_F		300		160	ns
Clock/Data Rise Time	t_R		300		160	ns
Clock/Data Rise Time for SCLK ≤ 100kHz	t_R		1000			ns

Power-Up Conditions

Power-up conditions apply to a software reset via the RST bit (bit 15) in the Configuration Register, or the 2-wire bus general call reset.

BASIC ADC FUNCTIONS

The two analog inputs to the INA220B-Q1 device, V_{IN+} and V_{IN-}, connect to a shunt resistor in the bus of interest. Bus voltage is measured at V_{BUS} pin. The INA220B-Q1 device is typically powered by a separate supply from 3 V to 5.5 V. The bus being sensed can vary from 0 V to 26 V. There are no special considerations for power-supply sequencing (for example, a bus voltage can be present with the supply voltage off, and vice-versa). The INA220B-Q1 device senses the small drop across the shunt for shunt voltage, and senses the voltage with respect to ground from V_{BUS} for the bus voltage.

When the INA220B-Q1 device is in the normal operating mode (that is, MODE bits of the Configuration Register are set to '111'), it continuously converts the shunt voltage up to the number set in the shunt voltage averaging function (Configuration Register, SADC bits). The device then converts the bus voltage up to the number set in the bus voltage averaging (Configuration Register, BADC bits). The mode control in the Configuration Register also permits selecting modes to convert only voltage or current, either continuously or in response to an event (triggered).

All current and power calculations are performed in the background and do not contribute to conversion time; conversion times shown in the Electrical Characteristics table can be used to determine the actual conversion time.

Power-down mode reduces the quiescent current and turns off current into the INA220B-Q1 device inputs, avoiding any supply drain. Full recovery from power-down requires 40 µs. ADC off mode (set by the Configuration Register, MODE bits) stops all conversions.

In triggered mode, writing any of the triggered convert modes into the Configuration Register (even if the desired mode is already programmed into the register) triggers a single-shot conversion.

Although the INA220B-Q1 device can be read at any time, and the data from the last conversion remain available, the conversion ready bit (Status Register, CNVR bit) is provided to help coordinate one shot or triggered conversions. The conversion ready bit is set after all conversions, averaging, and multiplication operations are complete.

The conversion ready bit clears under these conditions:

1. Writing to the Configuration Register, except when configuring the MODE bits for power-down or ADC off (Disable) modes;
2. Reading the Status Register; or
3. Triggering a single-shot conversion with the convert pin.

Power Measurement

Current and bus voltage are converted at different points in time, depending on the resolution and averaging mode settings. For instance, when configured for 12-bit and 128 sample averaging, up to 68 ms in time between sampling these two values is possible. Again, these calculations are performed in the background and do not add to the overall conversion time.

PGA Function

If larger full-scale shunt voltages are desired, the INA220B-Q1 device provides a PGA function that increases the full-scale range up to 2, 4, or 8 times (320 mV). Additionally, the bus voltage measurement has two full-scale ranges: 16 V or 32 V.

Compatibility with TI Hot Swap Controllers

The INA220B-Q1 device is designed for compatibility with hot swap controllers such the TI TPS2490. The TPS2490 uses a high-side shunt with a limit at 50 mV; the INA220B-Q1 device full-scale range of 40 mV enables the use of the same shunt for current sensing below this limit. When sensing is required at (or through) the 50 mV sense point of the TPS2490, the PGA of the INA220B-Q1 device can be set to ÷2 to provide an 80mV full-scale range.

Filtering and Input Considerations

Measuring current is often noisy, and such noise can be difficult to define. The INA220B-Q1 device offers several options for filtering by choosing resolution and averaging in the Configuration Register. These filtering options can be set independently for either voltage or current measurement.

The internal ADC is based on a delta-sigma (ΔΣ) front-end with a 500 kHz (±30%) typical sampling rate. This architecture has good inherent noise rejection; however, transients that occur at or very close to the sampling rate harmonics can cause problems. Because these signals are at 1 MHz and higher, they can be dealt with by incorporating filtering at the input of the INA220B-Q1 device. The high frequency enables the use of low-value series resistors on the filter for negligible effects on measurement accuracy. In general, filtering the INA220B-Q1 device input is only necessary if there

are transients at exact harmonics of the 500 kHz (±30%) sampling rate (> 1 MHz). Filter using the lowest possible series resistance and ceramic capacitor. Recommended values are 0.1 µF to 1 µF. Figure 19 shows the INA220B-Q1 device with an additional filter added at the input.

Overload conditions are another consideration for the INA220B-Q1 device inputs. The INA220B-Q1 device inputs are specified to tolerate 26 V across the inputs. A large differential scenario might be a short to ground on the load side of the shunt. This type of event can result in full power-supply voltage across the shunt (as long the power supply or energy storage capacitors support it). It must be remembered that removing a short to ground can result in inductive kickbacks that could exceed the 26 V differential and common-mode rating of the INA220B-Q1 device. Inductive kickback voltages are best dealt with by zener-type transient-absorbing devices (commonly called transzorbs) combined with sufficient energy storage capacitance.

In applications that do not have large energy storage electrolytics on one or both sides of the shunt, an input overstress condition may result from an excessive dV/dt of the voltage applied to the input. A hard physical short is the most likely cause of this event, particularly in applications with no large electrolytics present. This problem occurs because an excessive dV/dt can activate the ESD protection in the INA220B-Q1 device in systems where large currents are available. Testing has demonstrated that the addition of 10 Ω resistors in series with each input of the INA220B-Q1 device sufficiently protects the inputs against dV/dt failure up to the 26 V rating of the INA220B-Q1 device. These resistors have no significant effect on accuracy.

Simple Current Shunt Monitor Usage (No Programming Necessary)

The INA220B-Q1 device can be used without any programming if it is only necessary to read a shunt voltage drop and bus voltage with the default 12-bit resolution, 320 mV shunt full-scale range (PGA = ÷ 8), 32 V bus full-scale range, and continuous conversion of shunt and bus voltage.

Without programming, current is measured by reading the shunt voltage. The Current Register and Power Register are only available if the Calibration Register contains a programmed value.

Programming the INA220B-Q1

The default power-up states of the registers are shown in the INA220 register descriptions section of this data sheet. These registers are volatile, and if programmed to other than default values, must be reprogrammed at every device power-up. Detailed information on programming the Calibration Register specifically is given in the section, *Programming the INA220 Power Measurement Engine*.

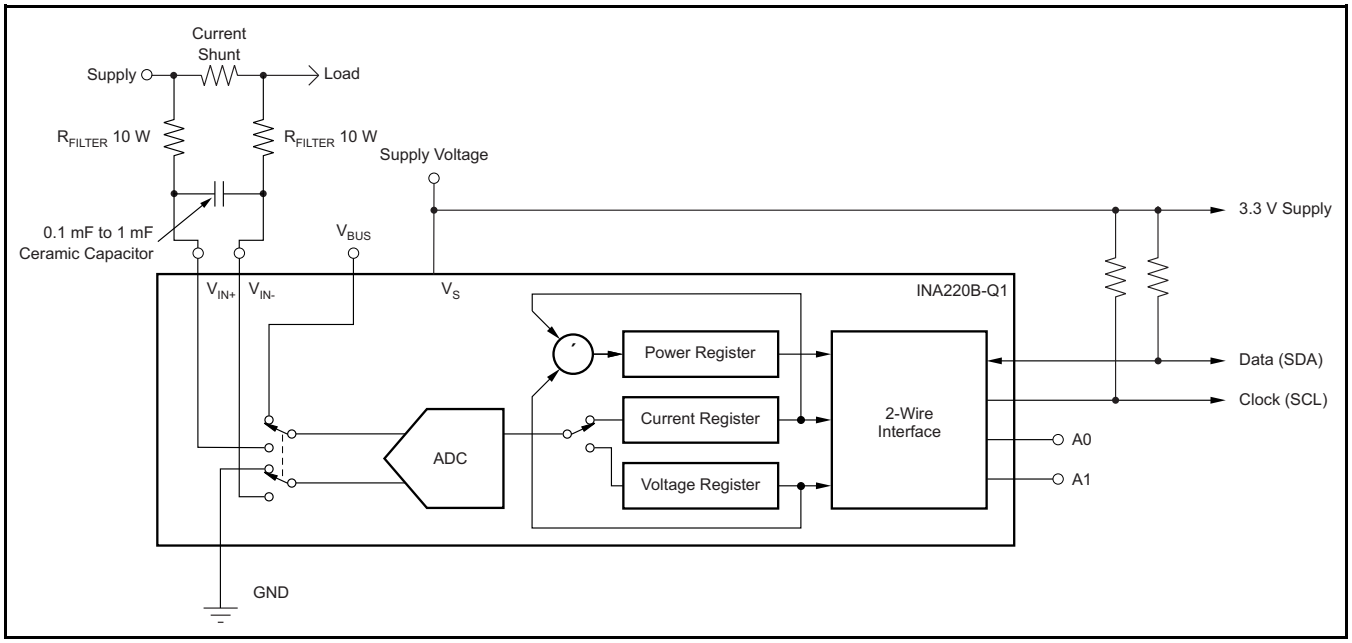


Figure 19. INA220B-Q1 Device With Input Filtering

PROGRAMMING THE INA220B-Q1 DEVICE POWER MEASUREMENT ENGINE

Calibration Register and Scaling

The Calibration Register makes it possible to set the scaling of the Current and Power Registers to whatever values are most useful for a given application. One strategy may be to set the Calibration Register such that the largest possible number is generated in the Current Register or Power Register at the expected full-scale point; this approach yields the highest resolution. The Calibration Register can also be selected to provide values in the Current and Power Registers that either provide direct decimal equivalents of the values being measured, or yield a round LSB number. After these choices have been made, the Calibration Register also offers possibilities for end user system-level calibration, where the value is adjusted slightly to cancel total system error.

Below are two examples for configuring the INA220B-Q1 device calibration. Both examples are written so the information directly relates to the calibration setup found in the INA220B-Q1 EVM software.

Calibration Example 1: Calibrating the INA220B-Q1 device with no possibility for overflow. (Note that the numbers used in this example are the same used with the INA220B-Q1 EVM software as shown in Figure 20)

1. Establish the following parameters:

   $V_{BUS\_MAX} = 32$

   $V_{SHUNT\_MAX} = 0.32$

   $R_{SHUNT} = 0.5$

2. Using Equation 1, determine the maximum possible current.

$$MaxPossible\_I = \frac{V_{SHUNT\_MAX}}{R_{SHUNT}}$$

$$MaxPossible\_I = 0.64 \quad (1)$$

3. Choose the desired maximum current value. This value is selected based on system expectations.

   Max_Expected_I = 0.6

4. Calculate the possible range of current LSBs. To calculate this range, first compute a range of LSBs that is appropriate for the design. Next, select an LSB within this range. Note that the results will have the most resolution when the minimum LSB is selected. Typically, an LSB is selected to be the nearest round number to the minimum LSB value.

$$Minimum\_LSB = \frac{Max\_Expected\_I}{32767}$$

$$Minimum\_LSB = 18.311 \times 10^{-6} \quad (2)$$

$$Maximum\_LSB = \frac{Max\_Expected\_I}{4096}$$

$$Maximum\_LSB = 146.520 \times 10^{-6} \quad (3)$$

   Choose an LSB in the range: Minimum_LSB<Selected_LSB < Maximum_LSB

   $Current\_LSB = 20 \times 10^{-6}$

   Note:

   This value was selected to be a round number near the Minimum_LSB. This selection allows for good resolution with a rounded LSB.

5. Compute the Calibration Register value using Equation 4:

$$Cal = \text{trunc}\left(\frac{0.04096}{Current\_LSB \times R_{SHUNT}}\right)$$

$$Cal = 4096 \quad (4)$$

6. Calculate the Power LSB, using Equation 5. Equation 5 shows a general formula; because the bus voltage measurement LSB is always 4 mV, the power formula reduces to the calculated result.

$$\text{Power\_LSB} = 20 \times \text{Current\_LSB}$$

$$\text{Power\_LSB} = 400 \times 10^{-6} \quad (5)$$

7. Compute the maximum current and shunt voltage values (before overflow), as shown by Equation 6 and Equation 7. Note that both Equation 6 and Equation 7 involve an If - then condition:

$$\text{Max\_Current} = \text{Current\_LSB} \times 32767$$

$$\text{Max\_Current} = 0.65534 \quad (6)$$

If Max_Current ≥ Max Possible_I then

Max_Current_Before_Overflow = MaxPossible_I

Else

Max_Current_Before_Overflow = Max_Current

End If

(Note that Max_Current is greater than MaxPossible_I in this example.)

Max_Current_Before_Overflow = 0.64 (Note: This result is displayed by software as seen in Figure 20)

$$\text{Max\_ShuntVoltage} = \text{Max\_Current\_Before\_Overflow} \times R_{SHUNT}$$

$$\text{Max\_ShuntVoltage} = 0.32 \quad (7)$$

If Max_ShuntVoltage ≥ V_{SHUNT_MAX}

Max_ShuntVoltage_Before_Overflow = V_{SHUNT_MAX}

Else

Max_ShuntVoltage_Before_Overflow= Max_ShuntVoltage

End If

(Note that Max_ShuntVoltage is greater than V_{SHUNT_MAX} in this example.)

Max_ShuntVoltage_Before_Overflow = 0.32 (Note: This result is displayed by software as seen in Figure 20)

8. Compute the maximum power with Equation 8.

$$\text{MaximumPower} = \text{Max\_Current\_Before\_Overflow} \times V_{BUS\_MAX}$$

$$\text{MaximumPower} = 20.48 \quad (8)$$

9. (Optional second calibration step) Compute corrected full-scale calibration value based on measured current.

INA220B-Q1_Current = 0.63484

MeasShuntCurrent = 0.55

$$\text{Corrected\_Full\_Scale\_Cal} = \text{trunc}\left[\frac{\text{Cal} \times \text{MeasShuntCurrent}}{\text{INA220\_Current}}\right]$$

$$\text{Corrected\_Full\_Scale\_Cal} = 3548 \quad (9)$$

Figure 20 illustrates how to perform the same procedure discussed in this example using the automated INA220B-Q1 EVM software. Note that the same numbers used in the nine-step example are used in the software example in Figure 20. Also note that Figure 20 illustrates which results correspond to which step (for example, the information entered in step 1 is enclosed in a box in Figure 20 and labeled).

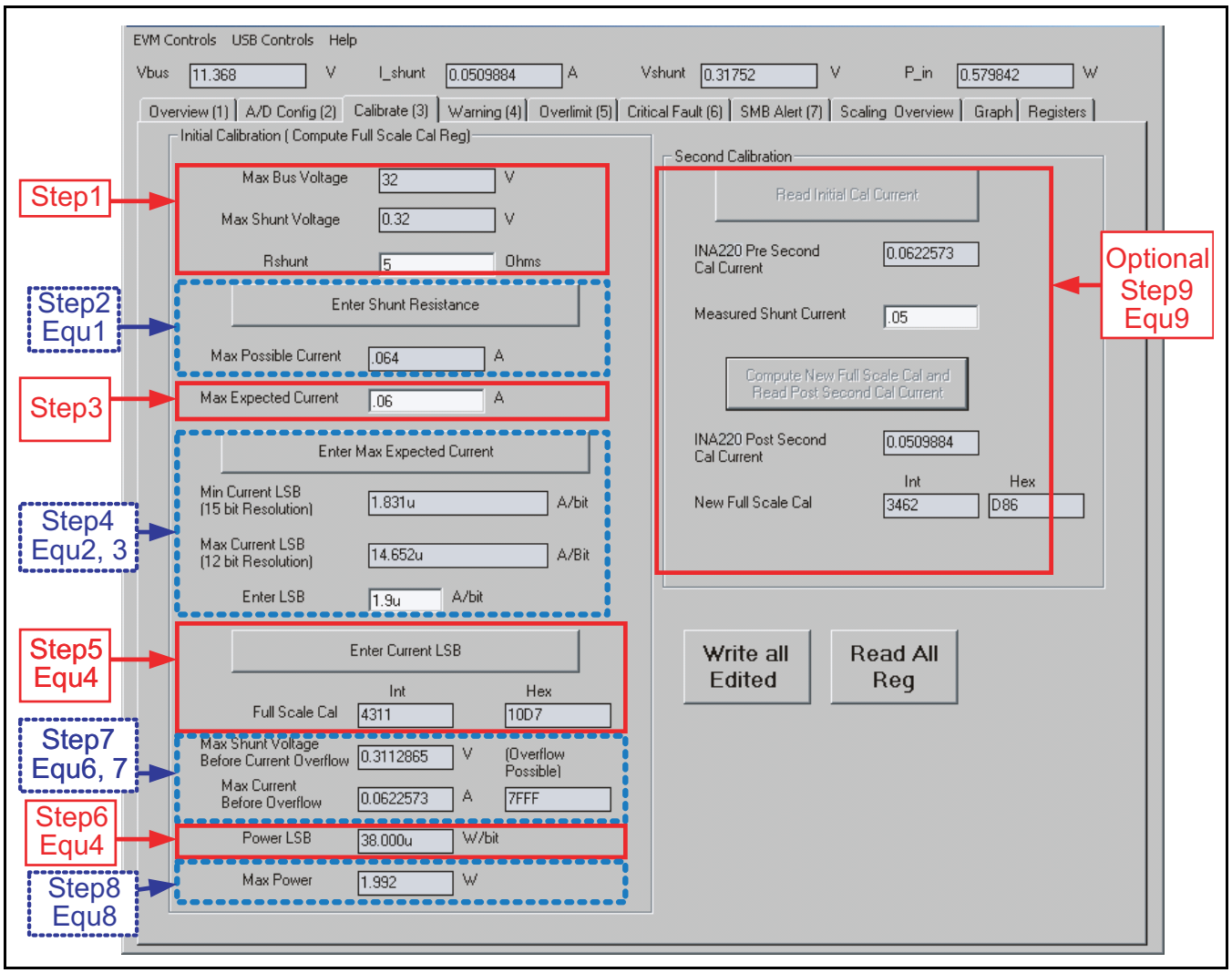


Figure 20. INA220B-Q1 EVM Calibration Software Automatically Computes Calibration Steps 1-9

Calibration Example 2 (Overflow Possible)

This design example uses the nine-step procedure for calibrating the INA220B-Q1 device where overflow is possible. Figure 21 illustrates how the same procedure is performed using the automated INA220B-Q1 EVM software. Note that the same numbers used in the nine-step example are used in the software example in Figure 21. Also note that Figure 21 illustrates which results correspond to which step (for example, the information entered in step 1 is circled in Figure 21 and labeled).

1. Establish the following parameters:

   V_{BUS_MAX} = 32

   V_{SHUNT_MAX} = 0.32

   R_{SHUNT} = 5

2. Determine the maximum possible current using Equation 10:

$$\text{MaxPossible\_I} = \frac{V_{SHUNT\_MAX}}{R_{SHUNT}}$$

$$\text{MaxPossible\_I} = 0.064 \tag{10}$$

3. Choose the desired maximum current value: Max_Expected_I, ≤ MaxPossible_I. This value is selected based on system expectations.

   Max_Expected_I = 0.06

4. Calculate the possible range of current LSBs. This calculation is done by first computing a range of LSBs that is appropriate for the design. Next, select an LSB withing this range. Note that the results will have the most resolution when the minimum LSB is selected. Typically, an LSB is selected to be the nearest round number to the minimum LSB.

$$\text{Minimum\_LSB} = \frac{\text{Max\_Expected\_I}}{32767}$$

$$\text{Minimum\_LSB} = 1.831 \times 10^{-6} \tag{11}$$

$$\text{Maximum\_LSB} = \frac{\text{Max\_Expected\_I}}{4096}$$

$$\text{Maximum\_LSB} = 14.652 \times 10^{-6} \tag{12}$$

   Choose an LSB in the range: Minimum_LSB<Selected_LSB<Maximum_LSB

   Current_LSB = 1.9×10^{-6}

   Note:

   This value was selected to be a round number near the Minimum_LSB. This section allows for good resolution with a rounded LSB.

5. Compute the Calibration Register using Equation 13:

$$\text{Cal} = \text{trunc}\left(\frac{0.04096}{\text{Current\_LSB} \times R_{SHUNT}}\right) \quad \text{Cal} = 4311 \tag{13}$$

6. Calculate the Power_LSB using Equation 14. Equation 14 shows a general formula; because the bus voltage measurement LSB is always 4 mV, the power formula reduces to calculate the result.

$$\text{Power\_LSB} = 20\ \text{Current\_LSB}$$

$$\text{Power\_LSB} = 38 \times 10^{-6} \tag{14}$$

7. Compute the maximum current and shunt voltage values (before overflow), as shown by Equation 15 and Equation 16. Note that both Equation 15 and Equation 16 involve an If - then condition.

Max_Current = Current_LSB × 32767

Max_Current = 0.06226 (15)

If Max_Current ≥ Max Possible_I then

Max_Current_Before_Overflow = MaxPossible_I

Else

Max_Current_Before_Overflow = Max_Current

End If

(Note that Max_Current is less than MaxPossible_I in this example.)

Max_Current_Before_Overflow = 0.06226 (Note: This result is displayed by software as seen in Figure 21)

Max_ShuntVoltage = Max_Current_Before_Overflow × R_{SHUNT}

Max_ShuntVoltage = 0.3113 (16)

If Max_ShuntVoltage ≥ V_{SHUNT_MAX}

Max_ShuntVoltage_Before_Overflow = V_{SHUNT_MAX}

Else

Max_ShuntVoltage_Before_Overflow = Max_ShuntVoltage

End If

(Note that Max_ShuntVoltage is less than V_{SHUNT_MAX} in this example)

Max_ShuntVoltage_Before_Overflow = 0.3113 (Note: This result is displayed by software as seen in Figure 21)

8. Compute the maximum power with equation 8.

MaximumPower = Max_Current_Before_Overflow × V_{BUS_MAX}

MaximumPower = 1.992 (17)

9. (Optional second calibration step) Compute the corrected full-scale calibration value based on measured current.

INA220B-Q1_Current = 0.06226

MeaShuntCurrent = 0.05

$$\text{Corrected\_Full\_Scale\_Cal} = \text{trunc}\left[\frac{\text{Cal} \times \text{MeasShuntCurrent}}{\text{INA220\_Current}}\right]$$

Corrected_Full_Scale_Cal = 3462 (18)

Figure 21 illustrates how to perform the same procedure discussed in this example using the automated INA220B-Q1 EVM software. Note that the same numbers used in the nine-step example are used in the software example in Figure 21.

Also note that Figure 21 illustrates which results correspond to which step (for example, the information entered in step 1 is enclosed in a box in Figure 21 and labeled).

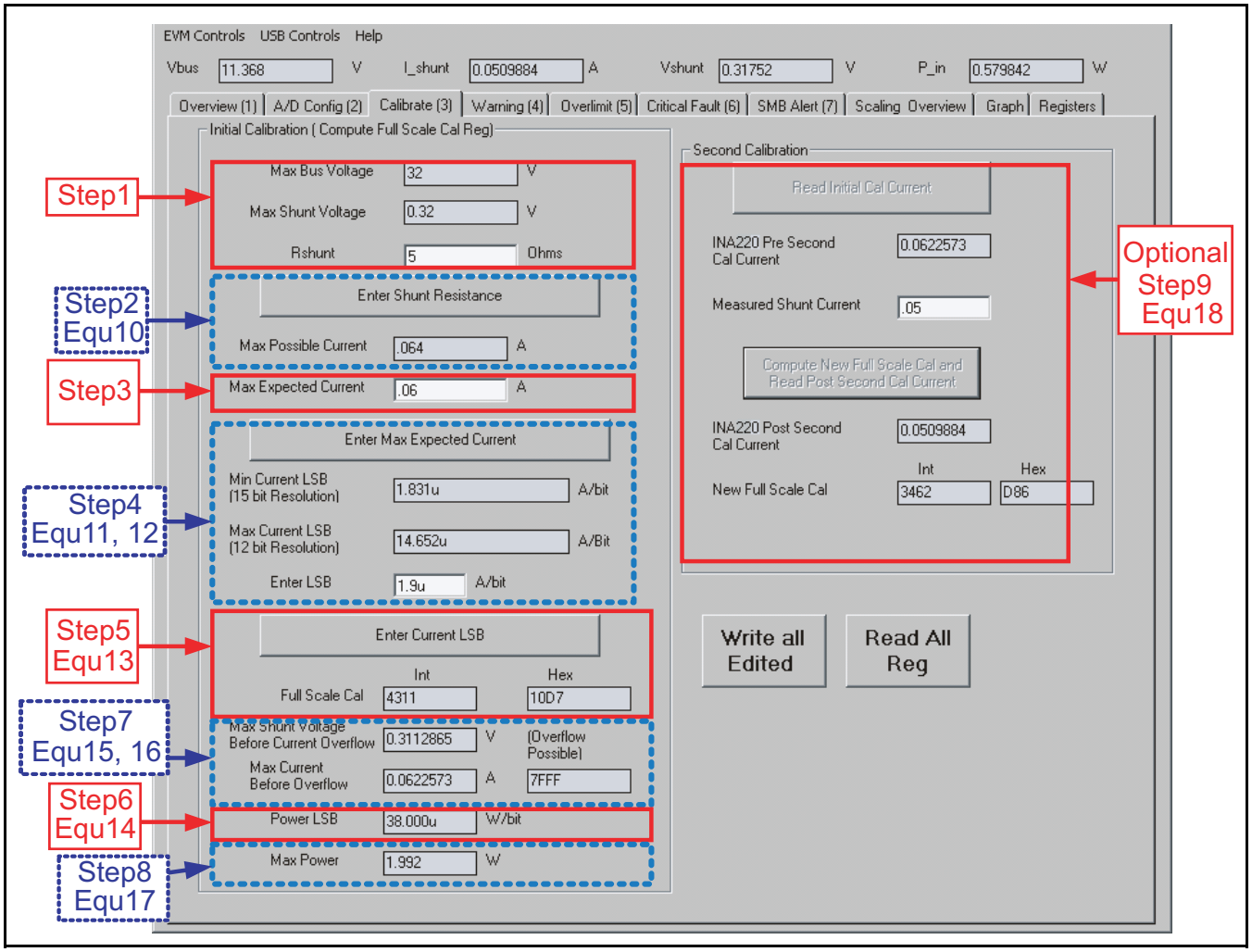


Figure 21. INA220B-Q1 EVM Calibration Software Automatically Computes Calibration Steps 1-9

CONFIGURE, MEASURE, AND CALCULATE EXAMPLE

In this example, the 10 A load creates a differential voltage of 20 mV across a 2 mΩ shunt resistor. The voltage present at the V_{IN-} pin is equal to the common-mode voltage minus the differential drop across the resistor. The bus voltage for the INA220B-Q1 device is measured at the external V_{BUS} input pin, which in this example is connected to the V_{IN-} pin to measure the voltage level delivered to the load. For this example, the voltage at the V_{IN-} pin is 11.98 V. For this particular range (40 mV full-scale), this small difference is not a significant deviation from the 12 V common-mode voltage. However, at larger full-scale ranges, this deviation can be much larger.

Note that the Bus Voltage Register bits are not right-aligned. In order to compute the value of the Bus Voltage Register contents using the LSB of 4 mV, the register must be shifted right by three bits. This shift puts the BD0 bit in the LSB position so that the contents can be multiplied by the 4 mV LSB value to compute the bus voltage measured by the device. The shifted value of the Bus Voltage Register contents is now equal to BB3h, a decimal equivalent of 2995. This value of 2995 multiplied by the 4 mV LSB results in a value of 11.98 V.

The Calibration Register (05h) is set in order to provide the device information about the current shunt resistor that was used to create the measured shunt voltage. By knowing the value of the shunt resistor, the device can then calculate the amount of current that created the measured shunt voltage drop. The first step when calculating the calibration value is setting the current LSB. The Calibration Register value is based on a calculation that has its precision capability limited by the size of the register and the Current Register LSB. The device can measure bidirectional current; thus, the MSB of the Current Register is a sign bit that allows for the rest of the 15 bits to be used for the Current Register value. It is common when using the current value calculations to use a resolution between 12 bits and 15 bits. Calculating the current LSB for each of these resolutions provides minimum and maximum values. These values are calculated assuming the maximum current that will be expected to flow through the current shunt resistor, as shown in Equation 2 and Equation 3. To simplify the mathematics, it is common to choose a round number located between these two points. For this example, the maximum current LSB is 3.66 mA/bit and the minimum current LSB would be 457.78 µA/bit assuming a maximum expected current of 15 A. For this example, a value of 1 mA/bit was chosen for the current LSB. Setting the current LSB to this value allows for sufficient precision while serving to simplify the math as well. Using Equation 4 results in a Calibration Register value of 20480, or 5000h.

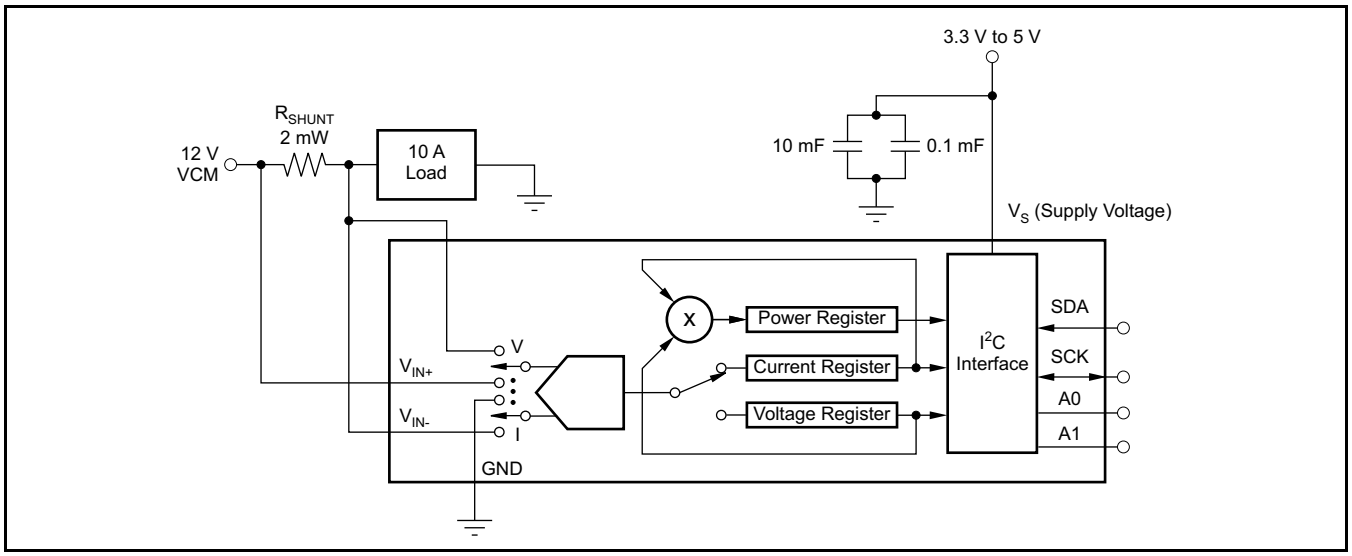


Figure 22. Example Circuit Configuration

The Current Register (04h) is then calculated by multiplying the shunt voltage contents by the Calibration Register and then dividing by 4095. For this example, the shunt voltage of 2000 is multiplied by the Calibration Register of 20480 and then divided by 4095 to yield a Current Register of 2712h.

The Power Register (03h) is then be calculated by multiplying the Current Register of 10002 by the Bus Voltage Register of 2995 and then dividing by 5000. For this example, the Power Register contents are 1767h, or a decimal equivalent of 5991. Multiplying this result by the power LSB that is 20 times the 1×10^{-3} current LSB, or 20×10^{-3}, results in a power calculation of 5991 × 20 mW/bit, which equals 119.82 W. This result matches what is expected for this register. A manual calculation for the power being delivered to the load would use 11.98 V (12VCM – 20 mV shunt drop) multiplied by the load current of 10 A to give a 119.8 W result.

Table 2 shows the steps for configuring, measuring, and calculating the values for current and power for this device.

Table 2. Configure, Measure, and Calculate Example(1)

STEP #	REGISTER NAME	ADDRESS	CONTENTS	ADJ	DEC	LSB	VALUE
Step 1	Configuration	00h	019Fh				
Step 2	Shunt	01h	07D0h		2000	10 µV	20 mV
Step 3	Bus	02h	5D98h	0BB3	2995	4 mV	11.98 V
Step 4	Calibration	05h	5000h		20480		
Step 5	Current	04h	2712h		10002	1 mA	10.002 A
Step 6	Power	03h	1767h		5991	20 mW	119.82 W

(1) Conditions: load = 10 A, V_{CM} = 12 V, R_{SHUNT} = 2 mΩ, V_{SHUNT} FSR = 40 mV, and V_{BUS} = 16 V.

REGISTER INFORMATION

The INA220B-Q1 device uses a bank of registers for holding configuration settings, measurement results, maximum and minimum limits, and status information. Table 3 summarizes the INA220B-Q1 device registers; Figure 13 illustrates the registers.

Register contents are updated 4 µs after completion of the write command. Therefore, a 4 µs delay is required between completion of a write to a given register and a subsequent read of that register (without changing the pointer) when using SCL frequencies in excess of 1 MHz.

Table 3. Summary of Register Set

POINTER ADDRESS			POWER-ON RESET		
HEX	REGISTER NAME	FUNCTION	BINARY	HEX	TYPE(1)
00	Configuration Register	All-register reset, settings for bus voltage range, PGA Gain, ADC resolution and averaging	00111001 10011111	399F	R/$\overline{W}$
01	Shunt Voltage	Shunt voltage measurement data	Shunt voltage	—	R
02	Bus Voltage	Bus voltage measurement data	Bus voltage	—	R
03	Power(2)	Power measurement data	00000000 00000000	0000	R
04	Current(2)	Contains the value of the current flowing through the shunt resistor	00000000 00000000	0000	R
05	Calibration	Sets full-scale range and LSB of current and power measurements; overall system calibration	00000000 00000000	0000	R/$\overline{W}$

(1) Type: **R** = Read-Only, **R/$\overline{W}$** = Read/Write.
(2) The Power Register and Current Register default to '0' because the Calibration Register defaults to '0', yielding a zero current value until the Calibration Register is programmed.

REGISTER DETAILS

All INA220B-Q1 device registers 16-bit registers are actually two 8-bit bytes through the 2-wire interface.

Configuration Register 00h (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RST	—	BRNG	PG1	PG0	BADC4	BADC3	BADC2	BADC1	SADC4	SADC3	SADC2	SADC1	MODE3	MODE2	MODE1
POR VALUE	0	0	1	1	1	0	0	1	1	0	0	1	1	1	1	1

Bit Descriptions

RST: **Reset Bit**

Bit 15 Setting this bit to '1' generates a system reset that is the same as power-on reset. Resets all registers to default values; this bit self-clears.

BRNG: **Bus Voltage Range**

Bit 13
0 = 16 V FSR
1 = 32 V FSR (default value)

PG: **PGA (Shunt Voltage Only)**

Bits 11, 12 Sets PGA gain and range. Note that the PGA defaults to ÷8 (320 mV range). Table 4 shows the gain and range for the various product gain settings.

Table 4. PG Bit Settings [12:11] (1)

PG1	PG0	GAIN	RANGE
0	0	1	±40 mV
0	1	÷2	±80 mV
1	0	÷4	±160 mV
1	1	÷8	±320 mV

(1) Shaded values are default.

BADC: **BADC Bus ADC Resolution/Averaging**

Bits 7–10 These bits adjust the Bus ADC resolution (9-, 10-, 11-, or 12-bit) or set the number of samples used when averaging results for the Bus Voltage Register (02h).

SADC: **SADC Shunt ADC Resolution/Averaging**

Bits 3–6 These bits adjust the Shunt ADC resolution (9-, 10-, 11-, or 12-bit) or set the number of samples used when averaging results for the Shunt Voltage Register (01h).
BADC (Bus) and SADC (Shunt) ADC resolution/averaging and conversion time settings are shown in Table 5.

Table 5. ADC Settings (SADC [6:3], BADC [10:7])(1)

ADC4	ADC3	ADC2	ADC1	MODE/SAMPLES	CONVERSION TIME
0	X(2)	0	0	9-bit	84 µs
0	X(2)	0	1	10-bit	148 µs
0	X(2)	1	0	11-bit	276 µs
0	X(2)	1	1	12-bit	532 µs
1	0	0	0	12-bit	532 µs
1	0	0	1	2	1.06 ms
1	0	1	0	4	2.13 ms
1	0	1	1	8	4.26 ms
1	1	0	0	16	8.51 ms
1	1	0	1	32	17.02 ms
1	1	1	0	64	34.05 ms
1	1	1	1	128	68.10 ms

(1) Shaded values are default.
(2) X = Don't care.

MODE: **Operating Mode**

Bits 0–2 Selects continuous, triggered, or power-down mode of operation. These bits default to continuous shunt and bus measurement mode. The mode settings are shown in Table 6.

Table 6. Mode Settings [2:0](1)

MODE3	MODE2	MODE1	MODE
0	0	0	Power-Down
0	0	1	Shunt Voltage, Triggered
0	1	0	Bus Voltage, Triggered
0	1	1	Shunt and Bus, Triggered
1	0	0	ADC Off (disabled)
1	0	1	Shunt Voltage, Continuous
1	1	0	Bus Voltage, Continuous
1	1	1	Shunt and Bus, Continuous

(1) Shaded values are default.

DATA OUTPUT REGISTERS

Shunt Voltage Register 01h (Read-Only)

The Shunt Voltage Register stores the current shunt voltage reading, V_{SHUNT}. Shunt Voltage Register bits are shifted according to the PGA setting selected in the Configuration Register (00h). When multiple sign bits are present, they will all be the same value. Negative numbers are represented in twos complement format. Generate the twos complement of a negative number by complementing the absolute value binary number and adding 1. Extend the sign, denoting a negative number by setting the MSB = '1'. Extend the sign to any additional sign bits to form the 16-bit word.

Example: For a value of V_{SHUNT} = –320 mV:

1. Take the absolute value (include accuracy to 0.01 mV) ==> 320.00
2. Translate this number to a whole decimal number ==> 32000
3. Convert it to binary ==> 111 1101 0000 0000
4. Complement the binary result : 000 0010 1111 1111
5. Add 1 to the complement to create the twos complement formatted result ==> 000 0011 0000 0000
6. Extend the sign and create the 16-bit word: 1000 0011 0000 0000 = 8300h (Remember to extend the sign to all sign-bits, as necessary based on the PGA setting)

At PGA = ÷8, full-scale range = ±320 mV (decimal = 32000, positive value hex = 7D00, negative value hex = 8300), and LSB = 10 µV.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SD14_8	SD13_8	SD12_8	SD11_8	SD10_8	SD9_8	SD8_8	SD7_8	SD6_8	SD5_8	SD4_8	SD3_8	SD2_8	SD1_8	SD0_8
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

At PGA = ÷4, full-scale range = ±160 mV (decimal = 16000, positive value hex = 3E80, negative value hex = C180), and LSB = 10 µV.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SIGN	SD13_4	SD12_4	SD11_4	SD10_4	SD9_4	SD8_4	SD7_4	SD6_4	SD5_4	SD4_4	SD3_4	SD2_4	SD1_4	SD0_4
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

At PGA = ÷2, full-scale range = ±80 mV (decimal = 8000, positive value hex = 1F40, negative value hex = E0C0), and LSB = 10 µV.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SIGN	SIGN	SD12_2	SD11_2	SD10_2	SD9_2	SD8_2	SD7_2	SD6_2	SD5_2	SD4_2	SD3_2	SD2_2	SD1_2	SD0_2
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

At PGA = ÷1, full-scale range = ±40 mV (decimal = 4000, positive value hex = 0FA0, negative value hex = F060), and LSB = 10 µV.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SIGN	SIGN	SIGN	SD11_1	SD10_1	SD9_1	SD8_1	SD7_1	SD6_1	SD5_1	SD4_1	SD3_1	SD2_1	SD1_1	SD0_1
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7. Shunt Voltage Register Format(1)

V_{SHUNT} Reading (mV)	Decimal Value	PGA = ÷ 8 (D15…….D0)	PGA = ÷ 4 (D15…….D0)	PGA = ÷ 2 (D15…….D0)	PGA = ÷ 1 (D15…….D0)
320.02	32002	0111 1101 0000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
320.01	32001	0111 1101 0000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
320.00	32000	0111 1101 0000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
319.99	31999	0111 1100 1111 1111	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
319.98	31998	0111 1100 1111 1110	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
⋮	⋮	⋮	⋮	⋮	⋮
160.02	16002	0011 1110 1000 0010	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
160.01	16001	0011 1110 1000 0001	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
160.00	16000	0011 1110 1000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
159.99	15999	0011 1110 0111 1111	0011 1110 0111 1111	0001 1111 0100 0000	0000 1111 1010 0000
159.98	15998	0011 1110 0111 1110	0011 1110 0111 1110	0001 1111 0100 0000	0000 1111 1010 0000
⋮	⋮	⋮	⋮	⋮	⋮
80.02	8002	0001 1111 0100 0010	0001 1111 0100 0010	0001 1111 0100 0000	0000 1111 1010 0000
80.01	8001	0001 1111 0100 0001	0001 1111 0100 0001	0001 1111 0100 0000	0000 1111 1010 0000
80.00	8000	0001 1111 0100 0000	0001 1111 0100 0000	0001 1111 0100 0000	0000 1111 1010 0000
79.99	7999	0001 1111 0011 1111	0001 1111 0011 1111	0001 1111 0011 1111	0000 1111 1010 0000
79.98	7998	0001 1111 0011 1110	0001 1111 0011 1110	0001 1111 0011 1110	0000 1111 1010 0000
⋮	⋮	⋮	⋮	⋮	⋮
40.02	4002	0000 1111 1010 0010	0000 1111 1010 0010	0000 1111 1010 0010	0000 1111 1010 0000
40.01	4001	0000 1111 1010 0001	0000 1111 1010 0001	0000 1111 1010 0001	0000 1111 1010 0000
40.00	4000	0000 1111 1010 0000	0000 1111 1010 0000	0000 1111 1010 0000	0000 1111 1010 0000
39.99	3999	0000 1111 1001 1111	0000 1111 1001 1111	0000 1111 1001 1111	0000 1111 1001 1111
39.98	3998	0000 1111 1001 1110	0000 1111 1001 1110	0000 1111 1001 1110	0000 1111 1001 1110
⋮	⋮	⋮	⋮	⋮	⋮
0.02	2	0000 0000 0000 0010	0000 0000 0000 0010	0000 0000 0000 0010	0000 0000 0000 0010
0.01	1	0000 0000 0000 0001	0000 0000 0000 0001	0000 0000 0000 0001	0000 0000 0000 0001
0	0	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000
–0.01	–1	1111 1111 1111 1111	1111 1111 1111 1111	1111 1111 1111 1111	1111 1111 1111 1111
–0.02	–2	1111 1111 1111 1110	1111 1111 1111 1110	1111 1111 1111 1110	1111 1111 1111 1110
⋮	⋮	⋮	⋮	⋮	⋮
–39.98	–3998	1111 0000 0110 0010	1111 0000 0110 0010	1111 0000 0110 0010	1111 0000 0110 0010
–39.99	–3999	1111 0000 0110 0001	1111 0000 0110 0001	1111 0000 0110 0001	1111 0000 0110 0001
–40.00	–4000	1111 0000 0110 0000	1111 0000 0110 0000	1111 0000 0110 0000	1111 0000 0110 0000
–40.01	–4001	1111 0000 0101 1111	1111 0000 0101 1111	1111 0000 0101 1111	1111 0000 0110 0000
–40.02	–4002	1111 0000 0101 1110	1111 0000 0101 1110	1111 0000 0101 1110	1111 0000 0110 0000
⋮	⋮	⋮	⋮	⋮	⋮
–79.98	–7998	1110 0000 1100 0010	1110 0000 1100 0010	1110 0000 1100 0010	1111 0000 0110 0000
–79.99	–7999	1110 0000 1100 0001	1110 0000 1100 0001	1110 0000 1100 0001	1111 0000 0110 0000
–80.00	–8000	1110 0000 1100 0000	1110 0000 1100 0000	1110 0000 1100 0000	1111 0000 0110 0000
–80.01	–8001	1110 0000 1011 1111	1110 0000 1011 1111	1110 0000 1100 0000	1111 0000 0110 0000
–80.02	–8002	1110 0000 1011 1110	1110 0000 1011 1110	1110 0000 1100 0000	1111 0000 0110 0000
⋮	⋮	⋮	⋮	⋮	⋮
–159.98	–15998	1100 0001 1000 0010	1100 0001 1000 0010	1110 0000 1100 0000	1111 0000 0110 0000
–159.99	–15999	1100 0001 1000 0001	1100 0001 1000 0001	1110 0000 1100 0000	1111 0000 0110 0000
–160.00	–16000	1100 0001 1000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–160.01	–16001	1100 0001 0111 1111	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–160.02	–16002	1100 0001 0111 1110	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
⋮	⋮	⋮	⋮	⋮	⋮
–319.98	–31998	1000 0011 0000 0010	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–319.99	–31999	1000 0011 0000 0001	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–320.00	–32000	1000 0011 0000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–320.01	–32001	1000 0011 0000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
–320.02	–32002	1000 0011 0000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000

(1) Out-of-range values are shown in grey shading.

Bus Voltage Register 02h (Read-Only)

The Bus Voltage Register stores the most recent bus voltage reading, V_{BUS}.

At full-scale range = 32 V (decimal = 8000, hex = 1F40), and LSB = 4 mV.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	BD12	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	CNVR	OVF
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

At full-scale range = 16 V (decimal = 4000, hex = 0FA0), and LSB = 4 mV.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	0	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	CNVR	OVF
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CNVR: **Conversion Ready**

Bit 1

Although the data from the last conversion can be read at any time, the INA220B-Q1 device conversion ready (CNVR) bit indicates when data from a conversion is available in the data output registers. The CNVR bit is set after all conversions, averaging, and multiplications are complete. CNVR will clear under the following conditions:

1.) Writing a new mode into the operating MODE bits in the Configuration Register (except for Power-down or Disable)

2.) Reading the Power Register

OVF: **Math Overflow Flag**

Bit 0

The Math Overflow Flag (OVF) is set when the power or current calculations are out of range. It indicates that current and power data may be meaningless.

Power Register 03h (Read-Only)

Full-scale range and LSB are set by the Calibration Register. See the *Programming the INA220 Power Measurement Engine* section.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Power Register records power in watts by multiplying the values of the current with the value of the bus voltage according to the equation:

$$\text{Power} = \frac{\text{Current} \times \text{BusVoltage}}{5000}$$

Current Register 04h (Read-Only)

Full-scale range and LSB depend on the value entered in the Calibration Register. See the *Programming the INA220 Power Measurement Engine* section. Negative values are stored in twos complement format.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CSIGN	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The value of the Current Register is calculated by multiplying the value in the Shunt Voltage Register with the value in the Calibration Register according to the equation:

$$\text{Current} = \frac{\text{ShuntVoltage} \times \text{Calibration Register}}{4096}$$

CALIBRATION REGISTER

Calibration Register 05h (Read/Write)

Current and power calibration are set by bits D15 to D1 of the Calibration Register. Note that bit D0 is not used in the calculation. This register sets the current that corresponds to a full-scale drop across the shunt. Full-scale range and the LSB of the current and power measurement depend on the value entered in this register. See the *Programming the INA220 Power Measurement Engine* section. This register is suitable for use in overall system calibration. Note that the '0' POR values are all default.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0(1)
BIT NAME	FS15	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) D0 is a *void* bit and will always be '0'. It is not possible to write a '1' to D0. CALIBRATION is the value stored in D15:D1.

ADDITIONAL APPLICATION IDEAS

Figure 23, Figure 24, and Figure 25 show the INA220B-Q1 device in additional circuit configurations for current, voltage, and power monitoring applications.

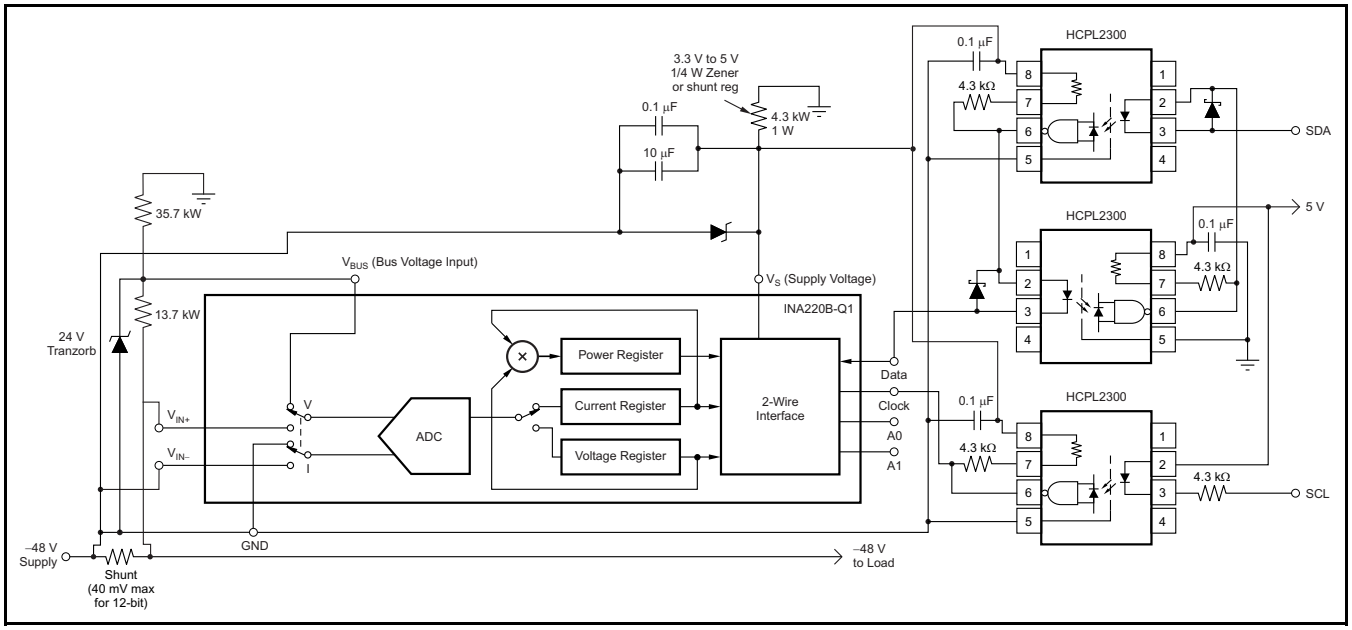


Figure 23. –48 V Telecom Current, Voltage, and Power Sense with Isolation

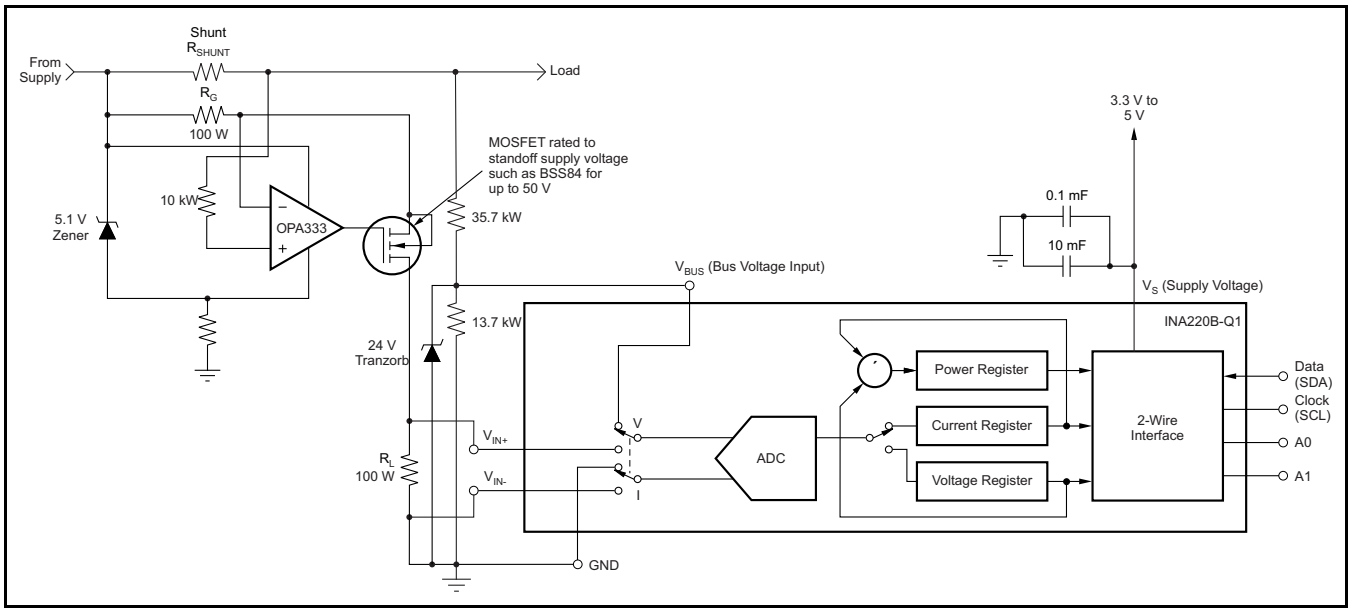


Figure 24. 48 V Telecom Current, Voltage, and Power Sense

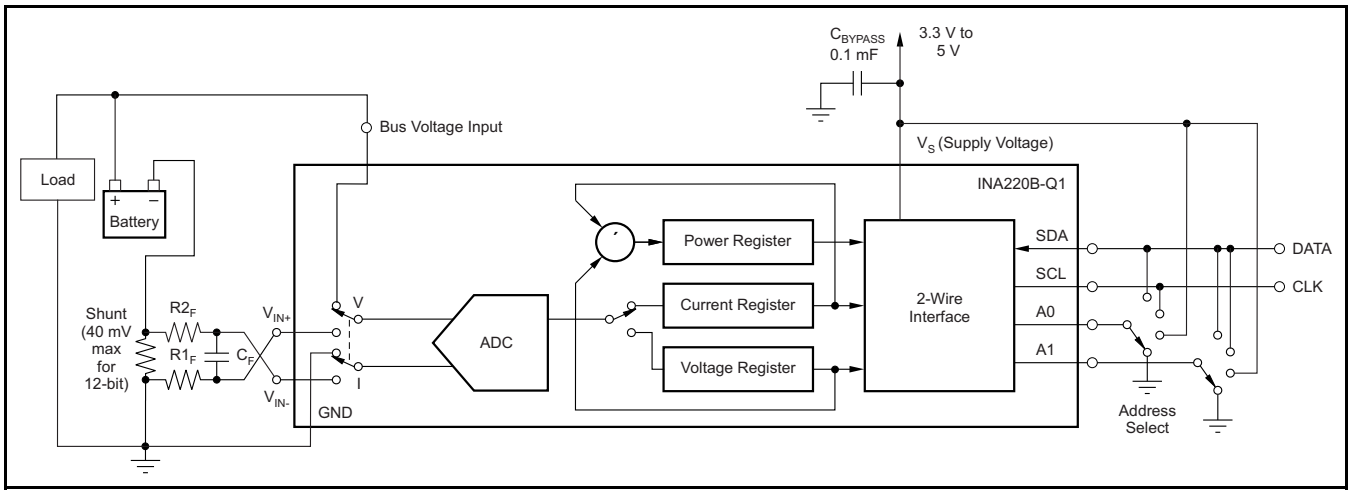


Figure 25. General Source Low-Side Sensing

REVISION HISTORY

Changes from Original (June 2012) to Revision A	Page
• Device went from preview to production	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
INA220BQDGSRQ1	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

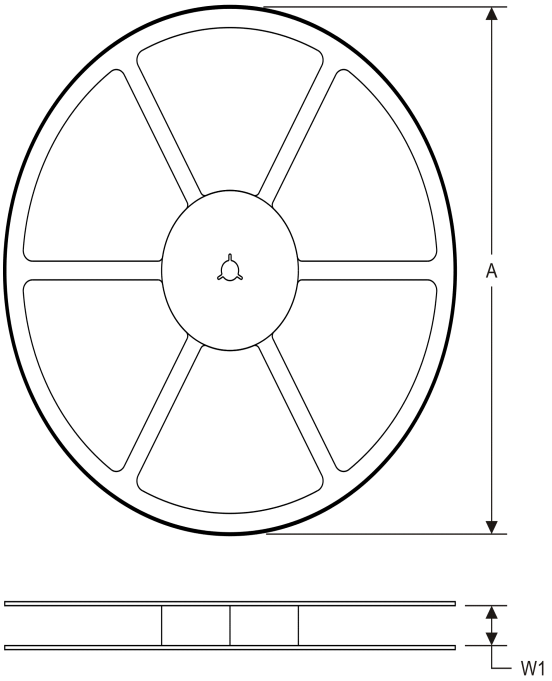
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

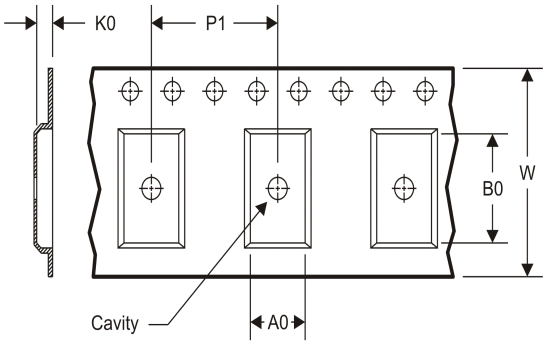
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



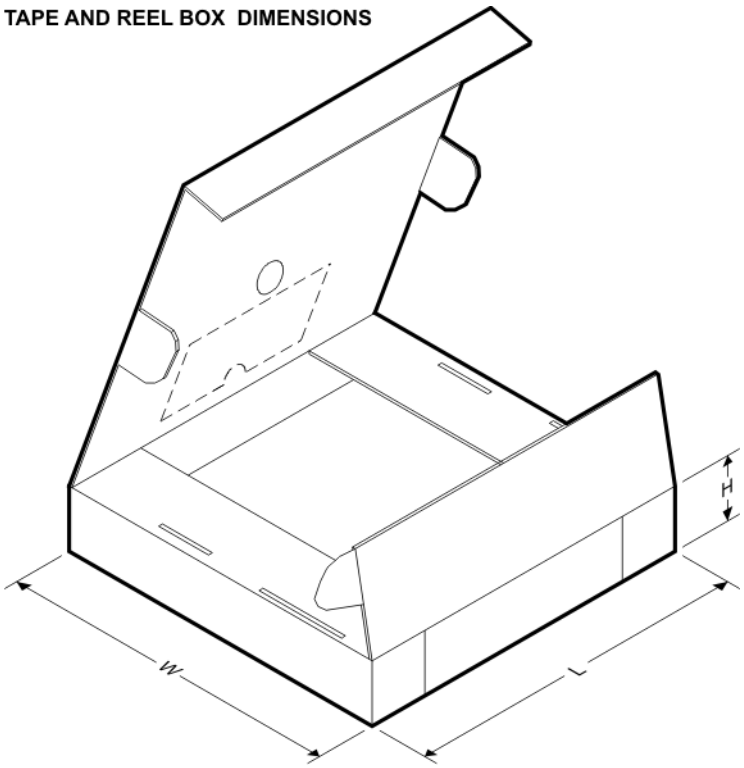
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA220BQDGSRQ1	MSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

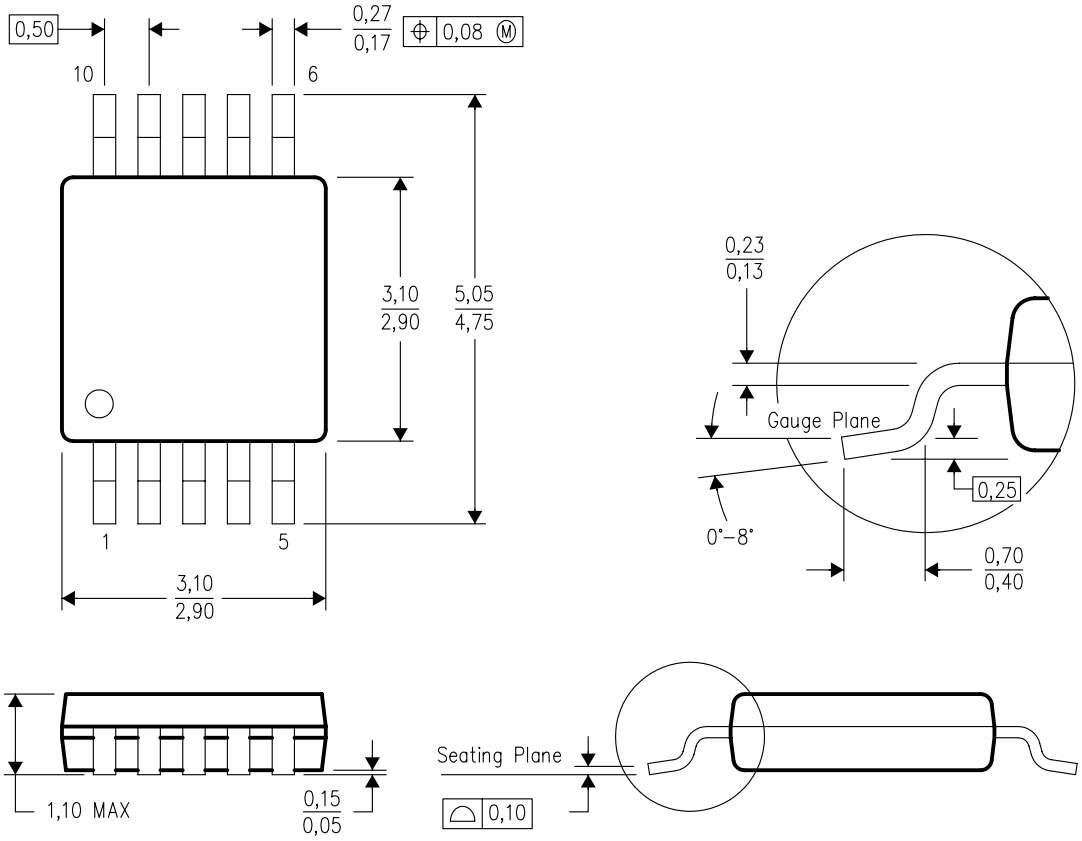
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA220BQDGSRQ1	MSOP	DGS	10	2500	366.0	364.0	50.0

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

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