CMLDM8005

SURFACE MOUNT SILICON DUAL P-CHANNEL ENHANCEMENT-MODE MOSFET

SOT-563 CASE

www.centralsemi.com

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CMLDM8005 consists of dual P-Channel enhancement-mode silicon MOSFETs designed for high speed pulsed amplifier and driver applications. These MOSFETs offer very low $r_{DS(ON)}$ and low threshold voltage.

MARKING CODE: CC8

APPLICATIONS:

- Load switch/Level shifting
- Battery charging
- Boost switch
- Electro-luminescent backlighting

FEATURES:

- ESD protection up to 1800V (Human Body Model)
- 350mW power dissipation
- Very low $r_{DS(ON)}$
- Low threshold voltage
- Logic level compatible
- Small, SOT-563 surface mount package
- Complementary dual N-Channel device: CMLDM7005

MAXIMUM RATINGS: (T_A=25°C)	**SYMBOL**		**UNITS**
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	8.0	V
Continuous Drain Current (Steady State - Note 1)	I_D	650	mA
Continuous Source Current (Body Diode)	I_S	250	mA
Maximum Pulsed Drain Current	I_{DM}	1.0	A
Power Dissipation (Note 1)	P_D	350	mW
Power Dissipation (Note 2)	P_D	300	mW
Power Dissipation (Note 2)	P_D	150	mW
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	°C
Thermal Resistance (Note 1)	Θ_{JA}	357	°C/W

ELECTRICAL CHARACTERISTICS PER TRANSISTOR: (T_A=25°C unless otherwise noted)

SYMBOL	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
I_{GSSF}, I_{GSSR}	V_{GS}=4.5V, V_{DS}=0			10	μA
I_{DSS}	V_{DS}=16V, V_{GS}=0			100	nA
BV_{DSS}	V_{GS}=0, I_D=250μA	20			V
$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	0.5		1.0	V
V_{SD}	V_{GS}=0, I_S=250mA			1.1	V
$r_{DS(ON)}$	V_{GS}=4.5V, I_D=350mA		0.25	0.36	Ω
$r_{DS(ON)}$	V_{GS}=2.5V, I_D=300mA		0.37	0.5	Ω
$r_{DS(ON)}$	V_{GS}=1.8V, I_D=150mA			0.8	Ω

Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 4.0mm^2
(2) FR-4 Epoxy PC Board with copper mounting pad area of 4.0mm^2
(3) FR-4 Epoxy PC Board with copper mounting pad area of 1.4mm^2

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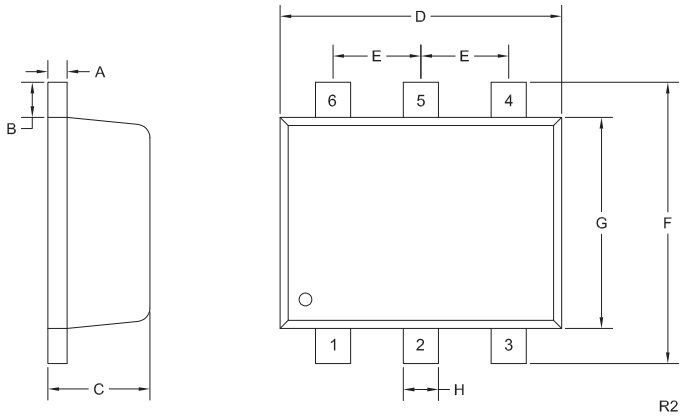
ELECTRICAL CHARACTERISTICS PER TRANSISTOR - Continued: (T_A=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	UNITS
g_{FS}	V_{DS}=10V, I_D=200mA	0.2		S
C_{rss}	V_{DS}=16V, V_{GS}=0, f=1.0MHz		25	pF
C_{iss}	V_{DS}=16V, V_{GS}=0, f=1.0MHz		100	pF
C_{oss}	V_{DS}=16V, V_{GS}=0, f=1.0MHz		21	pF
$Q_{g(tot)}$	V_{DS}=10V, V_{GS}=4.5V, I_D=200mA		1.2	nC
Q_{gs}	V_{DS}=10V, V_{GS}=4.5V, I_D=200mA		0.24	nC
Q_{gd}	V_{DS}=10V, V_{GS}=4.5V, I_D=200mA		0.36	nC
t_{on}	V_{DD}=10V, V_{GS}=4.5V, I_D=200mA, R_G=10Ω		38	ns
t_{off}	V_{DD}=10V, V_{GS}=4.5V, I_D=200mA, R_G=10Ω		48	ns

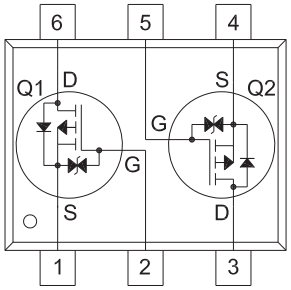
SOT-563 CASE - MECHANICAL OUTLINE



DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.0027	0.007	0.07	0.18
B	0.008		0.20	
C	0.017	0.024	0.45	0.60
D	0.059	0.067	1.50	1.70
E	0.020		0.50	
F	0.059	0.067	1.50	1.70
G	0.043	0.051	1.10	1.30
H	0.006	0.012	0.15	0.30

SOT-563 (REV: R2)

PIN CONFIGURATION



LEAD CODE:
1) Source Q1
2) Gate Q1
3) Drain Q2
4) Source Q2
5) Gate Q2
6) Drain Q1

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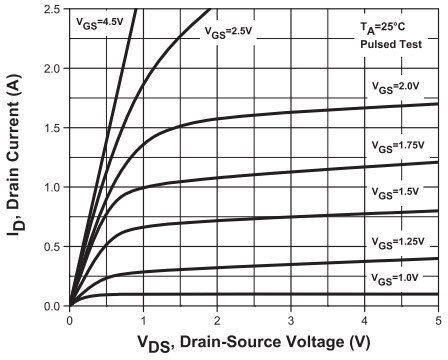
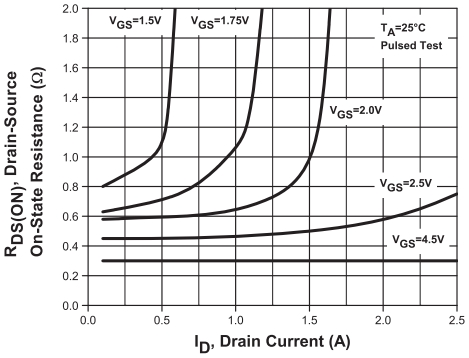
TYPICAL ELECTRICAL CHARACTERISTICS

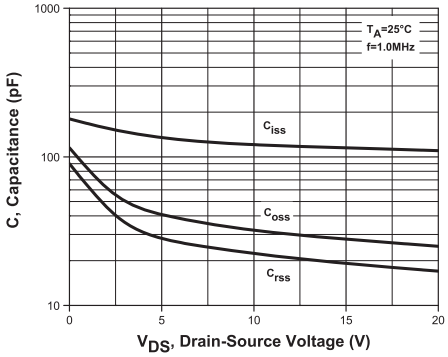
Output Characteristics



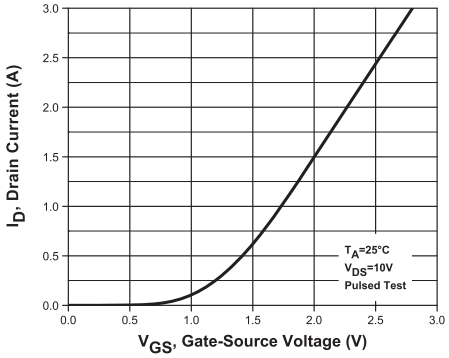
Drain Source On Resistance



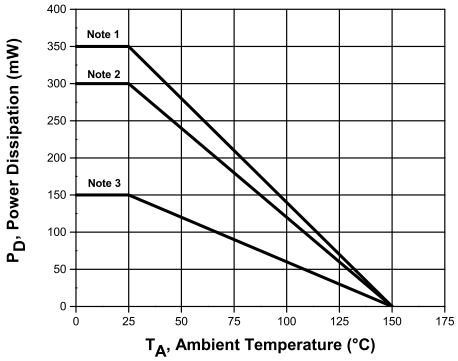
Capacitance



Transfer Characteristics



Power Derating



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SURFACE MOUNT SILICON DUAL P-CHANNEL ENHANCEMENT-MODE MOSFET

SERVICES

- Bonded Inventory
- Custom Electrical Screening
- Custom Electrical Characteristic Curves
- SPICE Models
- Custom Packaging
- Package Base Options
- Custom Device Development / Multi Discrete Modules (MDM™)
- Bare Die Available for Hybrid Applications

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