# SY88149HAL

## 1.25Gbps Burst-Mode Limiting Amplifier with Ultra-Fast Signal Assert Timing

## General Description

The SY88149HAL is a high-sensitivity, burst-mode capable, limiting-post amplifier designed for FTTH PON optical line terminal (OLT) receiver applications. The SY88149HAL satisfies the strict timing restrictions of the GPON standards by providing ultra-fast loss-of-signal (LOS) or signal-detect (SD) output. Auto reset and manual reset options are provided to control LOS/SD output timing. The device can be connected to burst-mode capable transimpedance amplifiers (TIAs) using AC or DC coupling.

The SY88149HAL generates a high-gain LVTTL LOS or SD output. A programmable LOS/SD level set pin ($LOS/SD_{LVL}$) sets the sensitivity of the input amplitude detection. For increased flexibility, this device also includes an option to select between LOS or SD output by using the LOS/SD SEL pin. The LOS/SD output can be fed back to the JAM input to maintain data output stability under an invalid input signal conditions. Typically, 3dB LOS/SD hysteresis is provided to prevent chattering.

The SY88149HAL operates from a single +3.3V power supply, over temperatures ranging from –40°C to +85°C. With its wide bandwidth and high gain, signals up to 1.25Gbps and as small as 5mVpp can be amplified to LVPECL levels.

All support documentation can be found on Micrel's web site at: www.micrel.com.

## Features

- <5ns SD Assert (LOS Deassert) time
- Option to AUTO RESET or manual RESET LOS/SD output
- Selectable LOS/SD output option
- High-sensitivity LOS/SD signal detect
- Low-noise LVPECL data outputs
- Squelching function to maintain output stability
- Programmable LOS/SD level set ($LOS/SD_{LVL}$)
- 5mVpp input sensitivity
- 1.25Gbps operation
- Single 3.3V power supply
- Available in a 16-pin (3mm × 3mm) QFN® package

## Applications

- GE-PON/GPON
- Gigabit Ethernet
- Fibre Channel
- OC-3/12/24 SONET/SDH
- High-gain line driver and line receiver
- Low-gain TIA interface

## Markets

- FTTH PON
- Datacom/Telecom
- Optical transceiver

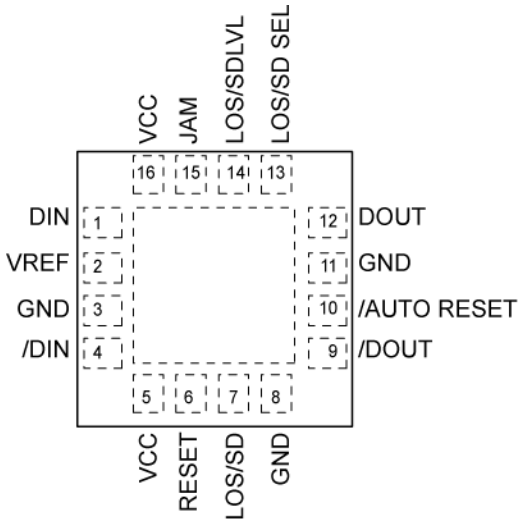
## Ordering Information

| Part Number | Package Type | Operating Range | Package Marking |
|---|---|---|---|
| SY88149HALMG | Lead-Free QFN-16 | Industrial | 149A with Pb-Free Bar-Line Indicator |
| SY88149HALMG TR[1] | Lead-Free QFN-16 | Industrial | 149A with Pb-Free Bar-Line Indicator |

**Notes:**

1. Tape and Reel.

## Pin Configuration




**16-Pin QFN® (QFN-16)**

## Pin Description

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 1, 4 | DIN, /DIN | Differential Data Inputs. If AC-coupled, terminate each pin to $V_{REF}$ with 50Ω. |
| 2 | VREF | Reference Voltage Output. Typically $V_{CC}$ – 1.3V. |
| 3, 11, 8 | GND | Device Ground. Exposed pad must be soldered (or equivalent) to the same potential as the ground pins. |
| 10 | /AUTO RESET | LVTTL Input. This pin is internally connected to a 25kΩ pull-up resistor and defaults to HIGH. When this pin is LOW or tied to ground, the /AUTO RESET function is enabled and SD deasserts or LOS asserts within 120ns (typical) after the last high-to-low transition of the burst input. When this pin is left floating or tied high, the AUTO RESET function is disabled and the SD deassert or LOS assert must be forced by using the manual RESET function. |
| 5, 16 | VCC | Positive power supply. Bypass with 0.1uF \| \| 0.01uF low ESR capacitors. 0.01uF capacitors should be as close as possible to VCC pins. |
| 6 | RESET | LVTTL Input. Apply a high-level signal (>2V) to this pin to reset the SD deassert time or LOS assert within 5ns. RESET defaults to LOW if left floating. If the /AUTO RESET function is not used, this RESET function needs to be used to quickly deassert the SD or assert LOS. This pin is internally connected to a 25kΩ pull-down resistor and defaults to LOW. |

## Pin Description (Continued)

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 7 | LOS/SD | LVTTL Output. Signal detect (SD) asserts high when the data input amplitude rises above the threshold sets by $SD_{LVL}$. Conversely, loss-of-signal (LOS) deasserts low when the data input amplitude rises above the threshold set by $LOS_{LVL}$. |
| 12, 9 | DOUT, /DOUT | LVPECL Outputs. When JAM disables the device, output DOUT is forced to logic LOW and output /DOUT is forced to logic HIGH. |
| 13 | LOS/SD SEL | Allows the user to select between whether LOS or SD is outputted on the LOS/SD pin. Also controls the polarity of the JAM input. When SD is selected, JAM is active HIGH and LOS/SD (Pin 7) operates as signal detect. Conversely, when LOS is selected, JAM is active LOW and LOS/SD operates as loss-of-signal. This pin is internally connected to a 25kΩ pull-up resistor and defaults to HIGH (SD output selected). |
| 14 | LOS/SDLVL | Voltage Input. Sets the LOS/SD level. A resistor from this pin to $V_{CC}$ sets the threshold for the data input amplitude at which LOS/SD will be asserted. |
| 15 | JAM | LVTTL Input. This JAM input acts as a squelch function and switches its polarity depending on LOS/SD SEL status. When LOS is selected, this pin is active LOW. When SD is selected, this pin is Active HIGH. To create a squelch function, connect JAM to LOS/SD. When JAM disables the device, output Q is forced to logic LOW and output /Q is forced to logic HIGH. Note that this input is internally connected to a 25kΩ pull-up resistor. |

## Absolute Maximum Ratings[1]

Supply Voltage ($V_{CC}$) ..... 0V to +4.0V
Input Voltage (DIN, /DIN) ..... 0 to $V_{CC}$
Output Current ($I_{OUT}$)
  Continuous ..... ±50mA
  Surge ..... ±100mA
EN Voltage ..... 0 to $V_{CC}$
$V_{REF}$ Current ..... -800µA to +500µA
$SD_{LVL}$ Voltage ..... $V_{REF}$ to $V_{CC}$
Lead Temperature (soldering, 20s) ..... 260°C
Storage Temperature ($T_s$) ..... –65°C to +150°C

## Operating Ratings[2]

Supply Voltage ($V_{CC}$) ..... +3.0V to +3.6V
Ambient Temperature ($T_A$) ..... –40°C to +85°C
Junction Temperature ($T_J$) ..... –40°C to +125°C
Junction Thermal Resistance[3]
  QFN® ($\theta_{JA}$) Still-Air ..... 60°C/W
  QFN® ($\Psi_{JB}$) Junction-to-Board ..... 38°C/W

## DC Electrical Characteristics

$V_{CC}$ = 3.0 to 3.6V; $T_A$ = –40°C to +85°C, typical values at $V_{CC}$ = 3.3V, $T_A$ = 25°C.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Power Supply Current | No output load | | 58 | 80 | mA |
| $LOS/SD_{LVL}$ | $LOS/SD_{LVL}$ Voltage | | $V_{REF}$ | | $V_{CC}$ | V |
| $V_{OH}$ | LVPECL Output HIGH Voltage | 50Ω to $V_{CC}$ – 2V | $V_{CC}$ – 1.085 | $V_{CC}$ – 0.955 | $V_{CC}$ – 0.880 | V |
| $V_{OL}$ | LVPECL Output LOW Voltage | 50Ω to $V_{CC}$ – 2V | $V_{CC}$ – 1.830 | $V_{CC}$ – 1.705 | $V_{CC}$ – 1.555 | V |
| $I_{OFFSET}$ | Input Offset Voltage | | | | 1 | mV |
| $V_{IHCMR}$ | Common Mode Range | Note 4 | GND + 1.4 | | $V_{CC}$ | V |
| $V_{REF}$ | Reference Voltage | | $V_{CC}$ – 1.48 | $V_{CC}$ – 1.32 | $V_{CC}$ – 1.16 | V |
| $I_{DIN}$ | Input Sink Current (DIN & /DIN) | No Input Load | | | 6 | uA |

## LVTTL DC Electrical Characteristics

$V_{CC}$ = 3.0 to 3.6V; $T_A$ = –40°C to +85°C, typical values at $V_{CC}$ = 3.3V, $T_A$ = 25°C.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | LVTTL Input HIGH Voltage | | 2.0 | | | V |
| $V_{IL}$ | LVTTL Input LOW Voltage | | | | 0.8 | V |
| $I_{IH\_JAM}$ | JAM Input HIGH Current | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = 2.7V | | | 20<br>20 | µA |
| $I_{IL\_JAM}$ | JAM Input LOW Current | $V_{IN}$ = 0.5V | –0.3 | | | mA |
| $I_{IH\_AR}$ | /AUTORESET Input HIGH Current | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = 2.7V | | | 100<br>20 | µA |
| $I_{IL\_AR}$ | /AUTORESET Input LOW Current | $V_{IN}$ = 0.5V | –0.3 | | | mA |

**Notes:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Thermal performance assumes the use of a 4-layer PCB. Exposed pad must be soldered to the device's most negative potential on the PCB.
4. VIHCMR is defined as common mode range of the VIH level on DIN and /DIN. It is the most positive level of the differential signal.

## LVTTL DC Electrical Characteristics (Continued)

$V_{CC}$ = 3.0 to 3.6V; $T_A$ = –40°C to +85°C, typical values at $V_{CC}$ = 3.3V, $T_A$ = 25°C.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IH\_RESET}$ | RESET Input HIGH Current | $V_{IN} = V_{CC}$<br>$V_{IN}$ = 2.7V | | | 300<br>250 | µA |
| $I_{IL\_RESET}$ | RESET Input LOW Current | $V_{IN}$ = 0.5V | 0 | | | mA |
| $V_{OH}$ | SD/LOS Output HIGH Level | $I_{OH}$ = –100uA | 2.1 | 2.7 | | V |
| $V_{OL}$ | SD/LOS Output LOW Level | $I_{OL}$ = 100uA | | 0.35 | 0.5 | V |

## AC Electrical Characteristics

$V_{CC}$ = 3.0V to 3.6V; $R_{LOAD}$ = 50Ω to $V_{CC}$ – 2V; $T_A$ = –40°C to +85°C.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | Output Rise/Fall Time (20% to 80%) | Note 5 | | | 260 | ps |
| $t_{JAM}$ | JAM Enable/Disable Time | | | | 2 | ns |
| $t_{AUTORESET}$ | SD Deassert or LOS Assert with Auto Reset Enabled. | | 100 | 120 | 150 | ns |
| $t_{RESET}$ | RESET time constant | Note 6 | | | 5 | ns |
| $t_{ON}$ | SD Assert Time/LOS Deassert time | | | | 5 | ns |
| $t_{JITTER}$ | Deterministic<br>Random | Note 7<br>Note 8 | | 15<br>5 | | $ps_{PP}$<br>$ps_{RMS}$ |
| $V_{ID}$ | Differential Input Voltage Swing | Figure 1 | 5 | | 1800 | $mV_{PP}$ |
| $V_{OD}$ | Differential Output Voltage Swing | $V_{ID} \geq 18mV_{PP}$ | | 1500 | | $mV_{PP}$ |
| $SD_{AL}$ /$LOS_{DL}$ | Low SD Assert/LOS De- Assert Level | $R_{LOS/SDLVL}$ = 10kΩ, Note 9, 10 | | 4 | | $mV_{PP}$ |
| $SD_{DL}$/$LOS_{AL}$ | Low SD Deassert /LOS Assert Level | $R_{LOS/SDLVL}$ = 10kΩ, Note 10 | | 3 | | $mV_{PP}$ |
| $HYS_L$ | Low SD/LOS Hysteresis | $R_{LOS/SDLVL}$ = 10kΩ, Note 11 | | 2.5 | | dB |
| $SD_{AM}$/$LOS_{DM}$ | Medium SD Assert/LOS Deassert Level | $R_{LOS/SDLVL}$ = 5kΩ, Note 10 | | 4.76 | | $mV_{PP}$ |
| $SD_{DM}$/$LOS_{AM}$ | Medium SD Deassert /LOS Assert Level | $R_{LOS/SDLVL}$ = 5kΩ, Note 10 | | 3.6 | | $mV_{PP}$ |
| $HYS_M$ | Medium SD/LOS Hysteresis | $R_{LOS/SDLVL}$ = 5kΩ, Note 11 | 2 | 3 | 4 | dB |
| $SD_{AH}$/$LOS_{DH}$ | High SD Assert/LOS De- Assert Level | $R_{LOS/SDLVL}$ = 50Ω, Note 10 | | 18 | | $mV_{PP}$ |
| $SD_{DH}$/$LOS_{AH}$ | High SD Deassert/ LOS Assert Level | $R_{LOS/SDLVL}$ = 50Ω, Note 10 | | 12.5 | | $mV_{PP}$ |
| $HYS_H$ | High SD/LOS Hysteresis | $R_{LOS/SDLVL}$ = 50Ω, Note 11 | 2 | 3 | 4 | dB |
| $B_{-3dB}$ | 3dB Bandwidth | | | 750 | | MHz |
| $A_{V(Diff)}$ | Differential Voltage Gain | | | 48 | | dB |
| $S_{21}$ | Single-Ended Small-Signal Gain | | | 42 | | dB |

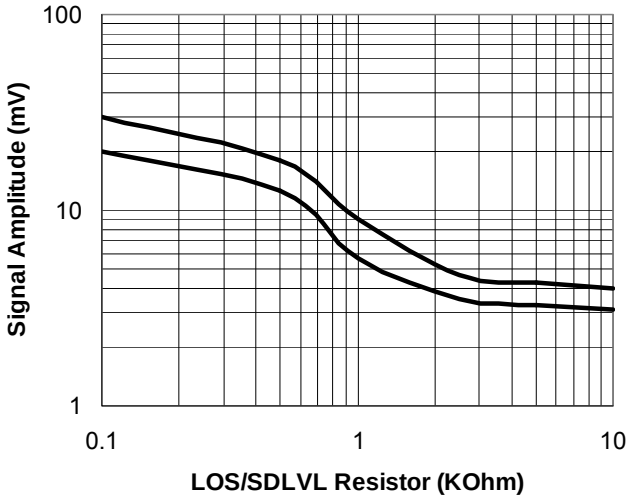
**Notes:**

5. Amplifier in limiting mode. Input is a 200MHz square wave.
6. The time between applying RESET and outputs being disabled.
7. Deterministic jitter measured using 1.25Gbps K28.7 pattern, $V_{ID}$ = 10$mV_{PP}$.
8. Random jitter measured using 1.25Gbps K28.7 pattern, $V_{ID}$ = 10$mV_{PP}$.
9. SD is the opposite polarity of LOS. Therefore, an SD Assert parameter is equivalent to a LOS deassert parameter and vice versa.
10. See “Typical Operating Characteristics” for a graph showing how to choose a particular $R_{LOS/SDLVL}$ for a particular assert and its associated deassert amplitude.
11. This specification defines electrical hysteresis as 20log(SD assert/SD deassert). The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2 depending upon the level of received optical power and ROSA characteristics. Based upon that ratio, the optical hysteresis corresponding to the electrical hysteresis range 3dB – 6dB, shown in the AC Characteristics table, will be 1.5dB-4dB optical hysteresis.

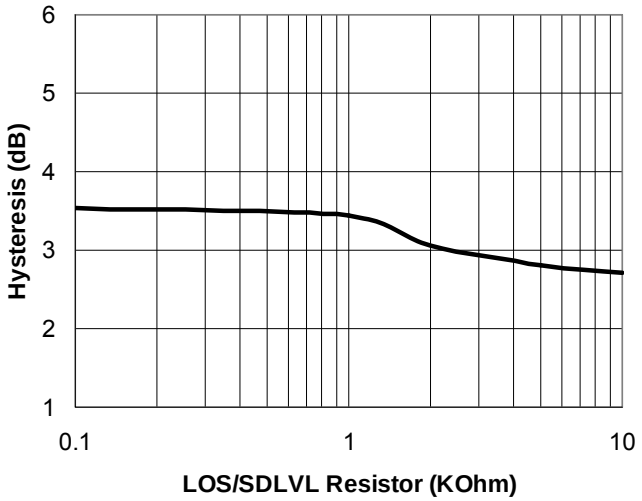
## Typical Operating Characteristics

$V_{CC}$ = 3.3V, $T_A$ = 25°C, $R_L$ = 50Ω to $V_{CC}$ – 2V, unless otherwise stated.

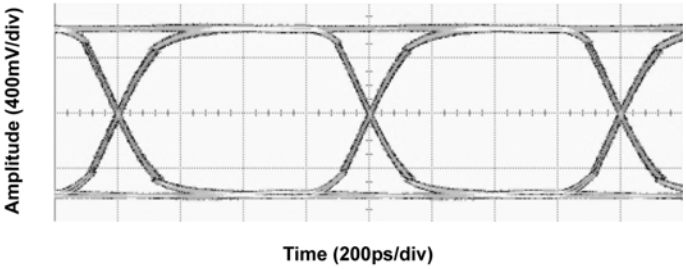
**LOS Assert/De-Assert Levels**



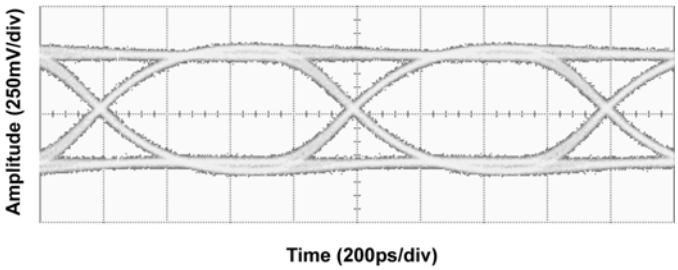

**LOS/SD Hysteresis**



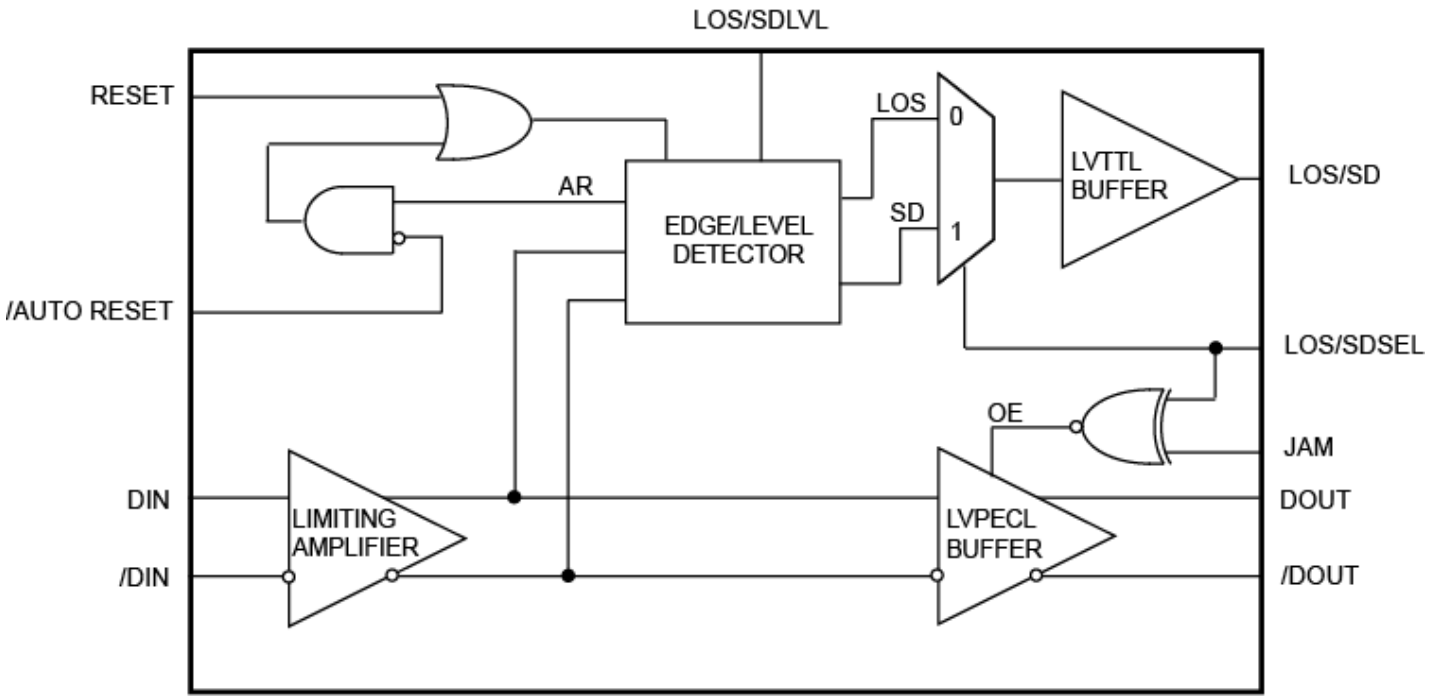

**PRBS-23 500mVpp Input @ 1.25Gbps**




**PRBS-23 7.5mVpp Input @ 1.25Gbps**



## Functional Block Diagram



## Detailed Description

The SY88149HAL is a high-sensitivity limiting post amplifier which operates on a +3.3V power supply over the industrial temperature range. Signals with data rates up to 1.25Gbps and as small as 5mVpp can be amplified. Depending on the LOS/SD SEL option, the SY88149HAL can generate an SD or LOS output, and allow feedback to the JAM input for output stability. $LOS/SD_{LVL}$ sets the sensitivity of the input amplitude detection.

To satisfy the stringent timing requirements of the GPON specifications, the signal detect circuit offers 5ns SD assert (LOS deassert) time and the option to deassert SD (assert LOS) using the /AUTO RESET or manual RESET function. When /AUTO RESET is enabled, SD deasserts/LOS asserts automatically within 120ns after the last high-to-low transition of the input burst. When the /AUTORESET function is disabled, the SD deassert/LOS assert time can be reset by using the provided RESET pin.

### Input Buffer

Figure 2 shows a simplified schematic of the input stage. The high sensitivity of the input amplifier allows signals as small as 5mVpp to be detected and amplified. The input buffer can allow input signals as large as $1800mV_{PP}$. Input signals are linearly amplified with a typically 48dB differential voltage gain until the outputs reach $1500mV_{PP}$ (typical). Applications requiring the SY88149HAL to operate with high-gain should have the upstream TIA placed as close as possible to the SY88149HAL's input pins. This ensures the best performance of the device.

### Output Buffer

The SY88149HAL's LVPECL output buffer is designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor to $V_{CC}$ – 2V for each output pin provides this. Figure 3 shows a simplified schematic of the output stage.

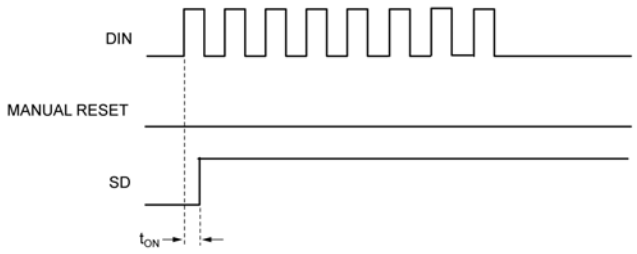
### Loss of Signal/Signal Detect

The SY88149HAL generates a chatter-free Signal-Detect (SD) or LOS LVTTL output, as shown in Figure 4. A highly-sensitive signal detect circuit is used to determine that the input amplitude is too small to be considered a valid input. LOS asserts high if the input amplitude falls below the threshold sets by LOS/SDLVL and deasserts low otherwise. SD asserts high if the input amplitude rises above threshold set by LOS/SDLVL and deasserts low otherwise. LOS/SD can be fed back to the JAM input to maintain output stability under the absence of an invalid signal condition. Typically, a 3dB hysteresis is provided to prevent chattering.

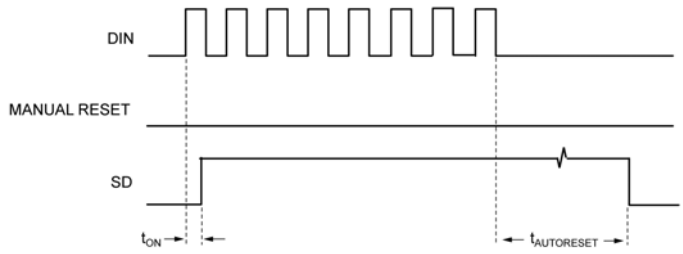
### LOS/SD Level Set

A programmable LOS/SD level pin ($LOS/SD_{LVL}$) sets the threshold of the input amplitude detection. Connecting an external resistor between $V_{CC}$ and $LOS/SD_{LVL}$ sets the voltage at $LOS/SD_{LVL}$. This voltage ranges from $V_{CC}$ to $V_{REF}$. The external resistor creates a voltage divider between $V_{CC}$ and $V_{REF}$, as shown in Figure 5. Set the $LOS/SD_{LVL}$ voltage closer to $V_{REF}$ or more sensitive LOS/SD detection or closer to $V_{CC}$ for higher inputs.

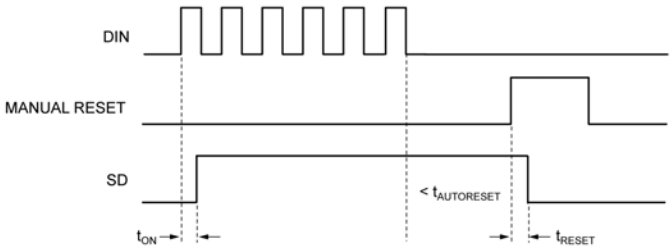
## Timing Diagrams




**No Manual RESET and /AUTORESET Tied HIGH**




**No Manual RESET and /AUTORESET Tied LOW**




**Manual RESET and /AUTORESET Tied HIGH or LOW**

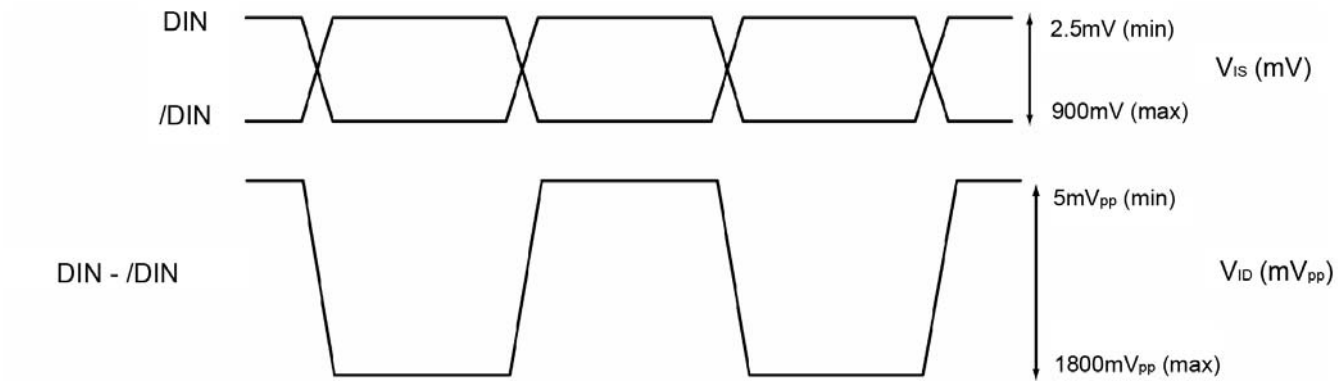



**Figure 1. VIS and VID Definition**

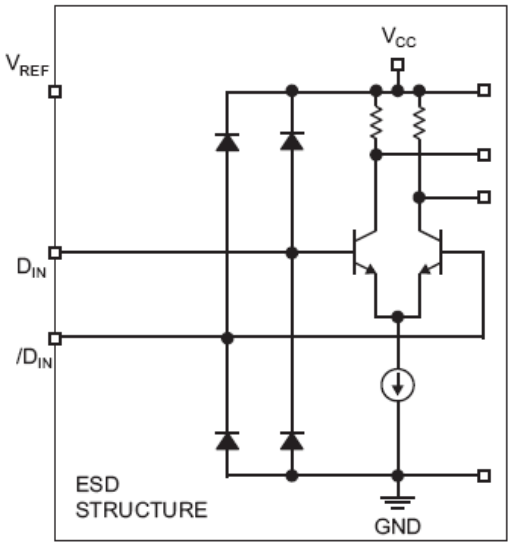



**Figure 2. Input Structure**

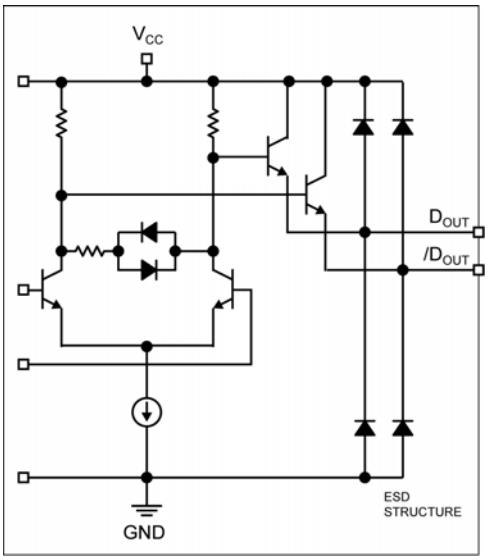



**Figure 3. Output Structure**

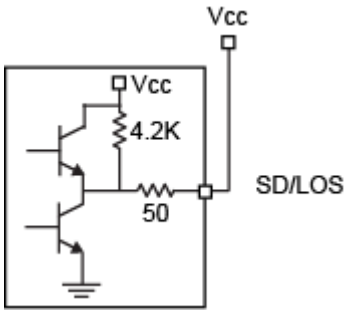



**Figure 4. SD Output Structure**

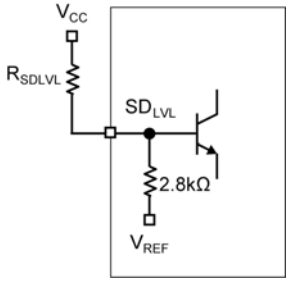
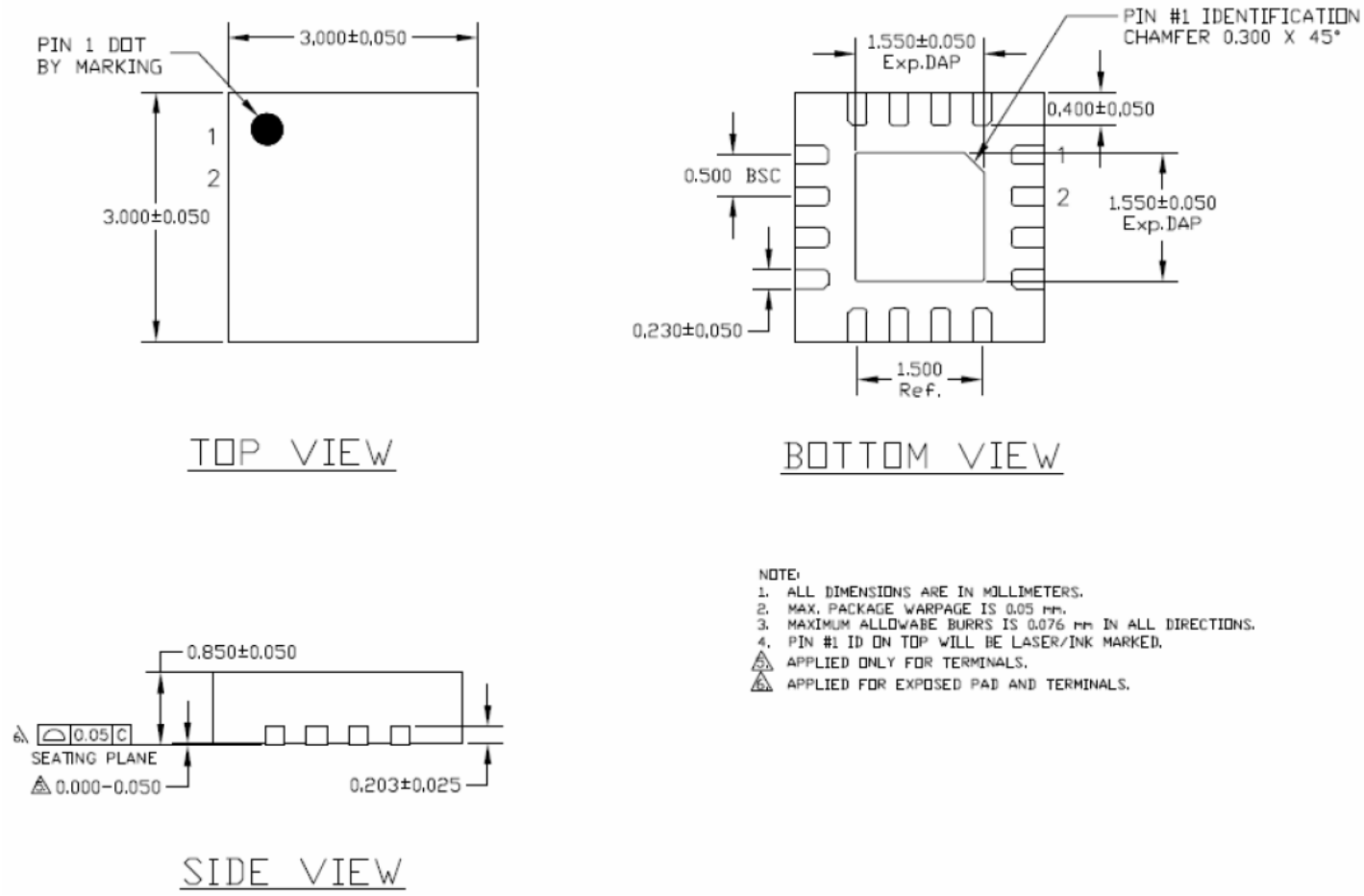



**Figure 5. LOS/$SD_{LVL}$ Setting Circuit**

## Package Information




**16-Pin QFN® (QFN-16)**

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