

PBSS4032SPN

30 V NPN/PNP low V_{CEsat} (BISS) transistor Rev. 2 — 14 October 2010

Product data sheet

1. **Product profile**

1.1 General description

NPN/PNP low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a SOT96-1 (SO8) medium power Surface-Mounted Device (SMD) plastic package.

Table 1. **Product overview**

Type number	Package I		NPN/NPN	PNP/PNP
	Nexperia	Name	complement	complement
PBSS4032SPN	SOT96-1	SO8	PBSS4032SN	PBSS4032SP

1.2 Features and benefits

- Low collector-emitter saturation voltage V_{CEsat}
- Optimized switching time
- High collector current capability I_C and I_{CM}
- High collector current gain (h_{FE}) at high I_C
- High efficiency due to less heat generation
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

1.3 Applications

- DC-to-DC conversion
- Battery-driven devices
- Power management
- Charging circuits

1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
TR1; NP	N low V _{CEsat} transistor					
V_{CEO}	collector-emitter voltage	open base	-	-	30	V
I _C	collector current		-	-	5.7	Α
I _{CM}	peak collector current	single pulse; $t_p \le 1$ ms	-	-	10	Α
R _{CEsat}	collector-emitter saturation resistance	$I_C = 4 \text{ A}; I_B = 0.4 \text{ A}$	<u>[1]</u> -	45	62.5	mΩ



Table 2. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
TR2; PN	P low V _{CEsat} transistor					
V_{CEO}	collector-emitter voltage	open base	-	-	-30	V
I _C	collector current		-	-	-4.8	Α
I_{CM}	peak collector current	single pulse; $t_p \le 1 \text{ ms}$	-	-	-10	Α
R _{CEsat}	collector-emitter saturation resistance	$I_C = -4 \text{ A}; I_B = -0.4 \text{ A}$	<u>[1]</u> -	65	98	mΩ

^[1] Pulse test: $t_p \le 300~\mu s;~\delta \le 0.02.$

2. Pinning information

Table 3. Pinning

	3		
Pin	Description	Simplified outline	Graphic symbol
1	emitter TR1		
2	base TR1	8 <u>7</u> <u>7</u> <u>7</u> <u>7</u> 5	8 7 6 5
3	emitter TR2		TR1 L TR2 L
4	base TR2		
5	collector TR2	1 1 1 1 4	1 2 3 4
6	collector TR2		006aaa985
7	collector TR1		
8	collector TR1		

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PBSS4032SPN	SO8	plastic small outline package; 8 leads; body width 3.9 mm $$	SOT96-1

4. Marking

Table 5. Marking codes

Type number	Marking code
PBSS4032SPN	4032SPN

5. Limiting values

Table 6. Limiting values

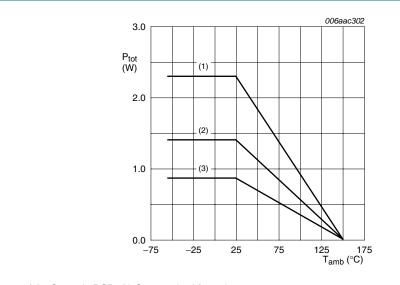
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
TR1 (NPN)					
I _C	collector current		-	5.7	Α
TR2 (PNP)					
I _C	collector current		-	-4.8	Α
Per transist	or; for the PNP transistor	with negative polarity			
V_{CBO}	collector-base voltage	open emitter	-	30	V
V_{CEO}	collector-emitter voltage	open base	-	30	V
V_{EBO}	emitter-base voltage	open collector	-	5	V
I _{CM}	peak collector current	single pulse; $t_p \le 1 \text{ ms}$	-	10	Α
I _B	base current		-	1	Α
P_{tot}	total power dissipation	$T_{amb} \le 25 ^{\circ}C$	[1] -	0.73	W
			[2] -	1	W
			[3] _	1.7	W
Per device					
P_{tot}	total power dissipation	$T_{amb} \le 25 ^{\circ}C$	[1] -	0.86	W
			[2] -	1.4	W
			[3] -	2.3	W
T _j	junction temperature		-	150	°C
T _{amb}	ambient temperature		-55	+150	°C
T_{stg}	storage temperature		-65	+150	°C

^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

^[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².

^[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



- (1) Ceramic PCB, Al₂O₃, standard footprint
- (2) FR4 PCB, mounting pad for collector 1 cm²
- (3) FR4 PCB, standard footprint

Fig 1. Per device: Power derating curves

6. Thermal characteristics

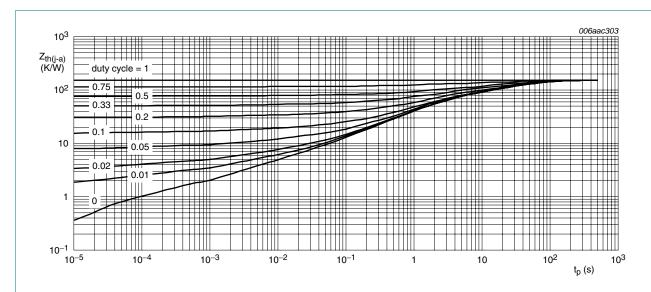
Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per trans	istor					
R _{th(j-a)}	thermal resistance from	in free air	<u>[1]</u> -	-	170	K/W
	junction to ambient		[2]	-	125	K/W
			[3]	-	75	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	40	K/W
Per devic	e					
R _{th(j-a)}	thermal resistance from	in free air	<u>[1]</u> -	-	145	K/W
	junction to ambient		[2]	-	90	K/W
			[3]	-	55	K/W

^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

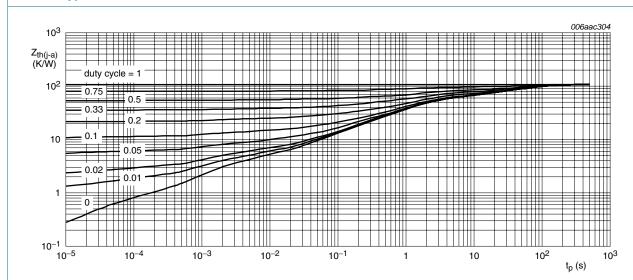
^[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².

^[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



FR4 PCB, standard footprint

Fig 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for collector 1 cm²

Fig 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

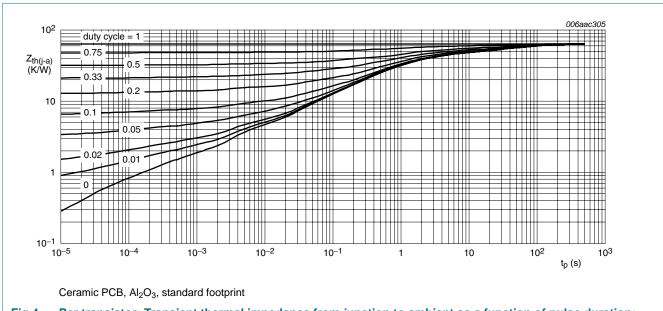


Fig 4. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 8. Characteristics

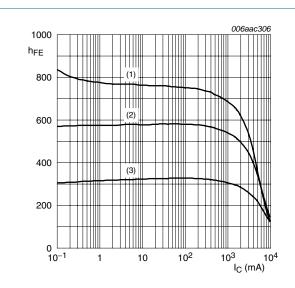
 $T_{amb} = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
TR1; NP	N Iow V _{CEsat} transisto	r					
I _{CBO}	collector-base	$V_{CB} = 30 \text{ V}; I_E = 0 \text{ A}$		-	-	100	nA
	cut-off current	$V_{CB} = 30 \text{ V}; I_E = 0 \text{ A};$ $T_j = 150 \text{ °C}$		-	-	50	μΑ
I _{CES}	collector-emitter cut-off current	$V_{CE} = 24 \text{ V}; V_{BE} = 0 \text{ V}$		-	-	100	nA
I _{EBO}	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_{C} = 0 \text{ A}$		-	-	100	nA
h _{FE}	DC current gain	V _{CE} = 2 V	[1]				
		I _C = 500 mA		300	500	-	
		I _C = 1 A		300	500	-	
		I _C = 2 A		250	450	-	
		I _C = 4 A		200	400	-	
		I _C = 6 A		150	300	-	
V_{CEsat}	collector-emitter		[1]				
	saturation voltage	I _C = 1 A; I _B = 50 mA		-	90	125	mV
		I _C = 1 A; I _B = 10 mA		-	130	180	mV
		I _C = 2 A; I _B = 40 mA		-	150	210	mV
		I _C = 4 A; I _B = 400 mA		-	185	250	mV
		I _C = 4 A; I _B = 40 mA		-	250	375	mV
		I _C = 6 A; I _B = 300 mA		-	300	450	mV
R _{CEsat}	collector-emitter saturation resistance	$I_C = 4 \text{ A}; I_B = 400 \text{ mA}$	[1]	-	45	62.5	mΩ
V_{BEsat}	base-emitter		[1]				
	saturation voltage	I _C = 1 A; I _B = 100 mA		-	0.76	0.9	V
		I _C = 4 A; I _B = 400 mA		-	0.91	1.05	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = 2 \text{ V}; I_{C} = 2 \text{ A}$	[1]	-	0.77	0.85	V
t _d	delay time	$V_{CC} = 12.5 \text{ V}; I_C = 1 \text{ A};$		-	35	-	ns
t _r	rise time	$I_{Bon} = 0.05 \text{ A}; I_{Boff} = -0.05 \text{ A}$		-	30	-	ns
t _{on}	turn-on time			-	65	-	ns
ts	storage time			-	150	-	ns
t _f	fall time			-	65	-	ns
t _{off}	turn-off time			-	215	-	ns
f _T	transition frequency	$V_{CE} = 10 \text{ V}; I_{C} = 100 \text{ mA};$ f = 100 MHz		-	140	-	MHz
C _c	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = i_e = 0 \text{ A};$ f = 1 MHz		-	65	-	pF

Table 8. Characteristics ...continued $T_{amb} = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
TR2; PN	P low V _{CEsat} transisto	r					
I _{CBO}	collector-base	$V_{CB} = -30 \text{ V}; I_E = 0 \text{ A}$		-	-	-100	nΑ
	cut-off current	$V_{CB} = -30 \text{ V}; I_E = 0 \text{ A};$ $T_j = 150 \text{ °C}$		-	-	-50	μΑ
I _{CES}	collector-emitter cut-off current	$V_{CE} = -24 \text{ V}; V_{BE} = 0 \text{ V}$		-	-	-100	nA
I _{EBO}	emitter-base cut-off current	$V_{EB} = -5 \text{ V}; I_C = 0 \text{ A}$		-	-	-100	nA
h _{FE}	DC current gain	V _{CE} = −2 V	[1]				
		$I_C = -500 \text{ mA}$		200	380	-	
		I _C = -1 A		200	330	-	
		I _C = −2 A		150	250	-	
		I _C = -4 A		60	100	-	
		I _C = −5 A		40	60	-	
V _{CEsat}	collector-emitter		[1]				
	saturation voltage	$I_C = -1 \text{ A}; I_B = -50 \text{ mA}$		-	-115	-165	mV
		$I_C = -1 \text{ A}; I_B = -10 \text{ mA}$		-	-170	-240	mV
		$I_C = -2 \text{ A}; I_B = -40 \text{ mA}$		-	-210	-300	mV
		$I_C = -4 \text{ A}; I_B = -400 \text{ mA}$		-	-260	-390	mV
		$I_C = -4 \text{ A}; I_B = -200 \text{ mA}$		-	-300	-450	mV
		$I_C = -5 \text{ A}; I_B = -250 \text{ mA}$		-	-340	-510	mV
R _{CEsat}	collector-emitter saturation resistance	$I_C = -4 \text{ A}; I_B = -400 \text{ mA}$	[1]	-	65	98	mΩ
V _{BEsat}	base-emitter		[1]				
	saturation voltage	$I_C = -1 \text{ A}; I_B = -100 \text{ mA}$		-	-0.8	-0.9	V
		$I_C = -4 \text{ A}; I_B = -400 \text{ mA}$		-	-0.99	-1.1	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -2 \text{ V}; I_{C} = -2 \text{ A}$	[1]	-	-0.81	-0.9	V
t _d	delay time	$V_{CC} = -12.5 \text{ V}; I_C = -1 \text{ A};$		-	30	-	ns
t _r	rise time	$I_{Bon} = -0.05 \text{ A}; I_{Boff} = 0.05 \text{ A}$		-	60	-	ns
t _{on}	turn-on time			-	90	-	ns
t _s	storage time			-	140	-	ns
t _f	fall time			-	80	-	ns
t _{off}	turn-off time			-	220	-	ns
f _T	transition frequency	$V_{CE} = -10 \text{ V}; I_{C} = -100 \text{ mA};$ f = 100 MHz		-	115	-	MHz
C _c	collector capacitance	$V_{CB} = -10 \text{ V}; I_E = i_e = 0 \text{ A};$ f = 1 MHz		-	85	-	pF

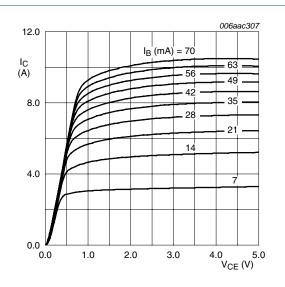
^[1] Pulse test: $t_p \le 300~\mu s;~\delta \le 0.02.$



$$V_{CE} = 2 V$$

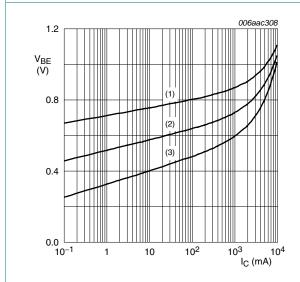
- (1) $T_{amb} = 100 \, ^{\circ}C$
- (2) $T_{amb} = 25 \, ^{\circ}C$
- (3) $T_{amb} = -55 \, ^{\circ}C$

Fig 5. TR1 (NPN): DC current gain as a function of collector current; typical values



 $T_{amb} = 25 \, ^{\circ}C$

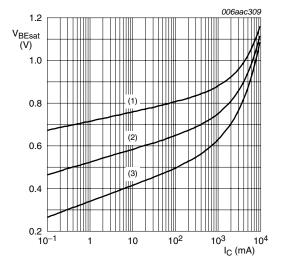
Fig 6. TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values





- (1) $T_{amb} = -55 \,^{\circ}C$
- (2) $T_{amb} = 25 \, ^{\circ}C$
- (3) $T_{amb} = 100 \, ^{\circ}C$

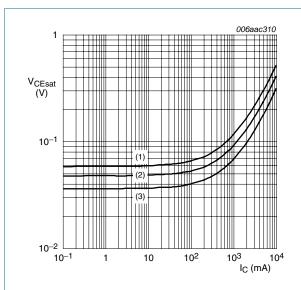
Fig 7. TR1 (NPN): Base-emitter voltage as a function of collector current; typical values



 $I_{\rm C}/I_{\rm B} = 20$

- (1) $T_{amb} = -55 \,^{\circ}C$
- (2) $T_{amb} = 25 \, ^{\circ}C$
- (3) $T_{amb} = 100 \, ^{\circ}C$

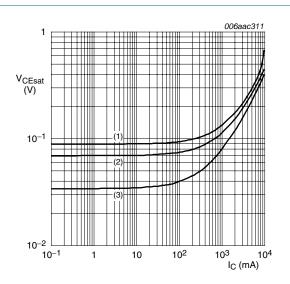
Fig 8. TR1 (NPN): Base-emitter saturation voltage as a function of collector current; typical values



$$I_{\rm C}/I_{\rm B} = 20$$

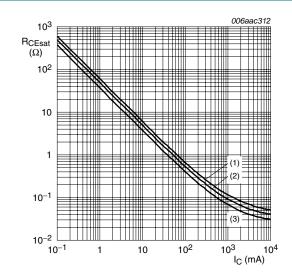
- (1) $T_{amb} = 100 \, ^{\circ}C$
- (2) $T_{amb} = 25 \, ^{\circ}C$
- (3) $T_{amb} = -55 \, ^{\circ}C$

Fig 9. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



- (1) $I_C/I_B = 100$
- (2) $I_C/I_B = 50$
- (3) $I_C/I_B = 10$

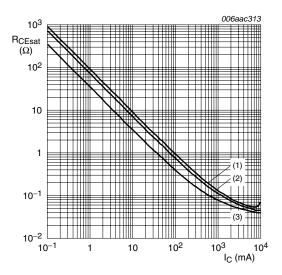
Fig 10. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values





- (1) $T_{amb} = 100 \, ^{\circ}C$
- (2) $T_{amb} = 25 \,^{\circ}C$
- (3) $T_{amb} = -55 \, ^{\circ}C$

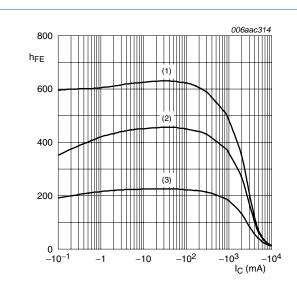
Fig 11. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values



$$T_{amb} = 25 \, ^{\circ}C$$

- (1) $I_C/I_B = 100$
- (2) $I_C/I_B = 50$
- (3) $I_C/I_B = 10$

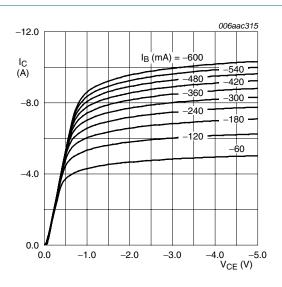
Fig 12. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values



$$V_{CE} = -2 V$$

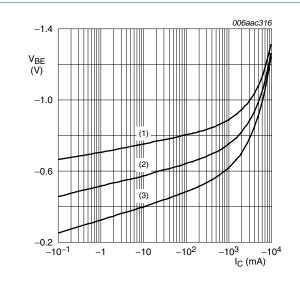
- (1) $T_{amb} = 100 \, ^{\circ}C$
- (2) $T_{amb} = 25 \, ^{\circ}C$
- (3) $T_{amb} = -55 \, ^{\circ}C$

Fig 13. TR2 (PNP): DC current gain as a function of collector current; typical values



 $T_{amb} = 25 \, ^{\circ}C$

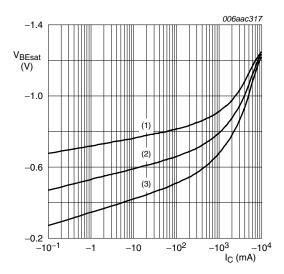
Fig 14. TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values





- (1) $T_{amb} = -55 \,^{\circ}C$
- (2) $T_{amb} = 25 \, ^{\circ}C$
- (3) $T_{amb} = 100 \, ^{\circ}C$

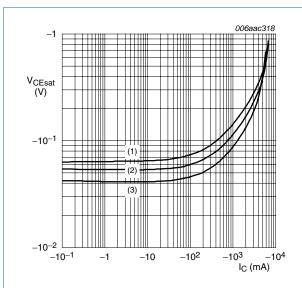
Fig 15. TR2 (PNP): Base-emitter voltage as a function of collector current; typical values



 $I_{\rm C}/I_{\rm B} = 20$

- (1) $T_{amb} = -55 \,^{\circ}C$
- (2) $T_{amb} = 25 \, ^{\circ}C$
- (3) $T_{amb} = 100 \, ^{\circ}C$

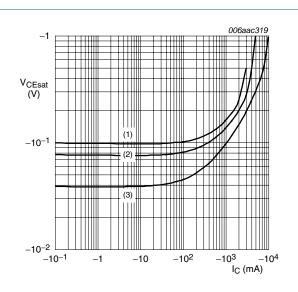
Fig 16. TR2 (PNP): Base-emitter saturation voltage as a function of collector current; typical values



$$I_{\rm C}/I_{\rm B} = 20$$

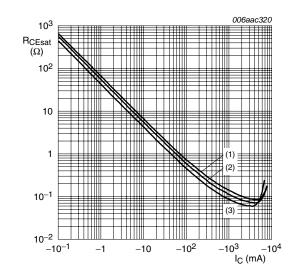
- (1) $T_{amb} = 100 \, ^{\circ}C$
- (2) $T_{amb} = 25 \,^{\circ}C$
- (3) $T_{amb} = -55 \,^{\circ}C$

Fig 17. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



- (1) $I_C/I_B = 100$
- (2) $I_C/I_B = 50$
- (3) $I_C/I_B = 10$

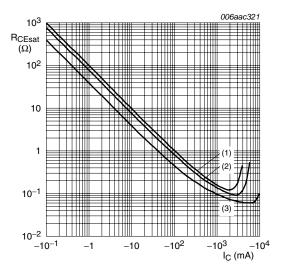
Fig 18. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values





- (1) $T_{amb} = 100 \, ^{\circ}C$
- (2) $T_{amb} = 25 \,^{\circ}C$
- (3) $T_{amb} = -55 \, ^{\circ}C$

Fig 19. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



$$T_{amb} = 25 \, ^{\circ}C$$

- (1) $I_C/I_B = 100$
- (2) $I_C/I_B = 50$
- (3) $I_C/I_B = 10$

Fig 20. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

8. Test information

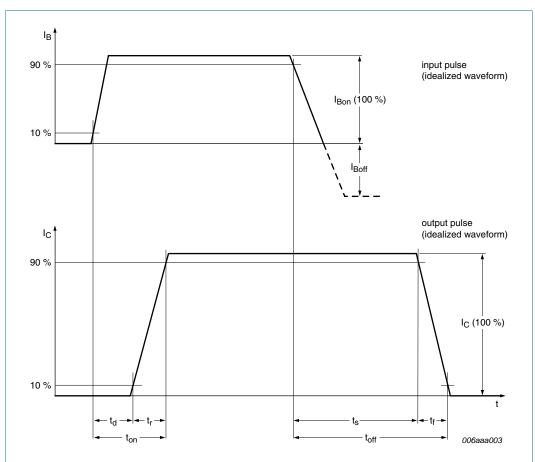


Fig 21. TR1 (NPN): BISS transistor switching time definition

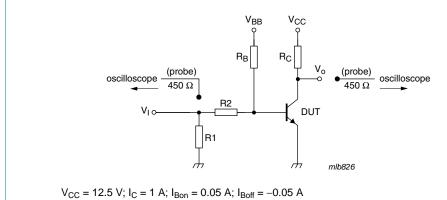


Fig 22. TR1 (NPN): Test circuit for switching times

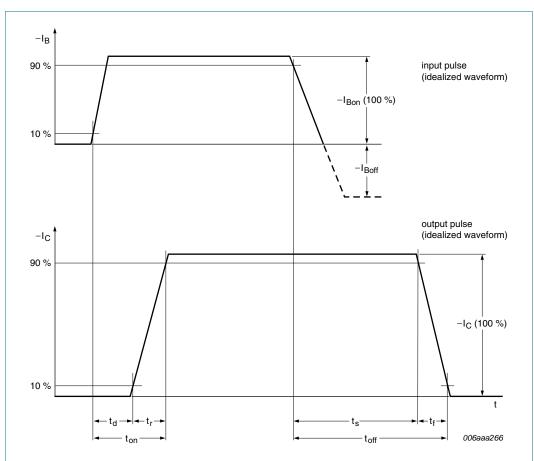
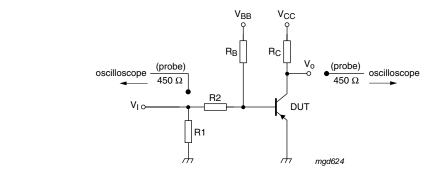


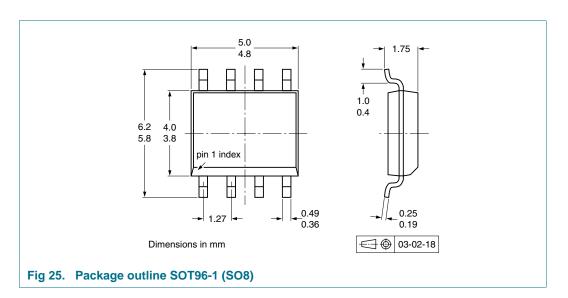
Fig 23. TR2 (PNP): BISS transistor switching time definition



 $V_{CC} = -12.5 \text{ V}; I_C = -1 \text{ A}; I_{Bon} = -0.05 \text{ A}; I_{Boff} = 0.05 \text{ A}$

Fig 24. TR2 (PNP): Test circuit for switching times

9. Package outline



10. Packing information

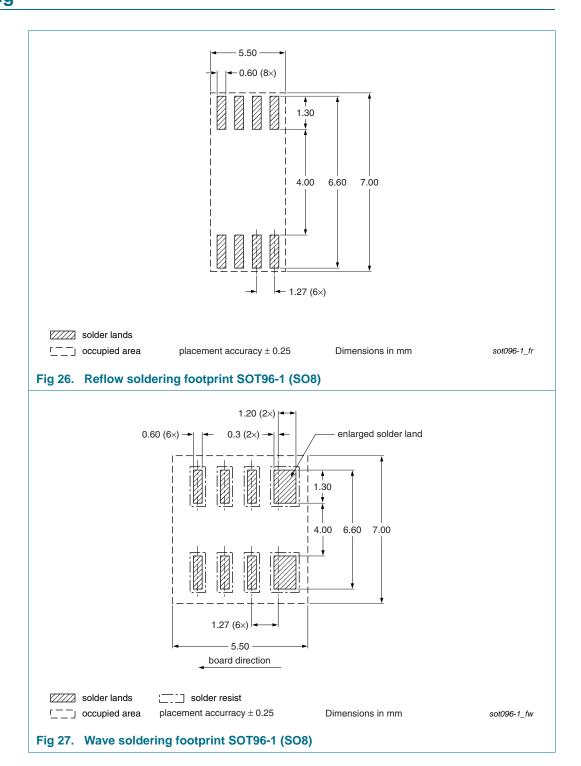
Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing quantity	
			1000	2500
PBSS4032SPN	SOT96-1	8 mm pitch, 12 mm tape and reel	-115	-118

^[1] For further information and the availability of packing methods, see Section 14.

11. Soldering



12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes			
PBSS4032SPN v.2	20101014	Product data sheet	-	PBSS4032SPN v.1			
Modifications: • Figure 1 "Per device: Power derating curves": updated.							
PBSS4032SPN v.1	20100714	Product data sheet	-	-			

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

13.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

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Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

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PBSS4032SPN

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Nexperia PBSS4032SPN

30 V NPN/PNP low V_{CEsat} (BISS) transistor

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14. Contact information

For more information, please visit: http://www.nexperia.com

For sales office addresses, please send an email to: salesaddresses@nexperia.com

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