

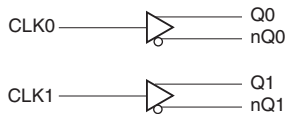
## GENERAL DESCRIPTION

The 85322 is a Dual LVCMOS / LVTTTL-to-Differential 2.5V / 3.3V LVPECL translator. The 85322 has selectable single ended clock inputs. The single ended clock input accepts LVCMOS or LVTTTL input levels and translate them to 2.5V / 3.3V LVPECL levels. The small outline 8-pin SOIC package makes this device ideal for applications where space, high performance and low power are important.

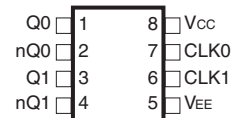
## FEATURES

- Two differential 2.5V/3.3V LVPECL outputs
- Selectable CLK0, CLK1 LVCMOS/LVTTTL clock inputs
- CLK0 and CLK1 can accepts the following input levels: LVCMOS or LVTTTL
- Maximum output frequency: 267MHz
- Part-to-part skew: 250ps (maximum)
- 3.3V operating supply voltage (operating range 3.135V to 3.465V)
- 2.5V operating supply voltage (operating range 2.375V to 2.625V)
- 0°C to 70°C ambient operating temperature
- Lead-Free package available

## BLOCK DIAGRAM



## PIN ASSIGNMENT



### 85322

#### 8-Lead SOIC

3.90mm x 4.92mm x 1.37mm body package

#### M Package

Top View

**TABLE 1. PIN DESCRIPTIONS**

| Number | Name            | Type   |        | Description  |
|--------|-----------------|--------|--------|--|
| 1, 2   | Q0, nQ0         | Output |        | Differential output pair. LVPECL interface levels. |
| 3, 4   | Q1, nQ1         | Output |        | Differential output pair. LVPECL interface levels. |
| 5      | V <sub>EE</sub> | Power  |        | Negative supply pin.                               |
| 6      | CLK1            | Input  | Pullup | LVC MOS / LV TTL clock input.                      |
| 7      | CLK0            | Input  | Pullup | LVC MOS / LV TTL clock input.                      |
| 8      | V <sub>CC</sub> | Power  |        | Positive supply pin.                               |

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol              | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------------|-----------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub>     | Input Capacitance     |                 |         | 4       |         | pF    |
| R <sub>PULLUP</sub> | Input Pullup Resistor |                 |         | 51      |         | kΩ    |

**ABSOLUTE MAXIMUM RATINGS**

|  |                          |
|--|--------------------------|
| Supply Voltage, $V_{CC}$                 | 4.6V                     |
| Inputs, $V_I$                            | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, $I_O$                           |                          |
| Continuous Current                       | 50mA                     |
| Surge Current                            | 100mA                    |
| Package Thermal Impedance, $\theta_{JA}$ | 112.7°C/W (0 lfpm)       |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C           |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

| Symbol   | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-------------------------|-----------------|---------|---------|---------|-------|
| $V_{CC}$ | Positive Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $I_{EE}$ | Power Supply Current    |                 |         |         | 25      | mA    |

**TABLE 3B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

| Symbol   | Parameter          | Test Conditions                          | Minimum | Typical | Maximum | Units   |
|----------|--------------------|--|---------|---------|---------|---------|
| $V_{IH}$ | Input High Voltage | CLK0, CLK1                               | 2       |         | 3.765   | V       |
| $V_{IL}$ | Input Low Voltage  | CLK0, CLK1                               | -0.3    |         | 1.3     | V       |
| $I_{IH}$ | Input High Current | CLK0, CLK1<br>$V_{CC} = V_{IN} = 3.465V$ |         |         | 5       | $\mu A$ |
| $I_{IL}$ | Input Low Current  | CLK0, CLK1<br>$V_{CC} = V_{IN} = 3.465V$ | -150    |         |         | $\mu A$ |

**TABLE 3C. LVPECL DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

| Symbol      | Parameter                         | Test Conditions            | Minimum        | Typical | Maximum        | Units |
|-------------|-----------------------------------|----------------------------|----------------|---------|----------------|-------|
| $V_{OH}$    | Output High Voltage; NOTE 1       | $V_{CC} = V_{IN} = 3.465V$ | $V_{CC} - 1.4$ |         | $V_{CC} - 0.9$ | V     |
| $V_{OL}$    | Output Low Voltage; NOTE 1        | $V_{CC} = V_{IN} = 3.465V$ | $V_{CC} - 2.0$ |         | $V_{CC} - 1.7$ | V     |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing |                            | 0.65           |         | 1.0            | V     |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

**TABLE 4A. AC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

| Symbol      | Parameter                    | Test Conditions    | Minimum | Typical | Maximum | Units |
|-------------|------------------------------|--------------------|---------|---------|---------|-------|
| $f_{MAX}$   | Output Frequency             |                    |         |         | 267     | MHz   |
| $t_{PD}$    | Propagation Delay; NOTE 1    | $f \leq 267MHz$    | 0.6     |         | 1.8     | ns    |
| tsk(pp)     | Part-to-Part Skew; NOTE 2, 3 |                    |         |         | 250     | ps    |
| $t_R / t_F$ | Output Rise/Fall Time        | 20% to 80% @ 50MHz | 300     |         | 700     | ps    |
| odc         | Output Duty Cycle            |                    | 40      |         | 60      | %     |

All parameters measured at 133MHz unless noted otherwise.

NOTE 1: Measured from  $V_{CC}/2$  of the input to the differential output crossing point.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

**TABLE 3D. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

| Symbol   | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-------------------------|-----------------|---------|---------|---------|-------|
| $V_{CC}$ | Positive Supply Voltage |                 | 2.375   | 2.5     | 2.625   | V     |
| $I_{EE}$ | Power Supply Current    |                 |         |         | 25      | mA    |

**TABLE 3E. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

| Symbol   | Parameter          | Test Conditions                         | Minimum | Typical | Maximum | Units   |
|----------|--------------------|---|---------|---------|---------|---------|
| $V_{IH}$ | Input High Voltage | CLK0, CLK1                              | 1.6     |         | 2.925   | V       |
| $V_{IL}$ | Input Low Voltage  | CLK0, CLK1                              | -0.3    |         | 0.9     | V       |
| $I_{IH}$ | Input High Current | CLK0, CLK1<br>$V_{CC} = V_{IN} = 2.625$ |         |         | 5       | $\mu A$ |
| $I_{IL}$ | Input Low Current  | CLK0, CLK1<br>$V_{CC} = V_{IN} = 2.625$ | -150    |         |         | $\mu A$ |

**TABLE 3F. LVPECL DC CHARACTERISTICS,  $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

| Symbol      | Parameter                         | Test Conditions | Minimum        | Typical | Maximum        | Units |
|-------------|-----------------------------------|-----------------|----------------|---------|----------------|-------|
| $V_{OH}$    | Output High Voltage; NOTE 1       |                 | $V_{CC} - 1.4$ |         | $V_{CC} - 0.9$ | V     |
| $V_{OL}$    | Output Low Voltage; NOTE 1        |                 | $V_{CC} - 2.0$ |         | $V_{CC} - 1.7$ | V     |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing |                 | 0.65           |         | 1.0            | V     |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

**TABLE 4B. AC CHARACTERISTICS,  $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

| Symbol      | Parameter                    | Test Conditions    | Minimum | Typical | Maximum | Units |
|-------------|------------------------------|--------------------|---------|---------|---------|-------|
| $f_{MAX}$   | Output Frequency             |                    |         |         | 215     | MHz   |
| $t_{PD}$    | Propagation Delay; NOTE 1    | $f \leq 215MHz$    | 0.8     |         | 2       | ns    |
| tsk(pp)     | Part-to-Part Skew; NOTE 2, 3 |                    |         |         | 250     | ps    |
| $t_R / t_F$ | Output Rise/Fall Time        | 20% to 80% @ 50MHz | 300     |         | 700     | ps    |
| odc         | Output Duty Cycle            |                    | 40      |         | 60      | %     |

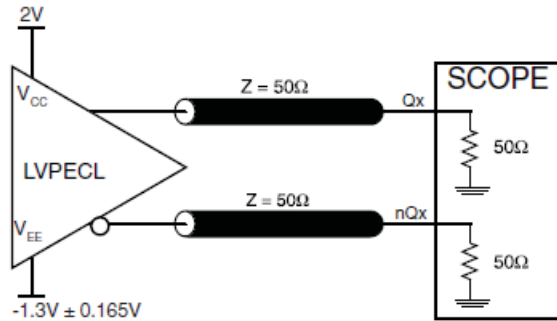
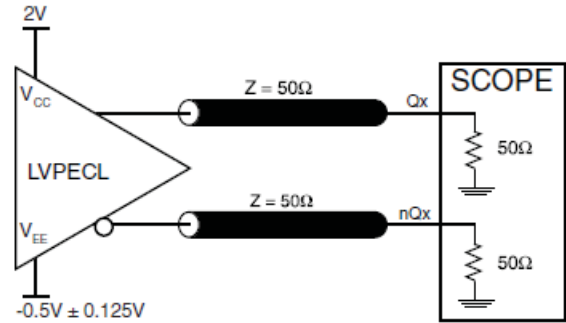
All parameters measured at 133MHz unless noted otherwise.

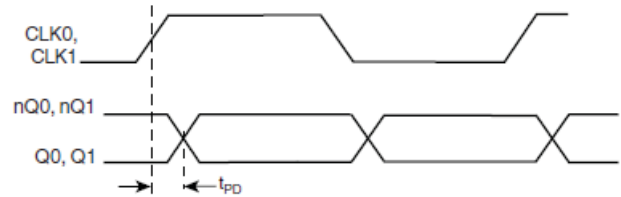
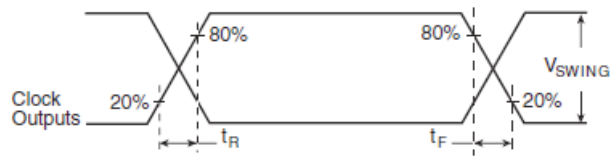
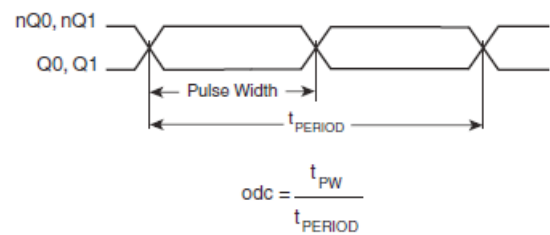
NOTE 1: Measured from  $V_{CC}/2$  of the input to the differential output crossing point.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65..

## PARAMETER MEASUREMENT INFORMATION


**3.3V OUTPUT LOAD AC TEST CIRCUIT**

**2.5V OUTPUT LOAD AC TEST CIRCUIT**

**PART-TO-PART SKEW**

**PROPAGATION DELAY**

**OUTPUT RISE/FALL TIME**

**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**

## APPLICATION INFORMATION

### TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to

drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 1A and 1B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

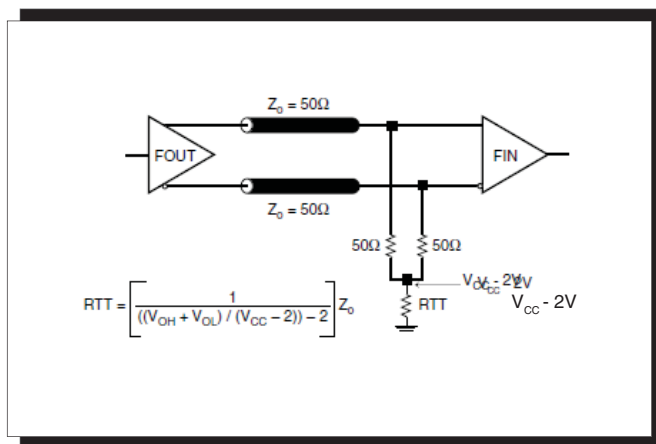


FIGURE 1A. LVPECL OUTPUT TERMINATION

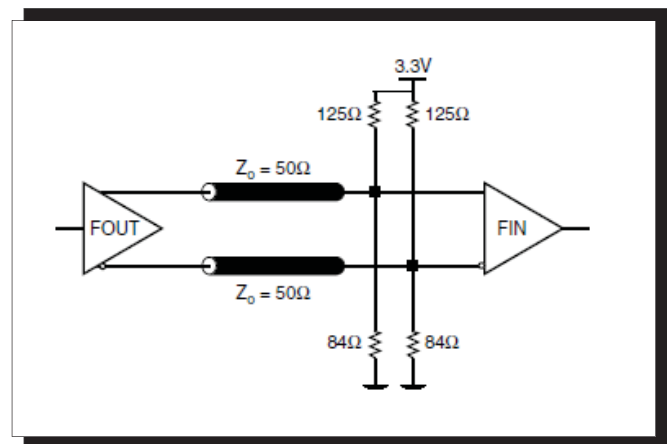


FIGURE 1B. LVPECL OUTPUT TERMINATION

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 85322. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 85322 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 25mA = 86.6mW$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $2 * 30mW = 60mW$

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 86.6mW + 60mW = 146.6mW$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 103.3°C/W per Table 5 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ C + 0.147W * 103.3^\circ C/W = 85.2^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 5. THERMAL RESISTANCE  $\theta_{JA}$  FOR 8-PIN SOIC, FORCED CONVECTION**

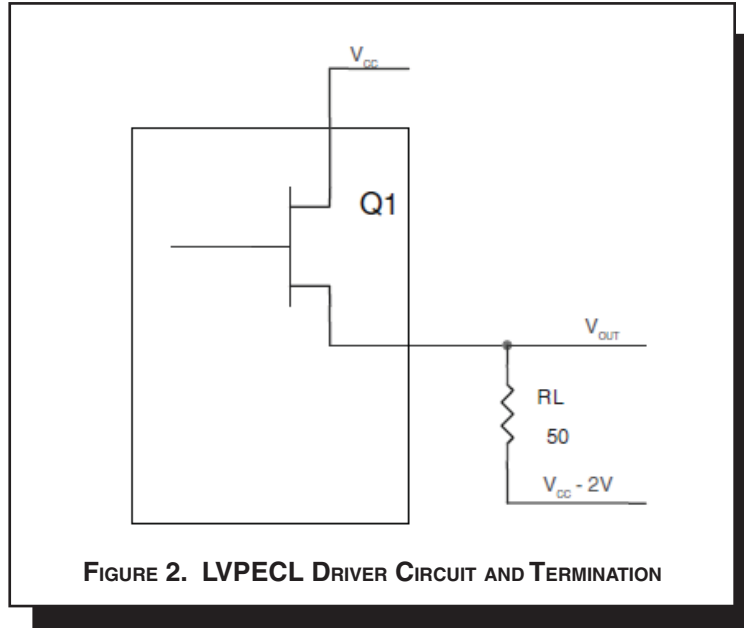
|  | $\theta_{JA}$ by Velocity (Linear Feet per Minute) |           |           |
|--|--|-----------|-----------|
|  | 0  | 200       | 500       |
| Single-Layer PCB, JEDEC Standard Test Boards | 153.3°C/W  | 128.5°C/W | 115.5°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards  | 112.7°C/W  | 103.3°C/W | 97.1°C/W  |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 2*.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.9V$

$$(V_{CC\_MAX} - V_{OH\_MAX}) = 0.9V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.7V$

$$(V_{CC\_MAX} - V_{OL\_MAX}) = 1.7V$$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

Total Power Dissipation per output pair =  $Pd\_H + Pd\_L = \mathbf{30mW}$



## RELIABILITY INFORMATION

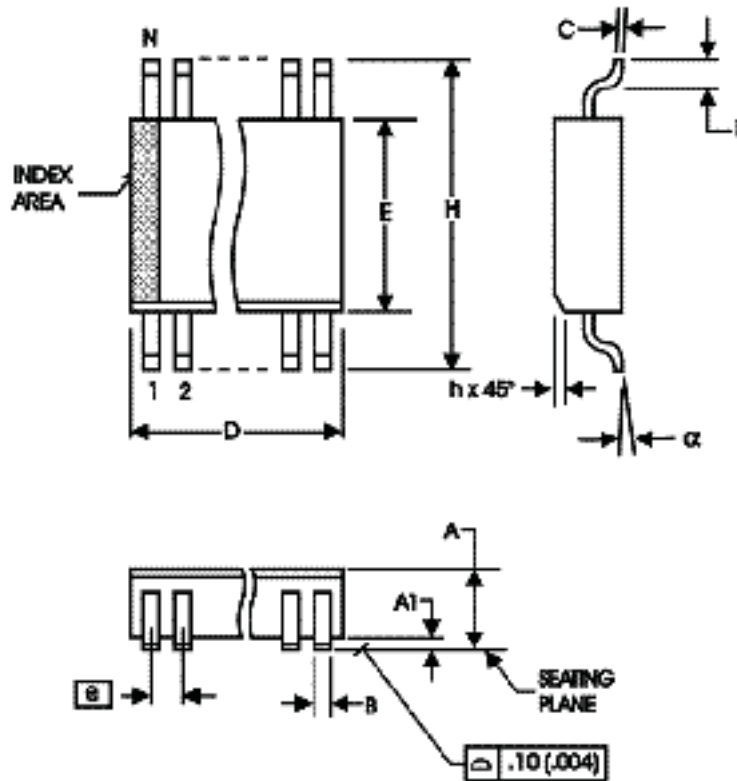
**TABLE 6.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 8 LEAD SOIC**

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) |           |            |            |
|--|-----------|------------|------------|
|  | <b>0</b>  | <b>200</b> | <b>500</b> |
| Single-Layer PCB, JEDEC Standard Test Boards       | 153.3°C/W | 128.5°C/W  | 115.5°C/W  |
| Multi-Layer PCB, JEDEC Standard Test Boards        | 112.7°C/W | 103.3°C/W  | 97.1°C/W   |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for 85322 is: 269

**PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC**

**TABLE 7. PACKAGE DIMENSIONS**

| SYMBOL | Millimeters |         |
|--------|-------------|---------|
|        | MINIMUM     | MAXIMUM |
| N      | 8           |         |
| A      | 1.35        | 1.75    |
| A1     | 0.10        | 0.25    |
| B      | 0.33        | 0.51    |
| C      | 0.19        | 0.25    |
| D      | 4.80        | 5.00    |
| E      | 3.80        | 4.00    |
| e      | 1.27 BASIC  |         |
| H      | 5.80        | 6.20    |
| h      | 0.25        | 0.50    |
| L      | 0.40        | 1.27    |
| α      | 0°          | 8°      |

Reference Document: JEDEC Publication 95, MS-012

**TABLE 8. ORDERING INFORMATION**

| <b>Part/Order Number</b> | <b>Marking</b> | <b>Package</b>          | <b>Shipping Packaging</b> | <b>Temperature</b> |
|--------------------------|----------------|-------------------------|---------------------------|--------------------|
| 85322AMLF                | 85322AML       | 8 lead "Lead-Free" SOIC | tube                      | 0°C to 70°C        |
| 85322AMLFT               | 853322AML      | 8 lead "Lead-Free" SOIC | tape & reel               | 0°C to 70°C        |

| REVISION HISTORY SHEET |                        |                            |  |          |
|------------------------|------------------------|----------------------------|--|----------|
| Rev                    | Table                  | Page                       | Description of Change  | Date     |
| A                      |                        | 9                          | Added Termination for LVPECL Outputs section.  | 5/30/02  |
| A                      |                        | 6                          | 3.3V Output Load Test Circuit Diagram, corrected $V_{EE} = -1.3V \pm 0.135V$   | 8/23/02  |
|                        |                        | 7                          | to read $V_{EE} = -1.3V \pm 0.165V$ .<br>Updated Output Rise/Fall Time Diagram.  |          |
| B                      | T2<br>T4A & T4B        | 2<br>3<br>3 & 4<br>6       | Pin Characteristics Table - changed $C_{IN}$ 4pF max. to 4pF typical.<br>Absolute Maximum Rating - changed Outputs rating.<br>3.3V and 2.5V AC Tables - changed tsk(pp) from 150ps max. to 250ps max. and reflects Features section on page 1.<br>Updated LVPECL Output Termination drawings.<br>Updated format.   | 6/12/03  |
| B                      | T8                     | 11                         | Ordering Information Table - added Lead Free part.   | 10/18/04 |
| C                      | T2<br>T3C<br>T3F<br>T8 | 2<br>3<br>4<br>7 - 8<br>11 | Pin Characteristics Table - deleted RPulldown row.<br>LVPECL 3.3V DC Characteristics Table -corrected $V_{OH}$ max. from $V_{CC} - 1.0V$ to $V_{CC} - 0.9V$ ; and $V_{SWING}$ max. from 0.85V to 1.0V.<br>LVPECL 2.5V DC Characteristics Table -corrected $V_{OH}$ max. from $V_{CC} - 1.0V$ to $V_{CC} - 0.9V$ ; and $V_{SWING}$ max. from 0.85V to 1.0V.<br>Power Considerations - corrected power dissipation to reflect $V_{OH}$ max in Table 3C & 3F.<br>Ordering Information Table - added lead-free note. | 4/11/07  |
| D                      | T8                     | 11<br>13                   | Updated datasheet's header/footer with IDT from ICS.<br>Removed ICS prefix from Part/Order Number column.<br>Added Contact Page.   | 7/31/10  |
| D                      | T8                     | 11                         | Removed ICS from the part number where needed.<br>Ordering Information - Removed leaded parts. Removed quantities for tape and reel. Deleted the LF note below the table.<br>Updated header and footer.  | 1/20/16  |



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