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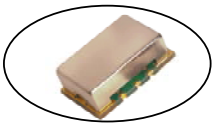
A Division of Crystek Corporation



Differential LVPECL Voltage Controlled Crystal Oscillator

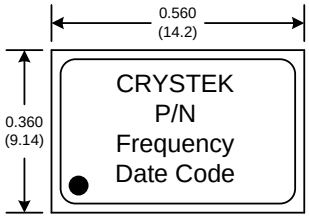
CVPD-920 Model
9×14 mm SMD, 3.3V, LVPECL

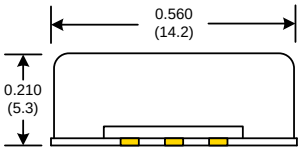
Frequency Range:		50 MHz to 125 MHz
Frequency Pulling:		±20ppm APR Min
Temperature Range:		0°C to 70°C
	(Option X)	-40°C to 85°C
Storage:		-45°C to 90°C
Input Voltage:		3.3V ±0.3V
Control Voltage:		1.65V ±1.65V
Input Current:		88mA Max
Output:		Differential LVPECL
	Symmetry:	45/55% Max @ zero crossing point
	Rise/Fall Time:	1nSec Max (20% to 80%)
	Linearity:	±10% Max
	Logic:	Terminated to Vcc-2V into 50 ohms "0" = Vcc-1.85V Min, Vcc-1.62V Max "1" = Vcc-1.02V Min, Vcc-0.81V Max
	Disable Time:	200nSec
	Start-up Time:	1mSec Typical, 2mSec Max
Phase Jitter:	12kHz to 80MHz	0.5pSec Typical, 1pSec RMS Max
Phase Noise:	10Hz	-65 dBc/Hz Typical
	100Hz	-98 dBc/Hz Typical
	1kHz	-125 dBc/Hz Typical
	10kHz	-140 dBc/Hz Typical
	100kHz	-145 dBc/Hz Typical
Aging:		<3ppm 1st year, <1ppm every year thereafter

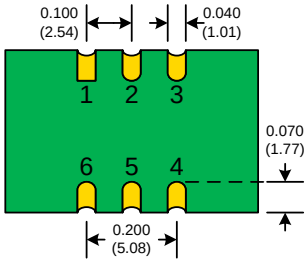
RoHS Compliant

CRYSTEK CORPORATION
MADE IN THE USA

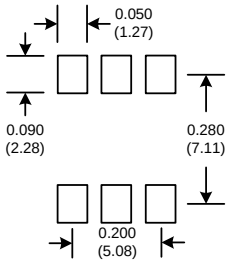
Designed to meet today's requirements for 3.3V Differential LVPECL applications. The CVPD-920 is produced using our cost saving FR5 PCB and UM-1 overtone crystal technology. This design offers considerable cost savings over other HFF VCXO products when broad frequency pulling is not required. Also available in 14 pin dip fully hermetic package.



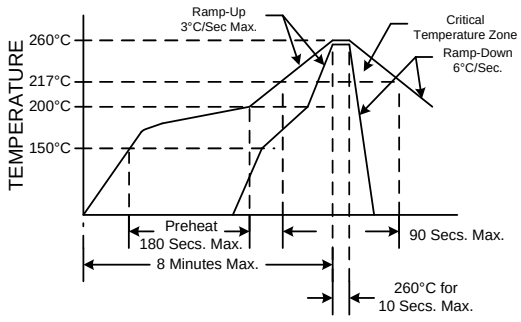




SUGGESTED PAD LAYOUT



RECOMMENDED REFLOW SOLDERING PROFILE



NOTE: Reflow Profile with 240°C peak also acceptable.

PIN	Function
1	Control Volt
2	E/D
3	GND
4	OUT
5	$\overline{\text{OUT}}$
6	Vcc

Crystek Part Number Guide

CVPD-920 X - 100.000
#1 #2 #3 #4

#1 Crystek 9×14 SMD PECL VCXO
#2 Model 920
#3 Temp. Range: Blank = 0/70°C, X = -40/85°C
#4 Frequency in MHz: 3 or 6 decimal places

Example:
CVPD-920X-100.000 = 3.3V, 45/55, -40/85°C, 100.000 MHz

Enable/Disable Function	
Pin 2	Output Pin
Open "0" level Vcc-1.620V Max "1" level Vcc-1.025V Min	Active Active Disabled
Disabled State: Pin 4 will assume a fixed level of logic "0" Pin 5 will assume a fixed level of logic "1"	

Specifications subject to change without notice.

TD-030701 Rev. H

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