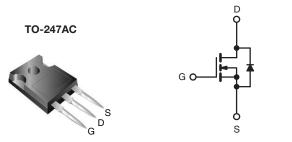


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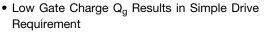
Power MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	500				
$R_{DS(on)}(\Omega)$	V _{GS} = 10 V 0.135				
Q _g (Max.) (nC)	190				
Q _{gs} (nC)	59				
Q _{gd} (nC)	84				
Configuration	Single				



N-Channel MOSFET

FEATURES





• Improved Gate, Avalanche and Dynamic dV/dt

- Fully Characterized Capacitance and Avalanche Voltage and Current
- Low R_{DS(on)}
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switching and High Frequency Circuits

ORDERING INFORMATION				
Package	TO-247AC			
Lead (Pb)-free	IRFP32N50KPbF			
Leau (FD)-liee	SiHFP32N50K-E3			
SnPb	IRFP32N50K			
SHED	SiHFP32N50K			

PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V _{DS}	500	V	
Gate-Source Voltage			V_{GS}	± 30	v	
Continuous Drain Current	V et 10 V	T _C = 25 °C	1-	32	А	
Continuous Drain Current	V _{GS} at 10 V	T _C = 100 °C	I _D	20		
Pulsed Drain Current ^a			I _{DM}	130		
Linear Derating Factor				3.7	W/°C	
Single Pulse Avalanche Energy ^b			E _{AS}	450	mJ	
Repetitive Avalanche Current ^a			I _{AR}	32	Α	
Repetitive Avalanche Energy ^a			E _{AR}	46	mJ	
Maximum Power Dissipation $T_C = 25 ^{\circ}C$			P_{D}	460	W	
Peak Diode Recovery dV/dt ^c			dV/dt	13	V/ns	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature) for 10 s				300 ^d		
Mounting Touris	6-32 or M3 screw			10	lbf ⋅ in	
Mounting Torque				1.1	N⋅m	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b. Starting T_J = 25 °C, L = 0.87 mH, R_g = 25 $\Omega,\,I_{AS}$ = 32 A.
- c. $I_{SD} \le 32$ A, $dI/dt \le 197$ A/ μ s, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C.
- d. 1.6 mm from case.

^{*} Pb containing terminations are not RoHS compliant, exemptions may apply

IRFP32N50K, SiHFP32N50K

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THERMAL RESISTANCE RATINGS					
PARAMETER SYMBOL TYP. MAX. UNIT					
Maximum Junction-to-Ambient	R _{thJA}	-	40		
Case-to-Sink, Flat, Greased Surface	R _{thCS}	0.24	-	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	-	0.26		

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		500	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	ce to 25 °C, I _D = 1 mA	-	0.54	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μA	3.0	-	5.0	V
Gate-Source Leakage	I _{GSS}		V _{GS} = ± 30 V	ı	-	± 100	nA
Zero Gate Voltage Drain Current		V _{DS} =	V _{DS} = 500 V, V _{GS} = 0 V		-	50	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 400 \	$V_{\rm S} = 0 \ V_{\rm S} = 150 \ ^{\circ}{\rm C}$	1	-	250	μΑ
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 32 A ^b	1	0.135	0.16	Ω
Forward Transconductance	g _{fs}	V _{DS}	= 50 V, I _D = 32 A	14	-	-	S
Dynamic							
Input Capacitance	C _{iss}		$V_{GS} = 0 V$	1	5280	-	
Output Capacitance	C _{oss}		$V_{DS} = 25 \text{ V},$	1	550	-	- pF
Reverse Transfer Capacitance	C _{rss}	f = 1	.0 MHz, see fig. 5	-	45	-	
Output Capacitance	C _{oss}		V _{DS} = 1.0 V, f = 1.0 MHz	ı	5630	-	
Output Capacitance		$V_{GS} = 0 V$	V _{DS} = 400 V, f = 1.0 MHz	1	155	-	
Effective Output Capacitance	C _{oss} eff.		V _{DS} = 0 V to 400 V ^c	-	265	-	
Total Gate Charge	Q_g			-	-	190	
Gate-Source Charge	Q_{gs}	$V_{GS} = 10 \text{ V}$ $I_D = 32 \text{ A}, V_{DS} = 400 \text{ V}^b$		-	-	59	nC
Gate-Drain Charge	Q_{gd}			-	-	84	
Turn-On Delay Time	t _{d(on)}	V_{DD} = 250 V, I_{D} = 32 A, Rg = 4.3 Ω , V_{GS} = 10 V ^b		-	28	-	- ns
Rise Time	t _r			1	120	-	
Turn-Off Delay Time	t _{d(off)}			-	48	-	
Fall Time	t _f			-	54	-	
Drain-Source Body Diode Characteristic	es	•					
Continuous Source-Drain Diode Current	Is	MOSFET symbol showing the integral reverse p - n junction diode		I	-	32	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	130	
Body Diode Voltage	V_{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = 32 \text{A}, V_{GS} = 0 \text{V}^{\text{b}}$		-	-	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 32 A, dl/dt = 100 A/μs ^b		-	530	800	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	9.0	13.5	μC
Body Diode Reverse Recovery Current	I _{RRM}			-	30	-	Α
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					1-2)

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b. Pulse width $\leq 400~\mu s;$ duty cycle $\leq 2~\%.$
- c. C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

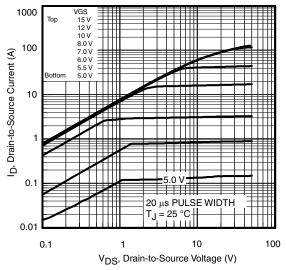


Fig. 1 - Typical Output Characteristics

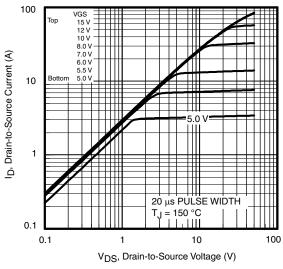


Fig. 2 - Typical Output Characteristics

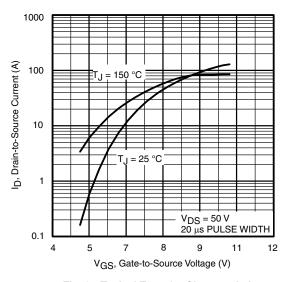


Fig. 3 - Typical Transfer Characteristics

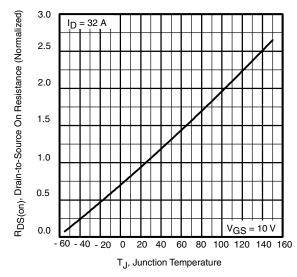


Fig. 4 - Normalized On-Resistance vs. Temperature

IRFP32N50K, SiHFP32N50K

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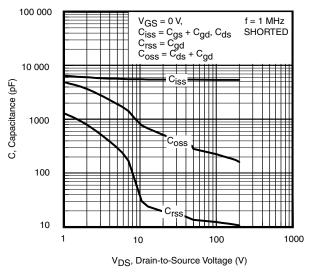


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

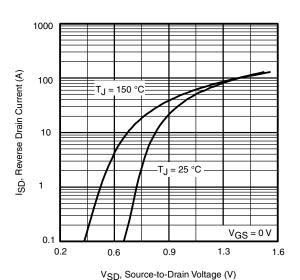


Fig. 7 - Typical Source-Drain Diode Forward Voltage

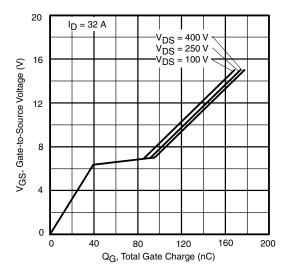


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

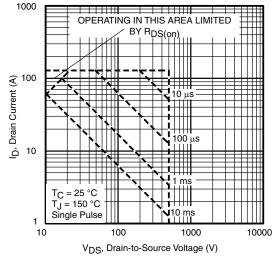


Fig. 8 - Maximum Safe Operating Area

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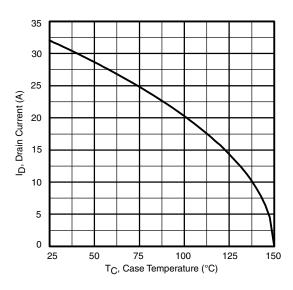


Fig. 9 - Maximum Drain Current vs. Case Temperature

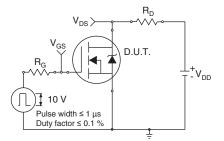


Fig. 10a - Switching Time Test Circuit

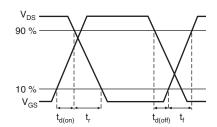


Fig. 10b - Switching Time Waveforms

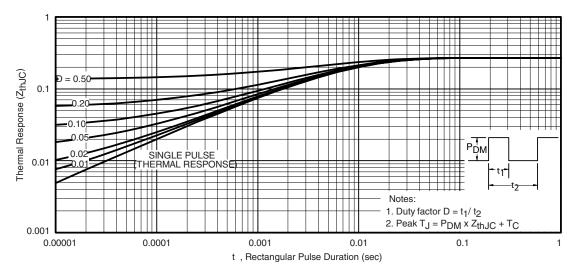
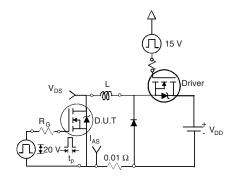
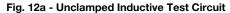


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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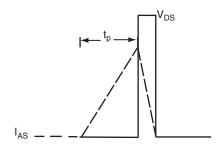


Fig. 12b - Unclamped Inductive Waveforms

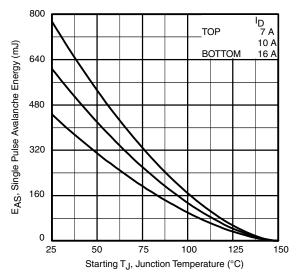


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

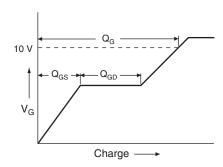


Fig. 13a - Basic Gate Charge Waveform

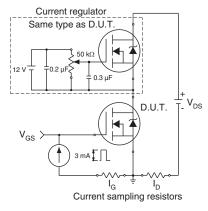
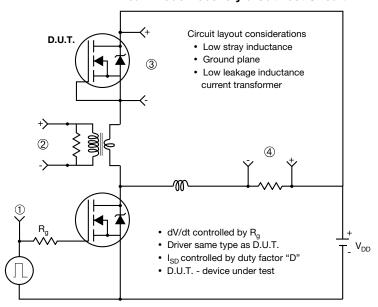


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



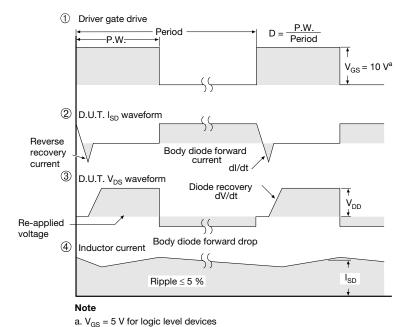
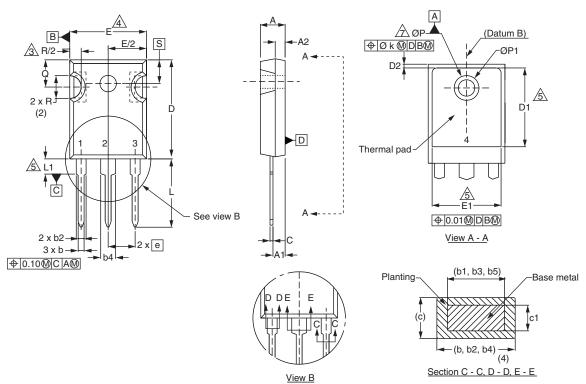


Fig. 14 - For N-Channel

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TO-247AC (High Voltage)



	MILLIMETERS		MILLIME		INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.		
Α	4.58	5.31	0.180	0.209		
A1	2.21	2.59	0.087	0.102		
A2	1.17	2.49	0.046	0.098		
b	0.99	1.40	0.039	0.055		
b1	0.99	1.35	0.039	0.053		
b2	1.53	2.39	0.060	0.094		
b3	1.65	2.37	0.065	0.093		
b4	2.42	3.43	0.095	0.135		
b5	2.59	3.38	0.102	0.133		
С	0.38	0.86	0.015	0.034		
c1	0.38	0.76	0.015	0.030		
D	19.71	20.82	0.776	0.820		
D1	13.08	-	0.515	-		

	MILLIMETERS		INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	=
е	5.46	BSC	0.215 BSC	
Øk	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
ØΡ	3.51	3.66	0.138	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

ECN: X13-0045-Rev. C, 18-Mar-13

DWG: 5971

Notes

- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Contour of slot optional.
- 3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
- 4. Thermal pad contour optional with dimensions D1 and E1. 5. Lead finish uncontrolled in L1.
- 6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
- 7. Outline conforms to JEDEC outline TO-247 with exception of dimension c.
- 8. Xian and Mingxin actually photo.



Revision: 18-Mar-13 Document Number: 91360



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Revision: 02-Oct-12 Document Number: 91000