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December 2014

FDMC8321LDC

N-Channel Power Trench[®] MOSFET 40 V, 108 A, 2.5 mΩ

Features

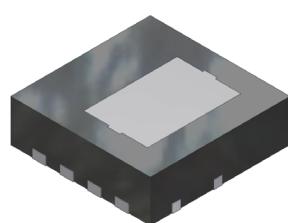
- Dual Cool[™] Top Side Cooling PQFN package
- Max $r_{DS(on)}$ = 2.5 mΩ at V_{GS} = 10 V, I_D = 27 A
- Max $r_{DS(on)}$ = 4.1 mΩ at V_{GS} = 4.5 V, I_D = 21 A
- High performance technology for extremely low $r_{DS(on)}$
- RoHS Compliant

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench[®] process. Advancements in both silicon and Dual Cool[™] package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

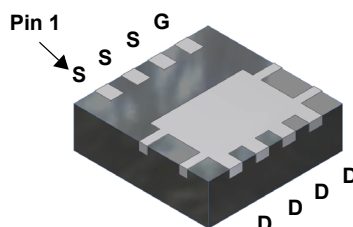
Applications

- Primary DC-DC Switch
- Motor Bridge Switch
- Synchronous Rectifier

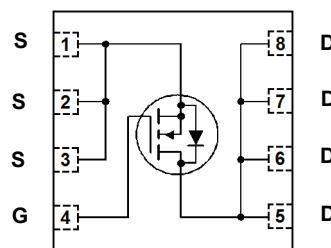


Top

Power 33



Bottom



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous $T_C = 25^\circ\text{C}$	108	A
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	27	
	-Pulsed (Note 4)	320	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	181	mJ
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	56	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	2.2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	42	

Package Marking and Ordering Information

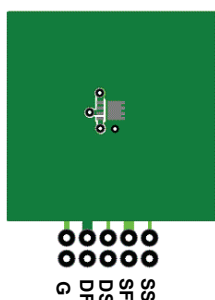
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
8321LD	FDMC8321LDC	Power33	13 "	12 mm	3000 units

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	5.0	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	2.2	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	42	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	105	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1c)	29	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1d)	40	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1e)	19	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1f)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1g)	30	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1h)	79	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	17	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	12	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1l)	16	

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 42 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 105 °C/W when mounted on a minimum pad of 2 oz copper

- c. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- d. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- e. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- f. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- g. 200FPM Airflow, No Heat Sink, 1 in² pad of 2 oz copper
- h. 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
- i. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- j. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- k. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- l. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. E_{AS} of 181 mJ is based on starting $T_J = 25$ °C, $L = 3$ mH, $I_{AS} = 11$ A, $V_{DD} = 40$ V, $V_{GS} = 10$ V. 100% tested at $L = 0.1$ mH, $I_{AS} = 35$ A.

4. Pulse I_d measured at 250μs, refer to Fig 11 SOA graph for more details.

Electrical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$		39		mV/ $^{\circ}\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	1.0	1.7	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$		-6		mV/ $^{\circ}\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 27\text{ A}$		2.0	2.5	m Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 21\text{ A}$		2.8	4.1	
		$V_{GS} = 10\text{ V}$, $I_D = 27\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$		3.0	3.8	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 27\text{ A}$		126		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		2832	3965	pF
C_{oss}	Output Capacitance			777	1090	pF
C_{rss}	Reverse Transfer Capacitance			66	105	pF
R_g	Gate Resistance		0.1	0.7	2.5	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\text{ V}$, $I_D = 27\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		13	23	ns
t_r	Rise Time			5.5	11	ns
$t_{d(off)}$	Turn-Off Delay Time			31	50	ns
t_f	Fall Time			4.8	10	ns
$Q_{g(TOT)}$	Total Gate Charge at 10 V	$V_{DD} = 20\text{ V}$, $I_D = 27\text{ A}$		43	60	nC
$Q_{g(TOT)}$	Total Gate Charge at 5 V			22	31	nC
Q_{gs}	Total Gate Charge			7.1		nC
Q_{gd}	Gate to Drain "Miller" Charge			6.1		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2.3\text{ A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\text{ V}$, $I_S = 27\text{ A}$ (Note 2)		0.8	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 27\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		31	50	ns
Q_{rr}	Reverse Recovery Charge			11	20	nC

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

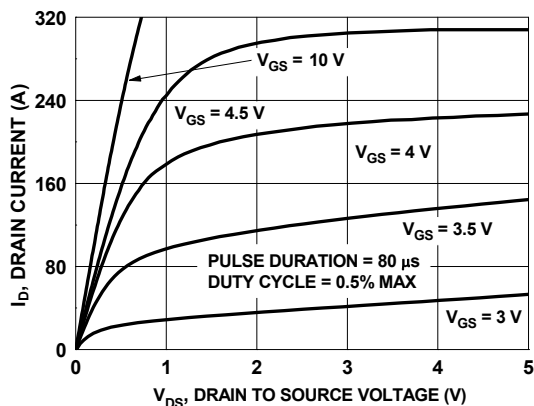


Figure 1. On Region Characteristics

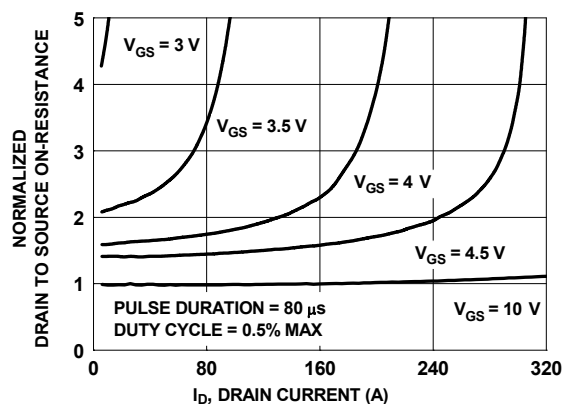


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

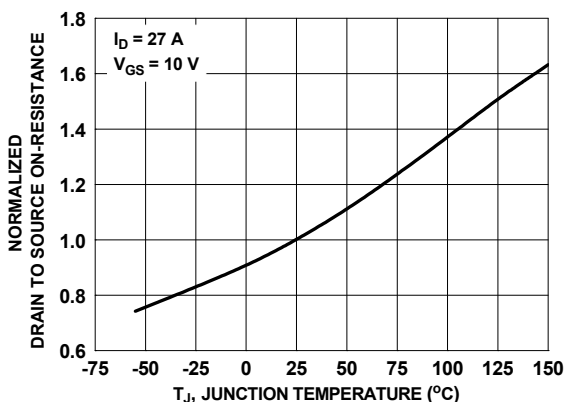


Figure 3. Normalized On Resistance vs Junction Temperature

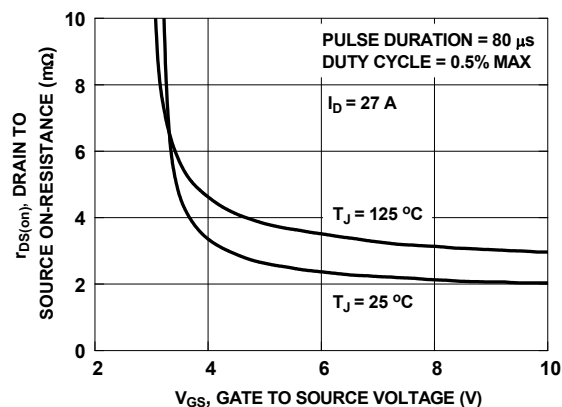


Figure 4. On-Resistance vs Gate to Source Voltage

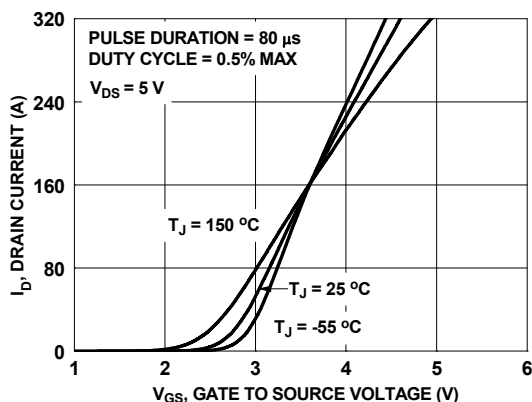


Figure 5. Transfer Characteristics

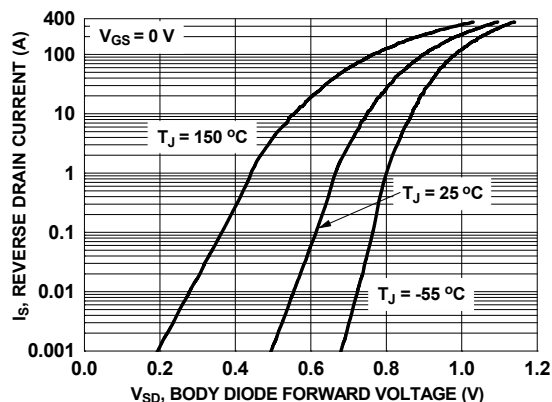


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

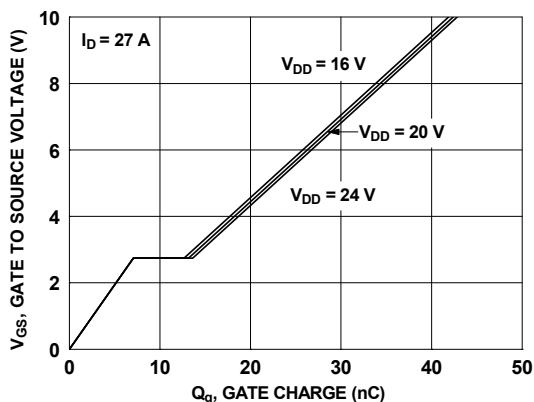


Figure 7. Gate Charge Characteristics

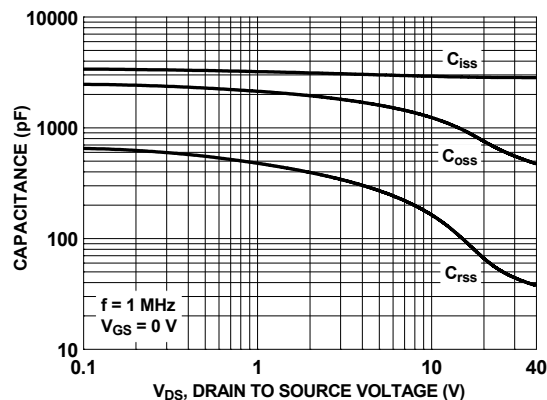


Figure 8. Capacitance vs Drain to Source Voltage

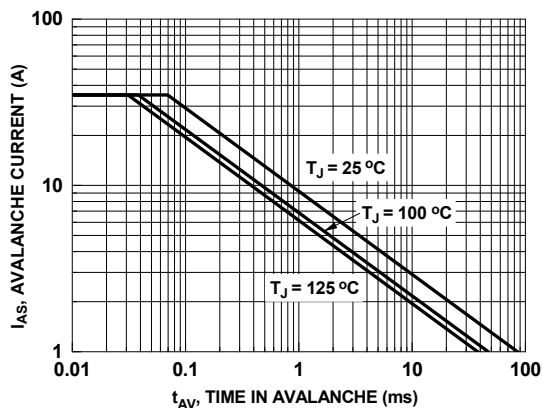


Figure 9. Unclamped Inductive Switching Capability

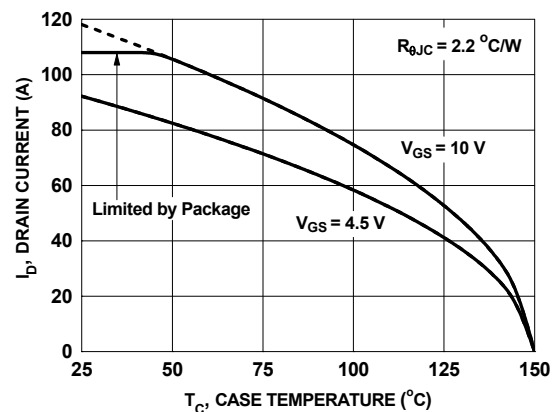


Figure 10. Maximum Continuous Drain Current vs Case Temperature

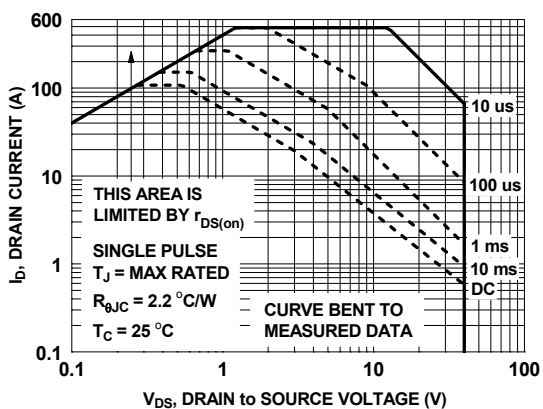


Figure 11. Forward Bias Safe Operating Area

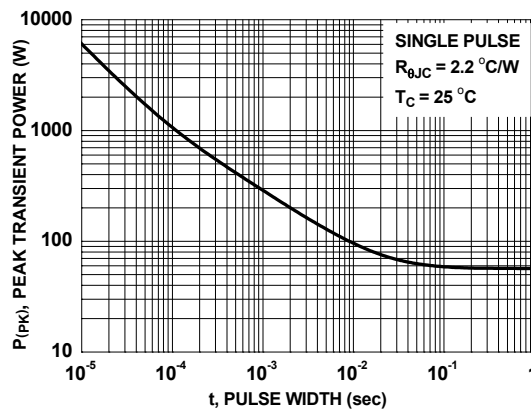


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted

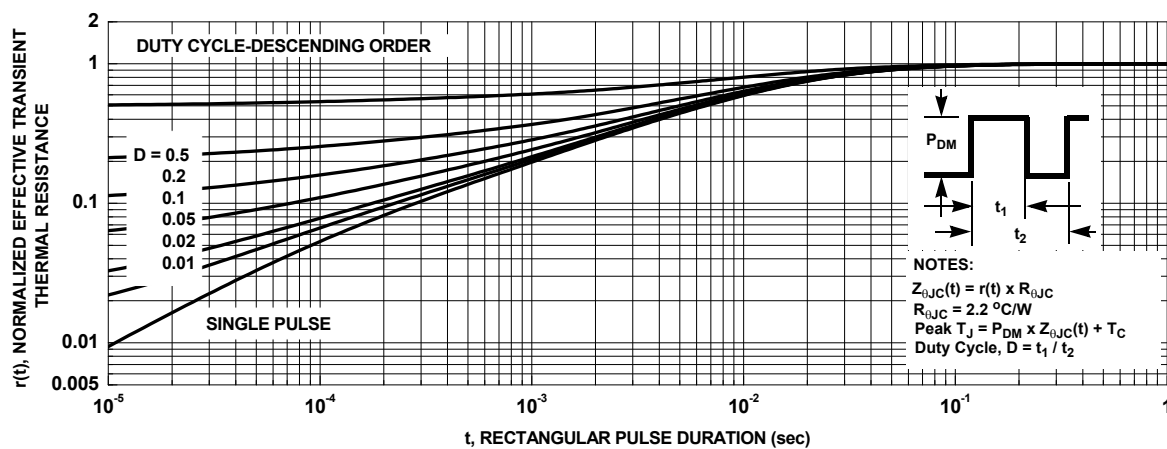
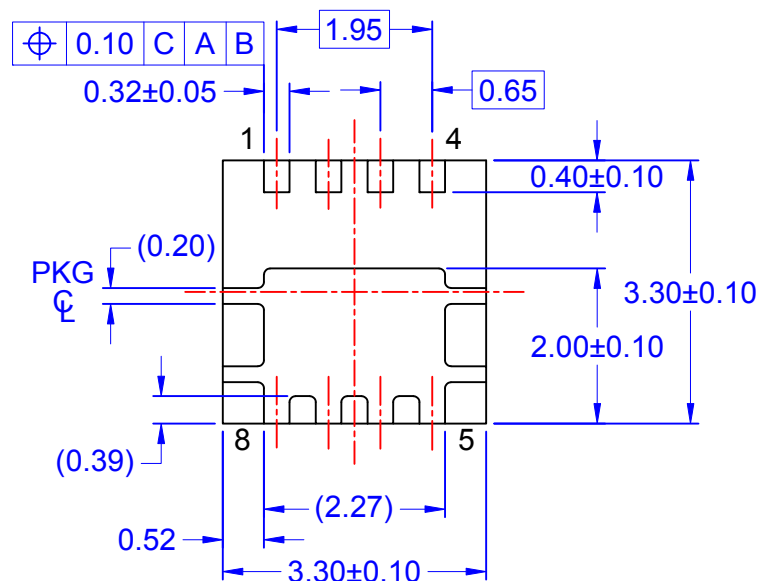
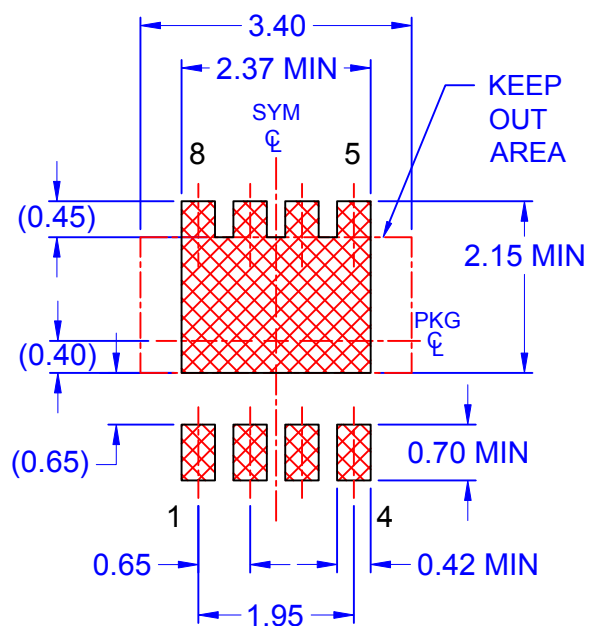


Figure 13. Junction-to-Case Transient Thermal Response Curve



- A) PACKAGE STANDARD REFERENCE:
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- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS
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- D) DIMENSIONING AND TOLERANCING PER
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