FemtoClock® NG Universal Frequency Translator with Phase Build-Out

IDT8T49N205I

PRELIMINARY PRODUCT BRIEF

This is a product brief and is intended to provide an overview only. Additional details are available from IDT. Contact information may be found on the last page.

General Description

The IDT8T49N205I is a highly flexible FemtoClock® NG general purpose, low phase noise Frequency Translator / Synthesizer with Phase Build-Out (PBO) suitable for networking and communications applications. It is able to generate any output frequency in the 0.98MHz - 312.5MHz range and most output frequencies in the 312.5MHz - 1,300MHz range (see Table 3 for details). A wide range of input reference clocks and a range of low-cost fundamental mode crystal frequencies may be used as the source for the output frequency.

The IDT8T49N205I has three operating modes to support a very broad spectrum of applications:

1 Frequency Synthesizer
- Synthesizes output frequencies from a 16MHz - 40MHz fundamental mode crystal.
- Fractional feedback division is used, so there are no requirements for any specific crystal frequency to produce the desired output frequency with a high degree of accuracy.

2) High-Bandwidth Frequency Translator
- Applications: PCI Express, Computing, General Purpose
- Translates any input clock in the 16MHz - 710MHz frequency range into any supported output frequency.
- This mode has a high PLL loop bandwidth in order to track input reference changes, such as Spread-Spectrum Clock modulation, so it will not attenuate much jitter on the input reference.

3) Low-Bandwidth Frequency Translator
- Applications: Networking & Communications.
- Translates any input clock in the 8kHz -710MHz frequency range into any supported output frequency.
- This mode supports PLL loop bandwidths in the 10Hz - 580Hz range and makes use of an external crystal to provide significant jitter attenuation.

This device provides two factory-programmed default power-up configurations burned into One-Time Programmable (OTP) memory. The configuration to be used is selected by the CONFIG pin. The two configurations are specified by the customer and are programmed by IDT during the final test phase from an on-hand stock of blank devices. The two configurations may be completely independent of one another.

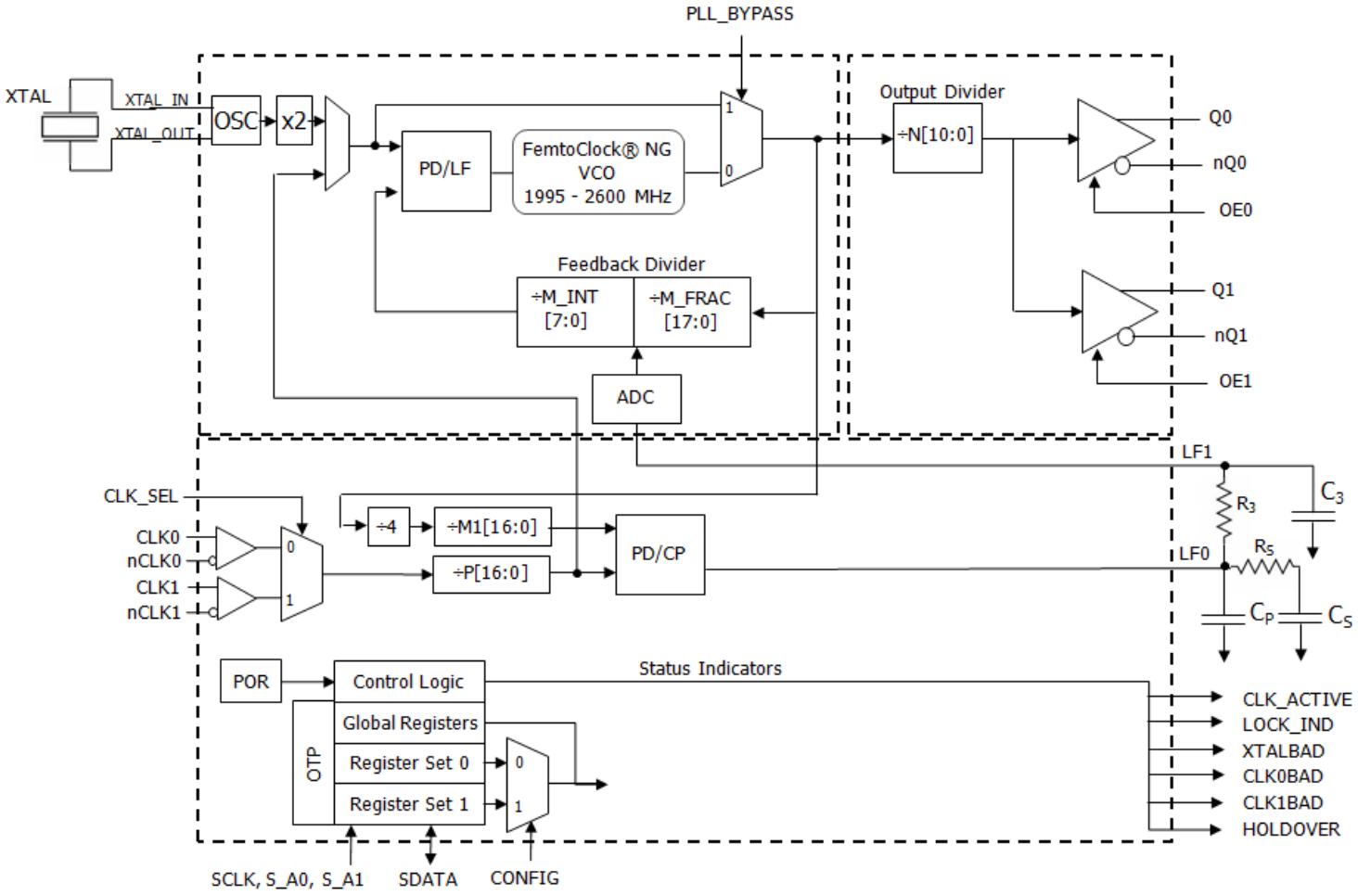
One usage example might be to install the device on a line card with two optional daughter cards: an OC-12 option requiring a 622.08MHz LVDS clock translated from a 19.44MHz input and a Gigabit Ethernet option requiring a 125MHz LVPECL clock translated from the same 19.44MHz input reference.

To implement other configurations, these power-up default settings can be overwritten after power-up using the I^2C interface and the device can be completely reconfigured. However, these settings would have to be re-written next time the device powers-up.

Features

- Fourth Generation FemtoClock® NG technology
- Universal Frequency Translator/Frequency Synthesizer
  - Zero ppm frequency translation
- Two outputs, individually programmable as LVPECL or LVDS
  - Both outputs may be set to use 2.5V or 3.3V output levels
  - Programmable output frequency: 0.98MHz up to 1,300MHz
- Two differential inputs support the following input types: LVPECL, LVDS, LVHSTL, HCSL
  - Input frequency range: 8kHz - 710MHz
- Phase Build-Out minimizes output phase change on switchover
- Crystal input frequency range: 16MHz - 40MHz
- Two factory-set register configurations for power-up default state
  - Power-up default configuration pin or register selectable
  - Configurations customized via One-Time Programmable ROM
  - Settings may be overwritten after power-up via I^2C
  - I^2C Serial interface for register programming
- RMS phase jitter at 155.52MHz, using a 40MHz crystal (12kHz - 20MHz): 463fs (typical), Low Bandwidth Mode (FracN)
- Output supply voltage modes:
  $V_{CC}/V_{CCA}/V_{CCO}$
  3.3V/3.3V/3.3V
  3.3V/3.3V/2.5V (LVPECL only)
  2.5V/2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) packaging

Complete Block Diagram



Functional Description

The IDT8T49N205I is designed to provide two copies of almost any desired output frequency within its operating range (0.98 - 1300MHz) from any input source in the operating range (8kHz - 710MHz). It is capable of synthesizing frequencies from a crystal or crystal oscillator source. The output frequency is generated regardless of the relationship to the input frequency. The output frequency will be exactly the required frequency in most cases. In most others, it will only differ from the desired frequency by a few ppb. IDT configuration software will indicate the frequency error, if any. The IDT8T49N205I can translate the desired output frequency from one of two input clocks. Again, no relationship is required between the input and output frequencies in order to translate to the output clock rate. In this frequency translation mode, a low-bandwidth, jitter attenuation option is available that makes use of an external fixed-frequency crystal or crystal oscillator to translate from a noisy input source. If the input clock is known to be fairly clean or if some modulation on the input needs to be tracked, then the high-bandwidth frequency translation mode can be used, without the need for the external crystal.

The input clock references and crystal input are monitored continuously and appropriate alarm outputs are raised both as register bits and hard-wired pins in the event of any out-of-specification conditions arising. Clock switching is supported in manual, revertive & non-revertive modes.

The IDT8T49N205I has two factory-programmed configurations that may be chosen from as the default operating state after reset. This is intended to allow the same device to be used in two different applications without any need for access to the I^2C registers. These defaults may be over-written by I^2C register access at any time, but those over-written settings will be lost on power-down. Please contact IDT if a specific set of power-up default settings is desired.

Configuration Selection

The IDT8T49N205I comes with two factory-programmed default configurations. When the device comes out of power-up reset the selected configuration is loaded into operating registers. The IDT8T49N205I uses the state of the CONFIG pin or CONFIG register bit (controlled by the CFG_PIN_REG bit) to determine which configuration is active. When the output frequency is changed either via the CONFIG pin or via internal registers, the output behavior may not be predictable during the register writing and output settling periods. Devices sensitive to glitches or runt pulses may have to be reset once reconfiguration is complete.

Once the device is out of reset, the contents of the operating registers can be modified by write access from the I^2C serial port. Users that have a custom configuration programmed may not require I^2C access.

It is expected that the IDT8T49N205I will be used almost exclusively in a mode where the selected configuration will be used from device power-up without any changes during operation. For example, the device may be designed into a communications line card that supports different I/O modules such as a standard OC-12 module running at 622.08MHz or a (255/237) FEC rate OC-12 module running at 669.32MHz. The different I/O modules would result in a different level on the CONFIG pin which would select different divider ratios within the IDT8T49N205I for the two different card configurations. Access via I^2C would not be necessary for operation using either of the internal configurations.

Operating Modes

The IDT8T49N205I has three operating modes. There are two frequency translator modes - low bandwidth and high bandwidth and a frequency synthesizer mode. The device will operate in the same mode regardless of which configuration is active.

Output Dividers & Supported Output Frequencies

In all 3 operating modes, the output stage behaves the same way, but different operating frequencies can be specified in the two configurations.

The internal VCO is capable of operating in a range anywhere from 1.995GHz - 2.6GHz. It is necessary to choose an integer multiplier of the desired output frequency that results in a VCO operating frequency within that range. The output divider stage N[10:0] is limited to selection of integers from 2 to 2046. Please refer to Table 3 for the values of N applicable to the desired output frequency.

Table 3. Output Divider Settings & Frequency Ranges

Register Setting	Frequency Divider	Minimum f_{OUT}	Maximum f_{OUT}
Nn[10:0]	**N**	**(MHz)**	**(MHz)**
0000000000x	2	997.5	1300
00000000010	2	997.5	1300
00000000011	3	665	866.7
00000000100	4	498.75	650
00000000101	5	399	520
0000000011x	6	332.5	433.3
0000000100x	8	249.4	325
0000000101x	10	199.5	260
...	Even N	1995 / N	2600 / N
1111111111x	2046	0.98	1.27

Frequency Synthesizer Mode

This mode of operation allows an arbitrary output frequency to be generated from a fundamental mode crystal input. For improved phase noise performance, the crystal input frequency may be doubled. As can be seen from the block diagram in *Figure 1,* only the upper feedback loop is used in this mode of operation. It is recommended that CLK0 and CLK1 be left unused in this mode of operation.

The upper feedback loop supports a delta-sigma fractional feedback divider. This allows the VCO operating frequency to be a non-integer multiple of the crystal frequency. By using an integer multiple only, lower phase noise jitter on the output can be achieved, however the use of the delta-sigma divider logic will provide excellent performance on the output if a fractional divisor is used.

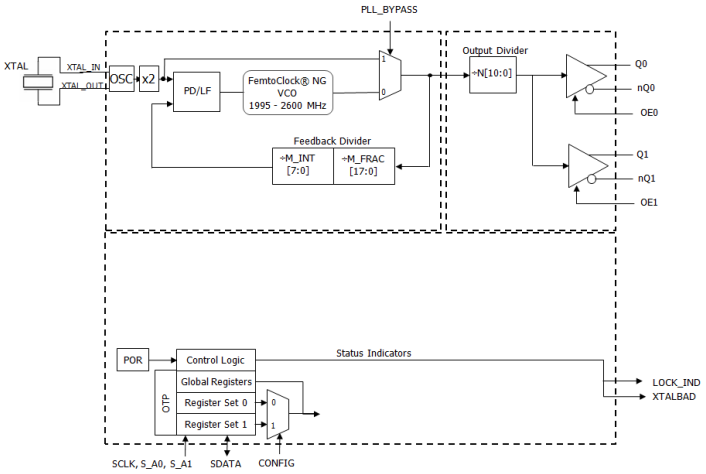


Figure 1. Frequency Synthesizer Mode Block Diagram

High-Bandwidth Frequency Translator Mode

This mode of operation is used to translate one of two input clocks of the same nominal frequency into an output frequency with little jitter attenuation. As can be seen from the block diagram in Figure 2, similarly to the Frequency Synthesizer mode, only the upper feedback loop is used.

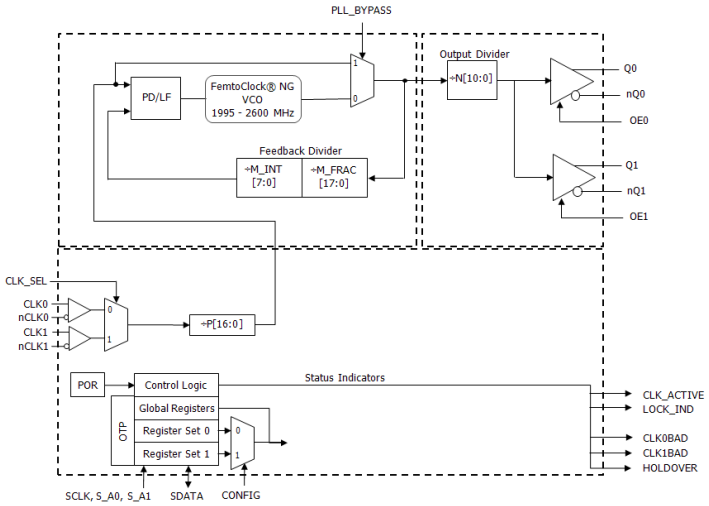


Figure 2. High Bandwidth Frequency Translator Mode Block Diagram

The input reference frequency range is now extended up to 710MHz. A pre-divider stage P is needed to keep the operating frequencies at the phase detector less than 100MHz.

Low-Bandwidth Frequency Translator Mode

As can be seen from the block diagram in Figure 3, this mode involves two PLL loops. The lower loop with the large integer dividers is the low bandwidth loop and it sets the output-to-input frequency translation ratio.This loop drives the upper DCXO loop (digitally controlled crystal oscillator) via an analog-digital converter.

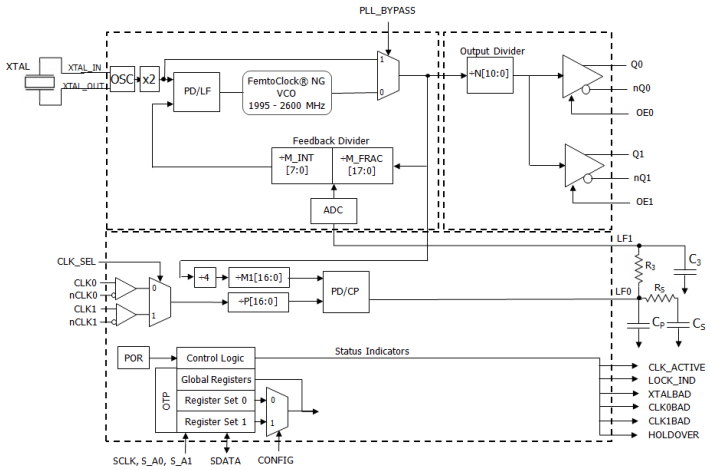


Figure 3. Low Bandwidth Frequency Translator Mode Block Diagram

The pre-divider stage is used to scale down the input frequency by an integer value to achieve a frequency in this range. By dividing down the fed-back VCO operating frequency by the integer divider M1[16:0] to as close as possible to the same frequency, exact output frequency translations can be achieved. For improved phase noise performance, the crystal input frequency may be doubled. The phase detector of the lower loop is designed to work with frequencies in the 8kHz - 16kHz range. For improved phase noise performance, the crystal input frequency may be doubled.

Alarm Conditions & Status Bits

The IDT8T49N205I monitors a number of conditions and reports their status via both output pins and register bits.

CLK_ACTIVE - indicates which input clock reference is being used to derive the output frequency.

LOCK_IND - This status is asserted on the pin & register bit when the PLL is locked to the appropriate input reference for the chosen mode of operation. The status bit will not assert until frequency lock has been achieved, but will de-assert once lock is lost.

XTALBAD - indicates if valid edges are being received on the crystal input.

CLK0BAD - indicates if valid edges are being received on the CLK0 reference input.

CLK1BAD - indicates if valid edges are being received on the CLK1 reference input. Behavior is as indicated for the CLK0BAD alarm, but with the CLK1 input being monitored and the CLK1BAD output pin & register bits being affected.

HOLDOVER - indicates that the device is not locked to a valid input reference clock. This can occur in Manual switchover mode if the selected reference input has gone bad, even if the other reference input is still good. In automatic mode, this will only assert if both input references are bad.

Input Reference Selection and Switching

When operating in Frequency Synthesizer mode, the CLK0 and CLK1 inputs are not used and the contents of this section do not apply. Except as noted below, when operating in either High or Low Bandwidth Frequency Translator mode, the contents of this section apply equally when in either of those modes.

Both input references CLK0 and CLK1 must be the same nominal frequency. These may be driven by any type of clock source, including crystal oscillator modules. A difference in frequency may cause the PLL to lose lock when switching between input references. Please contact IDT for the exact limits for your situation.

Manual Switching Mode

When set to Manual via Pin, then the IDT8T49N205I will use the CLK_SEL input pin to determine which input to use as a reference. Similarly, if set to Manual via Register, then the device will use the CLK_SEL register bit to determine the input reference. In either case, the PLL will lock to the selected reference if there is a valid clock present on that input.

If there is not a valid clock present on the selected input, the IDT8T49N205I will go into holdover or free-run state. In either case, the HOLDOVER alarm will be raised. This will occur even if there is a valid clock on the non-selected reference input. The device will recover from holdover / free-run state once a valid clock is re-established on the selected reference input.

The IDT8T49N205I will only switch input references on command from the user. The user must either change the CLK_SEL register bit (if in Manual via Register) or CLK_SEL input pin (if in Manual via Pin).

Automatic Switching Mode

When set to either of the automatic selection modes (Revertive or Non-Revertive), the IDT8T49N205I determines which input reference it prefers / starts from by the state of the CLK_SEL register bit only. The CLK_SEL input pin is not used in either Automatic switching mode.

Once the IDT8T49N205I has achieved a stable lock, it will remain locked to the preferred input reference as long as there is a valid clock on it. If at some point, that clock fails, then the device will automatically switch to the other input reference as long as there is a valid clock there. If there is not a valid clock on either input reference, the IDT8T49N205I will go into holdover or free-run state. In either case, the HOLDOVER alarm will be raised.

The device will recover from holdover / free-run state once a valid clock is re-established on either reference input. If clocks are valid on both input references, the device will choose the reference indicated by the CLK_SEL register bit.

If running from the non-preferred input reference and a valid clock returns, there is a difference in behavior between Revertive and Non-revertive modes. In Revertive mode, the device will switch back to the reference indicated by the CLK_SEL register bit even if there is still a valid clock on the non-preferred reference input. In Non-revertive mode, the IDT8T49N205I will not switch back as long as the non-preferred input reference still has a valid clock on it.

Switchover Behavior of the PLL

Even though the two input references have the same nominal frequency, there may be minor differences in frequency and potentially large differences in phase between them. The IDT8T49N205I has two options: Phase Build-Out or Phase-Slope Limiting to determine how it will adjust its output to the new input reference when operating in Low-Bandwidth mode. Only Phase-Slope limiting is available in High-Bandwidth mode.

In Phase Slope Limiting operation, the IDT8T49N205I will adjust the output phase at a fixed maximum rate until the output phase and frequency are now aligned to the new input reference. Phase will always be adjusted so that no unacceptably short clock periods are generated on the output of the IDT8T49N205I. Please contact IDT if more information on the maximum phase slope adjustment rate is needed.

In Phase Build-Out operation, the device will absorb most of the phase difference between the two inputs (or between the input and current VCO setting if recovering from holdover). Any phase difference that is not absorbed will be reflected on the output at the same maximum rate as in Phase Slope Limiting operation.

Holdover / Free-run Behavior

When both input references have failed (Automatic mode) or the selected input has failed (Manual mode), the IDT8T49N205I will enter holdover or free-run state.

If the device is programmed to perform Manual switching, once the selected input reference recovers, the IDT8T49N205I will switch back to that input reference. If programmed for either Automatic mode, the device will switch back to whichever input reference has a valid clock first.

The switchover that results from returning from holdover or free-run is handled in the same way as a switch between two valid input references as described in the previous section.

Output Configuration

The two outputs of the IDT8T49N205I both provide the same clock frequency. Both must operate from the same output voltage level of 3.3V or 2.5V, although this output voltage may be less than or equal to the core voltage (3.3V or 2.5V) the rest of the device is operating from. The output voltage level used on the two outputs is supplied on the V_{CCO} pin.

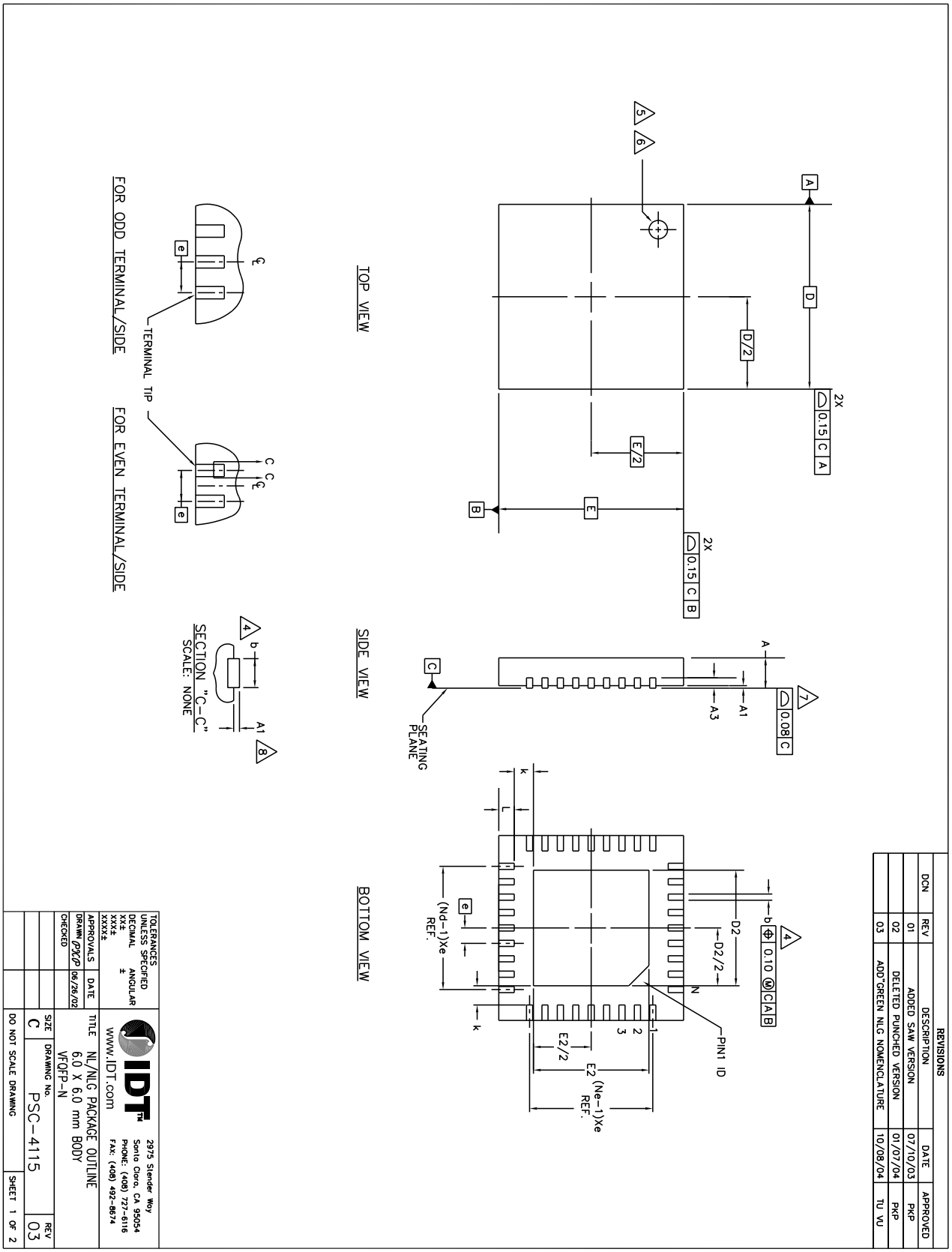
The two outputs are individually selectable as LVDS or LVPECL output types. These two selection bits are provided in each configuration to allow different output type settings under each configuration.

The two outputs can be enabled individually also via both register control bits and input pins. When both the OEn register bit and OEn pin are enabled, then the appropriate output is enabled. The OEn register bits default to enabled so that by default the outputs can be directly controlled by the input pins. Similarly, the input pins are provisioned with weak pull-ups so that if they are left unconnected, the output state can be directly controlled by the register bits. When the differential output is in the disabled state, it will show a high impedance condition.

Serial Interface Configuration Description

The IDT8T49N205I has an I^2C-compatible configuration interface to access any of the internal registers for frequency and PLL parameter programming. The IDT8T49N205I acts as a slave device on the I^2C bus and has the address 0b11011xx, where xx is set by the values on the S_A0 & S_A1 pins. The interface accepts byte-oriented block write and block read operations.

40 Lead VFQFN Package Outline and Package Dimensions



40 Lead VFQFN Package Outline and Package Dimensions, continued

SYMBOL	JEDEC VARIATION VJJC-3			NOTE
	MIN.	NOM.	MAX.	
e		0.65 BSC		
N		28		2
Nd		7		2
Ne		7		2
b	0.25	0.30	0.35	4
D2		–		10
E2		–		10

SYMBOL	JEDEC VARIATION VJJD-5			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		40		3
Nd		10		3
Ne		10		3
b	0.18	0.25	0.30	4
D2		–		10
E2		–		10

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.90	1.00	
A1	0.00	0.02	0.05	7
A3		0.20 REF.		
D		6.00 BSC		
E		6.00 BSC		
k	0.20	–	–	
L	0.35	0.40	0.45	

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. APPLIED TO EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY FOR TERMINALS.
9. THIS OUTLINES CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-220, VARIATION VJJC-3 & VJJD-5 WITH THE EXCEPTION OF D2 & E2.
10. DIMENSIONS D2 & E2 VARY DEPENDING ON DEVICE, SUPPLIER, ETC.

40 Lead VFQFN, D2/E2 EPAD Dimensions: 4.65mm x 4.65mm

REVISIONS			
DCN	REV	DESCRIPTION	DATE	APPROVED
	01	ADDED SAW VERSION	07/10/03	PKP
	02	DELETED PUNCHED VERSION	01/07/04	PKP
	03	ADD "GREEN" NLG NOMENCLATURE	10/08/04	TU VU

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APPROVALS	DATE	TITLE NL/NLG PACKAGE OUTLINE 6.0 X 6.0 mm BODY VFQFN-N	
DRAWN PKP	06/26/02		
CHECKED		SIZE C	DRAWING No. PSC-4115	REV 03
DO NOT SCALE DRAWING			SHEET 2 OF 2

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