LM321 Low Power Single Op Amp

Check for Samples: LM321

FEATURES

- **(V_{CC} = 5V, T_A = 25°C. Typical values unless specified.)**
- **Gain-Bandwidth Product 1MHz**
- **Low Supply Current 430µA**
- **Low Input Bias Current 45nA**
- **Wide Supply Voltage Range +3V to +32V**
- **Stable With High Capacitive Loads**
- **Single Version of LM324**

APPLICATIONS

- **Chargers**
- **Power Supplies**
- **Industrial: Controls, Instruments**
- **Desktops**
- **Communications Infrastructure**

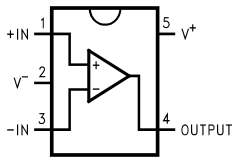
DESCRIPTION

The LM321 brings performance and economy to low power systems. With a high unity gain frequency and a specified 0.4V/µs slew rate, the quiescent current is only 430µA/amplifier (5V). The input common mode range includes ground and therefore the device is able to operate in single supply applications as well as in dual supply applications. It is also capable of comfortably driving large capacitive loads.

The LM321 is available in the SOT-23 package. Overall the LM321 is a low power, wide supply range performance op amp that can be designed into a wide range of applications at an economical price without sacrificing valuable board space.

Connection Diagram

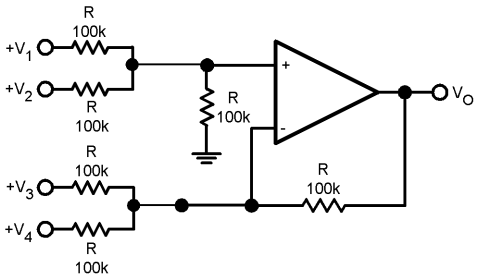
SOT-23



Top View

Application Circuit

DC Summing Amplifier
($V_{IN's}$ ≥ 0 V_{DC} and V_O ≥ V_{DC})



Where: $V_0 = V_1 + V_2 - V_3 - V_4$, $(V_1+V_2) \geq (V_3 + V_4)$ to keep $V_O > 0$ V_{DC}

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Differential Input Voltage	±Supply Voltage
Input Current (V_{IN} < −0.3V) (2)	50mA
Supply Voltage (V^+ - V^-)	32V
Input Voltage	−0.3V to +32V
Output Short Circuit to GND, V^+ ≤ 15V and T_A = 25°C (3)	Continuous
Storage Temperature Range	−65°C to 150°C
Junction Temperature (4)	150°C
Mounting Temperature	
Lead Temp (Soldering, 10 sec)	260°C
Infrared (10 sec)	215°C
Thermal Resistance to Ambient (θ_{JA})	265°C/W
ESD Tolerance (5)	300V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

(2) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.36V (at 25°C).

(3) Short circuits from the output V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground the maximum output current is approximately 40mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.

(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

(5) Human Body Model, 1.5kΩ in series with 100pF.

Operating Ratings (1)

Temperature Range	−40°C to 85°C
Supply Voltage	3V to 30V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

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Electrical Characteristics

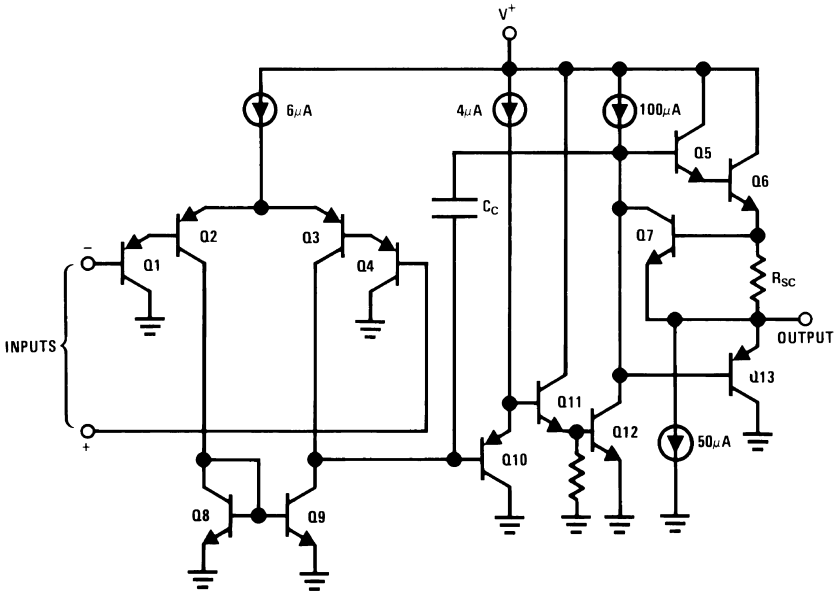
Unless otherwise specified, all limits specified for at T_A = 25°C; V^+ = 5V, V^- = 0V, V_O = 1.4V. **Boldface** limits apply at temperature extremes.

Symbol	Parameter		Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage		(3)		2	7 **9**	mV
I_{OS}	Input Offset Current				5	50 **150**	nA
I_B	Input Bias Current (4)				45	250 **500**	nA
V_{CM}	Input Common-Mode Voltage Range		V^+ = 30V (5) For CMRR > = 50dB	0		V^+ - 1.5 **V^+ -2**	V
A_V	Large Signal Voltage Gain		(V^+ = 15V, R_L = 2kΩ V_O = 1.4V to 11.4V)	25 **15**	100		V/mV
PSRR	Power Supply Rejection Ratio		R_S ≤ 10kΩ, V^+ ≤ 5V to 30V	65	100		dB
CMRR	Common Mode Rejection Ratio		R_S ≤ 10kΩ	65	85		dB
V_O	Output Swing	V_{OH}	V^+ = 30V, R_L = 2kΩ	**26**			V
			V^+ = 30V, R_L = 10kΩ	**27**	**28**		
		V_{OL}	V^+ = 5V, R_L = 10kΩ		**5**	**20**	mV
I_S	Supply Current, No Load		V^+ = 5V		0.430 **0.7**	1.15 **1.2**	mA
			V^+ = 30V		0.660 **1.5**	2.85 **3**	
I_{SOURCE}	Output Current Sourcing		V_{ID} = +1V, V^+ = 15V, V_O = 2V	20 **10**	40 **20**		mA
I_{SINK}	Output Current Sinking		V_{ID} = −1V V^+ = 15V, V_O = 2V	10 **5**	20 **8**		mA
			V_{ID} = −1V V^+ = 15V, V_O = 0.2V	12	100		µA
I_O	Output Short Circuit to Ground (6)		V^+ = 15V		40	85	mA
SR	Slew Rate		V^+ = 15V, R_L = 2kΩ, V_{IN} = 0.5 to 3V C_L = 100pF, Unity Gain		0.4		V/µs
GBW	Gain Bandwidth Product		V^+ = 30V, f = 100kHz, V_{IN} = 10mV, R_L =2kΩ, C_L = 100pF		1		MHz
φm	Phase Margin				60		deg
THD	Total Harmonic Distortion		f = 1kHz, A_V = 20dB R_L = 2kΩ, V_O = $2V_{PP}$, C_L = 100pF, V^+ = 30V		0.015		%
e_n	Equivalent Input Noise Voltage		f = 1kHz, R_S = 100Ω V^+ = 30V		40		$nV/\sqrt{Hz}$

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) V_O ≅ 1.4V, R_S = 0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+ - 1.5V) at 25°C.
(4) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
(5) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V^+ - 1.5V at 25°C, but either or both inputs can go to +32V without damage, independent of the magnitude of V^+.
(6) Short circuits from the output V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground the maximum output current is approximately 40mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.

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Simplified Schematic

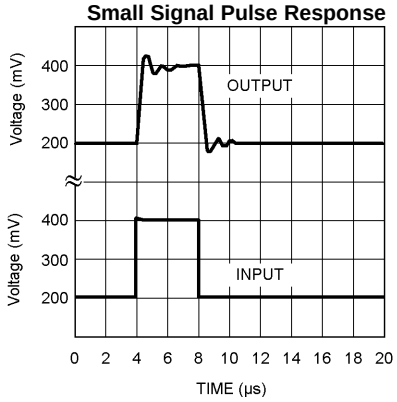


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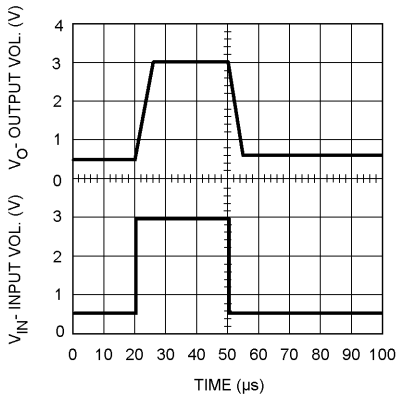
Typical Performance Characteristics

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

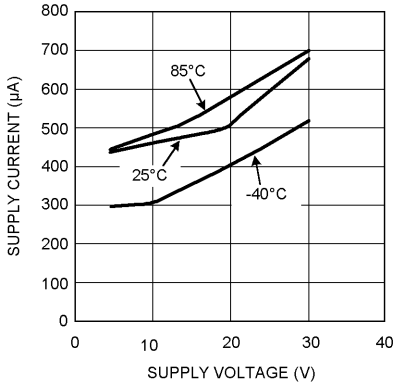
Small Signal Pulse Response



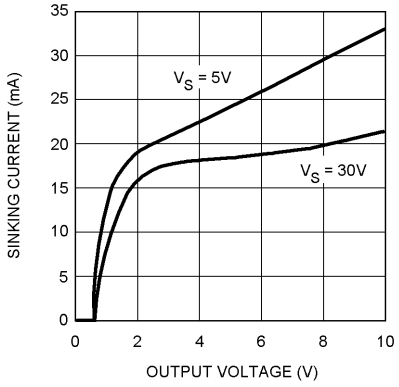
Large Signal Pulse Response



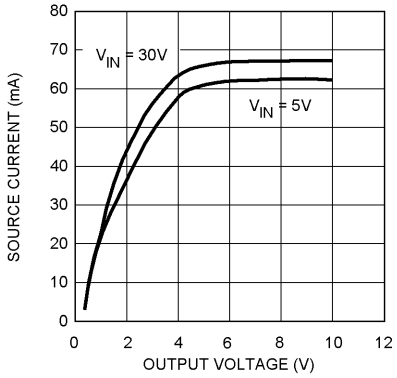
Supply Current vs. Supply Voltage



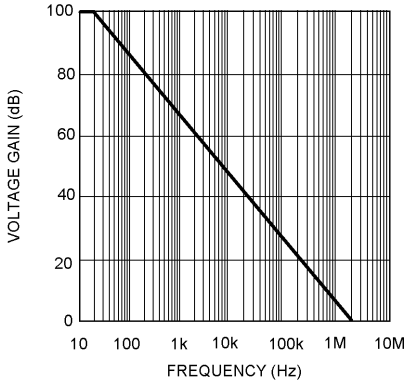
Sinking Current vs. Output Voltage



Source Current vs. Output Voltage



Open Loop Frequency Response



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APPLICATION HINTS

The LM321 op amp can operate with a single or dual power supply voltage, has true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. This amplifier operates over a wide range of power supply voltages, with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 3V.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C).An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply drain, the amplifier has a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For AC applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and to reduce distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if large load capacitance must be driven by the amplifier.

The bias network of the LM321 establishes a supply current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

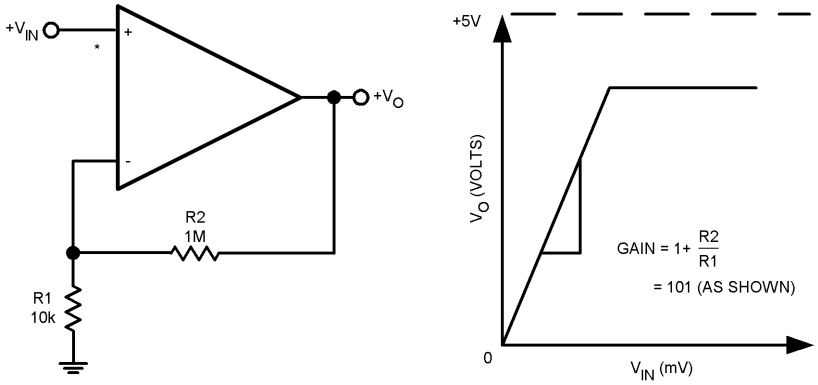
Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

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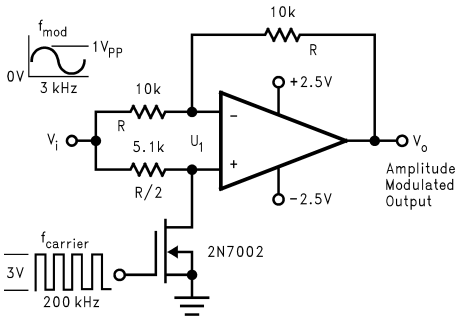
TYPICAL APPLICATIONS

Non-Inverting DC Gain (0V Input = 0V Output)

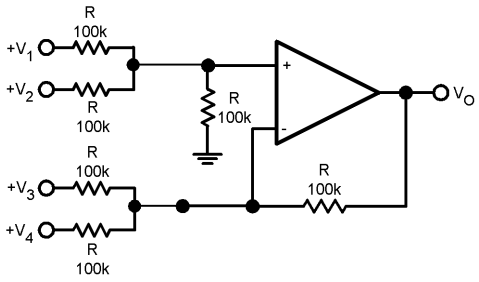


* R NOT NEEDED DUE TO TEMPERATURE INDEPENDENT I_{IN}

Amplitude Modulator Circuit

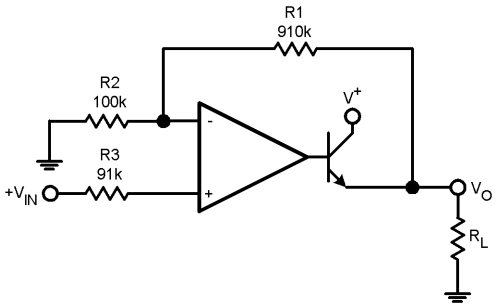


DC Summing Amplifier (V) ($V_{IN's} \geq 0\ V_{DC}$ and $V_O \geq V_{DC}$)



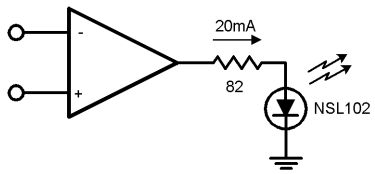
Where: $V_0 = V_1 + V_2 - V_3 - V_4$, $(V_1+V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

Power Amplifier

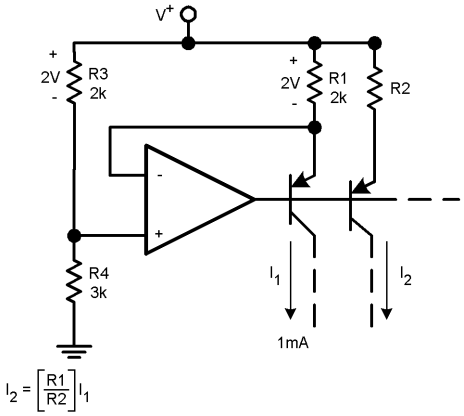


$V_0 = 0\ V_{DC}$ for $V_{IN} = 0\ V_{DC}$, $A_V = 10$

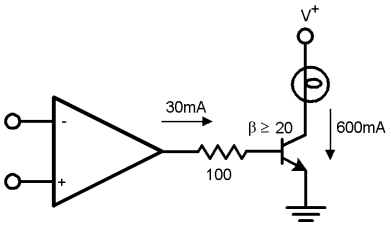
LED Driver



Fixed Current Sources



Lamp Driver



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REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	8

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM321MF	ACTIVE	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A63A	Samples
LM321MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A63A	Samples
LM321MFX	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	A63A	Samples
LM321MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A63A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

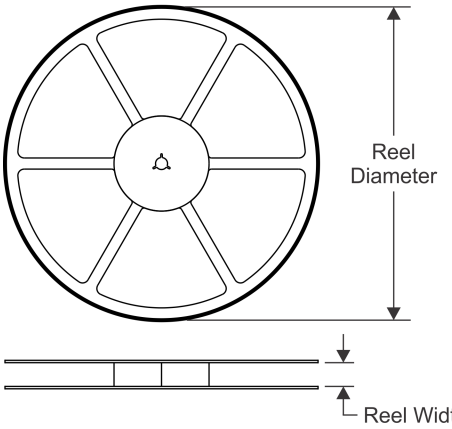
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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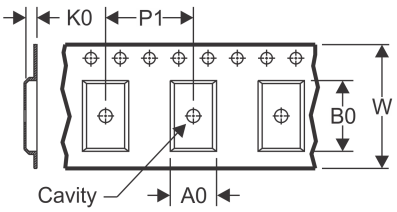
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

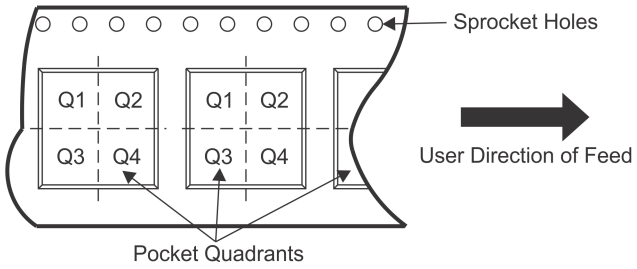


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

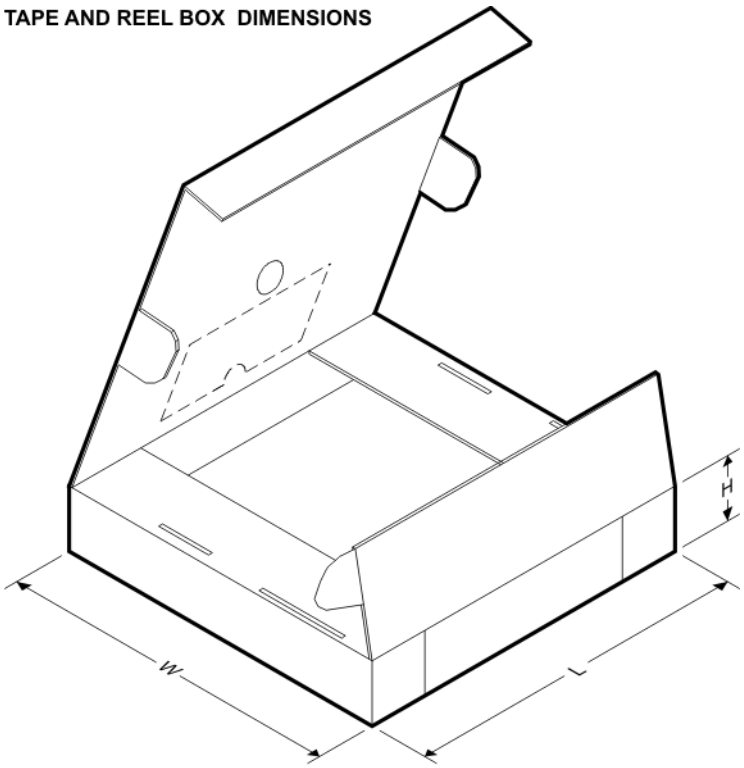
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM321MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM321MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM321MFX	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM321MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

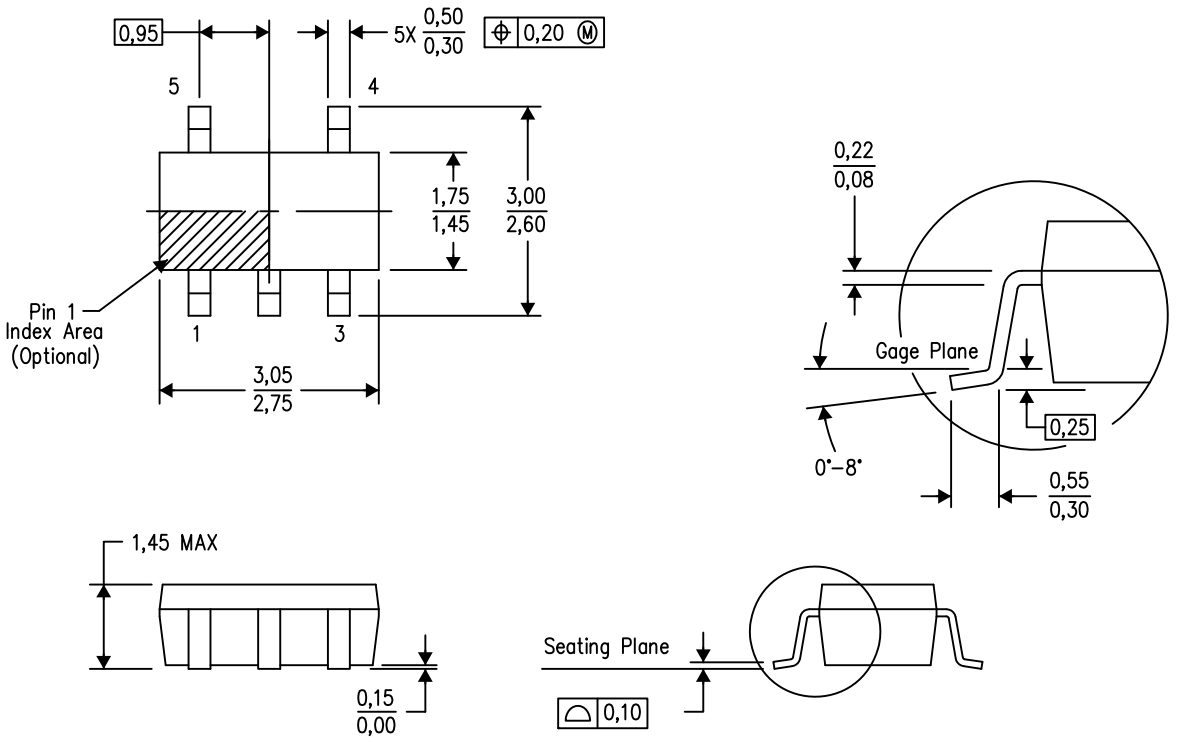
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM321MF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM321MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM321MFX	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM321MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

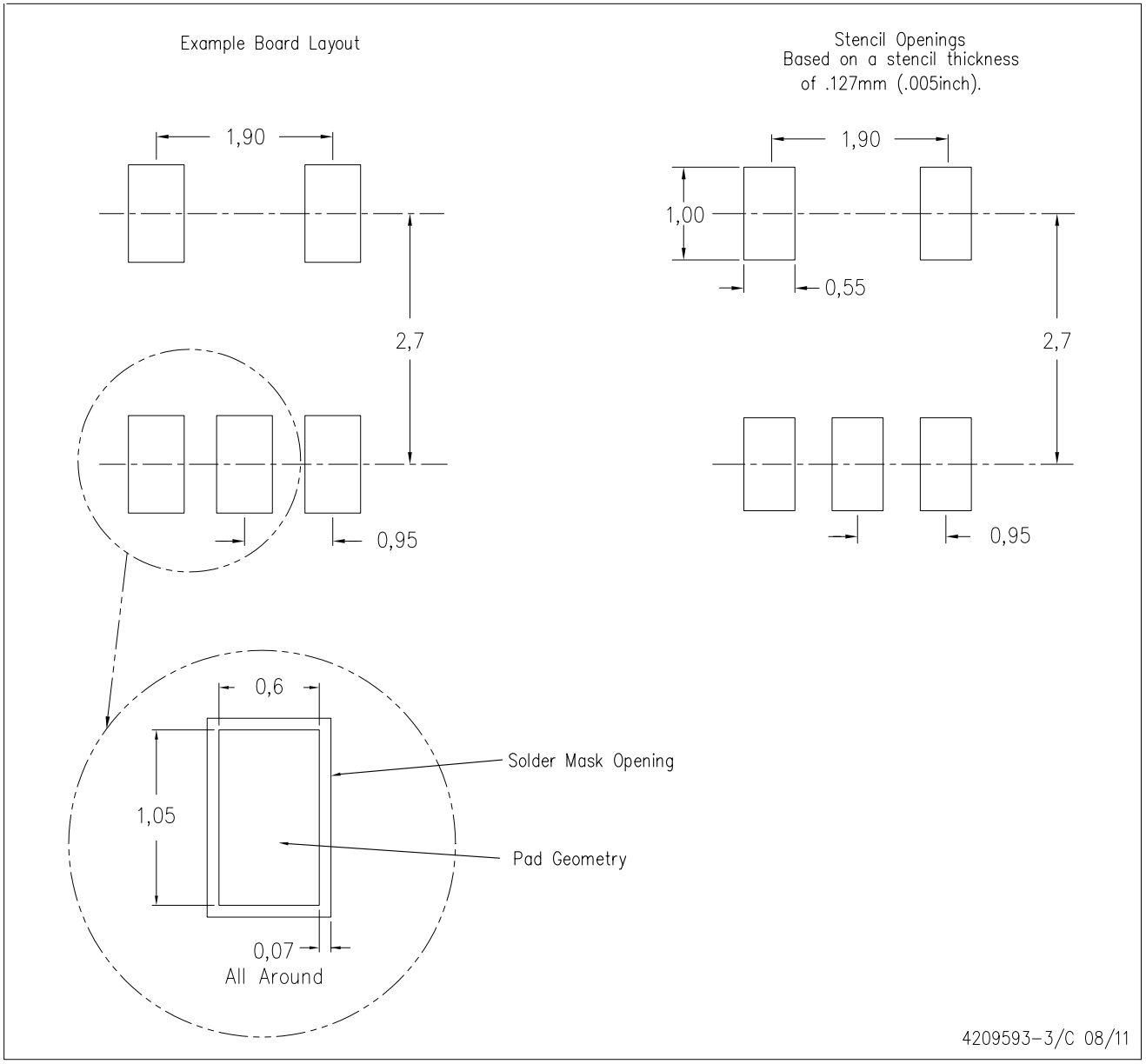
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/L 08/2013

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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