DATA SHEET

SKY73212-11: 1700-2000 MHz Diversity Downconversion Mixer with Integrated Integer-N PLL and VCO

Applications

- Cellular base station systems: GSM/EDGE, CDMA2000, WCDMA, TD-SCDMA
- Other wireless communication systems

Features

- RF frequency range: 1700 to 2000 MHz
- IF frequency range: 40 to 300 MHz
- Conversion gain: 9 dB
- IIP3: +24 dBm; OIP3: +33 dBm
- Noise Figure: 11 dB
- Integrated RF balun
- High linearity IF amplifier
- Integer-N frequency synthesizer
- Low phase-noise VCO
- Low RF output comparison spurs
- Programmable 18-bit N-counter and 11-bit R-counter
- Wide range of reference frequencies
- Programmable charge pump currents
- Flexible configuration that allows connection to an external VCO or PLL
- Digital lock detector
- Optional adjustment of the core, divider, and charge pump currents by external resistor
- Power supply for mixer: 5 V; power supply for synthesizer: 3.3 V
- Small, low-cost MCM (44-pin, 10 x 6 mm) SMT package (MSL3, 260 °C per JEDEC J-STD-020)

Skyworks Pb-free products are compliant with all applicable legislation. For additional information, refer to *Skyworks Definition of Lead (Pb)-Free*, document number SQ04-0073.

Description

Skyworks SKY73212-11 is a fully integrated diversity downconverter that includes a high linearity mixer, large dynamic range Intermediate Frequency (IF) amplifier, and a complete Voltage Controlled Oscillator (VCO), synthesizer, and Local Oscillator (LO) chain. Low loss RF baluns have also been included to reduce design complications and to lower system cost.

The SKY73212-11 features a 3rd Order Input Intercept Point (IIP3) of +24 dBm and a Noise Figure (NF) of 11 dB, which make the device an ideal solution for high dynamic range systems such as 2G/3G base station receivers.

The SKY73212-11 also includes a fully integrated wideband VCO/Integer-N frequency synthesizer. By applying internal VCO division, the output LO frequency can be set to the desired value while minimizing the phase noise.

The SKY73212-11 is controlled by a Serial Peripheral Interface (SPI) and is manufactured using a robust silicon BiCMOS process. The device has been designed for optimum long-term reliability. It is manufactured in a compact, 44-pin 10 x 6 mm Multi-Chip Module (MCM). A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

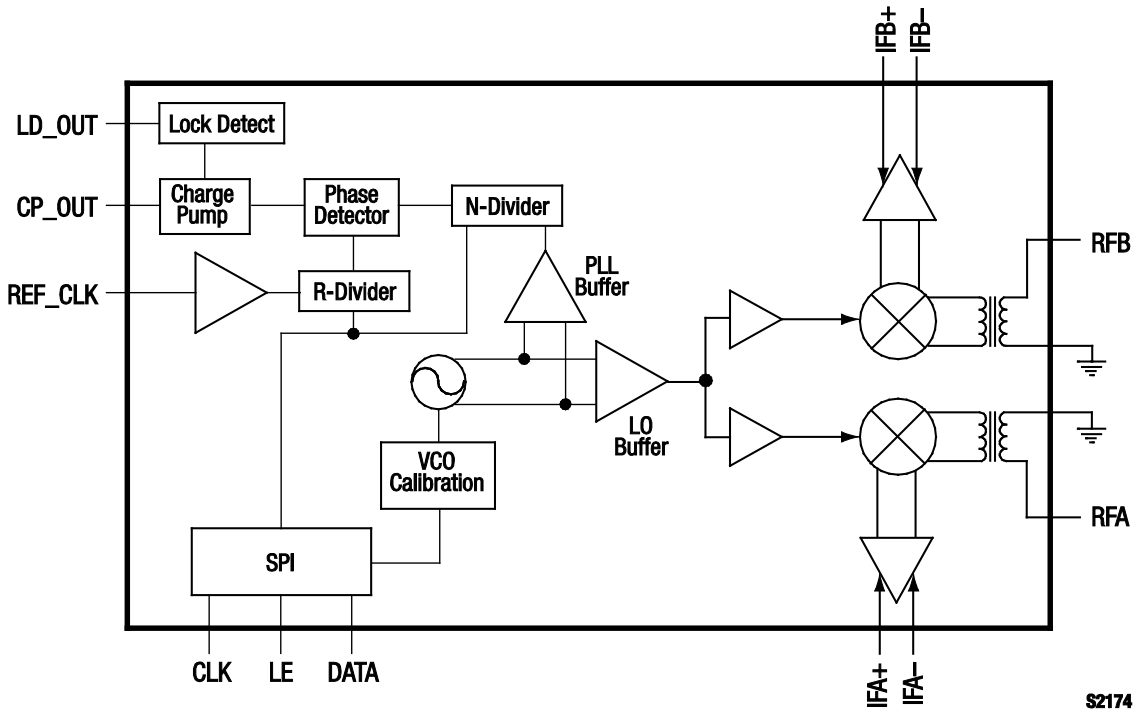


Figure 1. SKY73212-11 Block Diagram

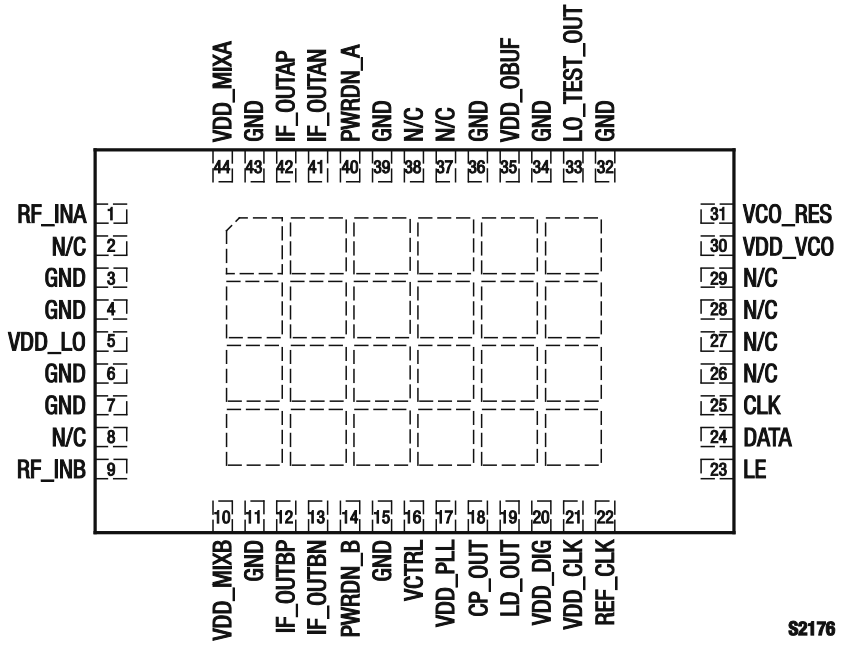


Figure 2. SKY73212-11 Pinout – 44-Pin MCM
(Top View)

Table 1. SKY73212-11 Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	RF_INA	RF input, channel A	23	LE	Latch enable input for the SPI
2	N/C	No connection	24	DATA	Data input for the SPI
3	GND	Ground	25	CLK	Clock input for the SPI
4	GND	Ground	26	N/C	No connection
5	VDD_LO	LO DC supply, +5 V	27	N/C	No connection
6	GND	Ground	28	N/C	No connection
7	GND	Ground	29	N/C	No connection
8	N/C	No connection	30	VDD_VCO	VCO supply, +3.3 V
9	RF_INB	RF input, channel B	31	VCO_RES	External resistor to set VCO bias
10	VDD_MIXB	Channel B mixer DC supply, +5 V	32	GND	Ground
11	GND	Ground	33	LO_TEST_OUT	LO test port
12	IF_OUTBP	Positive IF output, channel B	34	GND	Ground
13	IF_OUTBN	Negative IF output, channel B	35	VDD_OBUF	Dividers and LO buffer supply, +3.3 V
14	PWRDN_B	Mixer power down, channel B	36	GND	Ground
15	GND	Ground	37	N/C	No connection
16	VCTRL	VCO tuning voltage	38	N/C	No connection
17	VDD_PLL	PLL supply, +3.3 V	39	GND	Ground
18	CP_OUT	Charge pump output	40	PWRDN_A	Mixer power down, channel A
19	LD_OUT	Lock detect output	41	IF_OUTAN	Negative IF output, channel A
20	VDD_DIG	Supply for digital blocks, +3.3 V	42	IF_OUTAP	Positive IF output, channel A
21	VDD_CLK	Reference buffer supply, +3.3 V	43	GND	Ground
22	REF_CLK	Reference clock input	44	VDD_MIXA	Channel A mixer DC supply, +5 V

Functional Description

The SKY73212-11 is comprised of three main functional blocks:

- RF balun and passive mixer
- IF amplifier
- Synthesizer
- VCO
- VCO dividers and LO chain

RF Balun and Passive Mixer

The RF baluns provide a single ended input, which can easily be matched to 50 Ω using a simple external matching circuit. The RF baluns offer very low loss, and excellent amplitude and phase balance.

The high linearity SKY73212-11 integrates a passive, double balanced mixer that provides a very low conversion loss, and an excellent 3rd Order Input Insertion Point (IIP3).

Additionally, the balanced nature of the mixer provides for high port-to-port isolation.

LO Buffers

The LO section is optimized for low-side LO injection. The LO can be driven over a wide frequency range with only slight degradation in performance.

IF Amplifier

The SKY73212-11 includes high dynamic range IF amplifiers that follow the passive mixers in the signal path. The outputs require a supply voltage connection using inductive chokes. These choke inductors should be high-Q and have the ability to handle 200 mA or greater. A simple matching network allows the output ports to be matched to a balanced 200 Ω impedance.

The IF amplifiers are optimized for IF frequencies between 40 and 300 MHz. The IF amplifiers can be operated outside of this range, but with a slight degradation in performance.

Mixer Power Down

A power-down function for each IF amplifier and corresponding LO buffer is available in the SKY73212-11. The power-down function

is controlled through the PWRDN_A and PWRDN_B signals (pins 40 and 14, respectively):

PWRDN_A and PWRDN_B Input	Enable/Disable
High	Channels A/B disabled
Low	Channels A/B enabled

Synthesizer

The frequency synthesizer is composed of the R-divider, N-divider, phase detector, charge pump, and lock detector.

R-Divider

The 11-bit programmable R-divider divides the reference input frequency and generates the reference input for the phase detector. The R-divider range varies from 1 to $2^{11} - 1$(2047).

N-Divider

The N-divider consists of a selectable 16/17 or 32/33 prescaler, 13-bit main counter, and 5-bit swallow counter. The 18 bit N-divider ratio is calculated as:

$$N = P \times M - S$$

Where: P = Prescaler value
M = Main counter value
S = Swallow counter value

The N-divider range is from P^2 to $2^{18} - 1$. For a 32/33 prescaler, the N-divider range varies from 1024 to 262143.

Phase Detector

The phase detector is an edge-controlled digital circuit. The circuit has two inputs: the reference signal (*Ref*) and the N-divider output. There are two digital outputs (*Up* and *Dn*) that drive the charge pump.

When the input phase difference is positive, the *Up* output is pulled up to VDD. When the input phase difference is negative, the *Dn* output is pulled down to ground. This type of phase detector acts only on the positive edges of the input signals.

Charge Pump

The charge pump is used to convert the logic levels of the *Up* and *Dn* pulses, carrying the phase error between the reference and the divided signal into analog quantities/current pulses.

The output of the SKY73212-11 charge pump is programmable and varies between 1.2 mA and 7.2 mA. Additional adjustment of the charge pump current can be accomplished by changing the value of the external PLL bias resistor.

Lock Detector

The lock detector circuit is activated when the phase difference between the *Up* and *Dn* phase detector signals for a given number of comparison cycles is shorter than a fixed delay. The CMOS output is active high when the loop is locked. The lock detector can be monitored from pin 19 (LD_OUT).

VCO

The VCO is designed to generate the LO signal with the tuning function controlled by the synthesizer.

VCO Dividers and LO Chain

The divider chain consists of dividers and LO drivers. The LO section is optimized for low-side LO injection at an RF frequency of 1700 to 2000 MHz.

Digital Interface

A three-wire SPI provides mode and bias control, and control of the PLL. The serial interface consists of three signals: the bus clock (CLK), latch enable (LE), and the serial data line (DATA).

A write data stream consists of 25 bits:

Bits[15:0] provide the 16-bit data block.

Bits[20:16] provide the register address.

Bits[24:21] provide the device address (the SKY73212-11 is 0110b).

A timing diagram for the SPI write cycle is shown in Figure 3.

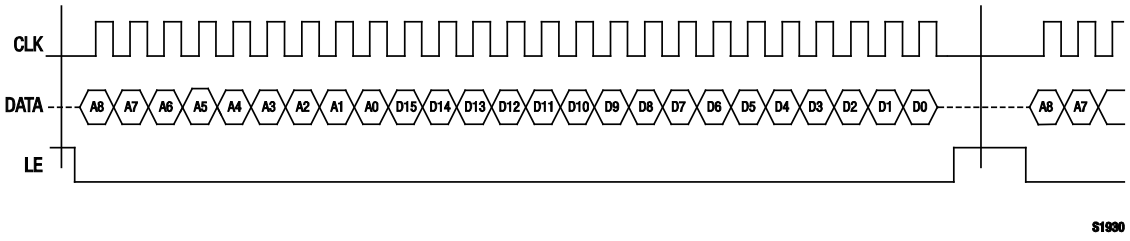


Figure 3. SPI Write Cycles

Serial Bus Timing

The SPI bus speed is programmable. Timing requirements for the CLK, DATA, and LE signals are provided in Table 2. A serial data input timing diagram is shown in Figure 4.

PLL Control Registers (R-Divider and N-Divider)

There are three digital PLL control registers that are used to store the R-divider and N-divider values: R_DIV, N_DIV1, and N_DIV2. By default, all registers are 25 bits wide. Bits[20:16] are the address bits of the registers. The 16 least significant bits (LSBs) represent the data bits.

Three values are needed to calculate the three PLL dividers: the desired frequency (F_{RF}), the VCO divider (D), and the frequency step size (F_{STEP}).

The VCO frequency (F_{VCO}) has a range of 2.7 GHz to 4.0 GHz, and is defined by the product of the desired frequency (F_{RF}) and the VCO divider, D:

$$F_{VCO} = F_{RF} \times D \quad (1)$$

The VCO divider (equal to 1, 2, 3, 4, or 8) is chosen so that the product of $F_{RF} \times D$ is within the specified VCO range.

Table 2. SPI Timing Requirements

Timing	Description	Minimum Time (ns)
t_{period}	Clock period	25
t_{high}	Clock high time	10
t_{su}	Data setup to clock rise	5
t_{hld}	Data hold from clock rise	5
t_{elch}	Enable low to clock rise	10
t_{width}	Enable high width	10
t_{efeh}	Clock fall to enable high	20

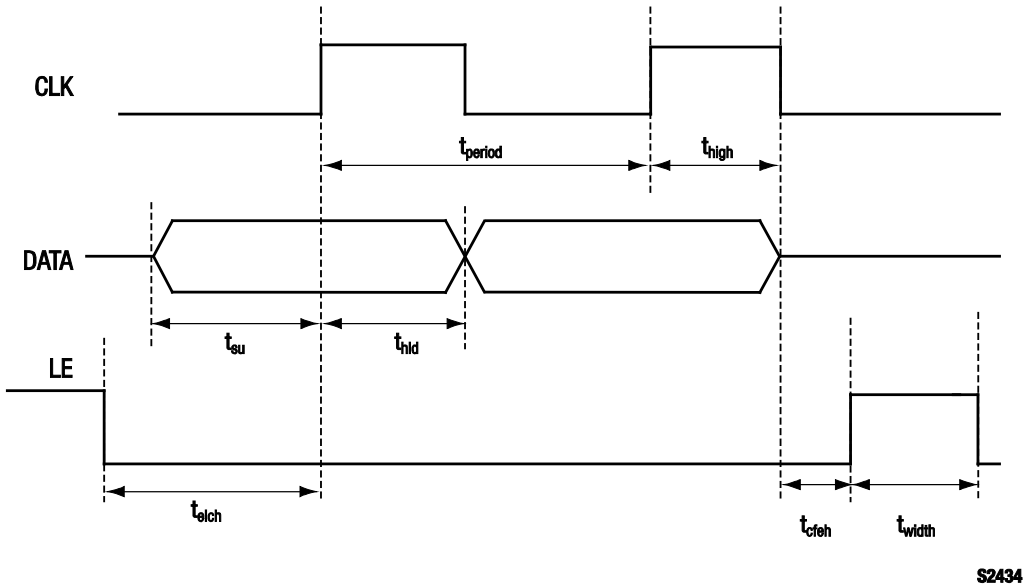


Figure 4. SPI Input Timing Diagram

The frequency step size (F_{STEP}) is a user-defined value. Given F_{STEP} and D, the comparison frequency (F_{COMP}) can be calculated by:

$$F_{COMP} = F_{STEP} \times D \quad (2)$$

The R_DIV register stores the value of the 16-bit R-divider that produces the desired comparison frequency (F_{COMP}) for the RF PLL according to the following equation:

$$R = \frac{F_{REF}}{F_{COMP}} \quad (3)$$

Where F_{REF} is the reference frequency provided to the device.

The N_DIV1 and N_DIV2 registers store the value of the N-divider according to the following equation:

$$N = \frac{F_{VCO}}{F_{REF}} \times R \quad (4)$$

Bits[1:0] of the N_DIV2 register are the most significant bits (MSBs) of the 18-bit representation of the N number.

Bits[15:0] of the N_DIV1 register are the LSBs of the 18-bit binary representation of the N number.

The calculated R-divider and N-divider values are programmed into the SKY73212-11 using the SPI interface.

Example:

A desired RF output frequency of 1800 MHz is required using a reference frequency of 76.8 MHz and a desired frequency step size of 400 kHz. If the VCO divider is equal to 2, the VCO frequency is 3600 MHz from Equation 1 and the comparison frequency is equal to 800 kHz from Equation 2.

From Equations 3 and 4, the R and N values become:

R = 96 = 1100000b

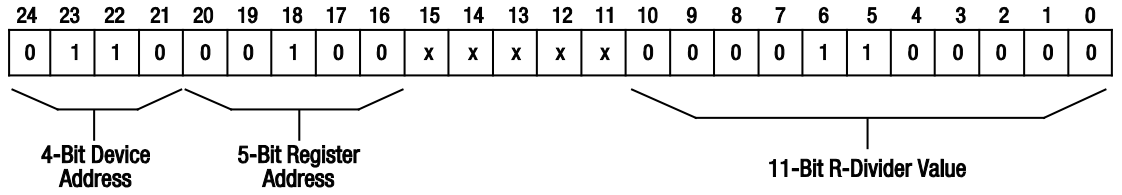
N = 4500 = 1000110010100b

These values would be programmed through the SPI interface.

Figure 5 represents the bits of the R_DIV register with the value of R = 96. Figures 6 and 7 represent the bits of the N_DIV1 and N_DIV2 registers, respectively, with the value of N = 4500.

Electrical and Mechanical Specifications

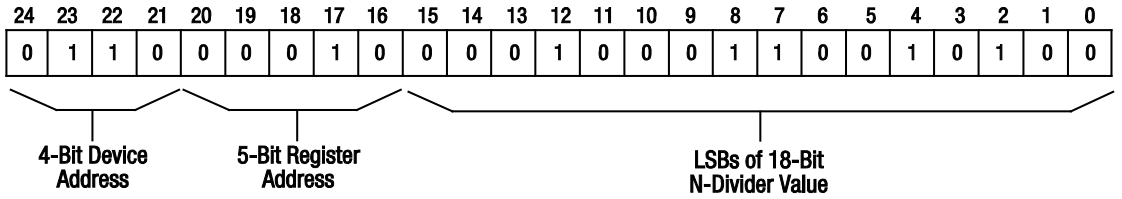
The absolute maximum ratings of the SKY73212-11 are provided in Table 3. The recommended operating conditions are specified in Table 4 and electrical specifications are provided in Table 5.



Note: Value of bits [15:11] can vary. Refer to the *Skyworks Wideband, Integer-N Phase-Locked Loop* Programming Guide, document number 201322.

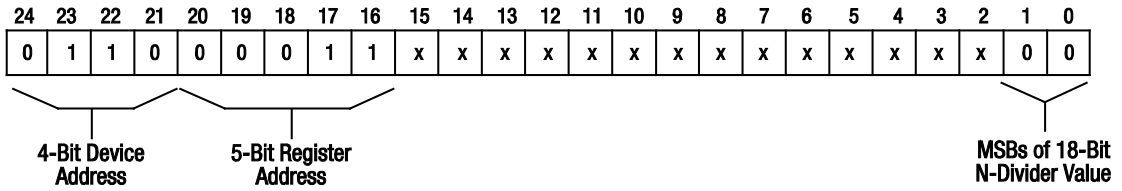
S1847b

Figure 5. R_DIV Register Showing an R-Divider Value of 96



S1849c

Figure 6. N_DIV1 Register Showing an N-Divider Value of 4500 (LSBs)



Note: Value of bits [15:2] can vary. Refer to the *Skyworks Wideband, Integer-N Phase-Locked Loop* Programming Guide, document number 201322. S1848b

Figure 7. N_DIV2 Register Showing an N-Divider Value of 4500 (MSBs)

Table 3. SKY73212-11 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Mixer supply voltage (VDD_MIXA, VDD_MIXB, VDD_LO pins)	V_{DD_5V}	4.5	5.0	5.5	V
Synthesizer supply voltage (VDD_VCO, VDD_OBUF, VDD_PLL, VDD_CLK, and VDD_DIG pins)	$V_{DD\_3.3V}$		3.3	3.6	V
Supply current: Mixer supply Synthesizer supply	 I_{DD_5V} $I_{DD\_3.3V}$			 440 150	 mA mA
RF input power	P_{IN}			+20	dBm
Operating case temperature	T_C	–40		+85	°C
Junction temperature	T_J			+150	°C
Storage case temperature	T_{STG}	–40		+125	°C

Notes: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***CAUTION**: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 4. SKY73212-11 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Mixer supply voltage (VDD_MIXA, VDD_MIXB, VDD_LO pins)	V_{DD_5V}	4.75	5.00	5.25	V
Synthesizer supply voltage (VDD_VCO, VDD_OBUF, VDD_PLL, VDD_CLK, and VDD_DIG pins)	$V_{DD\_3.3V}$	3.0	3.3	3.6	V
RF frequency range	f_{RF}	1700		2000	MHz
IF frequency range	f_{IF}	40		300	MHz
Supply current: Mixer supply Synthesizer supply	 I_{DD_5V} $I_{DD\_3.3V}$		 360 125	 400 140	 mA mA
Operating case temperature	T_C	–40		+85	°C
SPI logic levels (CLK, DATA, LE): Low High	 V_{IL} V_{IH}	 0.8 x $V_{DD\_3.3V}$		 0.2 x $V_{DD\_3.3V}$	 V V

Table 5. SKY73212-11 Electrical Specifications (1 of 2) (Note 1)
(V_{DD_5V} = +5 V, $V_{DD\_3.3V}$ = +3.3 V, T_C = +25 °C, RF Frequency = 1950 MHz, IF Frequency = 150 MHz, LO Frequency = 1800 MHz, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Mixer						
Conversion gain	G	f_{RF} = 1920 to 1980 MHz, V_{DD_5V} = 4.75 to 5.25 V, $V_{DD\_3.3V}$ = 3.0 to 3.6 V	7.5	8.5		dB
Gain variation over temperature		T_C = –40 to +85 °C		±0.7		dB
Noise Figure	NF	f_{RF} = 1920 to 1980 MHz, V_{DD_5V} = 4.75 to 5.25 V, $V_{DD\_3.3V}$ = 3.0 to 3.6 V		11	13	dB
Noise Figure variation over temperature		T_C = –40 to +85 °C		±1.0		dB
3rd order input intercept point	IIP3	f_{RF} = 1920 to 1980 MHz, P_{IN} = –10 dBm, 800 kHz tone spacing, V_{DD_5V} = 4.75 to 5.25 V, $V_{DD\_3.3V}$ = 3.0 to 3.6 V	+21.5	+24.0		dBm
IIP3 variation over temperature		T_C = –40 to +85 °C		±1.0		dB
Third order output intercept point	OIP3	f_{RF} = 1920 to 1980 MHz, P_{IN} = –10 dBm, 800 kHz tone spacing, V_{DD_5V} = 4.75 to 5.25 V, $V_{DD\_3.3V}$ = 3.0 to 3.6 V	+29.5	+33.0		dBm
2RF – 2LO	2x2	P_{IN} = –10 dBm		–65	–50	dBc
3RF – 3LO	3x3	P_{IN} = –10 dBm		–75	–67	dBc
1 dB Input Compression Point	IP1dB	f_{RF} = 1920 to 1980 MHz, V_{DD_5V} = 4.75 to 5.25 V, $V_{DD\_3.3V}$ = 3.0 to 3.6 V	+10	+13		dBm
1 dB Output Compression Point	OP1dB	f_{RF} = 1920 to 1980 MHz, V_{DD_5V} = 4.75 to 5.25 V, $V_{DD\_3.3V}$ = 3.0 to 3.6 V	+19.0	+20.5		dBm
Channel-to-channel isolation			50			dB
RF-to-IF isolation			30			dB
LO leakage @ RF port @ IF port					 –27 –45	 dBm dBm
Input return loss: RF port IF port	 Z_{IN_RF} Z_{IN_IF}	With external matching components		 –12 –12	 –7 –7	 dB dB

Table 5. SKY73212-11 Electrical Specifications (2 of 2) (Note 1)
(V_{DD_5v} = +5 V, $V_{DD\_3.3v}$ = +3.3 V, T_C = +25 °C, RF Frequency = 1950 MHz, IF Frequency = 150 MHz, LO Frequency = 1800 MHz, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Synthesizer						
Reference input frequency	f_{REF}		10.0	153.6	200.0	MHz
Reference input sensitivity			0.2	1.5		Vp-p
Charge pump current	I_{CP}		1.2	4.8	7.2	mA
Comparison spurs				–70	–66	dBc
Locking time		20 kHz bandwidth, 1 ppm frequency error			1	ms
Phase noise		@ 100 kHz @ 1 MHz @ 10 MHz		–100 –133 –150	–83 –128 –145	dBc/Hz dBc/Hz dBc/Hz
RMS phase error				0.9	1.1	deg

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Evaluation Board Description

The SKY73212-11 Evaluation Board is used to test the performance of the SKY73212-11 mixer. An Evaluation Board schematic diagram is provided in Figure 8. An assembly drawing for the Evaluation Board is shown in Figure 9 and the layer detail is provided in Figure 10.

Circuit Design Configurations

The following design considerations are general in nature and must be followed regardless of final use or configuration:

1. Paths to ground should be made as short as possible.
2. The ground pad of the SKY73212-11 has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Since the circuit board acts as the heat sink, it must shunt as much heat as possible from the device. Therefore, design the connection to the ground pad to dissipate the maximum wattage produced by the circuit board.
3. Skyworks recommends including external bypass capacitors on the V_{DD} voltage inputs of the device.

Package Dimensions

The PCB layout footprint for the SKY73212-11 is provided in Figure 11. Figure 12 shows the package dimensions for the 48-pin MCM and Figure 13 provides the tape and reel dimensions.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

THE SKY73212-11 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *PCB Design & SMT Assembly/Rework Guidelines for MCM-L Packages*, document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

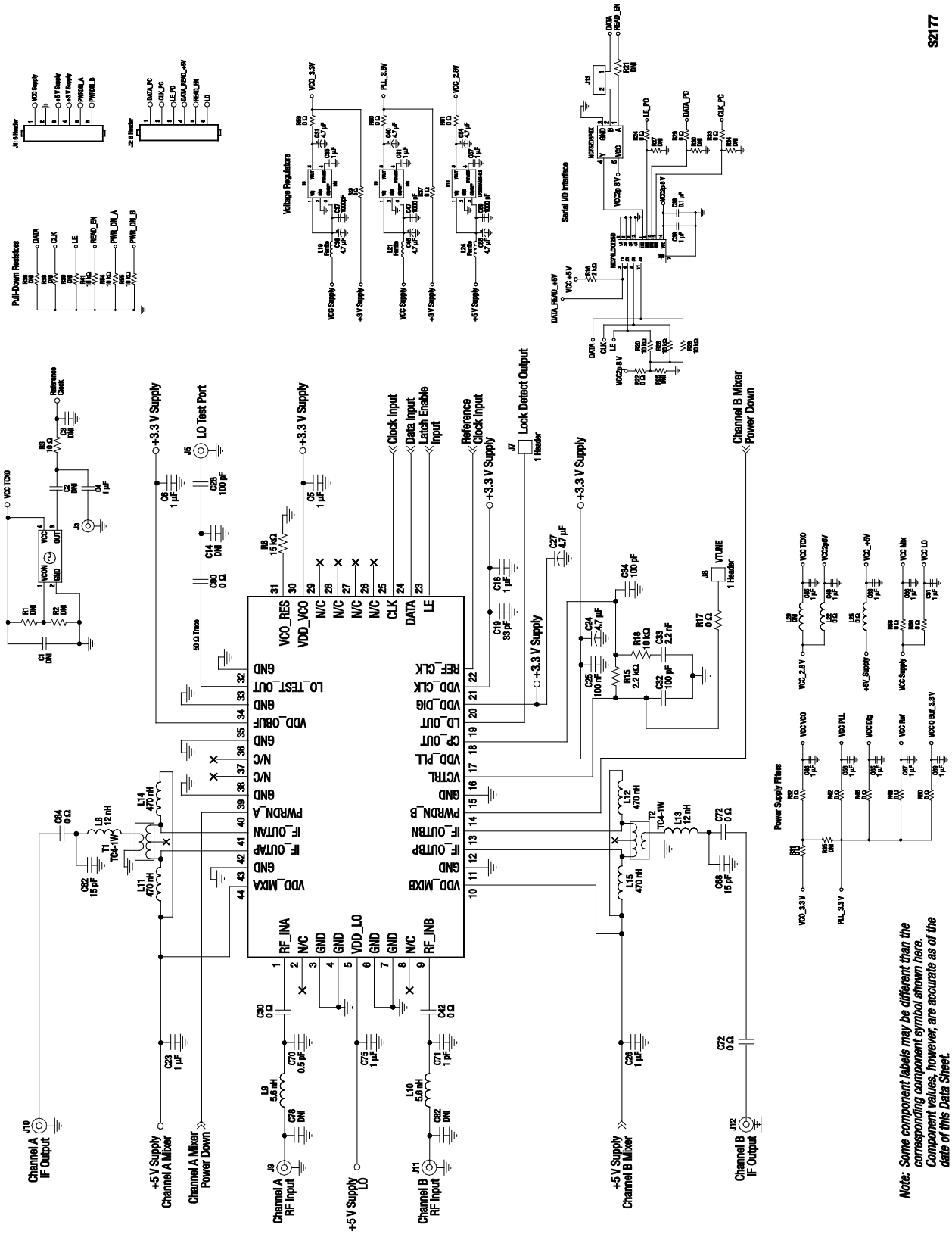


Figure 8. SKY73212-11 Evaluation Board Schematic

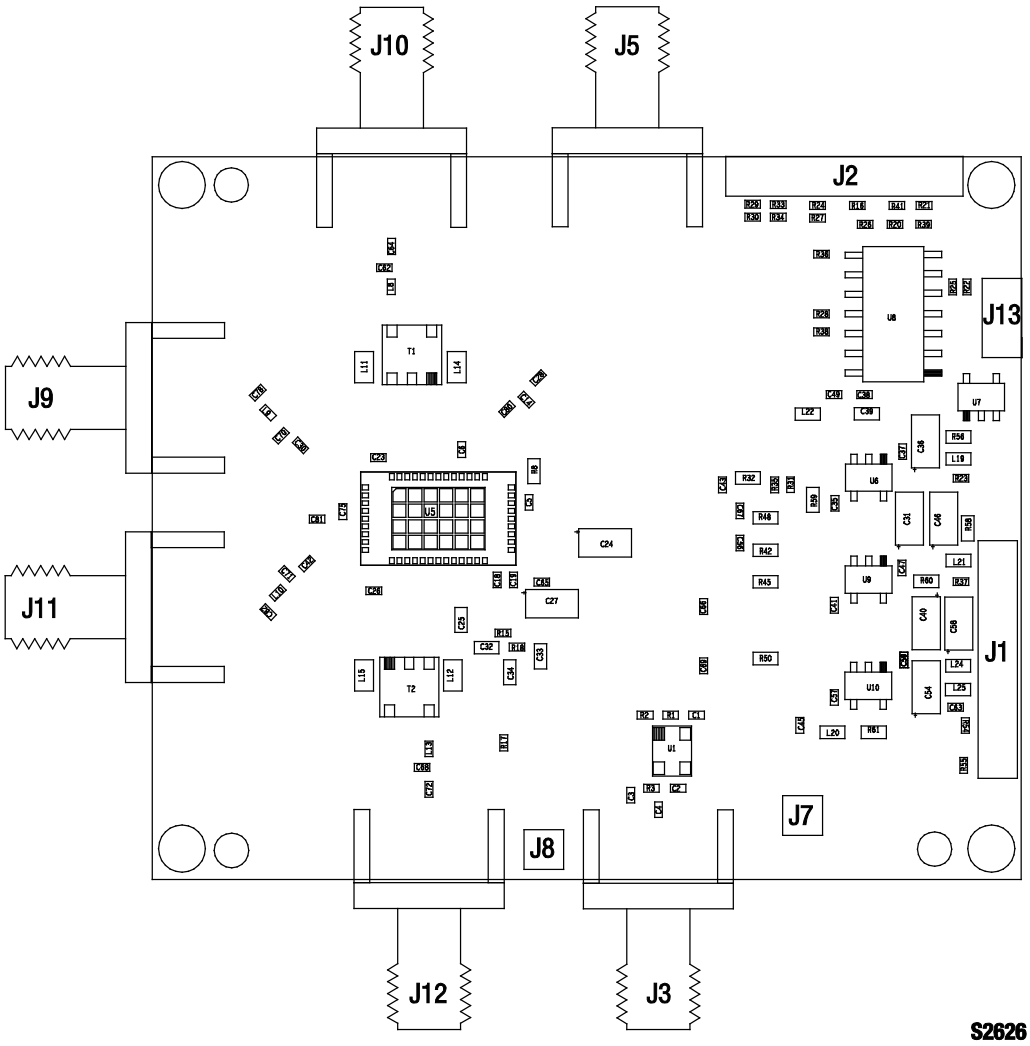
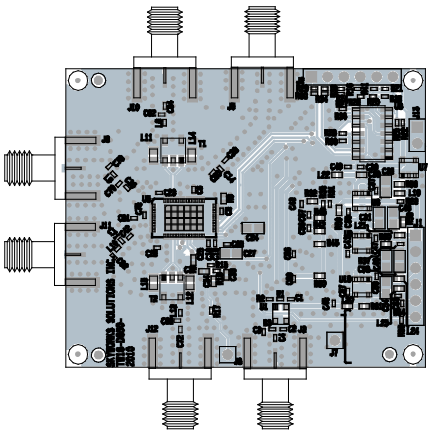
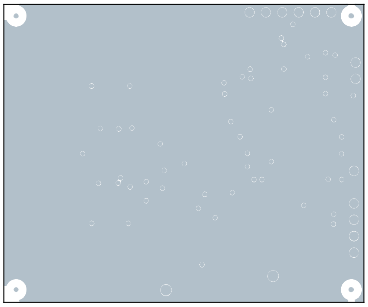


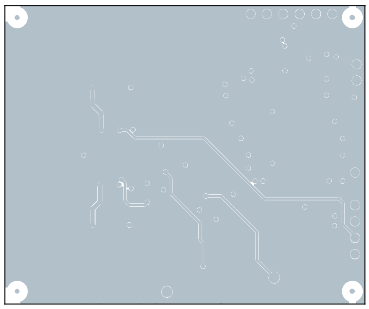
Figure 9. SKY73212-11 Evaluation Board Assembly Drawing



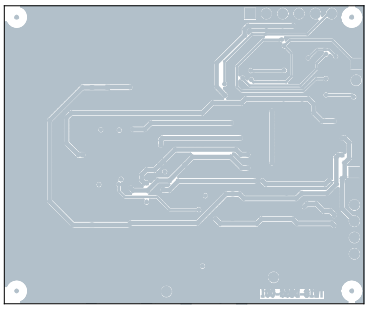
Layer 1: Top – Metal



Layer 2: Ground



Layer 3: Power Plane



Layer 4: Solid Ground Plane

S2627

Figure 10. SKY73212-11 Evaluation Board Layer Detail

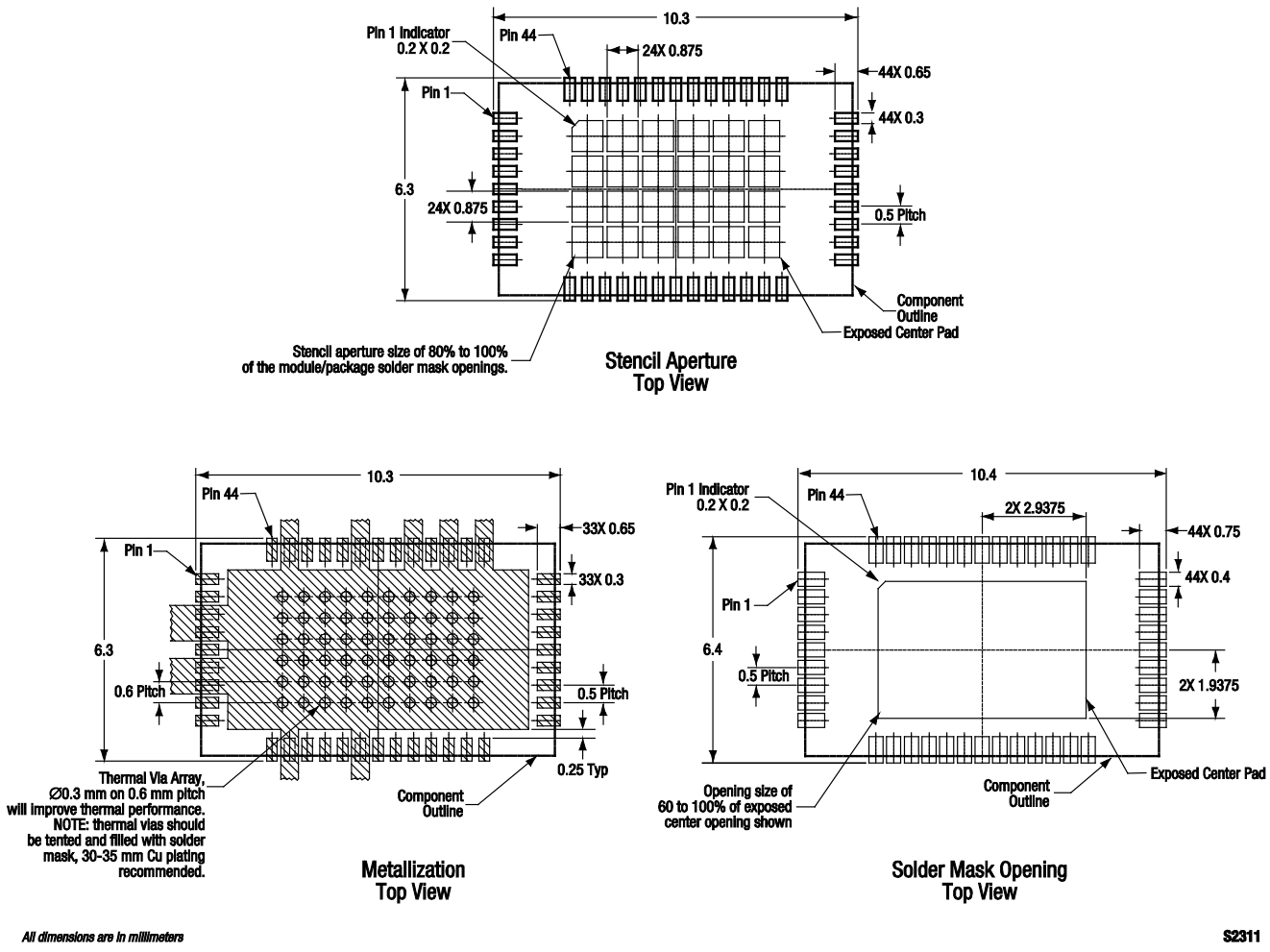


Figure 11. SKY73212-11 PCB Layout Footprint

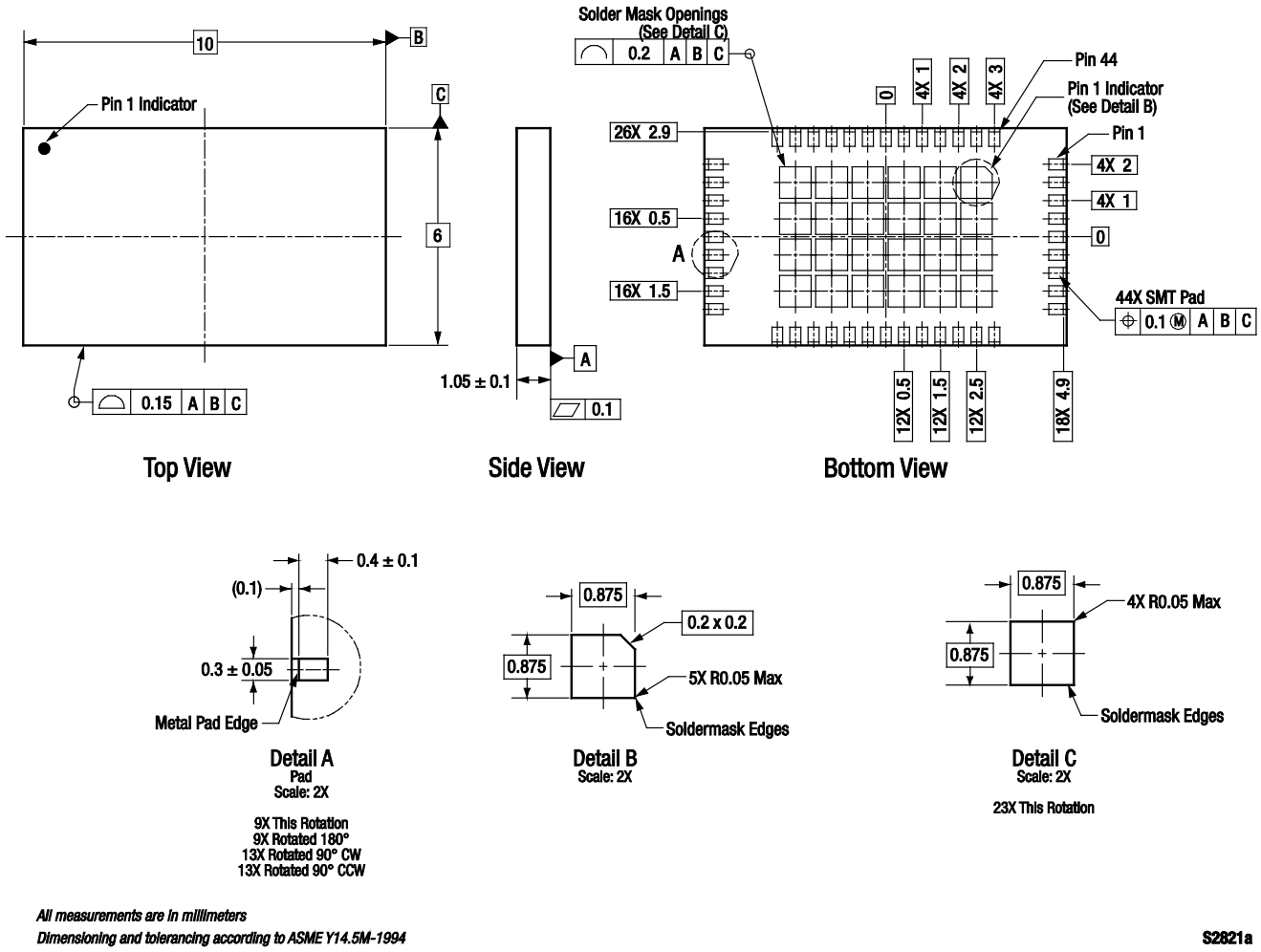
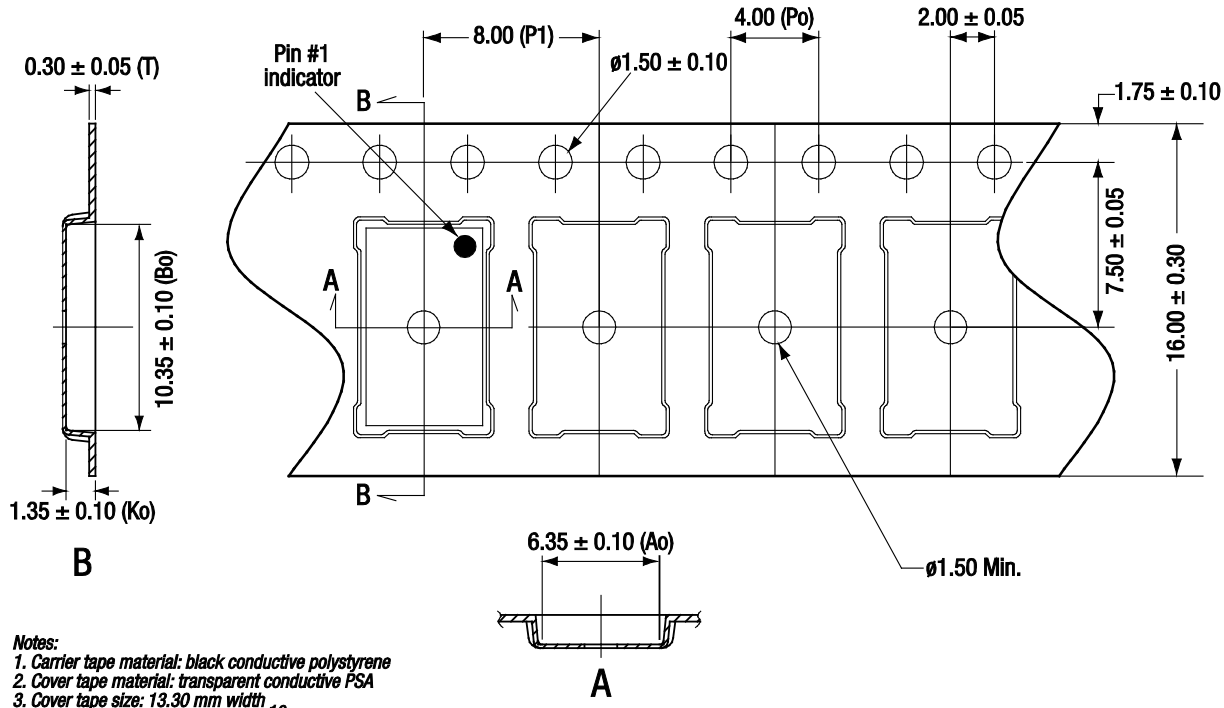


Figure 12. SKY73212-11 44-Pin MCM Package Dimensions



Notes:
1. Carrier tape material: black conductive polystyrene
2. Cover tape material: transparent conductive PSA
3. Cover tape size: 13.30 mm width
4. ESD surface resistivity is ≤1 x 10^{10} Ohms/square per EIA, JEDEC tape and reel specification.
5. Po/P1, 10 pitches cumulative tolerance on tape: ±0.20 mm.
6. Ao and Bo measurement point is 0.30 mm from bottom pocket.
7. All measurements are in millimeters

S2691

Figure 13. SKY73212-11 Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY73212-11 1700-2000 MHz Diversity Downconversion Mixer with PLL and VCO	SKY73212-11	TW18-D855-001