

MAX96708

14-Bit GMSL Deserializer with Coax or STP Cable Input

General Description

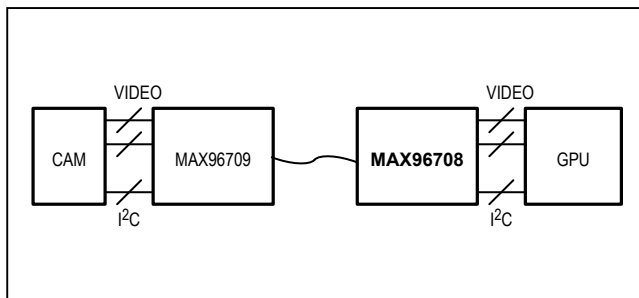
The MAX96708 is a compact deserializer especially suited for automotive camera applications. Features include adaptive equalization and an output crosspoint switch. An embedded control channel operates at 9.6kbps to 1Mbps in UART, I²C, and mixed UART/I²C modes, allowing programming of serializer, deserializer (SerDes), and camera registers, independent of video timing.

The deserializer can track data from a spread-spectrum serial input. The serial input meets ISO 10605 and IEC 61000-4-2 ESD standards. The core supply range is 1.7V to 1.9V and the I/O supply range is 1.7V to 3.6V. The device is available in a 32-pin (5mm x 5mm) TQFN package with 0.5mm lead pitch and operates over -40°C to +115°C temperature range.

Applications

- Automotive Camera Applications

Simplified Block Diagram



[Ordering Information](#) appears at end of data sheet.

Benefits and Features

- Ideal for Safety Camera Applications
 - Works with Low-Cost 50Ω Coax (100Ω STP) Cable
 - Error Detection of Video/Control Data
 - High-Immunity Mode for Robust Control-Channel EMC Tolerance
 - Best-in-Class Supply Current: 185mA (max)
 - Adaptive Equalization for 15m Cable at Full Speed
 - 32-Pin (5mm x 5mm) TQFN Package
 - Horizontal- and Vertical-Sync Encoding and Tracking
- High-Speed Deserialization for Megapixel Cameras
 - Up to 1.74Gbps Serial-Bit Rate
 - 6.25MHz to 87MHz x 12-Bit + H/V Data
 - 36.66MHz to 116MHz x 11-Bit + H/V Data
- Multiple Modes for System Flexibility
 - 9.6kbps to 1Mbps Control Channel in UART, I²C (with Clock Stretch), or UART-to-I²C Modes
 - 2:1 Input Mux for Camera Selection
 - 15 Hardware-Selectable I²C-Device Addresses
 - Pairs with Any Maxim GMSL Serializer
 - Crosspoint Switch Maps Data to any Output
- Reduces EMI and Shielding Requirements
 - Spread-Spectrum Serial-Input Tracking and Transfer to the Parallel Output
 - 1.7V to 1.9V Core and 1.7V to 3.6V I/O Supply
- Peripheral Features for System Verification
 - Built-In PRBS Receiver for BER Testing
 - Dedicated “Up/Down” GPI for Camera Frame Sync Trigger and Other Uses
- Meets AEC-Q100 Automotive Specification
 - -40°C to +115°C Operating Temperature Range
 - ±8kV Contact and ±15kV Air IEC 61000-4-2 and ISO 10605 ESD Protection

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Absolute Maximum Ratings

| | | | |
|--|--------------------------|--|-----------------|
| AVDD to EP* | -0.5V to +1.9V | Operating Temperature Range | -40°C to +115°C |
| DVDD to EP* | -0.5V to +1.9V | Junction Temperature | +150°C |
| IOVDD to EP* | -0.5V to +3.9V | Storage Temperature Range | -40°C to +150°C |
| LMN_ to EP* (15mA current limit) | -0.5V to +3.9V | Soldering Temperature (reflow) | +260°C |
| IN_+, IN_- to EP* | -0.5V to +1.9V | Continuous Power Dissipation $T_A = +70^\circ\text{C}$, 32-pin TQFN (derate 34.5 mW/°C above +70°C.) | 2758.6mW |
| All Other Pins to EP* | -0.5V to (IOVDD + 0.5V)V | <i>*EP connected to IC ground.</i> | |
| IN_+, IN_- Short Circuit to Ground or Supply | Continuous | | |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

32-Pin TQFN-EP

| | |
|---|-------------------------|
| PACKAGE CODE | T3255+8 |
| Outline Number | 21-0140 |
| Land Pattern Number | 90-0013 |
| Thermal Resistance, Single Layer Board: | |
| Junction-to-Ambient (θ_{JA}) | 47 |
| Junction-to-Case Thermal Resistance (θ_{JC}) | 1.7 |
| Thermal Resistance, Four Layer Board: | |
| Junction-to-Ambient (θ_{JA}) | 29 |
| Junction-to-Case Thermal Resistance (θ_{JC}) | 1.7 |

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

DC Electrical Characteristics

($V_{DVDD} = V_{AVDD} = 1.7$ to $1.9V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground, $T_A = -40^\circ C$ to $+115^\circ C$, Typical values are at, $V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------|--|-------------------------|-----|-----|---------|
| SINGLE-ENDED INPUTS (GPI, CXTP, I2CSEL, ADD_, HIM, PWDNB, MS) | | | | | | |
| High-Level Input Voltage | V_{IH1} | | $0.65 \times V_{IOVDD}$ | | | V |
| Low-Level Input Voltage | V_{IL1} | | $0.35 \times V_{IOVDD}$ | | | V |
| Input Current | I_{IN1} | $V_{IN} = 0$ to V_{IOVDD} | -20 | | 20 | μA |
| SINGLE-ENDED OUTPUTS (DOUT_, VS, HS, DE, PCLKOUT) | | | | | | |
| High-Level Output Voltage | V_{OH1} | $I_{OH} = -2mA$, DCS = 0 | $V_{IOVDD} - 0.3$ | | | V |
| | | $I_{OH} = -2mA$, DCS = 1 | $V_{IOVDD} - 0.2$ | | | |
| Low-Level Output Voltage | V_{OL1} | $I_{OL} = 2mA$, DCS = 0 | 0.3 | | | V |
| | | $I_{OL} = 2mA$, DCS = 1 | 0.2 | | | |
| High-Impedance Output Current | I_{OZ} | OUTENB = 1, $V_{OUT} = 0V$ or V_{IOVDD} | -20 | | 20 | μA |
| Output Short-Circuit Current | I_{OS} | DOUT_, $V_O = 0V$, DCS = 0, $V_{IOVDD} = 3.0V$ to $3.6V$ | 15 | 25 | 39 | mA |
| | | DOUT_, $V_O = 0V$, DCS = 0, $V_{IOVDD} = 1.7V$ to $1.9V$ | 3 | 7 | 13 | |
| | | DOUT_, $V_O = 0V$, DCS = 1, $V_{IOVDD} = 3.0V$ to $3.6V$ | 20 | 35 | 63 | |
| | | DOUT_, $V_O = 0V$, DCS = 1, $V_{IOVDD} = 1.7V$ to $1.9V$ | 5 | 10 | 21 | |
| | | PCLKOUT_, $V_O = 0V$, DCS = 0, $V_{IOVDD} = 3.0V$ to $3.6V$ | 15 | 33 | 50 | |
| | | PCLKOUT_, $V_O = 0V$, DCS = 0, $V_{IOVDD} = 1.7V$ to $1.9V$ | 5 | 10 | 17 | |
| | | PCLKOUT_, $V_O = 0V$, DCS = 1, $V_{IOVDD} = 3.0V$ to $3.6V$ | 30 | 54 | 97 | |
| | | PCLKOUT_, $V_O = 0V$, DCS = 1, $V_{IOVDD} = 1.7V$ to $1.9V$ | 9 | 16 | 32 | |

DC Electrical Characteristics (continued)

($V_{DVDD} = V_{AVDD} = 1.7$ to $1.9V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground, $T_A = -40^\circ C$ to $+115^\circ C$, Typical values are at, $V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------|---|-------------------|-------------------|-----|---------|
| UART/I²C and GENERAL-PURPOSE I/Os (RX/SDA, TX/SCL, GPIO_, ERRB, LOCK, LFLTb) with OPEN-DRAIN OUTPUTS | | | | | | |
| High-Level Input Voltage | V_{IH2} | | 0.7 x V_{IOVDD} | | | V |
| Low-Level Input Voltage | V_{IL2} | | | 0.3 x V_{IOVDD} | | V |
| Input Current | I_{IN2} | $V_{IN} = 0$ to V_{IOVDD} (Note 2), RX/SDA, TX/SCL | -110 | | 5 | μA |
| | I_{IN} | $V_{IN} = 0$ to V_{IOVDD} (Note 2), GPIO_, ERRB, LOCK | -80 | | 5 | |
| Low-Level Open-Drain Output Voltage | V_{OL} | $I_{OL} = 3mA$, $V_{IOVDD} = 1.7V$ to $1.9V$ | | | 0.4 | V |
| | | $I_{OL} = 3mA$, $V_{IOVDD} = 3.0V$ to $3.6V$ | | | 0.3 | |
| Input Capacitance | C_{IN} | Each pin (Note 3) | | | 10 | pF |
| OUTPUTS FOR REVERSE CONTROL CHANNEL (IN0+, IN0-, IN1+, IN1-) | | | | | | |
| Differential High-Output Peak Voltage ($V_{IN+} - V_{IN-}$) | V_{RODH} | Forward channel disabled, normal-immunity mode (Figure 1) | 30 | | 60 | mV |
| | | Forward channel disabled, high-immunity mode (Figure 1) | 50 | | 100 | |
| Differential Low-Output Peak Voltage ($V_{IN+} - V_{IN-}$) | V_{RODL} | Forward channel disabled, normal-immunity mode (Figure 1) | -60 | | -30 | mV |
| | | Forward channel disabled, high-immunity mode (Figure 1) | -100 | | -50 | |
| Single-Ended High-Output Peak Voltage | V_{ROSH} | Forward channel disabled, normal-immunity mode (Figure 1) | 30 | | 60 | mV |
| | | Forward channel disabled, high-immunity mode (Figure 1) | 50 | | 100 | |
| Single-Ended Low-Output Peak Voltage | V_{ROSL} | Forward channel disabled, normal-immunity mode (Figure 1) | -60 | | -30 | mV |
| | | Forward channel disabled, high-immunity mode (Figure 1) | -100 | | -50 | |

DC Electrical Characteristics (continued)

($V_{DVDD} = V_{AVDD} = 1.7$ to $1.9V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground, $T_A = -40^\circ C$ to $+115^\circ C$, Typical values are at, $V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--------------|---|------|-----|-----------------|----------|
| DIFFERENTIAL INPUTS (IN0+, IN0-, IN1+, IN1-) | | | | | | |
| Differential High-Input Threshold Peak Voltage ($V_{IN+} - V_{IN-}$) | $V_{IDH(P)}$ | Activity detector, medium threshold (0x22 D[6:5] = 01) (Figure 2) | | | 60 | mV |
| | | Activity detector, low threshold (0x22 D[6:5] = 00) (Figure 2) | | | 49 | |
| Differential Low-Input Threshold Peak Voltage ($V_{IN+} - V_{IN-}$) | $V_{IDL(P)}$ | Activity detector, medium threshold (0x22 D[6:5] = 01) (Figure 2) | -60 | | | mV |
| | | Activity detector, low threshold (0x22 D[6:5] = 00) (Figure 2) | -49 | | | |
| Input Common-Mode Voltage ($(V_{IN+} + V_{IN-})/2$) | V_{CMR} | | 1 | 1.3 | 1.6 | V |
| Differential-Input Resistance (Internal) | R_I | | 80 | 100 | 130 | Ω |
| SINGLE-ENDED INPUTS (IN0+, IN0-, IN1+, IN1-) | | | | | | |
| Single-Ended High-Input Threshold Peak Voltage | $V_{ISH(P)}$ | Activity detector, medium threshold (0x22 D[6:5] = 01) (Figure 3) | | | 43 | mV |
| | | Activity detector, low threshold (0x22 D[6:5] = 00) (Figure 3) | | | 33 | |
| Single-Ended Low-Input Threshold Peak Voltage | $V_{ISL(P)}$ | Activity detector, medium threshold (0x22 D[6:5] = 01) (Figure 3) | -43 | | | mV |
| | | Activity detector, low threshold (0x22 D[6:5] = 00) (Figure 3) | -33 | | | |
| Input Resistance (Internal) | R_I | | 40 | 50 | 65 | Ω |
| LINE FAULT DETECTION INPUTS (LMN0, LMN1) | | | | | | |
| Short-to-Ground Threshold | V_{TG} | (Figure 4) | | | 0.3 | V |
| Normal Threshold | V_{TN} | (Figure 4) | 0.57 | | 1.07 | V |
| Open Threshold | V_{TO} | (Figure 4) | 1.45 | | $V_{IO} + 0.06$ | V |
| Open-Input Voltage | V_{IO} | (Figure 4) | 1.47 | | 1.75 | V |
| Short-to-Battery Threshold | V_{TE} | (Figure 4) | 2.47 | | | V |

DC Electrical Characteristics (continued)

($V_{DVDD} = V_{AVDD} = 1.7$ to $1.9V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground, $T_A = -40^\circ C$ to $+115^\circ C$, Typical values are at, $V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------|--|-----|-----|-----|-------|
| POWER SUPPLY | | | | | | |
| Worst-Case Supply Current (Figure 5) | I_{WCS} | $f_{PCLKOUT} = 116MHz$, BWS = 0, double output, AVDD + DVDD (1.9V) | | 95 | 115 | |
| | | $f_{PCLKOUT} = 116MHz$, BWS = 0, double output, IOVDD (1.9V), $C_L = 5pF$ (DCS = 0) (Note 3) | | 22 | 25 | |
| | | $f_{PCLKOUT} = 116MHz$, BWS = 0, double output, IOVDD (1.9V), $C_L = 10pF$ (DCS = 1) (Note 3) | | 31 | 35 | |
| | | $f_{PCLKOUT} = 116MHz$, BWS = 0, double output, IOVDD (3.6V), $C_L = 5pF$ (DCS = 0) (Note 3) | | 44 | 49 | |
| | | $f_{PCLKOUT} = 116MHz$, BWS = 0, double output, IOVDD (3.6V), $C_L = 10pF$ (DCS = 1) (Note 3) | | 63 | 70 | |
| | | $f_{PCLKOUT} = 87MHz$, BWS = 1, double output, IOVDD (1.9V), AVDD + DVDD (1.9V) | | 95 | 115 | |
| | | $f_{PCLKOUT} = 87MHz$, BWS = 1, double output, IOVDD (1.9V), $C_L = 5pF$ (DCS = 0) (Note 3) | | 17 | 19 | |
| | | $f_{PCLKOUT} = 87MHz$, BWS = 1, double output, IOVDD (1.9V), $C_L = 10pF$ (DCS = 1) (Note 3) | | 24 | 27 | |
| | | $f_{PCLKOUT} = 87MHz$, BWS = 1, double output, IOVDD (3.6V), $C_L = 5pF$ (DCS = 0) (Note 3) | | 33 | 36 | |
| | | $f_{PCLKOUT} = 87MHz$, BWS = 1, double output, IOVDD (3.6V), $C_L = 10pF$ (DCS = 1) (Note 3) | | 44 | 49 | |
| | | $f_{PCLKOUT} = 58MHz$, BWS = 0, single output, AVDD + DVDD (1.9V) | | 70 | 84 | |
| | | $f_{PCLKOUT} = 58MHz$, BWS = 0, single output, IOVDD (1.9V), $C_L = 5pF$ (DCS = 0) (Note 3) | | 11 | 13 | |
| | | $f_{PCLKOUT} = 58MHz$, BWS = 0, single output, IOVDD (3.6V), $C_L = 10pF$ (DCS = 1) (Note 3) | | 15 | 18 | |

DC Electrical Characteristics (continued)

($V_{DVDD} = V_{AVDD} = 1.7$ to $1.9V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground, $T_A = -40^\circ C$ to $+115^\circ C$, Typical values are at, $V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------|---|-----|----------|-----|---------|
| POWER SUPPLY (continued) | | | | | | |
| Worst-Case Supply Current (Figure 5) (continued) | I_{WCS} | $f_{PCLKOUT} = 58MHz$, BWS = 0, single output, IOVDD (3.6V), $C_L = 5pF$ (DCS = 0) (Note 3) | | 22 | 25 | mA |
| | | $f_{PCLKOUT} = 58MHz$, BWS = 0, single output, IOVDD (3.6V), $C_L = 10pF$ (DCS = 1) (Note 3) | | 30 | 34 | |
| | | $f_{PCLKOUT} = 43.5MHz$, BWS = 1, single output, AVDD + DVDD (1.9V) | | 70 | 84 | |
| | | $f_{PCLKOUT} = 43.5MHz$, BWS = 1, single output, IOVDD (1.9V), $C_L = 5pF$ (DCS = 0) (Note 3) | | 8 | 10 | |
| | | $f_{PCLKOUT} = 43.5MHz$, BWS = 1, single output, IOVDD (1.9V), $C_L = 10pF$ (DCS = 1) (Note 3) | | 12 | 14 | |
| | | $f_{PCLKOUT} = 43.5MHz$, BWS = 1, single output, IOVDD (3.6V), $C_L = 5pF$ (DCS = 0) (Note 3) | | 16 | 18 | |
| | | $f_{PCLKOUT} = 43.5MHz$, BWS = 1, single output, IOVDD (3.6V), $C_L = 10pF$ (DCS = 1) (Note 3) | | 22 | 25 | |
| Sleep-Mode Supply Current | I_{CCS} | Wake-up receivers enabled | | 54 | 160 | μA |
| | | Wake-up receivers disabled | | 15 | 100 | |
| Power-Down Supply Current | I_{CCZ} | PWDNB = low | | 15 | 100 | μA |
| ESD PROTECTION | | | | | | |
| IN+, IN- (Note 4) | V_{ESD} | Human Body Model, $R_D = 1.5k\Omega$, $C_S = 100pF$ | | ± 8 | | kV |
| | | IEC 61000-4-2, $R_D = 330\Omega$, $C_S = 150pF$, Contact discharge | | ± 10 | | |
| | | IEC 61000-4-2, $R_D = 330\Omega$, $C_S = 150pF$, Air discharge | | ± 15 | | |
| | | ISO 10605, $R_D = 2k\Omega$, $C_S = 330pF$, Contact discharge | | ± 10 | | |
| | | ISO 10605, $R_D = 2k\Omega$, $C_S = 330pF$, Air discharge | | ± 30 | | |
| All Other Pins (Note 5) | V_{ESD} | Human Body Model, $R_D = 1.5k\Omega$, $C_S = 100pF$ | | ± 4 | | kV |
| | | Machine Model | | 250 | | V |

AC Electrical Characteristics

(V_{DVDD} = V_{AVDD} = 1.7 to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground, T_A = -40°C to +115°C, Typical values are at, V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|----------------------|---|-------|-------|-------|-------|
| PARALLEL CLOCK OUTPUT (PCLKOUT) | | | | | | |
| Clock Frequency | f _{PCLKOUT} | BWS = 1, DRS = 1, single output | 6.25 | | 12.5 | MHz |
| | | BWS = 0, DRS = 1, single output | 8.33 | | 16.66 | |
| | | BWS = 1, DRS = 0, single output | 12.5 | | 43.5 | |
| | | BWS = 0, DRS = 0, single output | 16.66 | | 58 | |
| | | BWS = 1, DRS = 0, double output | 25 | | 87 | |
| | | BWS = 0, DRS = 0, double output | 33.33 | | 116 | |
| Data Valid Before Clock | t _{DVB} | PCLKOUT and DOUT ₊ , DCS = 1, C _L = 10pF or DCS = 0, C _L = 5pF, nonstaggered DOUT ₊ | 0.4T | 0.5T | | ns |
| | | PCLKOUT and DOUT ₊ , DCS = 1, C _L = 10pF or DCS = 0, C _L = 5pF, staggered DOUT ₊ | 0.35T | 0.4T | | |
| Data Valid After Clock | t _{DVA} | PCLKOUT and DOUT ₊ , DCS = 1, C _L = 10pF or DCS = 0, C _L = 5pF, nonstaggered DOUT ₊ | 0.35T | 0.4T | | ns |
| | | PCLKOUT and DOUT ₊ , DCS = 1, C _L = 10pF or DCS = 0, C _L = 5pF, staggered DOUT ₊ | 0.3T | 0.35T | | |
| Clock Jitter | t _J | RMS period jitter, spread off, 1.74Gbps PRBS pattern, UI = 1/f _{PCLKOUT} , DBL = 1, double output) | | 0.05 | | UI |
| | | Period jitter; peak-to-peak, spread off, 1.74Gbps, PRBS pattern, UI = 1/f _{PCLKOUT} , DBL = 0, single output) | | 0.01 | | |
| I²C/UART PORT TIMING | | | | | | |
| I ² C/UART Bit Rate | | | 9.6 | | 1000 | kbps |
| Output Rise Time | t _R | 30% to 70%, C _L = 10pF to 100pF, 1kΩ pullup to IOVDD | 20 | | 150 | ns |
| Output Fall Time | t _F | 70% to 30%, C _L = 10pF to 100pF, 1kΩ pullup to IOVDD | 20 | | 150 | ns |
| I²C TIMING (Figure 6) | | | | | | |
| SCL Clock Frequency | f _{SCL} | Low f _{SCL} range: (I2CMSTBT = 010, I2CSLVSH = 10) | 9.6 | | 100 | kHz |
| | | Mid f _{SCL} range: (I2CMSTBT 101, I2CSLVSH = 01) | >100 | | 400 | |
| | | High f _{SCL} range: (I2CMSTBT = 111, I2CSLVSH = 00) | >400 | | 1000 | |

AC Electrical Characteristics (continued)

($V_{DVDD} = V_{AVDD} = 1.7$ to $1.9V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground, $T_A = -40^\circ C$ to $+115^\circ C$, Typical values are at, $V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|--------------|------------------|------|-----|------|---------|
| START Condition Hold Time | $t_{HD:STA}$ | fSCL range, Low | 4 | | | μs |
| | | fSCL range, Mid | 0.6 | | | |
| | | fSCL range, High | 0.26 | | | |
| Low Period of SCL Clock | t_{LOW} | fSCL range, Low | 4.7 | | | μs |
| | | fSCL range, Mid | 1.3 | | | |
| | | fSCL range, High | 0.5 | | | |
| High Period of SCL Clock | t_{HIGH} | fSCL range, Low | 4 | | | μs |
| | | fSCL range, Mid | 0.6 | | | |
| | | fSCL range, High | 0.26 | | | |
| Repeated START Condition Setup Time | $t_{SU:STA}$ | fSCL range, Low | 4.7 | | | μs |
| | | fSCL range, Mid | 0.6 | | | |
| | | fSCL range, High | 0.26 | | | |
| Data Hold Time | $t_{HD:DAT}$ | fSCL range, Low | 0 | | | ns |
| | | fSCL range, Mid | 0 | | | |
| | | fSCL range, High | 0 | | | |
| Data Setup Time | $t_{SU:DAT}$ | fSCL range, Low | 250 | | | ns |
| | | fSCL range, Mid | 100 | | | |
| | | fSCL range, High | 50 | | | |
| Setup Time for STOP Condition | $t_{SU:STO}$ | fSCL range, Low | 4 | | | μs |
| | | fSCL range, Mid | 0.6 | | | |
| | | fSCL range, High | 0.26 | | | |
| Bus Free Time | t_{BUF} | fSCL range, Low | 4.7 | | | μs |
| | | fSCL range, Mid | 1.3 | | | |
| | | fSCL range, High | 0.5 | | | |
| Data Valid Time | $t_{VD:DAT}$ | fSCL range, Low | | | 3.45 | μs |
| | | fSCL range, Mid | | | 0.9 | |
| | | fSCL range, High | | | 0.45 | |
| Data Valid Acknowledge Time | $t_{VD:ACK}$ | fSCL range, Low | | | 3.45 | μs |
| | | fSCL range, Mid | | | 0.9 | |
| | | fSCL range, High | | | 0.45 | |
| Pulse Width of Spikes Suppressed | t_{SP} | fSCL range, Low | | | 50 | ns |
| | | fSCL range, Mid | | | 50 | |
| | | fSCL range, High | | | 50 | |
| Capacitive load each bus line | C_B | | | | 100 | pF |

AC Electrical Characteristics (continued)

($V_{DVDD} = V_{AVDD} = 1.7$ to $1.9V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground, $T_A = -40^\circ C$ to $+115^\circ C$, Typical values are at, $V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------|---|------|-----|------|---------|
| SWITCHING CHARACTERISTICS (Note 3) | | | | | | |
| PCLKOUT Rise-and-Fall Time (Figure 7) | t_R, t_F | 20% to 80%, $V_{IOVDD} = 1.7V$ to $1.9V$, DCS = 1, $C_L = 10pF$ | 0.4 | | 2.2 | ns |
| | | 20% to 80%, $V_{IOVDD} = 1.7V$ to $1.9V$, DCS = 0, $C_L = 5pF$ | 0.5 | | 2.8 | |
| | | 20% to 80%, $V_{IOVDD} = 3.0V$ to $3.6V$, DCS = 1, $C_L = 10pF$ | 0.25 | | 1.8 | |
| | | 20% to 80%, $V_{IOVDD} = 3.0V$ to $3.6V$, DCS = 0, $C_L = 5pF$ | 0.3 | | 2 | |
| Parallel Data Rise-and-Fall Time (Figure 7) | t_R, t_F | 20% to 80%, $V_{IOVDD} = 1.7V$ to $1.9V$, DCS = 1, $C_L = 10pF$ | 0.5 | | 3.1 | ns |
| | | 20% to 80%, $V_{IOVDD} = 1.7V$ to $1.9V$, DCS = 0, $C_L = 5pF$ | 0.6 | | 3.8 | |
| | | 20% to 80%, $V_{IOVDD} = 3.0V$ to $3.6V$, DCS = 1, $C_L = 10pF$ | 0.3 | | 2.2 | |
| | | 20% to 80%, $V_{IOVDD} = 3.0V$ to $3.6V$, DCS = 0, $C_L = 5pF$ | 0.4 | | 2.4 | |
| Deserializer Delay | t_{SD} | (Figure 8) (Note 6) | | | 2160 | Bits |
| Reverse Control-Channel Output Rise Time | t_R | No forward-channel data transmission | 180 | | 400 | ns |
| Reverse Control-Channel Output Fall Time | t_F | No forward-channel data transmission | 180 | | 400 | ns |
| GPI-to-GPO Delay | t_{GPIO} | Deserializer GPI to serializer GPO (Figure 9) | | | 350 | μs |
| Lock Time (Note 3) | t_{LOCK} | (Figure 10) AEQ on | | | 1.6 | ms |
| | | (Figure 10) AEQ off | | | 1 | |
| Power-Up Time | t_{PU} | (Figure 11) | | | 6.5 | ms |
| Active Output to High-Imped- ance Time | t_{OAZ} | (Figure 12, Figure 13) CC write OUTENB = 1 | | | 250 | ns |
| Active High-Impedance to Output Time | t_{OZA} | (Figure 12, Figure 13) CC write OUTENB = 0 | | | 250 | ns |

Note 1: Limits are 100% production tested at $T_A = +115^\circ C$. Limits over the operating temperature range are guaranteed by design and characterization, unless otherwise noted.

Note 2: I_{IN} min is due to voltage drop across the internal pullup resistor.

Note 3: Not production tested. Guaranteed by design.

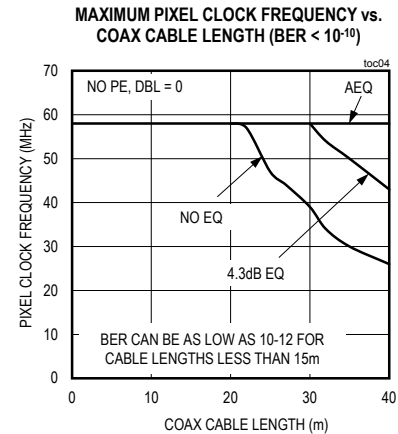
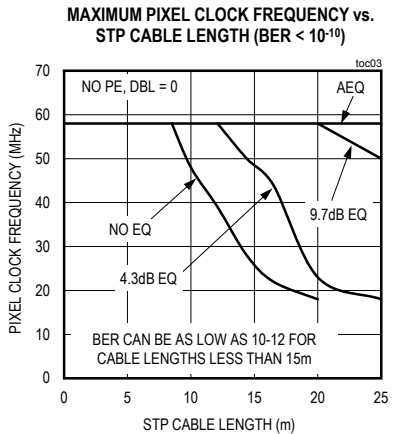
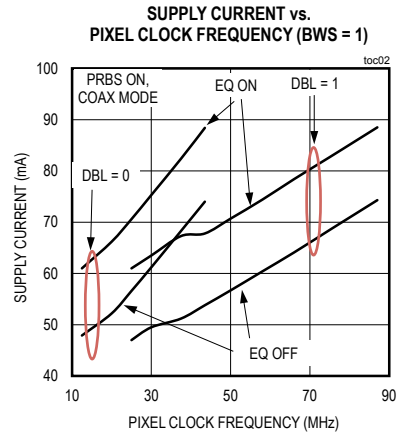
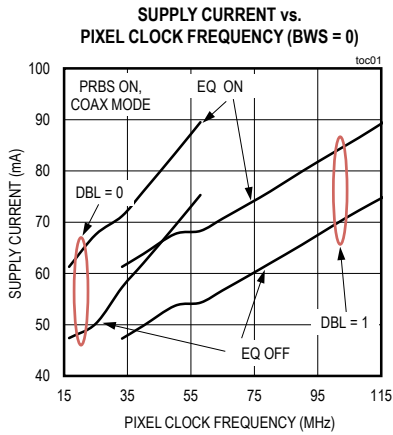
Note 4: Specified pin to ground.

Note 5: Specified pin to all supply/ground.

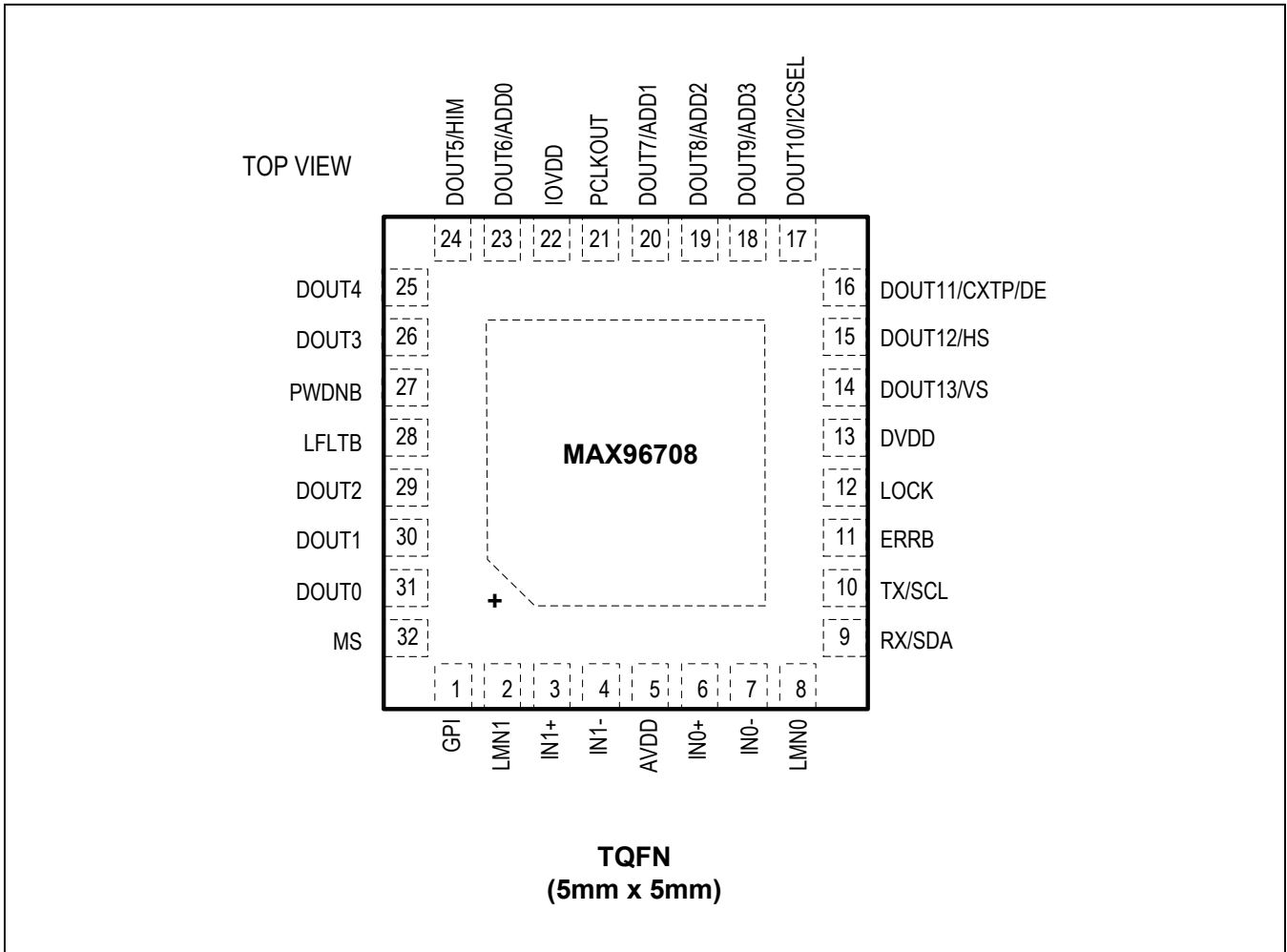
Note 6: Measured in serial link bit times. Bit time = $1/(30 \times f_{PCLKOUT})$ for BWS = GND. Bit time = $1/(40 \times f_{PCLKOUT})$ for BWS = 1.

Typical Operating Characteristics

($V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Configuration



Pin Description

| PIN | NAME | FUNCTION | REF SUPPLY | TYPE |
|---|--------------------|---|------------|---------|
| POWER | | | | |
| 5 | AVDD | 1.8V Analog Power Supply. Bypass AVDD to EP with 0.1 μ F and 0.001 μ F capacitors placed as close as possible to the device, with the smaller-value capacitor closest to AVDD. | | Power |
| 13 | DVDD | 1.8V Digital Power Supply. Bypass DVDD to EP with 0.1 μ F and 0.001 μ F capacitors placed as close as possible to the device, with the smaller-value capacitor closest to DVDD. | | Power |
| 22 | IOVDD | I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to EP with 0.1 μ F and 0.001 μ F capacitors placed as close as possible to the device, with the smaller-value capacitor closest to IOVDD. | | Power |
| EP | — | Exposed Pad. EP is internally connected to device ground. Must connect EP to the PCB ground plane through a via array for proper thermal and electrical performance. | | Power |
| HIGH-SPEED DIGITAL | | | | |
| High-Speed Digital / Multifunction | | | | |
| 14 | DOUT13/VS | Parallel-Data/Vertical-Sync Output. Defaults to parallel-data output on power-up. Vertical-sync output when HS/VS encoding is enabled. | IOVDD | Digital |
| 15 | DOUT12/HS | Parallel-Data/Horizontal-Sync Output. Defaults to parallel-data output on power-up. Horizontal-sync output when HS/VS encoding is enabled. | IOVDD | Digital |
| 16 | DOUT11/ CXTP/DE | Parallel-Data Output/Cable-Type Input/Data-Enable Output with internal pulldown to EP. CX/TP is latched at power-up, or when resuming from power-down mode (PWDNB = low), and switches to parallel/data-enable output after power-up. Connect CXTP to IOVDD with a 30k Ω resistor to set high (coax mode), or leave open to set low (twisted-pair mode). | IOVDD | Digital |
| 17 | DOUT10/ I2CSEL | Parallel-Data Output/I ² C-Select Input with Internal Pulldown to EP. I2CSEL is latched at power-up, or when resuming from power-down mode (PWDNB = low), and switches to parallel-data output after power-up. Connect I2CSEL to IOVDD with a 30k Ω resistor to set high (I ² C interface), or leave open to set low (UART interface). | IOVDD | Digital |
| 18 | DOUT9/ ADD3 | Parallel-Data Output/Address Input with Internal Pulldown to EP. ADD3 is latched at power-up, or when resuming from power-down mode (PWDNB = low), and switches to parallel-data output after power-up. Connect ADD3 to IOVDD with a 30k Ω resistor to set high, or leave open to set low. | IOVDD | Digital |
| 19 | DOUT8/ ADD2 | Parallel-Data Output/Address Input with Internal Pulldown to EP. ADD2 is latched at power-up, or when resuming from power-down mode (PWDNB = low), and switches to parallel-data output after power-up. Connect ADD2 to IOVDD with a 30k Ω resistor to set high, or leave open to set low. | IOVDD | Digital |

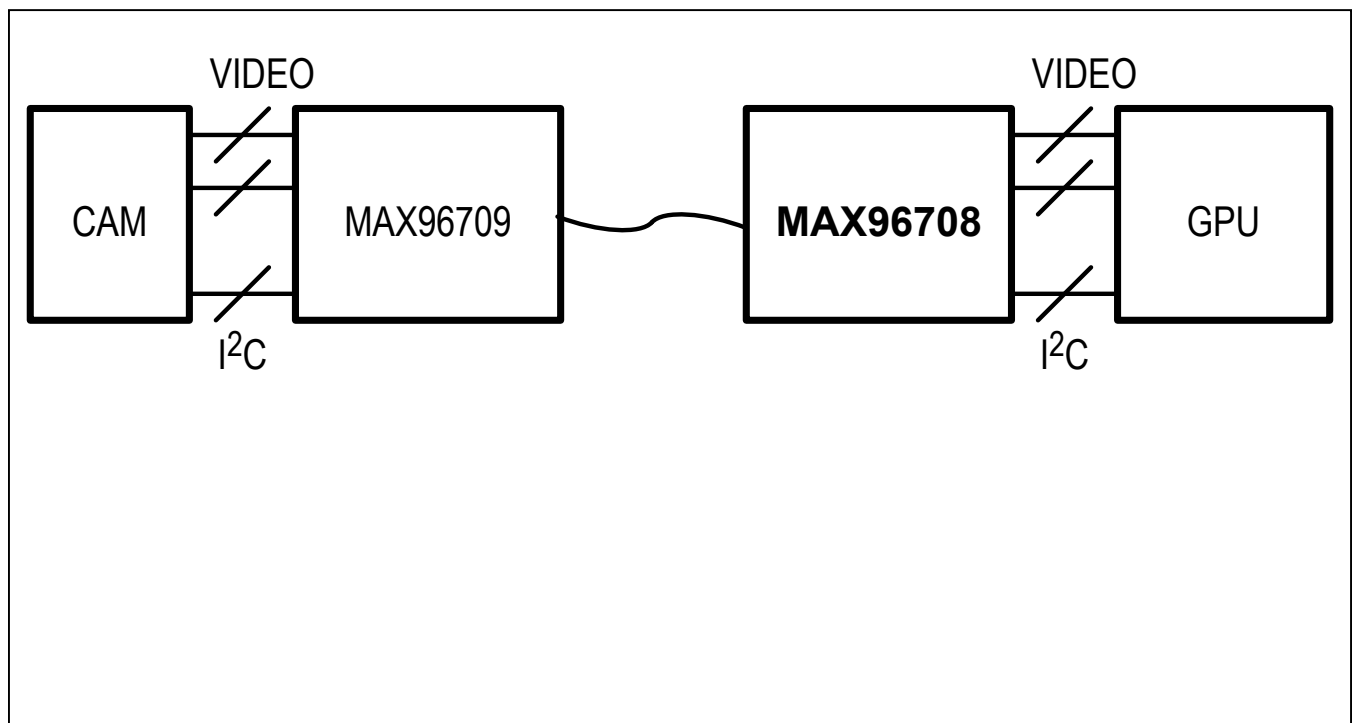
Pin Description (continued)

| PIN | NAME | FUNCTION | REF SUPPLY | TYPE |
|---|----------------|--|------------|---------|
| 20 | DOUT7/ ADD1 | Parallel-Data Output/Address Input with Internal Pulldown to EP. ADD1 is latched at power-up, or when resuming from power-down mode (PWDNB = low), and switches to parallel-data output after power-up. Connect ADD1 to IOVDD with a 30kΩ resistor to set high, or leave open to set low. | IOVDD | Digital |
| 23 | DOUT6/ ADD0 | Parallel-Data Output/Address Input with Internal Pulldown to EP. ADD0 is latched at power-up, or when resuming from power-down mode (PWDNB = low), and switches to parallel-data output after power-up. Connect ADD0 to IOVDD with a 30kΩ resistor to set high, or leave open to set low. | IOVDD | Digital |
| 24 | DOUT5/HIM | Parallel-Data Output/High-Immunity Mode Input with Internal Pulldown to EP. HIM input latched at power-up, or when resuming from power-down mode (PWDNB = low), and switches to parallel-data output after power-up. Connect HIM to IOVDD with a 30kΩ resistor to set high, or leave open to set low. HIGHIMM in the serializer must be set to the same value. | IOVDD | Digital |
| High-Speed Digital / Single Function | | | | |
| 21 | PCLKOUT | Parallel-Clock Output. Provides timing signal to latch parallel-data outputs to the input of another device. | IOVDD | Digital |
| 25 | DOUT4 | Parallel-Data Output | IOVDD | Digital |
| 26 | DOUT3 | Parallel-Data Output | IOVDD | Digital |
| 29 | DOUT2 | Parallel-Data Output | IOVDD | Digital |
| 30 | DOUT1 | Parallel-Data Output | IOVDD | Digital |
| 31 | DOUT0 | Parallel-Data Output | IOVDD | Digital |
| LINE FAULT | | | | |
| 2 | LMN1 | Line-Fault Monitor Input 1 (see Figure 4) | | Analog |
| 8 | LMN0 | Line-Fault Monitor Input 0 (see Figure 4) | | Analog |
| 28 | LFLT B | Line-Fault Output. LFLT B is active low, and has a 60kΩ internal pullup to IOVDD. LFLT B low indicates a line-fault condition at LMN0, or LMN1. LFLT B is output high when PWDNB is low. | IOVDD | Digital |
| OTHER PINS | | | | |
| 1 | GPI | General-Purpose Input with Internal Pulldown to EP. Serializer GPO (or INT) output follows the state of the GPI. | IOVDD | Digital |
| 3 | IN1+ | Noninverting CML Serial-Data Input 1. Coax input when CXTP is high. | | |
| 4 | IN1- | Inverting CML Serial-Data Input 1 | | |
| 6 | IN0+ | Noninverting CML Serial-Data Input 0. Coax input when CXTP is high. | | |
| 7 | IN0- | Inverting CML Serial-Data Input 0 | | |
| 9 | RX/SDA | Receive/Serial Data. Input/output with internal 30kΩ pullup to IOVDD. In UART mode, RX/SDA is the Rx input of the serializer's UART. In I ² C mode, RX/SDA is the SDA input/output of the serializer's I ² C master/slave. RX/SDA has an open-drain driver and requires a pullup resistor. | IOVDD | Digital |

Pin Description (continued)

| PIN | NAME | FUNCTION | REF SUPPLY | TYPE |
|-----|--------|---|------------|---------|
| 10 | TX/SCL | Transmit/Serial Clock. Input/output with internal 30kΩ pullup to IOVDD. In UART mode, TX/SCL is the Tx output of the serializer's UART. In I ² C mode, TX/SCL is the SCL input/output of the serializer's I ² C master/slave. TX/SCL has an open-drain driver and requires a pullup resistor. | IOVDD | Digital |
| 11 | ERRB | Error Output. Active-low, open-drain video data error output with internal pullup to IOVDD. ERRB goes low when decoding errors during normal operation exceed a programmed threshold, or when at least one PRBS error is detected during a PRBS test. ERRB is output high when PWDNB is low. | IOVDD | Digital |
| 12 | LOCK | Lock Output. Open-drain output with internal pullup to IOVDD. LOCK high indicates PLLs are locked with correct serial-word boundary alignment. LOCK low indicates PLLs are not locked, or incorrect serial-word boundary alignment. LOCK is low when the configuration link is active. LOCK is output high when PWDNB is low. | IOVDD | Digital |
| 27 | PWDNB | Active-Low, Power-Down Input with Internal Pulldown to EP. Set PWDNB low to enter power-down mode to reduce power consumption. | IOVDD | Digital |
| 32 | MS | Mode-Select Input with Internal Pulldown to EP. Set MS low to select base mode. Set MS high to select bypass mode. | IOVDD | Digital |

Functional Diagrams



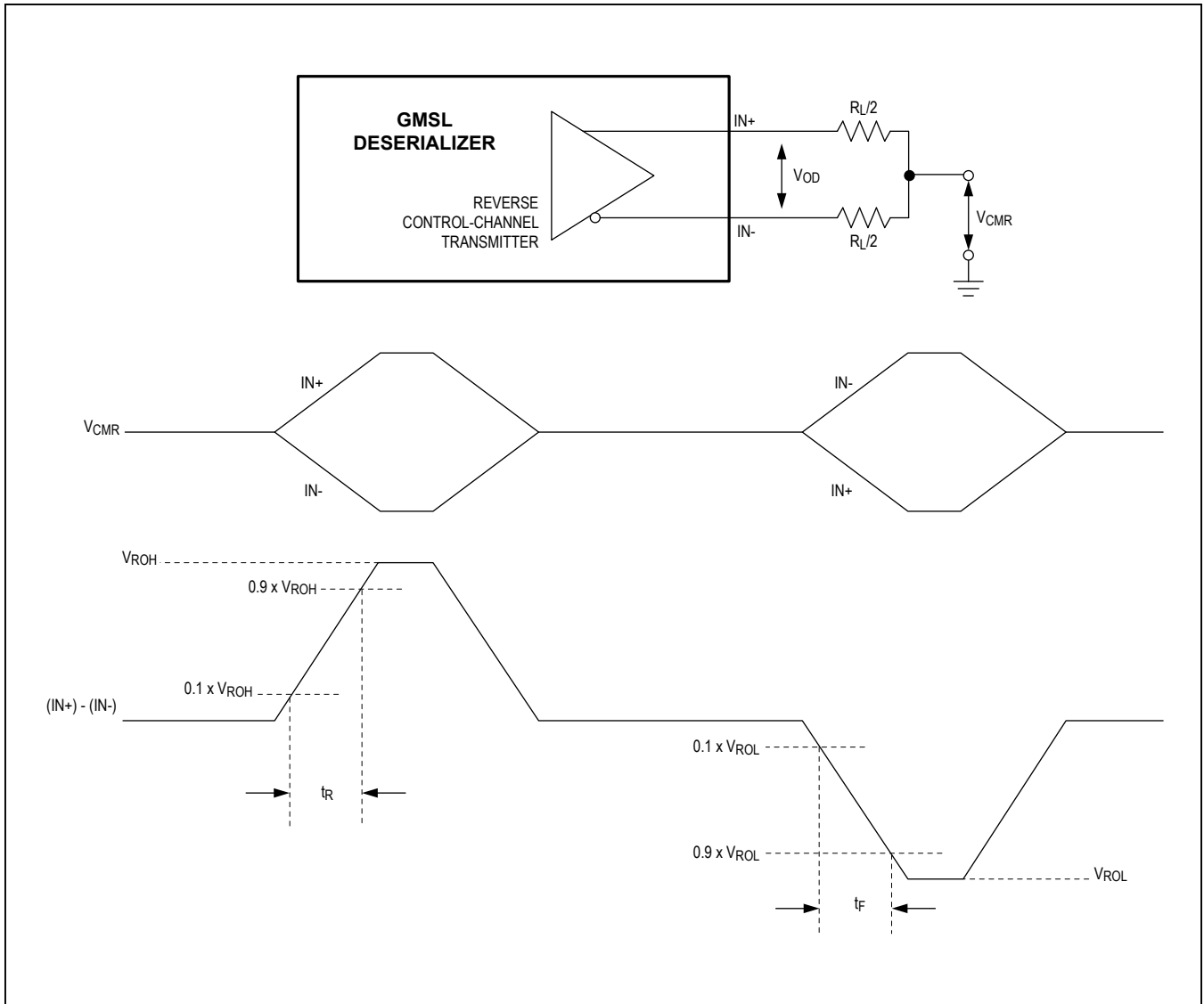


Figure 1. Reverse Control-Channel Output Parameters

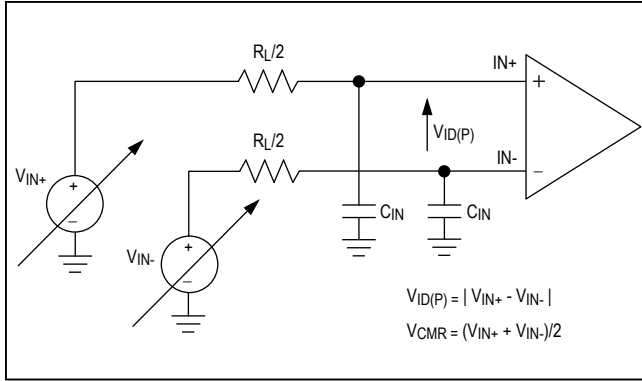


Figure 2. Test Circuit for Differential Input Measurement

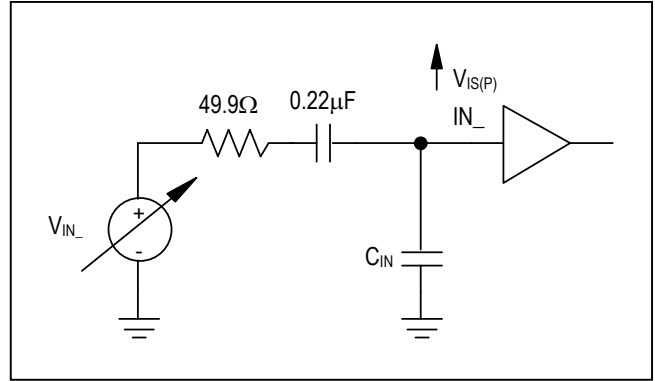


Figure 3. Test Circuit for Single-Ended Input Measurement

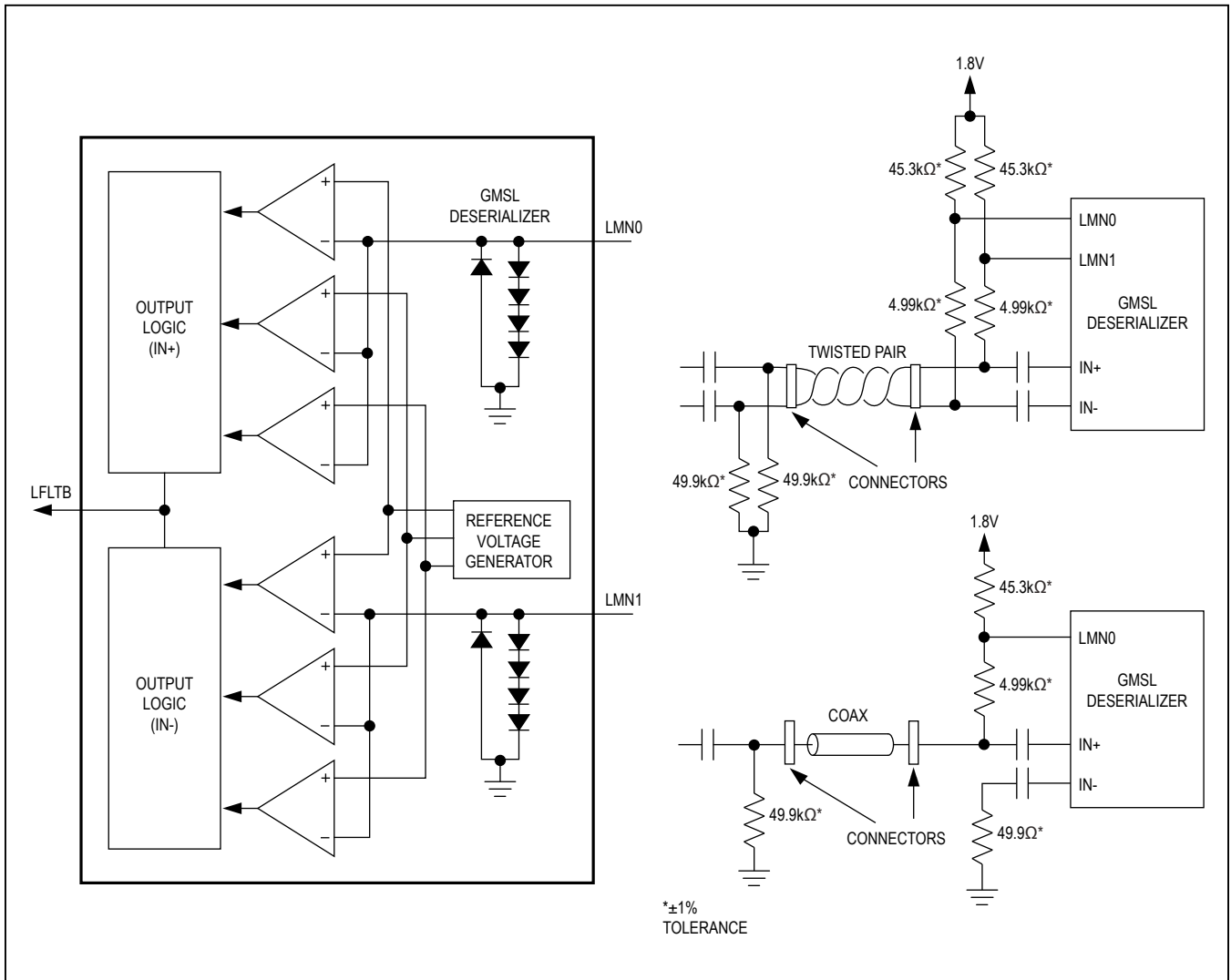


Figure 4. Line Fault

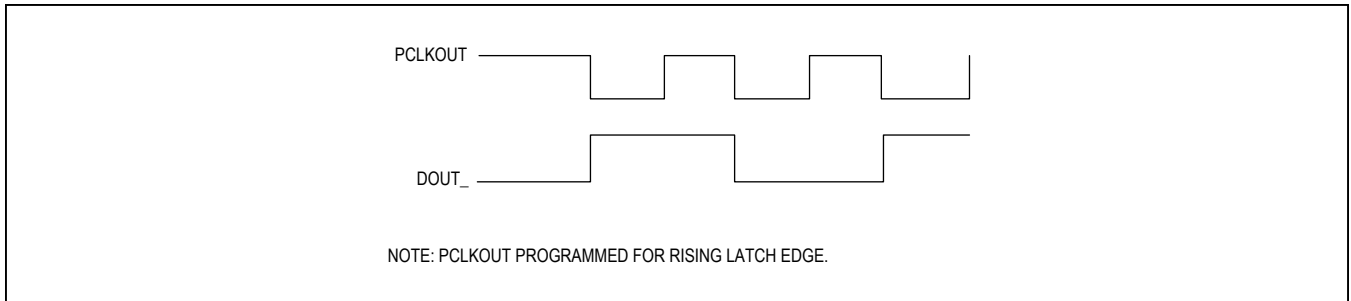


Figure 5. Worst-Case Pattern Output

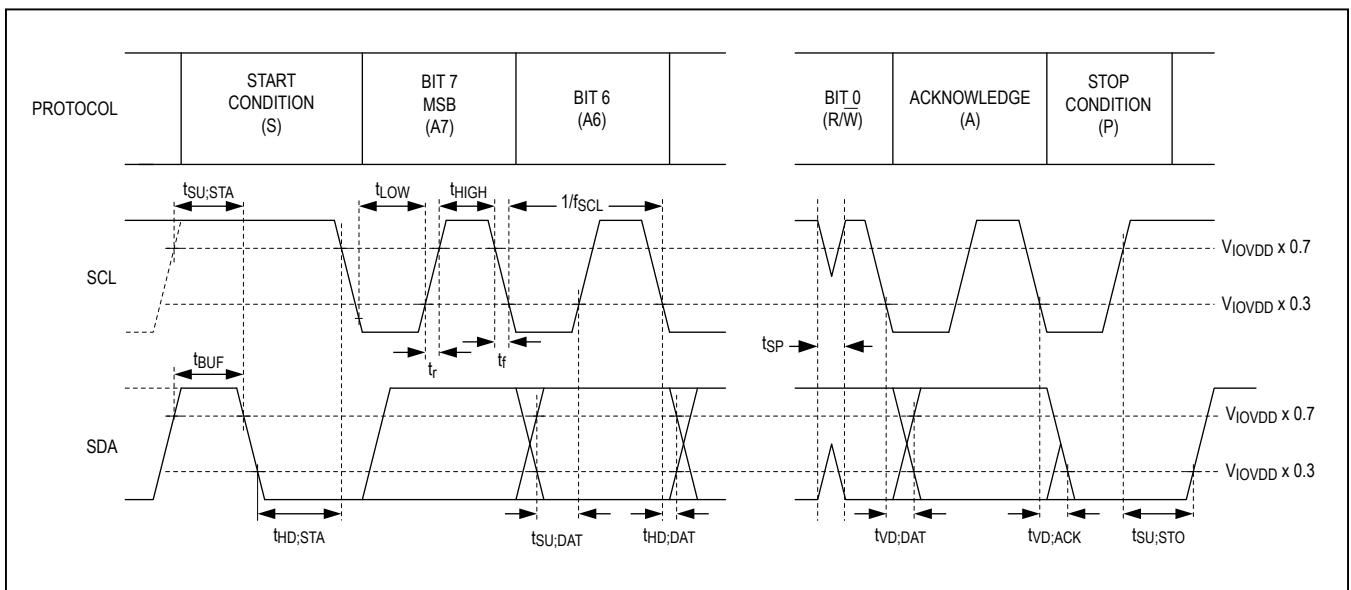


Figure 6. I²C Timing Parameters

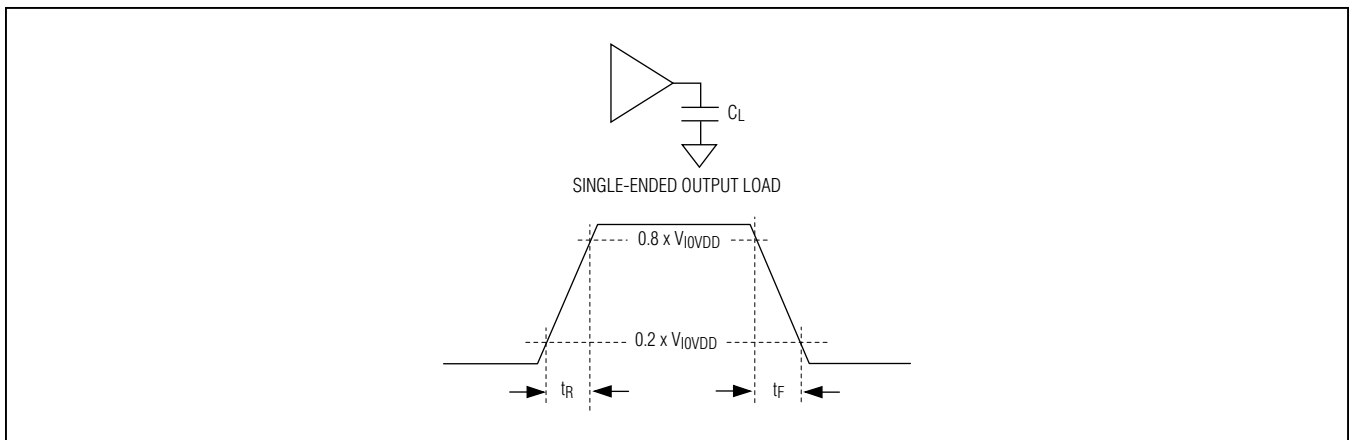


Figure 7. Output Rise-and-Fall Times

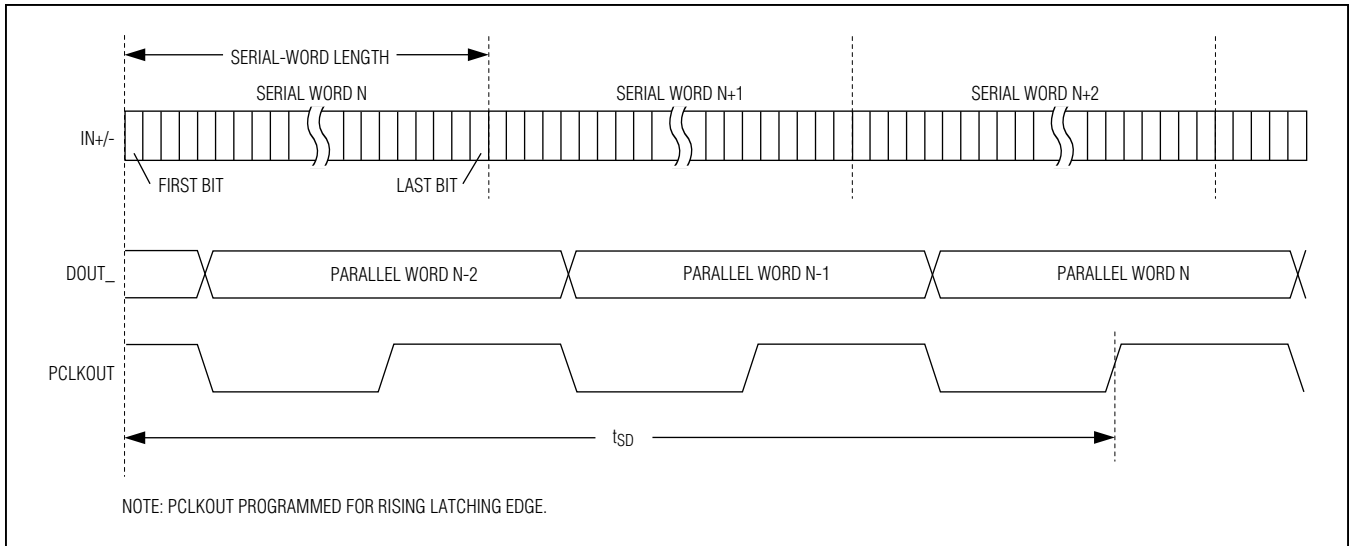


Figure 8. Deserializer Delay

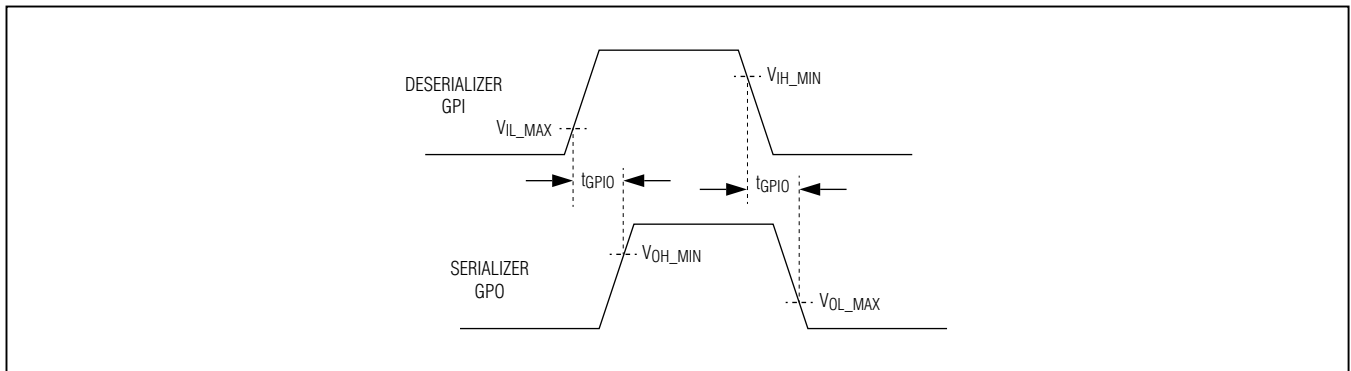


Figure 9. GPI-to-GPO Delay

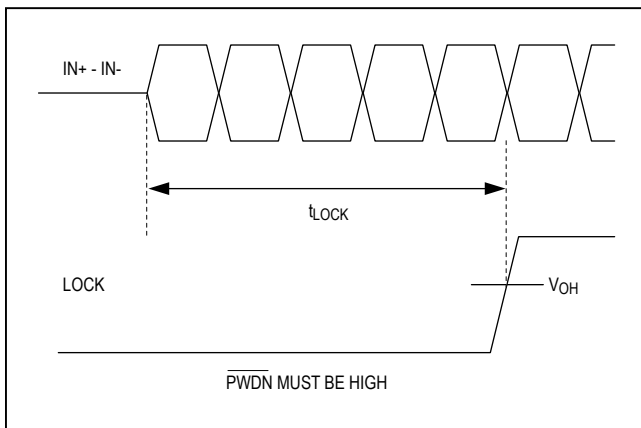


Figure 10. Lock Time

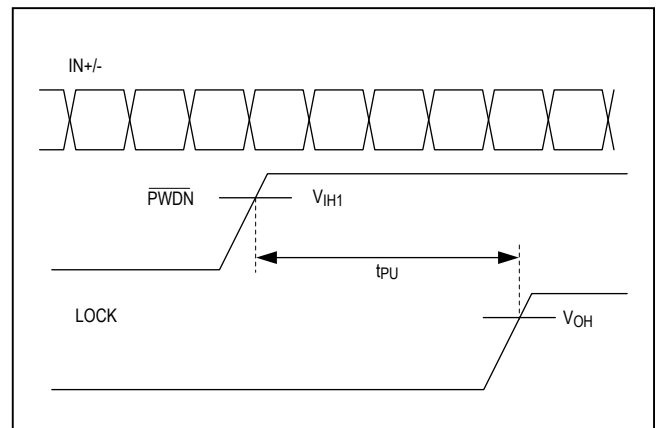


Figure 11. Power-Up Delay

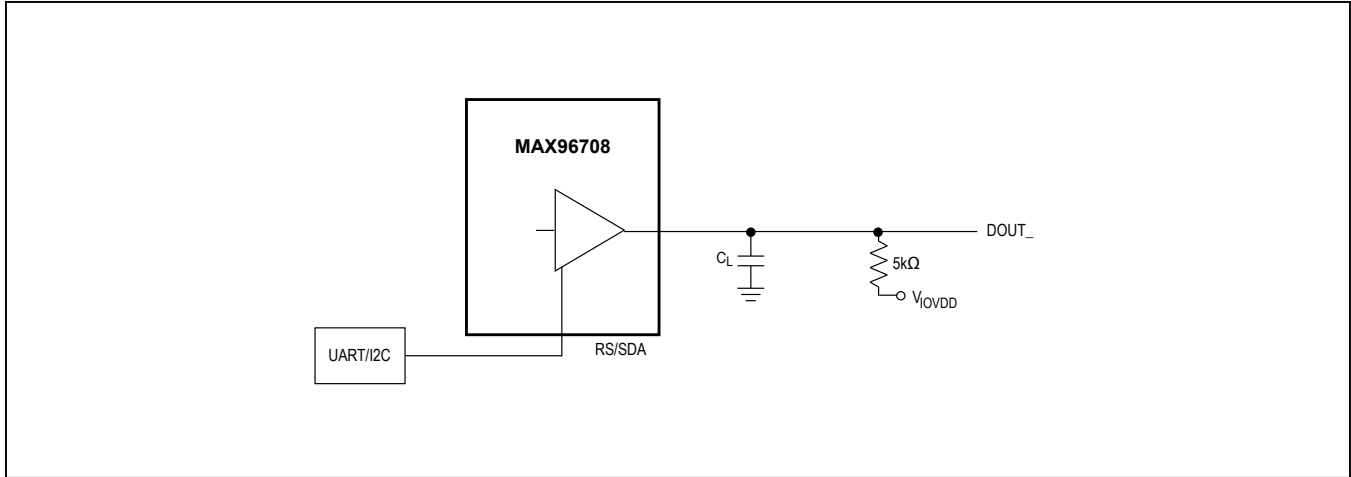


Figure 12. Active Output to High-Impedance Time, High Impedance to Active-Output Time Test Circuit

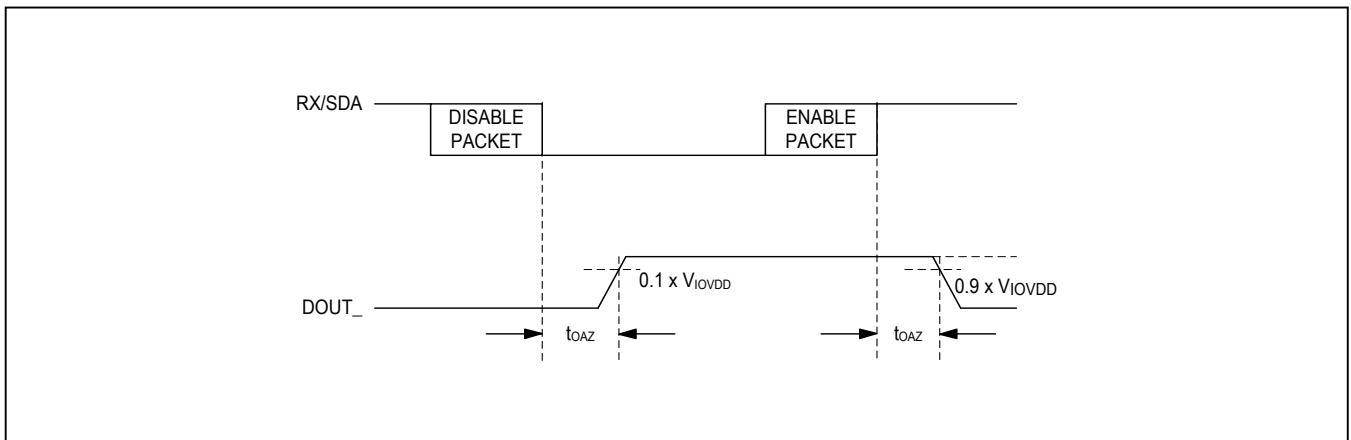


Figure 13. Active Output to High-Impedance Time, High Impedance to Active-Output Time

Detailed Description

The MAX96708 deserializer is a compact device with features especially suited for automotive camera applications. The device operates at a variety of output widths and word rates up to a total serial-data rate up to 1.75Gbps. Two modes offer a 116MHz parallel clock rate with 11 bits of video data or 87MHz parallel clock rate with 14 bits of video data. An embedded 9.6kbps to 1Mbps control channel programs the serializer, deserializer, and any attached UART or I²C peripherals.

To promote safety applications, the device features CRC protection of video data. In addition, high-immunity mode reduces the effects of bit errors corrupting communication. Automatic equalization, along with a PRBS tester, allow for in-system optimization of the link.

This device operates over the -40°C to +115°C automotive temperature range.

Serial Link Signaling and Data Format

The serializer scrambles the input parallel data and combines this with the forward control data. The data is then encoded for transmission and output as a single bitstream at several times the input word rate (depending on bus width). The deserializer receives the serial data and recovers the clock signal. The data is then deserialized, decoded, and descrambled into parallel output data and forward control data.

Operating Modes

The GMSL devices are configurable to operate in many modes, depending on the application. These modes allow for a more efficient use of serial bandwidth. Most of these settings are set during system design and are configured using the external configuration pins, or through register bits.

Video/Configuration Link

In normal operation, the serializer runs in video-link mode (SEREN = 1) with video data and control data sent across the serial link. Set SEREN = 0 in the serializer to turn off serialization. The serializer powers up in video-link mode, and requires a valid PCLK for operation.

The configuration link is available to set up the serializer, deserializer, and peripherals when PCLK is not available.

Set SEREN = 0 and CLINK = 1 in the serializer to enable the configuration link (SEREN = 1 forces the serializer into video-link mode). Once PCLK has been established, turn on the video link (SEREN = 1).

By default, video-link mode requires a valid PCLK for operation. Set AUTO_CLINK bit = 1 (if supported), and SEREN = 1 in the serializer to automatically switch between the video link and configuration link whenever PCLK is not present.

Single and Double Modes of Operation

Single-/double-mode operation configures the available 1.74Gbps bandwidth into a variety of widths and word rates. Single-mode operation is compatible with all GMSL devices, and serializes one parallel word for each serial word. Double mode serializes two half-width parallel words for each serial word, and results in a 2x increase in parallel word-rate range (compared to single mode). Set DBL = 0 for single-mode operation and DBL = 1 for double-mode operation.

HS/VS Encoding

By default, GMSL assigns a video bit slot to HSYNC, VSYNC, and DE (if used). With HS/VS encoding, the device instead encodes special packets to sync signals to free up additional video bit slots. Set HVEN = 1 to turn on HS/VS encoding (DE, if enabled uses up a video bit). HS/VS encoding requires that HSYNC, VSYNC, and DE (if used) remain high during the active video, and low during the blanking period. Use HS/VS inversion when using reverse-polarity sync signals.

Error Detection

The serial link's 8b/10b encoding/decoding, and 1-bit parity detect bit errors that occur on the serial link. An optional 6-bit CRC check is available at the expense of 6 video bits. To activate 6-bit CRC mode, set PXL_CRC = 1 in the remote-side device first, and then in the local-side device. When using 6-bit CRC mode, the available internal bus width is reduced by 6 bits in single-input mode (DBL = 0) and 3 bits in double-input mode (DBL = 1). Note that the input bus width may already have been reduced due to pin availability of the serializer or deserializer; thus, the reduction of bandwidth from CRC may not be visible (see [Table 3](#)).

Bus Widths

The serial link has multiple bus-width settings that determine the parallel bus width and the resulting parallel word rate. The serial link operates to a maximum serial bit rate of 1.74Gbps. The BWS bit determines if each serial packet is 30 or 40 bits long, which translates to a maximum serial packet rate; thus, a maximum parallel word rate of 58MHz or 43.5MHz when BWS = 0 or 1, respectively. Decoding translates the 30- or 40-bit serial packets into 24, or 32 parallel bits. One bit is used for parity, while a second is reserved for the control channel. An additional 6 bits is used during optional 6-bit CRC. In addition, double mode splits the remaining word size in

half if used. The remaining bits can be used for video bits minus any sync bits if HV encoding is not used.

Note: The following modes list the internal bus widths. The number of available input and output pins may limit the actual bus width available.

24-Bit Mode (Figure 14)

When BWS = 0, the 30-bit serial packet corresponds with three 8b/10b symbols, representing 24 bits (24-bit mode). After parity and control channel, this leaves 16/22 bits of video data if CRC is/is not used (single mode), or 8/11 bits of video data if CRC is/is not used (double mode).

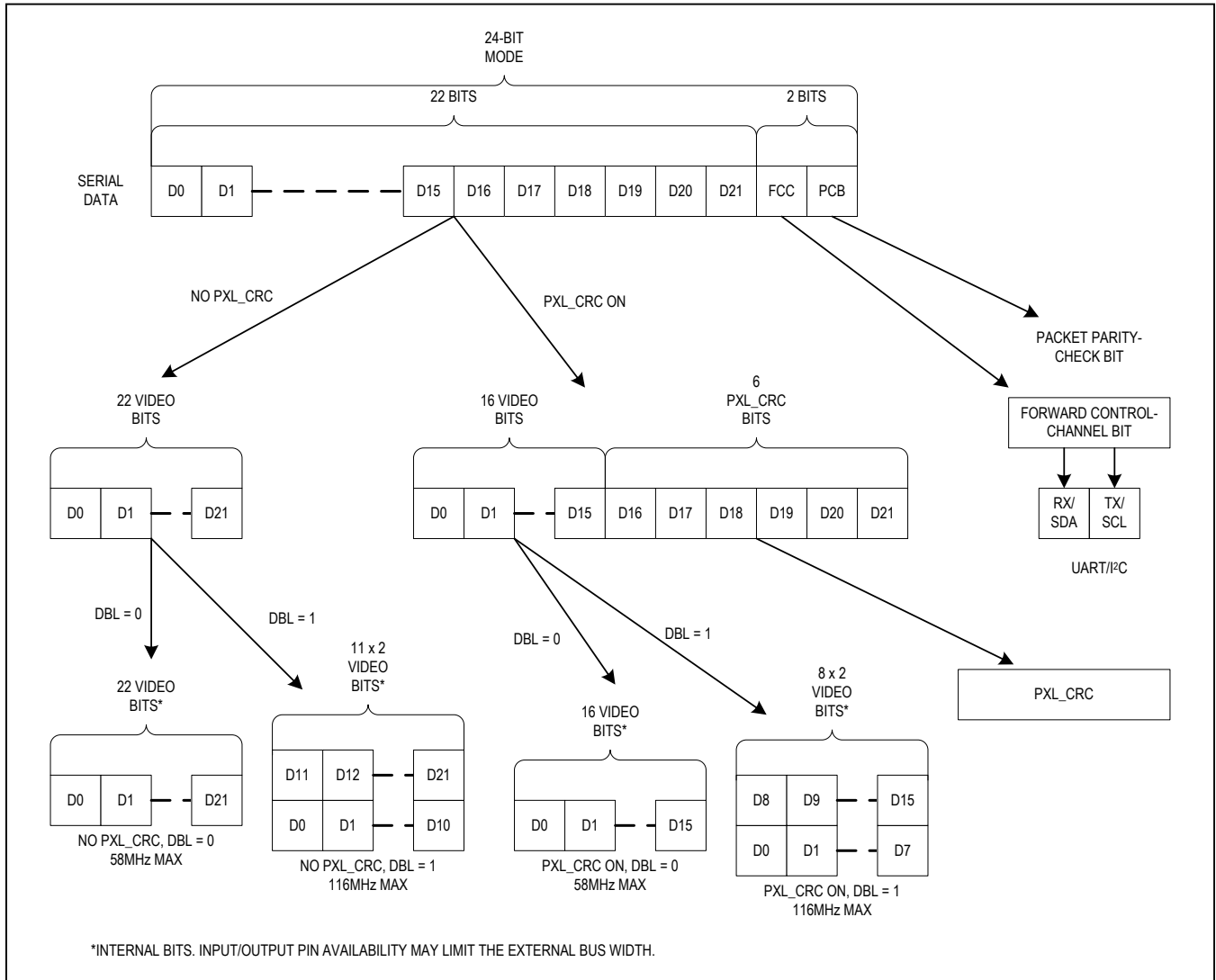


Figure 14. 24-Bit Mode Serial-Data Format

32-Bit Mode (Figure 15)

When BWS = 1 the 40-bit serial packet corresponds with four 8b/10b symbols, representing 32 bits (32-bit mode). After parity and control channel, this leaves 24/30 bits of video data if CRC is/is not used (single mode), or 12/15 bits of video data if CRC is/is not used (double mode).

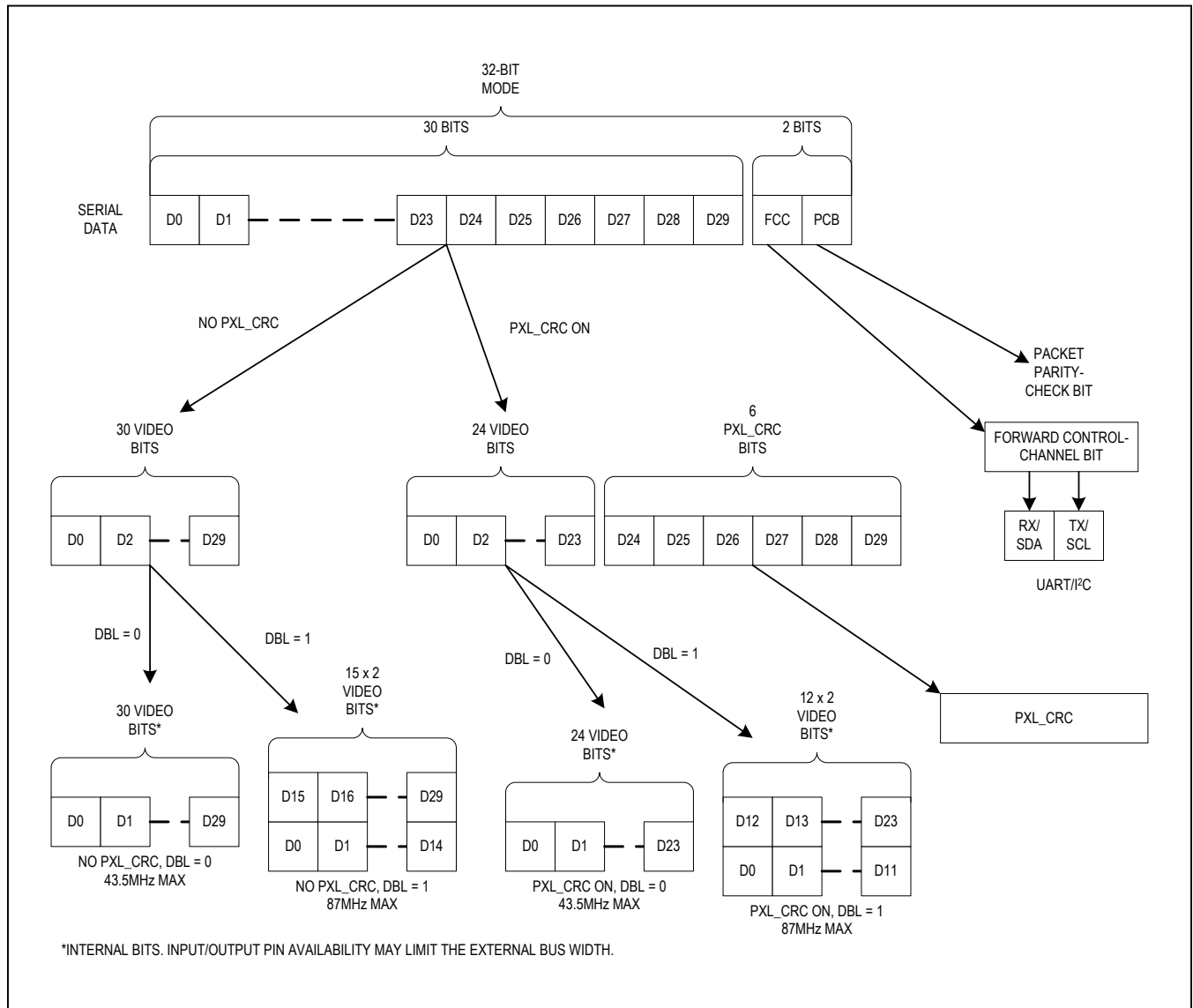


Figure 15. 32-Bit Mode Serial-Data Format

Control Channel and Register Programming

The control channel sends I²C or UART information across the serial link for control of the serializer, deserializer, and any attached peripherals. The control channel is multiplexed onto the serial link and is available with or without the video channel.

Forward Control Channel

Control data sent from the serializer to the deserializer is sent on the forward control channel. The data is encoded as one of the serial bits in the forward high-speed link. After deserialization, the forward control-channel data is extracted from the serial link. The forward control-channel bandwidth exceeds the maximum external control data rate, and all data sent on the forward control channel appears on the remote side after transmission delay of a few bit times.

Reverse Control Channel

Control data sent from the deserializer to the serializer is sent on the reverse control channel. The data is encoded as a series of 1 μ s pulses, with a maximum raw data rate of 1Mbps. High-immunity mode is available to increase the robustness of the reverse control channel at a reduced raw bit rate of 500kbps (Table 1). In high-immunity mode, set HPFTUNE = 00 in the deserializer when the serial bit rate is larger than 1Gbps. Setting the REV_FAST bit = 1 increases this rate back to 1Mbps. In I²C mode, when the input data rate (after encoding) exceeds the reverse data rate, the input clock is held through clock stretching to slow the external clock to match the internal bit rate.

UART Interface

The UART interface, compatible with all GMSL devices, sends commands from device to device through several UART packets. Set I2CSEL = 0 to set the device to use UART protocol.

I²C Interface

The serial link connects the serializer and deserializer I²C interfaces together through the control channel. When an I²C master sends a command to one side of the link (local side) the control channel forwards this information to and from the other side of the link (remote side), allowing a single microcontroller to configure the serializer, deserializer, and peripherals. The microcontroller can be located on the serializer side (display applications) and the deserializer side (camera applications). Dual- μ C operations are supported as long as a software-arbitration method is used. The serial link assumes that only one microcontroller is talking at any given time.

Remote-End Operation

When an I²C master initiates communication on the local slave device (the serializer/deserializer directly connected to the master), the remote-side device acts as a master device that sends data forwarded from the local-side device, and forwards any data received from peripherals attached to the remote-side device. This remote-side master device operates according to the timing settings in the I²C Master setting register. Set the master settings to match the timing settings used by the external microcontroller.

Clock-Stretch Timing

The I²C interface uses clock stretching to allow time for data to be forwarded across the serial link. The master microcontroller, along with any attached peripherals, must accept clock stretching of the GMSL devices.

GPO/GPI Control

GPO on the serializer follows GPI transitions on the deserializer. This GPO/GPI function can be used to transmit signals such as a frame sync in a surround-view camera system (see the [Providing a Frame Sync \(Camera Applications\)](#) section).

Table 1. Reverse Control-Channel Modes

| HIM PIN SETTING | REVFASST BIT | REVERSE CONTROL-CHANNEL MODE | MAX UART/I ² C BIT RATE (kbps) |
|-----------------|--------------|--|---|
| Low | X | Legacy reverse control-channel mode (compatible with all GMSL devices) | 1000 |
| High | 0 | High-immunity mode | 500 |
| | 1 | Fast high-immunity mode (requires serial-data rate > 1.25Gbps) | 1000 |

X = Don't care.

Adaptive Line Equalizer

The deserializer includes an adaptive line equalizer to compensate for higher cable attenuation at higher frequencies. The cable equalizer has 12 levels of compensation to handle up to 30m coax and 15m STP cable lengths. At initial lock, the adaptive equalizer selects the optimum compensation level. The device can be programmed to re-adapt periodically, or manually to compensate for any significant changes in the transmission environment.

Spread-Spectrum Tracking

The deserializer can track a spread input clock, eliminating the need for multiple spread clocks.

Cable-Type Configuration and Input MUX

The driver inputs are programmable for two kinds of cable: 100Ω twisted pair and 50Ω coax (contact the factory for devices compatible with 75Ω cables). In coax mode, connect IN0+ to OUT+ of the serializer. Connect IN1+ to OUT+ of the second serializer. Control-channel data is sent to the serializer selected with the GMSL_IN_SEL bit. Leave all unused IN_ pins unconnected, or connect them to ground through 50Ω and a capacitor for increased power-supply rejection. If OUT- is not used, connect OUT- to V_{DD} through a 50Ω resistor (Figure 16). When there are μCs at the serializer, and at each deserializer, only one μC can communicate at a time. Disable forward and reverse channel links according to the communicating deserializer connection to prevent contention in I²C-to-I²C mode.

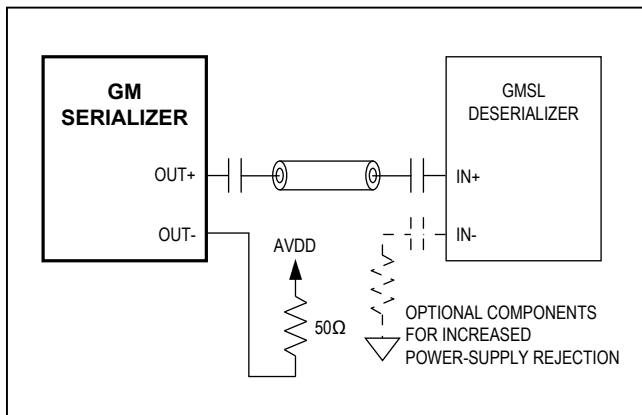


Figure 16. Coax Connection

Crosspoint Switch

The crosspoint switch routes data between the parallel input/output and the SerDes (Figure 17). The anything-to-anything routing assures the mapping between the video source and destination.

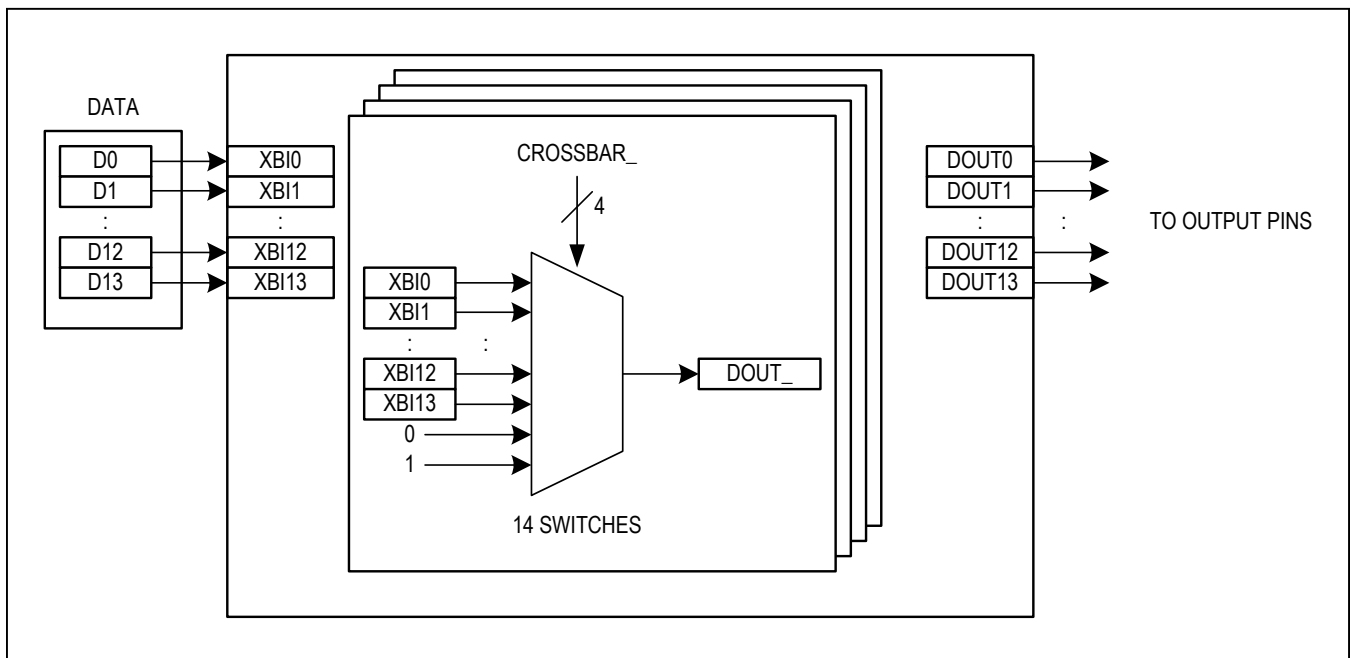


Figure 17. Crosspoint-Switch Dataflow

Shutdown/Sleep Modes

Several sleep and shutdown modes are available when full operation is not needed.

Configuration Link

When the high-speed video link is not needed, or unavailable, a configuration link can be used in its place. In configuration-link mode, the parallel-digital input/output is disabled, the LOCK pin remains low, and the serial link internally generates its own clock, to allow full operation of the control channel (UART/I²C and GPIO).

Serialization Disable

When the serial link is not needed, such as when downstream devices are powered off, the user can disable serialization. In this mode, all forward communication is shut down. The user can reenables serialization either locally or through the reverse channel.

Sleep Mode

To reduce power consumption further, the devices can be put into sleep mode. In this mode, all registers keep their programmed values, and all functions in the device are powered down except for the wake-up detectors on the local I²C/UART interface, and the serial link. Any activity seen by the wake-up detectors temporarily turns on the control-channel interface. During this time, a micro-controller can command the device to exit sleep mode. See the [Entering/Exiting Sleep Mode](#) section.

Power-Down Mode

The lowest power-consumption mode is power-down mode. In this mode, all functions are powered down, and all register values are lost.

Link-Startup Procedure

[Table 2](#) lists the startup procedure for image-sensing applications. The control channel is available after the video link or the configuration link is established. If the deserializer powers up after the serializer, the control channel becomes unavailable until 2ms after power-up.

Table 2. Link-Startup Procedure

| NO. | MC | SERIALIZER | DESERIALIZER |
|-----|--|---|--|
| — | µC connected to deserializer. | Set all configuration inputs. | Set all configuration inputs. |
| 1 | Powers up. Wait t _{PJ} . | Powers up and loads default settings. Establishes video link when valid PCLK available. | Powers up and loads default settings. Locks to video-link signal if available. |
| 1a | (If no PCLK) Programs CLINKEN, SEREN, and/or AUTOCLINK bits. Wait 5ms after each command. | Establishes configuration link. | Locks to config link if available. |
| 1b | (If not locked) Sets any additional configuration bits that are mismatched between serializer and deserializer (e.g BWS, CX/TP). Wait 5ms for lock after each command. | Configuration changed. Reestablishes configuration/video link if needed. | Configuration changed. Locks to configuration/video link. |
| 2 | Sets Register 0x07 configuration bits in the serializer (DBL, BWS, PXL_CRC, etc.). Wait 2ms. | Configuration changed. Reestablishes config/video link if needed | Loss of lock may occur. |
| 3 | Sets Register 0x07 configuration bits in the deserializer (DBL, BWS, PXL_CRC, etc.). Wait 5ms for lock to re-establish. | — | Configuration changed. Locks to configuration/video link. |
| 4 | Writes rest of serializer/deserializer configuration bits. | Configuration changed. | Configuration changed. |
| 5 | Writes camera/peripheral configuration bits. | Forwards commands from µC to serializer. | Forwards commands to camera/peripherals. |
| 5a | If in configuration link: When PCLK is available, set SEREN = 1. Wait 5ms for lock. | Enables video link. | Locks to video link. |

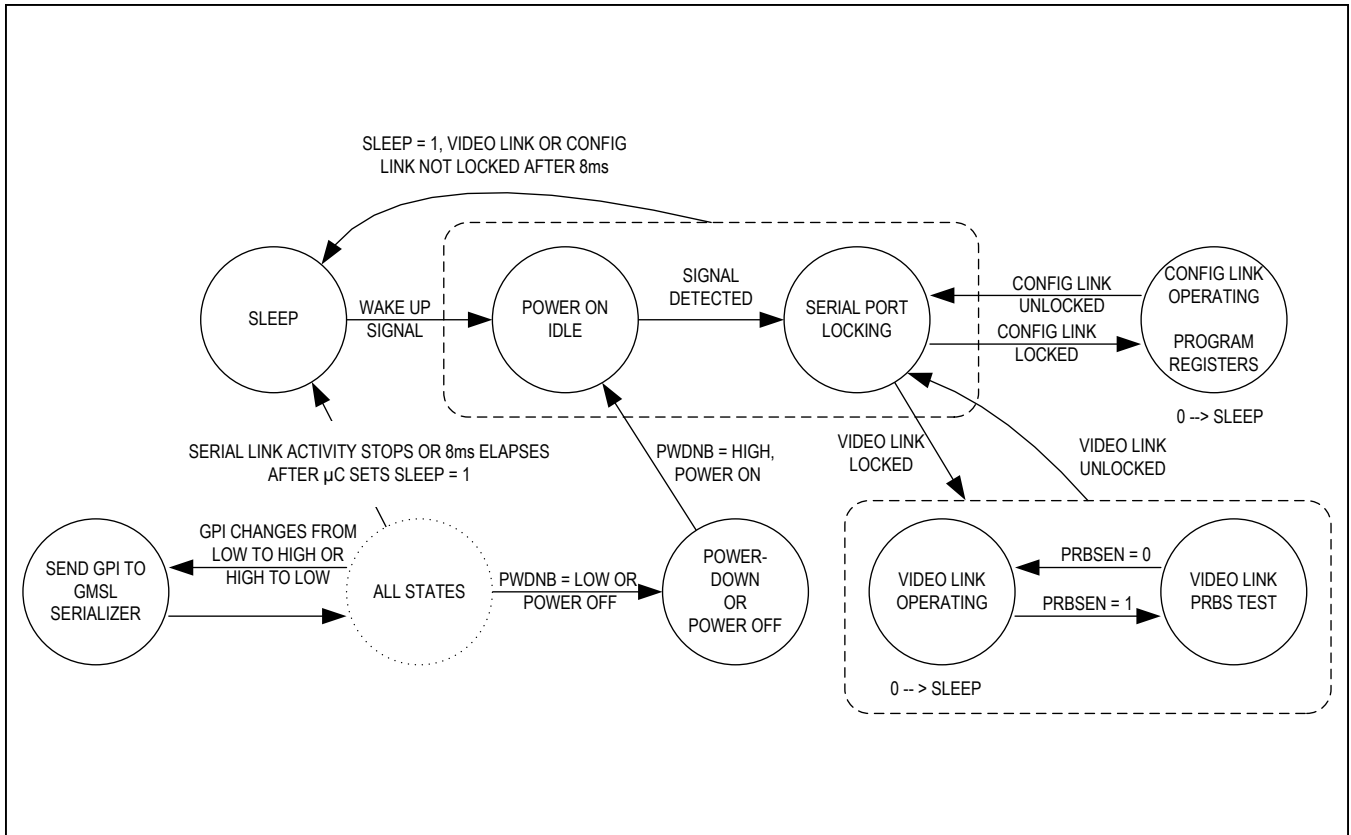


Figure 18. State Diagram

Register Map

| OFFSET | NAME | MSB | | | | | | | LSB |
|--------|-------------|-----------------|-----------------|-----------------|-----------------|--------------|-------------|-----------------|-----------|
| 0x00 | seraddr | SERADDR[6:0] | | | | | | | RSVD |
| 0x01 | desaddr | DESADDR[6:0] | | | | | | | CFG-BLOCK |
| 0x02 | invpinh | INVPINH[5:0] | | | | | SRNG[1:0] | | |
| 0x03 | invpinl | INVPINL[7:0] | | | | | | | |
| 0x04 | main config | LOCKED | OUTENB | PRBSEN | SLEEP | INTTYPE[1:0] | | REVCCEN | FWDDCEN |
| 0x05 | eqtune | I2C-METHOD | DCS | HVTR_MODE | EN_EQ | EQTUNE[3:0] | | | |
| 0x06 | hvsrsrc | HIGHIMM | RSVD | RSVD | RSVD | RSVD | HV_SRC[2:0] | | |
| 0x07 | config | DBL | DRS | BWS | ES | RSVD | HVEN | CXTP | PXL_CRC |
| 0x08 | lflt_en | LFLT_EN_POS | LFLT_EN_NEG | GPI_EN | DISSTAG | ERR_RST | RSVD | RSVD[1:0] | |
| 0x09 | i2csrc A | I2C_SRC_A[6:0] | | | | | | | RSVD |
| 0x0A | i2cdst A | I2C_DST_A[6:0] | | | | | | | RSVD |
| 0x0B | i2csrc B | I2C_SRC_B[6:0] | | | | | | | RSVD |
| 0x0C | i2cdst B | I2C_DST_B[6:0] | | | | | | | RSVD |
| 0x0D | i2cconfig | I2C_LOC_ACK | I2C_SLV_SH[1:0] | | I2C_MST_BT[2:0] | | | I2C_SLV_TO[1:0] | |
| 0x0E | det_thr | DET_THR[7:0] | | | | | | | |
| 0x0F | filt_track | GMSL_IN_SEL | EN_DE_FILTER | EN_HS_FILTER | EN_VS_FILTER | DE_EN | HTRACK | VTRACK | PRBS_TYPE |
| 0x10 | rsvd_10 | RSVD[1:0] | | RSVD | RSVD[3:0] | | | | RSVD |
| 0x11 | rsvd_11 | RSVD[3:0] | | | | RSVD[1:0] | | RSVD[1:0] | |
| 0x12 | underbst | UNDERBST_DET_EN | RSVD | RSVD[1:0] | | RSVD | DIS_WAKE | RSVD | RSVD |
| 0x13 | rsvd_13 | RSVD | RSVD | RSVD | RSVD[4:0] | | | | |
| 0x14 | aeq | AEQ_EN | AEQ_PER_MODE | AEQ_MAN_TRG_REQ | RSVD[4:0] | | | | |
| 0x15 | det_err | DET_ERR[7:0] | | | | | | | |
| 0x16 | prbs_err | PRBS_ERR[7:0] | | | | | | | |
| 0x17 | lf | RSVD | RSVD | PRBS_OK | GPI_IN | LF_NEG[1:0] | | LF_POS[1:0] | |
| 0x18 | rsvd_18 | RSVD[7:0] | | | | | | | |
| 0x19 | rsvd_19 | RSVD[7:0] | | | | | | | |
| 0x1A | rsvd_1a | RSVD[7:0] | | | | | | | |
| 0x1B | i2csel | RSVD | RSVD | RSVD | RSVD | I2CSEL | RSVD | RSVD | RSVD |
| 0x1C | rsvd_1c | RSVD | RSVD | RSVD[5:0] | | | | | |
| 0x1D | aeq_bst | RSVD | RSVD | RSVD | UNDERBOOST_DET | AEQ_BST[3:0] | | | |
| 0x1E | id | ID[7:0] | | | | | | | |

| OFFSET | NAME | MSB | | | | | | LSB |
|--------|----------|-----------|------|------|---------|---------------|--|-----|
| 0x1F | revision | RSVD | RSVD | RSVD | HDCPCAP | REVISION[3:0] | | |
| 0x20 | rsvd_20 | RSVD[7:0] | | | | | | |
| 0x21 | rsvd_21 | RSVD[7:0] | | | | | | |
| 0x22 | rsvd_22 | RSVD[7:0] | | | | | | |
| 0x23 | rsvd_23 | RSVD[7:0] | | | | | | |

| | | | | | | | | | |
|------|-------------|--------------------|-----------|-----------|-----------|----------------------|--------------|-----------|------|
| 0x65 | crossbar 0 | CROSSBAR_N_0[3:0] | | | | CROSSBAR_N+1_0[3:0] | | | |
| 0x66 | crossbar 2 | CROSSBAR_N_2[3:0] | | | | CROSSBAR_N+1_2[3:0] | | | |
| 0x67 | crossbar 4 | CROSSBAR_N_4[3:0] | | | | CROSSBAR_N+1_4[3:0] | | | |
| 0x68 | crossbar 6 | CROSSBAR_N_6[3:0] | | | | CROSSBAR_N+1_6[3:0] | | | |
| 0x69 | crossbar 8 | CROSSBAR_N_8[3:0] | | | | CROSSBAR_N+1_8[3:0] | | | |
| 0x6A | crossbar 10 | CROSSBAR_N_10[3:0] | | | | CROSSBAR_N+1_10[3:0] | | | |
| 0x6B | crossbar 12 | CROSSBAR_N_12[3:0] | | | | CROSSBAR_N+1_12[3:0] | | | |
| 0x96 | rsvd_96 | RSVD[1:0] | | RSVD[1:0] | | RSVD | RSVD | RSVD | RSVD |
| 0x97 | rev_fast | REV_FAST | RSVD | RSVD[5:0] | | | | | |
| 0x98 | rsvd_98 | RSVD | RSVD | RSVD[5:0] | | | | | |
| 0x99 | rsvd_99 | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD |
| 0x9A | rsvd_9a | RSVD | RSVD | RSVD[1:0] | | RSVD[2:0] | | | RSVD |
| 0x9B | rsvd_9b | RSVD | RSVD[1:0] | | RSVD[2:0] | | | RSVD[1:0] | |
| 0x9C | rsvd_9c | RSVD | RSVD[1:0] | | RSVD | RSVD[3:0] | | | |
| 0x9D | rsvd_9d | RSVD | RSVD | RSVD | RSVD | SOFT_PD | RSVD | RSVD | RSVD |
| 0x9E | rsvd_9e | RSVD | RSVD[1:0] | | RSVD[2:0] | | | RSVD | RSVD |
| 0x9F | rsvd_9f | RSVD | RSVD | RSVD | RSVD | RSVD | HPFTUNE[1:0] | | RSVD |
| 0xA0 | rsvd_a0 | RSVD | RSVD | RSVD[1:0] | | RSVD[3:0] | | | |
| 0xA1 | rsvd_a1 | RSVD[2:0] | | | RSVD[4:0] | | | | |
| 0xA2 | rsvd_a2 | RSVD[7:0] | | | | | | | |
| 0xA3 | rsvd_a3 | RSVD[3:0] | | | | RSVD[3:0] | | | |
| 0xA4 | rsvd_a4 | RSVD[2:0] | | | RSVD | RSVD | RSVD | RSVD[1:0] | |
| 0xA5 | rsvd_a5 | RSVD[3:0] | | | | RSVD[1:0] | | RSVD[1:0] | |
| 0xA6 | rsvd_a6 | RSVD | RSVD | RSVD | RSVD | RSVD[1:0] | | RSVD[1:0] | |

| | | | | | | | | | |
|------|---------|-----------|-----------|------|-----------|------|------|------|------|
| 0xC9 | rsvd_c9 | RSVD[7:0] | | | | | | | |
| 0xCA | rsvd_ca | RSVD | RSVD | RSVD | RSVD[1:0] | | RSVD | RSVD | RSVD |
| 0xCB | rsvd_cb | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD |
| 0xCC | rsvd_cc | RSVD | RSVD[6:0] | | | | | | |
| 0xCD | rsvd_cd | RSVD | RSVD[6:0] | | | | | | |

| | | | | | | | | | |
|------|---------|-----------|------|------|------|-----------|--|--|--|
| 0xFD | rsvd_fd | RSVD[7:0] | | | | | | | |
| 0xFE | rsvd_fe | RSVD[3:0] | | | | RSVD[3:0] | | | |
| 0xFF | rsvd_ff | RSVD | RSVD | RSVD | RSVD | RSVD[3:0] | | | |

seraddr (0x00)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|-------------|
| Field | SERADDR[6:0] | | | | | | | RSVD |
| Reset | 1000000b | | | | | | | 0b |
| Access Type | Write, Read | | | | | | | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|--|
| SERADDR | 7:1 | Serializer Address: Serializer device address | 0000000: I ² C write/read address is 0x00, 0x01 0000001: I ² C write/read address is 0x02, 0x03 XXXXXXX: I ² C write/read address is XXXXXXXX0, XXXXXXXX1 1111111: I ² C write/read address is 0xFE, 0xFF |
| RSVD | 0 | Reserved: Do not change from default value | 0: Reserved |

desaddr (0x01)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|-------------|
| Field | DESADDR[6:0] | | | | | | | CFGBLOCK |
| Reset | XXXXXXXb | | | | | | | 0b |
| Access Type | Write, Read | | | | | | | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--|
| DESADDR | 7:1 | Deserializer Address: Deserializer device address (initial value depends on ADD3, ADD2, ADD1, and ADD0 pin settings latched at power-up) | 0000000: I ² C write/read address is 0x00, 0x01 0000001: I ² C write/read address is 0x02, 0x03 XXXXXXX: I ² C write/read address is XXXXXXXX0, XXXXXXXX1 1111111: I ² C write/read address is 0xFE, 0xFF |
| CFGBLOCK | 0 | Configuration Block. When 1, make all registers read only | 0: Set all write/read registers as writable 1: Set all registers as read only |

invpinh (0x02)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|-------------|---|
| Field | INVPINH[5:0] | | | | | | SRNG[1:0] | |
| Reset | 000000b | | | | | | 11b | |
| Access Type | Write, Read | | | | | | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--|
| INVPINH | 7:2 | Invert Output Pins High: Invert output pins D8–D13 | XXXXX0: Do not invert D8 XXXXX1: Invert D8 XXXX0X: Do not invert D9 XXXX1X: Invert D9 XXX0XX: Invert D10 XXX1XX: Do not invert D10 XX0XXX: Do not invert D11 XX1XXX: Invert D11 X0XXXX: Do not invert D12 X1XXXX: Invert D12 0XXXXX: Do not invert D13 1XXXXX: Invert D13 |
| SRNG | 1:0 | Serial Data-Rate Range | 00: 0.5 to 1Gbps 01: 1 to 1.74Gbps 1X: Autodetect serial range |

invpinl (0x03)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field | INVPINL[7:0] | | | | | | | |
| Reset | 0000000b | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--|
| INVPINL | 7:0 | Invert Output Pins Low: Invert output pins D0–D7 | XXXXXXX0: Do not invert D0 XXXXXXX1: Invert D0 XXXXXX0X: Do not invert D1 XXXXXX1X: Invert D1 XXXXX0XX: Do not invert D2 XXXXX1XX: Invert D2 XXXX0XXX: Do not invert D3 XXXX1XXX: Invert D3 XXX0XXXX: Do not invert D4 XXX1XXXX: Invert D4 XX0XXXXX: Do not invert D5 XX1XXXXX: Invert D5 X0XXXXXX: Do not invert D6 X1XXXXXX: Invert D6 0XXXXXXX: Do not invert D7 1XXXXXXX: Invert D7 |

main config (0x04)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------|-------------|-------------|-------------|--------------|---|-------------|-------------|
| Field | LOCKED | OUTENB | PRBSEN | SLEEP | INTTYPE[1:0] | | REVCEN | FWDCEN |
| Reset | Xb | 0b | 0b | 0b | 01b | | 1b | 1b |
| Access Type | Read Only | Write, Read | Write, Read | Write, Read | Write, Read | | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|---|
| LOCKED | 7 | LOCK Output: LOCK output pin level | 0: Video link not locked 1: Video link locked |
| OUTENB | 6 | Outputs Enable Bar: Disable outputs | 0: Enable DOUT_ outputs 1: Disable DOUT_ outputs |
| PRBSEN | 5 | PRBS Test Enable | 0: Set device for normal operation 1: Enable PRBS test |
| SLEEP | 4 | Sleep Mode: Activate sleep mode | 0: Set device for normal operation 1: Put device into sleep mode |
| INTTYPE | 3:2 | Interface Type: Local control-channel interface when I2CSEL = 0 | 00: UART-to-I ² C conversion 01: UART 1X: Disable local control channel |
| REVCEN | 1 | Reverse Control-Channel Enable: Enable reverse control channel from deserializer | 0: Disable reverse control-channel receiver 1: Enable reverser control-channel receiver |
| FWDCEN | 0 | Forward Control-Channel Enable: Enable forward control channel to deserializer | 0: Disable forward control-channel transmitter 1: Enable forward control-channel transmitter |

eqtune (0x05)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-------------|-------------|-------------|-------------|-------------|---|---|---|
| Field | I2C-METHOD | DCS | HVTR_MODE | EN_EQ | EQTUNE[3:0] | | | |
| Reset | 0b | 0b | 1b | 1b | 1001b | | | |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------|------|---|---|
| I2CMETHOD | 7 | I²C Method: Skip register address when converting UART to I ² C | 0: Send the register address during UART-to-I ² C conversion 1: Do not send the register address during UART-to-I ² C conversion |
| DCS | 6 | Driver Current Selection: Driver current selection for CMOS outputs | 0: Set device for normal operation 1: Increase CMOS driver current |
| HVTR_MODE | 5 | HV Tracking Mode: HV tracking allows continuous HSYNC format | 0: Use partial periodic HV tracking 1: Use partial and full periodic HV tracking |
| EN_EQ | 4 | Enable Equalizer: Enable equalizer for manual and adaptive modes | 0: Disable equalization 1: Enable equalization |
| EQTUNE | 3:0 | Equalizer Tune: Equalizer boost level at 750MHz (effective when Adaptive EQ is turned off) | 0000: 1.6dB manual EQ setting 0001: 2.1dB manual EQ setting 0010: 2.8dB manual EQ setting 0011: 3.5dB manual EQ setting 0100: 4.3dB manual EQ setting 0101: 5.2dB manual EQ setting 0110: 6.3dB manual EQ setting 0111: 7.3dB manual EQ setting 1000: 8.5dB manual EQ setting 1001: 9.7dB manual EQ setting 1010: 11dB manual EQ setting 1011: 12.2dB manual EQ setting 11XX: Do Not Use |

hvsrc (0x06)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-------------|-------------|-------------|-------------|-------------|-------------|---|---|
| Field | HIGHIMM | RSVD | RSVD | RSVD | RSVD | HV_SRC[2:0] | | |
| Reset | Xb | 1b | 1b | 0b | 1b | 111b | | |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|--|
| HIGHIMM | 7 | Hgh-Immunity Mode: Default value depends on the state of the HIM input. | 0: Use legacy reverse-channel mode 1: Use high-immunity mode |
| RSVD | 6 | Reserved: Do not change from default value | 1: Reserved |
| RSVD | 5 | Reserved: Do not change from default value | 1: Reserved |
| RSVD | 4 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 3 | Reserved: Do not change from default value | 1: Reserved |
| HV_SRC | 2:0 | HS/VS Source Selection: HS/VS bit selection | 000: Use D18/D19 for HS/VS (use this setting when the serializer is a 3.125Gbps device; otherwise, this setting is for use with the MAX9273 when DBL = 0 or HVEN = 1) 001: Use D14/D15 for HS/VS (for use with the MAX9271/MAX96705 when DBL = 0 or HVEN = 1) 010: Use D12/D13 for HS/VS (for use with the MAX96707 when DBL = 0 or HVEN = 1) 011: Use D0/D1 for HS/VS (for use with the MAX9271/MAX9273/MAX96705/MAX96707 when DBL = 1 and HVEN = 0) 10X: Do Not Use 110: Automatically determine the source of HSYNC/VSYNC (for use with the MAX96707) 111: Automatically determine the source of HSYNC/VSYNC (for use with the MAX96705) |

config (0x07)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Field | DBL | DRS | BWS | ES | RSVD | HVEN | CXTP | PXL_CRC |
| Reset | 0b | 0b | 0b | 0b | 0b | 0b | Xb | 0b |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--|
| DBL | 7 | Double-Output Mode | 0: Use single-rate output 1: Use double-rate output (2x word rate at 1/2x width) |
| DRS | 6 | Data-Rate Select | 0: Use normal data-rate output 1: Use 1/2 rate data output (for use with low data rates) |
| BWS | 5 | Bus-Width Select | 0: Set bus width for 22-bit bus, 24-bit mode 1: Set bus width for 30-bit bus (32-bit mode) |
| ES | 4 | Edge Select | 0: Set output data valid on rising edge of PCLKOUT 1: Set output data valid on falling edge of PCLKOUT |
| RSVD | 3 | Reserved: Do not change from default value | 0: Reserved |
| HVEN | 2 | HS/VS Encoding Enable | 0: Disable HS/VS encoding 1: Enable HS/VS encoding |
| CXTP | 1 | Coax/TP Select | 0: Use differential-output mode (for use with twisted-pair cable) 1: Use single-ended output mode (for use with coax cable) |
| PXL_CRC | 0 | Pixel CRC Enable: Pixel error-detection type | 0: Use 1-bit parity (compatible with all devices) 1: Use 6-bit CRC |

lflt_en (0x08)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---|
| Field | LFLT_EN_POS | LFLT_EN_NEG | GPI_EN | DISSTAG | ERR_RST | RSVD | RSVD[1:0] | |
| Reset | 1b | Xb | 1b | 0b | 0b | 0b | 01b | |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------|------|---|---|
| LFLT_EN_POS | 7 | Line-Fault Detector Enable Positive Line: Enable line-fault detector LMN0 | 0: Disable line-fault detector LMN0 1: Enable line-fault detector LMN0 |
| LFLT_EN_NEG | 6 | Line-Fault Detector Enable Negative Line: Enable line-fault detector LMN1; disabled by default in coax mode and enabled by default in twisted-pair mode | 0: Disable line-fault detector LMN1 1: Enable line-fault detector LMN1 |
| GPI_EN | 5 | GPI-to-GPO Enable: Enable GPI-to-GPO signal transmission to serializer | 0: Disable GPI-to-GPO transmission 1: Enable GPI-to-GPO transmission |
| DISSTAG | 4 | Disable Staggering: Disable staggering of outputs | 0: Enable staggering of DOUT_outputs 1: Disable staggering of DOUT_outputs |
| ERR_RST | 3 | Error Reset: When set to 1, automatically reset DET_ERR 1µs after ERROR pin is asserted | 0: Disable automatic reset of DETERR_register 1: Enable automatic reset of DETERR_register |
| RSVD | 2 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 1:0 | Reserved: Do not change from default value | 01: Reserved |

i2csrc (0x09, 0x0B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|-------------|
| Field | I2C_SRC[6:0] | | | | | | | RSVD |
| Reset | 0b | | | | | | | 0b |
| Access Type | Write, Read | | | | | | | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--|
| I2C_SRC | 7:1 | I²C Address Translator Source: I ² C address translator source A | 0000000: I ² C write/read address is 0x00, 0x01 0000001: I ² C write/read address is 0x02, 0x03 XXXXXXX: I ² C write/read address is XXXXXXXX0, XXXXXXXX1 1111111: I ² C write/read address is 0xFE, 0xFF |
| RSVD | 0 | Reserved: Do not change from default value | 0: Reserved |

i2cdst (0x0A, 0x0C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|-------------|
| Field | I2C_DST[6:0] | | | | | | | RSVD |
| Reset | 0b | | | | | | | 0b |
| Access Type | Write, Read | | | | | | | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|--|
| I2C_DST | 7:1 | I2C address translator destination: I2C address translator destination A | 0000000: I2C write/read address is 0x00, 0x01 0000001: I2C write/read address is 0x02, 0x03 XXXXXXXX: I2C write/read address is XXXXXXXX0, XXXXXXXX1 1111111: I2C write/read address is 0xFE, 0xFF |
| RSVD | 0 | Reserved: Do not change from default value | 0: Reserved |

i2config (0x0D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-----------------|---|-----------------|---|-----------------|---|---|
| Field | I2C_LOC_ACK | I2C_SLV_SH[1:0] | | I2C_MST_BT[2:0] | | I2C_SLV_TO[1:0] | | |
| Reset | 0b | 01b | | 101b | | 10b | | |
| Access Type | Write, Read | Write, Read | | Write, Read | | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------|------|--|--|
| I2C_LOC_ACK | 7 | I2C-to-I2C Slave Local Acknowledge: When forward channel is not available | 0: Disable local acknowledge when forward channel is not available 1: Enable local acknowledge when forward channel is not available |
| I2C_SLV_SH | 6:5 | I2C-to-I2C Slave Setup and Hold Time Setting: Setup, hold (typ) | 00: (352, 117)ns 01: (469, 234)ns 10: (938, 352)ns 11: (1406, 469)ns |
| I2C_MST_BT | 4:2 | I2C-to-I2C Master Bit Rate Setting: Min, typ, max. | 000: (6.61, 8.47, 9.92)kbps bit rate 001: (22.1, 28.3, 33.2)kbps bit rate 010: (66.1, 84.7, 99.2)kbps bit rate 011: (82, 105, 123)kbps bit rate 100: (136, 173, 203)kbps bit rate 101: (265, 339, 397)kbps bit rate 110: (417, 533, 625)kbps bit rate 111: (654, 837, 980)kbps bit rate |
| I2C_SLV_TO | 1:0 | I2C-to-I2C Slave Remote-Side Timeout Setting: Typ | 00: 64µs timeout 01: 256µs timeout 10: 1024µs timeout 11: I2C timeout disabled |

det_thr (0x0E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field | DET_THR[7:0] | | | | | | | |
| Reset | 0000000b | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--|
| DET_THR | 7:0 | Detected Errors Threshold: Threshold for detected errors | 00000000: Value is 0 00000001: Value is 1, XXXXXXXX 11111111: Value is 255 |

filt_track (0x0F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Field | GMSL_IN_SEL | EN_DE_FILT | EN_HS_FILT | EN_VS_FILT | DE_EN | HTRACK | VTRACK | PRBS_TYPE |
| Reset | 0b | 0b | 0b | 0b | 0b | 0b | 0b | 1b |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-------------|------|---|---|
| GMSL_IN_SEL | 7 | Select GMSL Input | 0: Select IN0+, IN0- 1: Select IN1+, IN1- |
| EN_DE_FILT | 6 | Enable DE Glitch Filtering: Enable glitch filtering on DOUT11 | 0: Disable glitch filtering on DOUT11 1: Enable glitch filtering on DOUT11 |
| EN_HS_FILT | 5 | Enable HS Glitch Filtering: Enable glitch filtering on DOUT12 | 0: Disable glitch filtering on DOUT12 1: Enable glitch filtering on DOUT12 |
| EN_VS_FILT | 4 | Enable VS Glitch Filtering: Enable glitch filtering on DOUT13 | 0: Disable glitch filtering on DOUT13 1: Enable glitch filtering on DOUT13 |
| DE_EN | 3 | DE Processing Enable: Enable processing separate HS and DE signals | 0: Disable processing HS and DE signals 1: Enable processing HS and DE signals |
| HTRACK | 2 | HS Tracking Enable | 0: Disable HS tracking 1: Enable HS tracking |
| VTRACK | 1 | VS Tracking Enable | 0: Disable VS tracking 1: Enable VS tracking |
| PRBS_TYPE | 0 | PRBS Type Select: PRBS type select | 0: GMSL default style PRBS test 1: MAX9272 style PRBS |

rsvd_10 (0x10)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|-------------|-------------|---|---|---|-------------|
| Field | RSVD[7:6] | | RSVD | RSVD[4:1] | | | | RSVD |
| Reset | 00b | | 0b | 0001b | | | | 0b |
| Access Type | Write, Read | | Write, Read | Write, Read | | | | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|----------------|
| RSVD | 7:6 | Reserved: Do not change from default value | 00: Reserved |
| RSVD | 5 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 4:1 | Reserved: Do not change from default value | 0001: Reserved |
| RSVD | 0 | Reserved: Do not change from default value | 0: Reserved |

rsvd_11

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|-------------|---|-------------|---|
| Field | RSVD[7:4] | | | | RSVD[3:2] | | RSVD[1:0] | |
| Reset | 1111b | | | | 00b | | 00b | |
| Access Type | Write, Read | | | | Write, Read | | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|----------------|
| RSVD | 7:4 | Reserved: Do not change from default value | 1111: Reserved |
| RSVD | 3:2 | Reserved: Do not change from default value | 00: Reserved |
| RSVD | 1:0 | Reserved: Do not change from default value | 00: Reserved |

underbst (0x12)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------------|-------------|-------------|---|-------------|---------------|-------------|-------------|
| Field | UNDER- BST_DET_ EN | RSVD | RSVD[5:4] | | RSVD | DIS_ RWAKE | RSVD | RSVD |
| Reset | 0b | 1b | 01b | | 0b | 0b | 1b | 0b |
| Access Type | Write, Read | Write, Read | Write, Read | | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------|------|---|---|
| UNDERBST_DET_EN | 7 | Underboost-Detection Enable: Allow underboost detection driving ERRORB pin | 0: Disable underboost detection driving ERROR pin 1: Enable underboost detection driving ERROR pin |
| RSVD | 6 | Reserved: Do not change from default value | 1: Reserved |
| RSVD | 5:4 | Reserved: Do not change from default value | 01: Reserved |
| RSVD | 3 | Reserved: Do not change from default value | 0: Reserved |
| DIS_RWAKE | 2 | Disable Remote Wake-up | 0: Enable remote wake-up 1: Disable remote wake-up |
| RSVD | 1 | Reserved: Do not change from default value | 1: Reserved |
| RSVD | 0 | Reserved: Do not change from default value | 0: Reserved |

rsvd_13 (0x13)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|----------------------|-------------|---|---|---|---|
| Field | RSVD | RSVD | RSVD | RSVD[4:0] | | | | |
| Reset | 1b | 1b | 0b | 01101b | | | | |
| Access Type | Write, Read | Write, Read | Write 1 to Set, Read | Write, Read | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|-----------------|
| RSVD | 7 | Reserved: Do not change from default value | 1: Reserved |
| RSVD | 6 | Reserved: Do not change from default value | 1: Reserved |
| RSVD | 5 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 4:0 | Reserved: Do not change from default value | 01101: Reserved |

aeq (0x14)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|--------------|----------------------|-------------|---|---|---|---|
| Field | AEQ_EN | AEQ_PER_MODE | AEQ_MAN_TRG_REQ | RSVD[4:0] | | | | |
| Reset | 1b | 0b | 0b | 00000b | | | | |
| Access Type | Write, Read | Write, Read | Write 1 to Set, Read | Write, Read | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------|------|--|---|
| AEQ_EN | 7 | Adaptive Equalization Enable: Enable adaptive equalization | 0: Disable AEQ 1: Enable AEQ |
| AEQ_PER_MODE | 6 | Adaptive Equalization Periodic Mode Select | 0: Set AEQ to use nonperiodic mode 1: Set AEQ to use periodic mode |
| AEQ_MAN_TRG_REQ | 5 | Adaptive Equalization Manual Fine-Tune Request: Rising edge of this register triggers AEQ fine tuning when not in periodic mode | 0: Do not trigger AEQ fine tuning 1: Write 1 to this bit to manually trigger the AEQ fine tuning |
| RSVD | 4:0 | Reserved: Do not change from default value | 00000: Reserved |

det_err (0x15)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field | DET_ERR[7:0] | | | | | | | |
| Reset | XXXXXXXXb | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------------------------|---|
| DET_ERR | 7:0 | Detected Error Counter | 00000000: Value is 0 00000001: Value is 1 XXXXXXXX 11111111: Value is 255. |

prbs_err (0x16)

| | | | | | | | | |
|--------------------|---------------|----------|----------|----------|----------|----------|----------|----------|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | PRBS_ERR[7:0] | | | | | | | |
| Reset | XXXXXXXXb | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------|-------------|---------------------------|--|
| PRBS_ERR | 7:0 | PRBS Error Counter | 00000000: Value is 0 00000001: Value is 1 XXXXXXXX 11111111: Value is 255 |

If (0x17)

| | | | | | | | | |
|--------------------|-----------|-----------------|-----------|-----------|-------------|----------|-------------|----------|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | RSVD | RSVD | PRBS_OK | GPI_IN | LF_NEG[1:0] | | LF_POS[1:0] | |
| Reset | Xb | Xb | Xb | Xb | XXb | | XXb | |
| Access Type | Read Only | Read Clears All | Read Only | Read Only | Read Only | | Read Only | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|-----------------|-------------|--|--|
| RSVD | 7 | Reserved: Do not change from default value | X: Reserved |
| RSVD | 6 | Reserved: | X: Reserved |
| PRBS_OK | 5 | PRBS OK: MAX9271/MAX9273-compatible PRBS test for link is terminated normally; check PRBS_ERR register for the PRBS success; for other SerDes read PRBS_ERR registers | 0: No MAX9271/MAX9273-compatible PRBS test completed 1: MAX9271/MAX9273-compatible PRBS test completed normally |
| GPI_IN | 4 | GPI Pin Level | 0: GPI is input low 1: GPI is input high |
| LF_NEG | 3:2 | Line Fault: Line-fault status of the indicated input LF_POS → LMN0 LF_NEG → LMN1 | 00: Short to battery detected 01: Short to ground detected 10: No faults detected 11: Open cable detected |
| LF_POS | 1:0 | Line Fault: Line-fault status of the indicated input LF_POS → LMN0 LF_NEG → LMN1 | 00: Short to battery detected 01: Short to ground detected 10: No faults detected 11: Open cable detected |

rsvd_18 (0x18)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------|---|---|---|---|---|---|---|
| Field | RSVD[7:0] | | | | | | | |
| Reset | XXXXXXXXb | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--------------------|
| RSVD | 7:0 | Reserved: Do not change from default value | XXXXXXXX: Reserved |

rsvd_19 (0x19)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------|---|---|---|---|---|---|---|
| Field | RSVD[7:0] | | | | | | | |
| Reset | XXXXXXXXb | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-----------------|--------------------|
| RSVD | 7:0 | Reserved | XXXXXXXX: Reserved |

rsvd_1a (0x1A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------|---|---|---|---|---|---|---|
| Field | RSVD[7:0] | | | | | | | |
| Reset | XXXXXXXXb | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-----------------|--------------------|
| RSVD | 7:0 | Reserved | XXXXXXXX: Reserved |

i2csel (0x1B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|-------------|-----------|-----------------|-----------|-----------|
| Field | RSVD | RSVD | RSVD | RSVD | I2CSEL | RSVD | RSVD | RSVD |
| Reset | 0b | 0b | 0b | 0b | Xb | Xb | Xb | Xb |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Read Only | Read Clears All | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|--|
| RSVD | 7 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 6 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 5 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 4 | Reserved: Do not change from default value | 0: Reserved |
| I2CSEL | 3 | I2CSEL Pin Level: Detected I2CSEL pin level | 0: Low-I2CSEL pin detected (UART) 1: High-I2CSEL pin detected (I2C) |
| RSVD | 2 | Reserved: | X: Reserved |
| RSVD | 1 | Reserved: Do not change from default value | X: Reserved |
| RSVD | 0 | Reserved: Do not change from default value | X: Reserved |

rsvd_1c (0x1C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-----------|---|---|---|---|---|
| Field | RSVD | RSVD | RSVD[5:0] | | | | | |
| Reset | 0b | 0b | XXXXXXb | | | | | |
| Access Type | Write, Read | Write, Read | Read Only | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|------------------|
| RSVD | 7 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 6 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 5:0 | Reserved: | XXXXXX: Reserved |

aeq_bst (0x1D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|-----------------|--------------|---|---|---|
| Field | RSVD | RSVD | RSVD | UNDER-BOOST_DET | AEQ_BST[3:0] | | | |
| Reset | 0b | 0b | 0b | Xb | XXXXb | | | |
| Access Type | Write, Read | Write, Read | Write, Read | Read Only | Read Only | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------------|------|---|--|
| RSVD | 7 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 6 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 5 | Reserved: Do not change from default value | 0: Reserved |
| UNDERBOOST_DET | 4 | Underboost Detected: '1' indicates that an underboost is detected when the AEQ is at the maximum setting | 0: Normal operation 1: Underboost (at maximum AEQ gain) detected |
| AEQ_BST | 3:0 | Adaptive Equalizer Boost Value: Selected adaptive equalizer value; settings correspond to gain at 750MHz | 0000: 1.6dB EQ setting 0001: 2.1dB EQ setting 0010: 2.8dB EQ setting 0011: 3.5dB EQ setting 0100: 4.3dB EQ setting 0101: 5.2dB EQ setting 0110: 6.3dB EQ setting 0111: 7.3dB EQ setting 1000: 8.5dB EQ setting 1001: 9.7dB EQ setting 1010: 11dB EQ setting 1011: 12.2dB EQ setting 11XX: Reserved |

id (0x1E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------|---|---|---|---|---|---|---|
| Field | ID[7:0] | | | | | | | |
| Reset | XXXXXXXXb | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--------------------|
| ID | 7:0 | Device ID: 8-bit value depends on the GMSL device attached | 01001100: MAX96708 |

revision (0x1F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|-----------|---------------|---|---|---|
| Field | RSVD | RSVD | RSVD | HDCPCAP | REVISION[3:0] | | | |
| Reset | 0b | 0b | 0b | Xb | XXXXb | | | |
| Access Type | Write, Read | Write, Read | Write, Read | Read Only | Read Only | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|---|
| RSVD | 7 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 6 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 5 | Reserved: Do not change from default value | 0: Reserved |
| HDCPCAP | 4 | HDCP Capability: '1' = HDCP capable | 0: Device does not have HDCP 1: Device is HDCP capable |
| REVISION | 3:0 | Device Revision | 0000: Value is 0 0001: Value is 1 1111: Value is 15 |

rsvd (0x20 to 0x23)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------|---|---|---|---|---|---|---|
| Field | RSVD[7:0] | | | | | | | |
| Reset | XXXXXXXXb | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|------------------|--------------------|
| RSVD | 7:0 | Reserved: | XXXXXXXX: Reserved |

crossbar (0x65 to 0x6B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|-------------------|---|---|---|
| Field | CROSSBAR_N[3:0] | | | | CROSSBAR_N+1[3:0] | | | |
| Reset | XXXXb | | | | XXXXb | | | |
| Access Type | Write, Read | | | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|--------------|------|---|---|
| CROSSBAR_N | 7:4 | Crossbar Setting: CROSSBAR selects the internal signal to connect to the output pin, DOUT_. Register crossbar_(N) contains settings for two outputs, with CROSSBAR_(N) at D[7:4] and CROSSBAR_(N+1) at D[3:0]. Default settings for CROSSBAR(N) connects internal signal D(N) to its respective DOUT(N) pin. | 0000: Connect D0 to output 0001: Connect D1 to output ::: 1101: Connect D13 to output 1110: Force output low 1111: Force output high |
| CROSSBAR_N+1 | 3:0 | Crossbar Setting: CROSSBAR selects the internal signal to connect to the output pin, DOUT_. Register crossbar_(N) contains settings for two outputs, with CROSSBAR_(N) at D[7:4] and CROSSBAR_(N+1) at D[3:0]. Default settings for CROSSBAR(N) connects internal signal D(N) to its respective DOUT(N) pin. | 0000: Connect D0 to output 0001: Connect D1 to output ::: 1101: Connect D13 to output 1110: Force output low 1111: Force output high |

rsvd_96 (0x96)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-------------|---|-------------|---|-------------|-------------|-------------|-------------|
| Field | RSVD[1:0] | | RSVD[1:0] | | RSVD | RSVD | RSVD | RSVD |
| Reset | 01b | | 01b | | 0b | 0b | 0b | 1b |
| Access Type | Write, Read | | Write, Read | | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--------------|
| RSVD | 7:6 | Reserved: Do not change from default value | 01: Reserved |
| RSVD | 5:4 | Reserved: Do not change from default value | 01: Reserved |
| RSVD | 3 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 2 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 1 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 0 | Reserved: Do not change from default value | 1: Reserved |

rev_fast (0x97)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-------------|-------------|-------------|---|---|---|---|---|
| Field | REV_FAST | RSVD | RSVD[5:0] | | | | | |
| Reset | 0b | 0b | 100010b | | | | | |
| Access Type | Write, Read | Write, Read | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|---|
| REV_FAST | 7 | Reverse-Channel Fast Mode | 0: Disable reverse-channel fast mode 1: Enable reverse-channel fast mode |
| RSVD | 6 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 5:0 | Reserved: Do not change from default value | 100010: Reserved |

rsvd_98 (0x98)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-------------|-------------|-------------|---|---|---|---|---|
| Field | RSVD | RSVD | RSVD[5:0] | | | | | |
| Reset | 1b | 0b | 011010b | | | | | |
| Access Type | Write, Read | Write, Read | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|------------------|
| RSVD | 7 | Reserved: Do not change from default value | 1: Reserved |
| RSVD | 6 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 5:0 | Reserved: Do not change from default value | 011010: Reserved |

rsvd_99 (0x99)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Field | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD |
| Reset | 0b | 1b | 0b | 0b | 0b | 0b | 0b | 0b |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|-------------|
| RSVD | 7 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 6 | Reserved: Do not change from default value | 1: Reserved |
| RSVD | 5 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 4 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 3 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 2 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 1 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 0 | Reserved: Do not change from default value | 0: Reserved |

rsvd_9a (0x9A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-------------|-------------|-------------|---|-------------|---|---|-------------|
| Field | RSVD | RSVD | RSVD[1:0] | | RSVD[2:0] | | | RSVD |
| Reset | 0b | 0b | 10b | | 010b | | | 0b |
| Access Type | Write, Read | Write, Read | Write, Read | | Write, Read | | | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|---------------|
| RSVD | 7 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 6 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 5:4 | Reserved: Do not change from default value | 10: Reserved |
| RSVD | 3:1 | Reserved: Do not change from default value | 010: Reserved |
| RSVD | 0 | Reserved: Do not change from default value | 0: Reserved |

rsvd_9b (0x9B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|---|-------------|---|---|-------------|---|
| Field | RSVD | RSVD[1:0] | | RSVD[2:0] | | | RSVD[1:0] | |
| Reset | 0b | 01b | | 001b | | | 10b | |
| Access Type | Write, Read | Write, Read | | Write, Read | | | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|---------------|
| RSVD | 7 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 6:5 | Reserved: Do not change from default value | 01: Reserved |
| RSVD | 4:2 | Reserved: Do not change from default value | 001: Reserved |
| RSVD | 1:0 | Reserved: Do not change from default value | 10: Reserved |

rsvd_9c (0x9C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|---|-------------|-------------|---|---|---|
| Field | RSVD | RSVD[1:0] | | RSVD | RSVD[3:0] | | | |
| Reset | 0b | 10b | | 1b | 0100b | | | |
| Access Type | Write, Read | Write, Read | | Write, Read | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|----------------|
| RSVD | 7 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 6:5 | Reserved: Do not change from default value | 10: Reserved |
| RSVD | 4 | Reserved: Do not change from default value | 1: Reserved |
| RSVD | 3:0 | Reserved: Do not change from default value | 0100: Reserved |

rsvd_9d (0x9D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|-------------|----------------------|-------------|-------------|-------------|
| Field | RSVD | RSVD | RSVD | RSVD | SOFT_PD | RSVD | RSVD | RSVD |
| Reset | 0b | 0b | 1b | 01b | 0b | 0b | 0b | 0b |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write 1 to Set, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--|
| RSVD | 7 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 6 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 5 | Reserved: Do not change from default value | 1: Reserved |
| RSVD | 4 | Reserved: Do not change from default value | 01: Reserved |
| SOFT_PD | 3 | Reserved: Do not change from default value | 0: Normal operation 1: Reset the device |
| RSVD | 2 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 1 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 0 | Reserved: Do not change from default value | 0: Reserved |

rsvd_9e (0x9E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-------------|-------------|---|-------------|---|---|-------------|-------------|
| Field | RSVD | RSVD[1:0] | | RSVD[2:0] | | | RSVD | RSVD |
| Reset | 1b | 10b | | 010b | | | 0b | 0b |
| Access Type | Write, Read | Write, Read | | Write, Read | | | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|---------------|
| RSVD | 7 | Reserved: Do not change from default value | 1: Reserved |
| RSVD | 6:5 | Reserved: Do not change from default value | 10: Reserved |
| RSVD | 4:2 | Reserved: Do not change from default value | 010: Reserved |
| RSVD | 1 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 0 | Reserved: Do not change from default value | 0: Reserved |

rsvd_9f (0x9F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-------------|-------------|-------------|-------------|-------------|--------------|---|-------------|
| Field | RSVD | RSVD | RSVD | RSVD | RSVD | HPFTUNE[1:0] | | RSVD |
| Reset | 0b | 0b | 0b | 0b | 0b | 01b | | 0b |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|--|
| RSVD | 7 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 6 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 5 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 4 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 3 | Reserved: Do not change from default value | 0: Reserved |
| HPFTUNE | 2:1 | Equalizer High-Pass Filter Cutoff Frequency | 00: 7.5MHz cutoff frequency 01: 3.75MHz cutoff frequency 10: 2.5MHz cutoff frequency 11: 1.87MHz cutoff frequency |
| RSVD | 0 | Reserved: Do not change from default value | 0: Reserved |

rsvd_a0 (0xA0)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-------------|-------------|-------------|---|-------------|---|---|---|
| Field | RSVD | RSVD | RSVD[1:0] | | RSVD[3:0] | | | |
| Reset | 1b | 0b | 10b | | 1110b | | | |
| Access Type | Write, Read | Write, Read | Write, Read | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|----------------|
| RSVD | 7 | Reserved: Do not change from default value | 1: Reserved |
| RSVD | 6 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 5:4 | Reserved: Do not change from default value | 10: Reserved |
| RSVD | 3:0 | Reserved: Do not change from default value | 1110: Reserved |

rsvd_a1(0xA1)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|-------------|---|---|---|---|
| Field | RSVD[2:0] | | | RSVD[4:0] | | | | |
| Reset | 010b | | | 00100b | | | | |
| Access Type | Write, Read | | | Write, Read | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|-----------------|
| RSVD | 7:5 | Reserved: Do not change from default value | 010: Reserved |
| RSVD | 4:0 | Reserved: Do not change from default value | 00100: Reserved |

rsvd_a2 (0xA2)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field | RSVD[7:0] | | | | | | | |
| Reset | 00100000b | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|--------------------|
| RSVD | 7:0 | Reserved: Do not change from default value | 00100000: Reserved |

rsvd_a3 (0xA3)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|-------------|---|---|---|---|
| Field | RSVD[3:0] | | | RSVD[3:0] | | | | |
| Reset | 0110b | | | 1011b | | | | |
| Access Type | Write, Read | | | Write, Read | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|----------------|
| RSVD | 7:4 | Reserved: Do not change from default value | 0110: Reserved |
| RSVD | 3:0 | Reserved: Do not change from default value | 1011: Reserved |

rsvd_a4 (0xA4)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|-------------|-------------|-------------|-------------|---|
| Field | RSVD[2:0] | | | RSVD | RSVD | RSVD | RSVD[1:0] | |
| Reset | 101b | | | 1b | 0b | 1b | 01b | |
| Access Type | Write, Read | | | Write, Read | Write, Read | Write, Read | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|---------------|
| RSVD | 7:5 | Reserved: Do not change from default value | 101: Reserved |
| RSVD | 4 | Reserved: Do not change from default value | 1: Reserved |
| RSVD | 3 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 2 | Reserved: Do not change from default value | 1: Reserved |
| RSVD | 1:0 | Reserved: Do not change from default value | 01: Reserved |

rsvd_a5 (0xA5)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|-------------|---|-------------|---|
| Field | RSVD[3:0] | | | | RSVD[1:0] | | RSVD[1:0] | |
| Reset | 1100b | | | | 11b | | 01b | |
| Access Type | Write, Read | | | | Write, Read | | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|----------------|
| RSVD | 7:4 | Reserved: Do not change from default value | 1100: Reserved |
| RSVD | 3:2 | Reserved: Do not change from default value | 11: Reserved |
| RSVD | 1:0 | Reserved: Do not change from default value | 01: Reserved |

rsvd_a6 (0xA6)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|-------------|-------------|---|-------------|---|
| Field | RSVD | RSVD | RSVD | RSVD | RSVD[1:0] | | RSVD[1:0] | |
| Reset | 0b | 0b | 0b | 0b | 00b | | 01b | |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--------------|
| RSVD | 7 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 6 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 5 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 4 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 3:2 | Reserved: Do not change from default value | 00: Reserved |
| RSVD | 1:0 | Reserved: Do not change from default value | 01: Reserved |

rsvd_c9 (0xC9)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------|---|---|---|---|---|---|---|
| Field | RSVD[7:0] | | | | | | | |
| Reset | XXXXXXXXb | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--------------------|
| RSVD | 7:0 | Reserved: Do not change from default value | XXXXXXXX: Reserved |

rsvd_ca (0xCA)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-----------|-----------|-----------|---|-----------|-----------|-----------|
| Field | RSVD | RSVD | RSVD | RSVD[1:0] | | RSVD | RSVD | RSVD |
| Reset | 0b | Xb | Xb | XXb | | Xb | Xb | Xb |
| Access Type | Write, Read | Read Only | Read Only | Read Only | | Read Only | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--------------|
| RSVD | 7 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 6 | Reserved: Do not change from default value | X: Reserved |
| RSVD | 5 | Reserved: Do not change from default value | X: Reserved |
| RSVD | 4:3 | Reserved: Do not change from default value | XX: Reserved |
| RSVD | 2 | Reserved: Do not change from default value | X: Reserved |
| RSVD | 1 | Reserved: Do not change from default value | X: Reserved |
| RSVD | 0 | Reserved: Do not change from default value | X: Reserved |

rsvd_cb (0xCB)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-------------|
| Field | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD | RSVD |
| Reset | Xb | Xb | Xb | Xb | Xb | Xb | Xb | 0b |
| Access Type | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|-------------|
| RSVD | 7 | Reserved: Do not change from default value | X: Reserved |
| RSVD | 6 | Reserved: Do not change from default value | X: Reserved |
| RSVD | 5 | Reserved: Do not change from default value | X: Reserved |
| RSVD | 4 | Reserved: Do not change from default value | X: Reserved |
| RSVD | 3 | Reserved: | X: Reserved |
| RSVD | 2 | Reserved: | X: Reserved |
| RSVD | 1 | Reserved: | X: Reserved |
| RSVD | 0 | Reserved: Do not change from default value | 0: Reserved |

rsvd_cc (0xCC)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-----------|---|---|---|---|---|---|
| Field | RSVD | RSVD[6:0] | | | | | | |
| Reset | 0b | XXXXXXXXb | | | | | | |
| Access Type | Write, Read | Read Only | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--------------------|
| RSVD | 7 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 6:0 | Reserved: Do not change from default value | XXXXXXXX: Reserved |

rsvd_cd (0xCD)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|-----------|---|---|---|---|---|
| Field | RSVD | | RSVD[6:0] | | | | | |
| Reset | 0b | | XXXXXXXXb | | | | | |
| Access Type | Write, Read | | Read Only | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|--------------------|
| RSVD | 7 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 6:0 | Reserved: Do not change from default value | XXXXXXXX: Reserved |

rsvd_fd (0xFD)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field | RSVD[7:0] | | | | | | | |
| Reset | 0b | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|-------------|
| RSVD | 7:0 | Reserved: Do not change from default value | 0: Reserved |

rsvd_fe (0xFE)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|-------------|---|---|---|
| Field | RSVD[3:0] | | | | RSVD[3:0] | | | |
| Reset | 0b | | | | 0b | | | |
| Access Type | Write, Read | | | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|-------------|
| RSVD | 7:4 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 3:0 | Reserved: Do not change from default value | 0: Reserved |

rsvd_ff (0xFF)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|-------------|-----------|---|---|---|
| Field | RSVD | RSVD | RSVD | RSVD | RSVD[3:0] | | | |
| Reset | 0b | 0b | 0b | 0b | XXXXb | | | |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Read Only | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|---|----------------|
| RSVD | 7 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 6 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 5 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 4 | Reserved: Do not change from default value | 0: Reserved |
| RSVD | 3:0 | Reserved: Do not change from default value | XXXX: Reserved |

Applications Information

Parallel Interface

The CMOS parallel-interface data width is programmable and depends on the application. Using a larger width (BWS = 1) results in a lower-pixel clock rate, while a smaller width (BWS = 0) allows a higher-pixel clock rate.

Bus Data Width

The bus data width depends on the selected modes. The available bus width is less when using error detection or when in double mode (DBL = 1). [Table 3](#) shows the available bit widths and default mapping for various modes.

Table 3. Output-Data Width Selection

| REGISTER BIT SETTINGS | | | | OUTPUT MAPPING |
|-----------------------|-----|---------|------|-------------------|
| DBL | BWS | PXL_CRC | HVEN | |
| 1 | 1 | 1 | 1 | DOUT11:0, HS, VS |
| 1 | 1 | 1 | 0 | DOUT11:0 |
| 1 | 1 | 0 | 1 | DOUT11:0*, HS, VS |
| 1 | 1 | 0 | 0 | DOUT13:0* |
| 1 | 0 | 1 | 1 | DOUT7:0, HS, VS |
| 1 | 0 | 1 | 0 | DOUT7:0 |
| 1 | 0 | 0 | 1 | DOUT10:0, HS, VS |
| 1 | 0 | 0 | 0 | DOUT10:0 |
| 0 | 1 | 1 | 1 | DOUT11:0*, HS, VS |
| 0 | 1 | 1 | 0 | DOUT13:0* |
| 0 | 1 | 0 | 1 | DOUT11:0*, HS, VS |
| 0 | 1 | 0 | 0 | DOUT13:0* |
| 0 | 0 | 1 | 1 | DOUT11:0*, HS, VS |
| 0 | 0 | 1 | 0 | DOUT13:0* |
| 0 | 0 | 0 | 1 | DOUT11:0*, HS, VS |
| 0 | 0 | 0 | 0 | DOUT13:0* |

*The bit width is limited by the number of available outputs.

Bus Data Rates

The bus data rate depends on the settings BWS and DBL. [Table 4](#) lists the available PCLK rates available for different bus-width settings. For lower PCLK rates, set DBL = 0 (if DBL = 1 in both the serializer and deserializer).

Crossbar Switch

By default, the crossbar switch connects the serializer input pins DIN_ and HS/VS (when HV encoding is used) to the corresponding deserializer output pins DOUT_ and HS/VS when DBL of the serializer and deserializer match. When there is a DBL mismatch use [Table 5](#), [Table 66](#), and [Table 7](#) to map the serial bits to the crossbar inputs. Reprogram the crossbar switch when changing the output pin assignments.

Crossbar Switch Programming

Each output pin can be assigned any of the 14 DOUT signals. Multiple outputs can share the same input. To force an output low, and ignore the input, set CROSSBAR_bit = 1110. To force an output high set CROSSBAR_ = 1111.

Recommended Crossbar Switch Programming Procedure

The following procedure programs the crossbar switch to reassign input/output pin locations:

- 1) For the crossbar output equivalent of DOUT0 (XBO0) select which pin to map (e.g., DOUT4 → XBI4).
- 2) Set the crossbar bits (CROSSBAR0) to the desired selected mapped input (e.g., CROSSBAR0 = 0100).
- 3) Repeat for the other crossbar outputs.

Table 4. Data-Rate Selection Table

| DRS | DBL | BWS | PCLK RANGE (MHZ) |
|-----|-----|-----|------------------|
| 0 | 1 | 1 | 25 to 87 |
| 0 | 1 | 0 | 33.3 to 116 |
| 0 | 0 | 1 | 12.5 to 43.5 |
| 0 | 0 | 0 | 16.7 to 58 |
| 1* | 0 | 1 | 6.25 to 12.5 |
| 1* | 0 | 0 | 8.33 to 16.7 |

*Use DRS = 1 with legacy devices only (MAX92XX).

Table 5. Output Map (DBL = 0 or DBL = 1, First Word)

| BIT SETTING | | | | | | OUTPUT BITS (FIRST WORD) | | | | | | | | | | | | | |
|-------------|----|----|----|----|-----|--------------------------|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|
| DB | HV | BW | CR | DE | SC* | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 | A11 | A12 | A13 |
| 0 | 0 | X | X | 0 | 1 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 14 | 15 |
| 0 | 0 | X | X | 1 | 1 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 13 | 14 | 15 |
| 0 | 0 | X | X | X | 2 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
| 0 | 1 | X | X | 1 | 1 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 13 | H | V |
| 0 | 1 | X | X | 1 | 2 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | H | V |
| 0 | 1 | X | X | 0 | 1,2 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | H | V |
| 1 | 0 | 0 | 0 | X | 3 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | Z | Z | Z |
| 1 | 0 | 0 | 1 | X | 3 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | Z | Z | Z | Z | Z | Z |
| 1 | 0 | 1 | 0 | X | 3 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
| 1 | 0 | 1 | 1 | X | 3 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | Z | Z |
| 1 | 1 | 0 | 0 | 0 | 1,2 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | Z | HL | VL |
| 1 | 1 | 0 | 0 | 1 | 1,2 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | Z | 10 | HL | VL |
| 1 | 1 | 0 | 1 | 0 | 1,2 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | Z | Z | Z | Z | HL | VL |
| 1 | 1 | 0 | 1 | 1 | 1,2 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Z | Z | Z | Z | 7 | HL | VL |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 13 | HL | VL |
| 1 | 1 | 1 | 0 | 1 | 2 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | HL | VL |
| 1 | 1 | 1 | 0 | 0 | 1,2 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | HL | VL |
| 1 | 1 | 1 | 1 | X | 1,2 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | HL | VL |

Table 6. Output Map (DBL = 1, Second Word)

| BIT SETTING | | | | | | OUTPUT BITS (SECOND WORD) | | | | | | | | | | | | | |
|-------------|----|----|----|----|-----|---------------------------|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|
| DB | HV | BW | CR | DE | SC* | B0 | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 | B9 | B10 | B11 | B12 | B13 |
| 1 | 0 | 0 | 0 | X | 3 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | Z | Z | Z |
| 1 | 0 | 0 | 1 | X | 3 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | Z | Z | Z | Z | Z | Z |
| 1 | 0 | 1 | 0 | X | 3 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 |
| 1 | 0 | 1 | 1 | X | 3 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | Z | Z |
| 1 | 1 | 0 | 0 | 0 | 1,2 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | Z | HH | VH |
| 1 | 1 | 0 | 0 | 1 | 1,2 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | Z | 21 | HH | VH |
| 1 | 1 | 0 | 1 | 0 | 1,2 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | Z | Z | Z | Z | HH | VH |
| 1 | 1 | 0 | 1 | 1 | 1,2 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | Z | Z | Z | Z | 15 | HH | VH |
| 1 | 1 | 1 | 0 | 1 | 1 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 28 | HH | VH |
| 1 | 1 | 1 | 0 | 1 | 2 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | HH | VH |
| 1 | 1 | 1 | 0 | 0 | 1,2 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | HH | VH |
| 1 | 1 | 1 | 1 | X | 1,2 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | HH | VH |

Table 7. Legend

| BIT SETTINGS | | MAPPED SYNC OUTPUTS | |
|------------------|-----------------------|---------------------|----------------------------|
| DB | Double mode bit DBL | H | HSYNC (when DBL = 0) |
| HV | H/V Encoding bit HVEN | V | VSYNC (when DBL = 0) |
| BW | BWS bit | D | DE (when DBL = 0) |
| — | — | HH | HSYNC (high word, DBL = 1) |
| CR | PXL_CRC bit | VH | VSYNC (high word, DBL = 1) |
| DE | DEEN | DH | DE (high word, DBL = 1) |
| SC* | HV_SRC (dec) | HL | HSYNC (low word, DBL = 1) |
| X | 1 or 0 | VL | VSYNC (low word, DBL = 1) |
| BIT COLOR | | DL | DE (low word, DBL = 1) |
| | Sync Bits | # | Serial Bits |
| | Output on first word | Z | Zero |
| | Output on second word | | |
| | Zero | | |

*HV_SRC is automatically set by default. MAX96705 mode automatically sets HV_SRC to 0, 1, or 3 according to the other bit settings above. MAX96707 mode automatically sets HV_SRC to 0, 2, or 3 according to the other bit settings above.

Control-Channel Interfaces

I²C

Set I2CSEL = 1 to configure the control channel for I²C-to-I²C mode. In this mode, the control channel forwards I²C commands from the microcontroller side to the other side of the GMSL link. The remote device acts as an I²C master to the other peripherals connected to the remote side device. I²C-to-I²C mode uses clock stretching to hold the microcontroller until the data and the acknowledge/no-acknowledge have been sent across the link.

I²C Bit Rate

The I²C interface accepts bit rates from 9.6kbps to 1Mbps. The local I²C rate is set by the microcontroller. The remote I²C rate is set by the remote device. By default the control channel is set up for a 400kbps-to-I²C bit rate. Program the I2C_MSTBT and SLV_SH bits (register 0x0D) to match the desired microcontroller I²C rate.

Software Programming of the Device Addresses

The serializer and deserializer have programmable device addresses. This allows multiple GMSL devices, along with I²C peripherals, to coexist on the same control channel. The serializer device address is in register 0x00 of each device, while the deserializer device address is in register 0x01 of each device. To change a device address, first write to the device whose address changes (register 0x00 of the serializer for serializer device address change, or register 0x01 of the deserializer for deserializer device address change). Then write the same address into the corresponding register on the other device (register 0x00 of the deserializer for serializer device address change, or register 0x01 of the serializer for deserializer device address change).

I²C Address Translation

The device supports I²C address translation for up to two device addresses. Use address translation to assign unique device addresses to peripherals with limited I²C addresses. Source addresses (address to translate from) are stored in registers 0x09 and 0x0B. Destination addresses (address to translate to) are stored in registers 0x0A and 0x0C.

Configuration Blocking

The device can block changes to its registers. Set CFGBLOCK to make all registers read only. Once set, the registers remain blocked until the supplies are removed or until PWDNB is low.

Cascaded/Parallel Devices

GMSL supports cascaded and parallel devices connected through I²C. When cascading or using parallel links, all I²C commands are forwarded to all links. Each link attempts to hold the control channel until it receives an acknowledge/non-acknowledge from the remote side device. It is important to keep the control channel active between links in order to prevent timeout. If a link is unused, keep the control channel clear by turning on the configuration link, disconnecting the I²C lines, or powering down the unused device.

Dual μ C Control

Most systems use a single microcontroller; however, μ Cs can reside on each side simultaneously and trade off running the control channel. Contention occurs if both μ Cs attempt to use the control channel at the same time. It is up to the user to prevent this contention by implementing a higher-level protocol. In addition, the control channel does not provide arbitration between I²C masters on both sides of the link. An acknowledge frame is not generated when communication fails due to contention. If communication across the serial link is not required, the μ Cs can disable the forward and reverse control channel using the FWDCCEN and REVCCEN bits (0x04, D[1:0]) in the serializer/deserializer. Communication across the serial link is stopped and contention between μ Cs cannot occur.

UART

Set I2CSEL = 0 to configure the control channel for UART or UART to I²C. In this mode, the control channel forwards UART commands from the microcontroller side to the other side of the GMSL link. When INTTYPE = 00, the remote device acts as an I²C master to the other peripherals connected to the remote side device. UART-to-I²C mode does not support devices that use clock stretching.

Base Mode

In base mode, UART packets control the serializer, deserializer and attached peripherals.

UART Timing

In base mode, the UART idles high (through a pullup resistor). Each GMSL-UART byte consists of a START bit, 8 data bits, an even-parity bit and a stop bit (Figure 19). Keep the idle time between bytes of the same UART packet to less than 4 bit times. The GMSL-UART protocol is listed in Figure 20. A write packet consists of a SYNC byte (Figure 21). Device address byte, Starting register address byte, number of bytes to write, and the data bytes. The slave device responds with an acknowledge byte (Figure 22) if the write was successful. A Read packet consists of a SYNC byte, Device address byte, Starting register address byte, and number of bytes to read. The slave device responds with an acknowledge byte and the read data bytes.

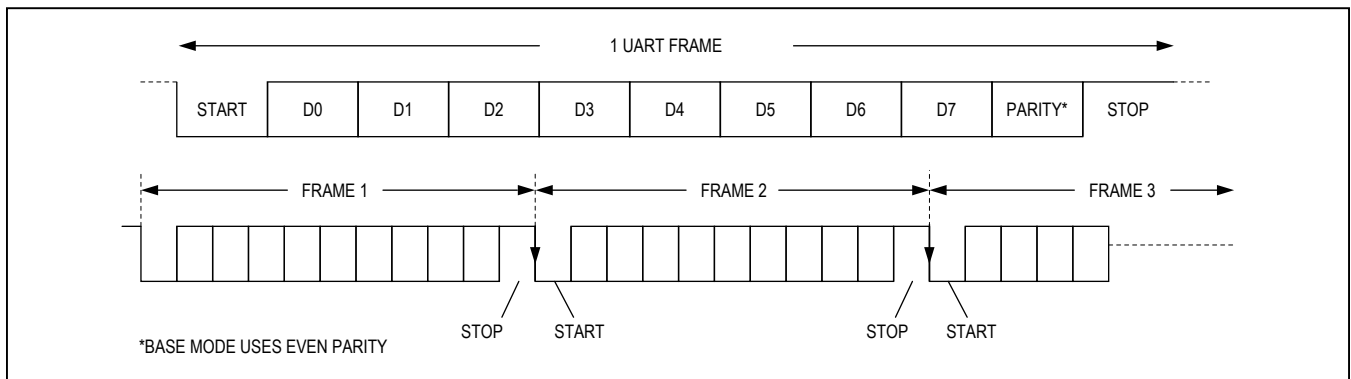


Figure 19. GMSL-UART Data Format for Base Mode

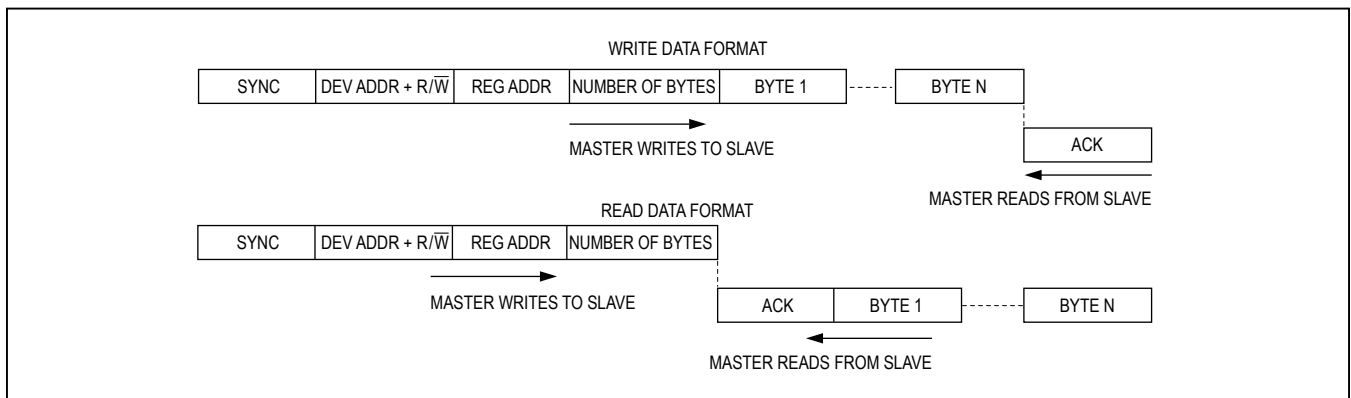


Figure 20. GMSL-UART Protocol for Base Mode

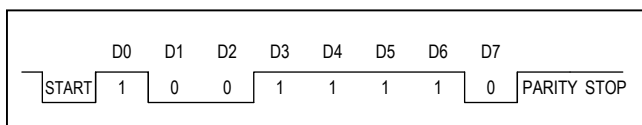


Figure 21. SYNC Byte (0x79)

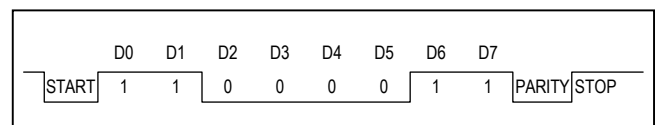


Figure 22. ACK Byte (0xC3)

UART-to-I²C Conversion

When using the UART control channel, the remote-side device can communicate to I²C peripherals through UART-to-I²C conversion. Set the INTTYPE bits in the remote side device to "00" to activate UART-to-I²C conversion. The converted I²C bit rate is the same as the incoming UART bit rate. I²C peripherals must not use clock stretching in order to be compatible with UART-to-I²C conversion.

There are two possible methods the devices use to convert UART to I²C. In the first method, I²CMETHOD = 0. The register address is sent with the I²C communication (*Figure 23*). For devices that do not use a register address (such as the MAX7324) set I²CMETHOD = 1 and send a dummy byte in place of the register address (*Figure 24*). In this method, the remote device omits sending the register address.

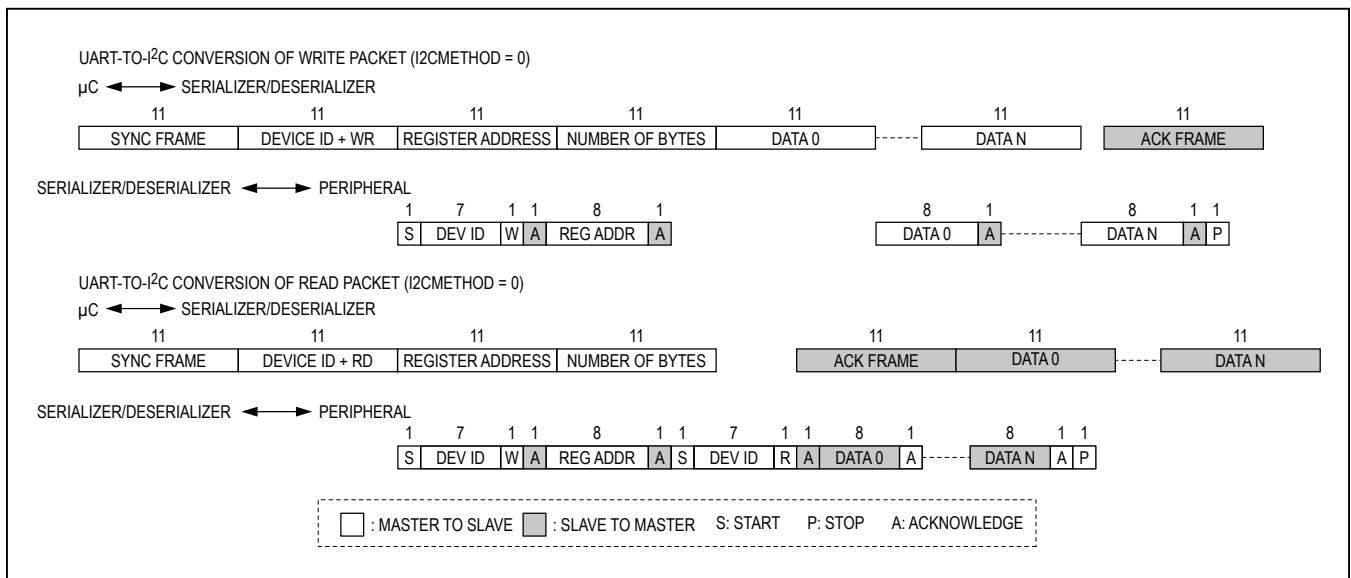


Figure 23. Format Conversion Between GMSL UART and I²C with Register Address (I²CMETHOD = 0)

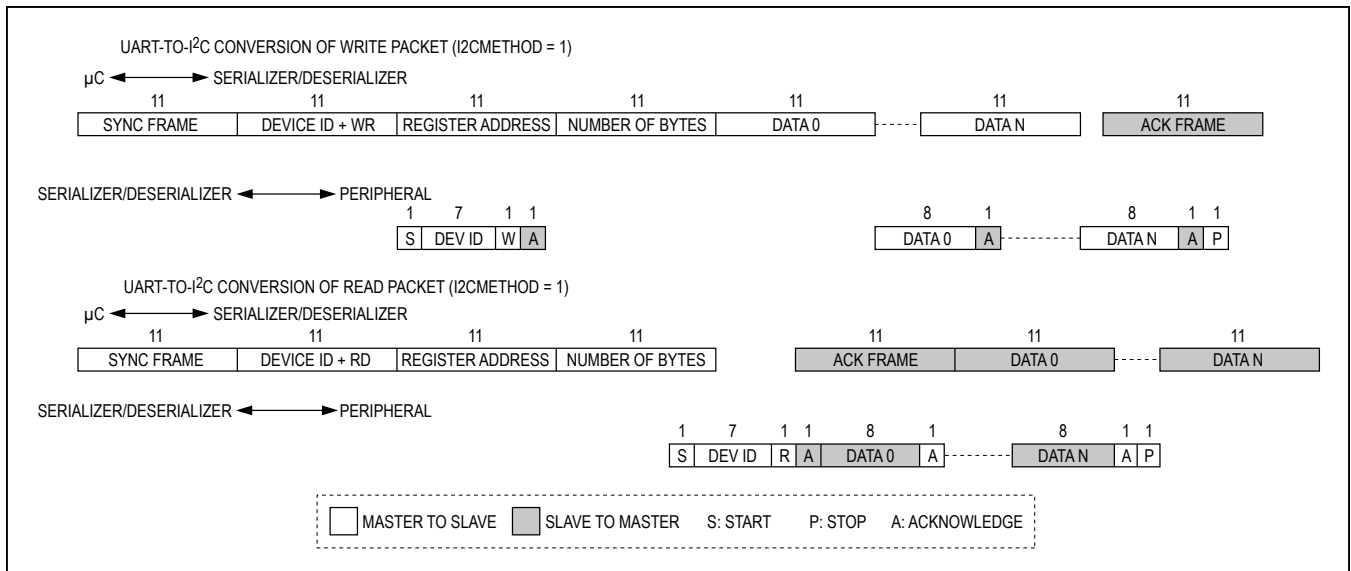


Figure 24. Format Conversion Between GMSL UART and I²C without Register Address (I²CMETHOD = 1)

Table 8. Default-Device Address

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|------|------|----|------|------|----|-----|
| 1 | ADD3 | ADD2 | 1 | ADD1 | ADD0 | 0 | R/W |

Note: ADD[3:0] pin settings latched at power-up.

UART Bypass Mode

In UART bypass mode, the control channel acts as a full-duplex 9.6kbps to 1Mbps link that forwards UART commands across the serial link without responding to the packets themselves. Set MS high to enter bypass mode (wait 1ms after setting bypass mode if the μ C is connected on the deserializer side). Bypass uses bit rates from 9.6kbps to 1Mbps. Do not send a logic-low value longer than 100 μ s when using the GPI/GPO functionality.

Device Address

The SerDes have a 7-bit-long slave address stored in registers 0x00 and 0x01. The bit following a 7-bit slave address is the R/W bit, which is low for a write command and high for a read command. External inputs determine the default slave address as shown in Table 8. After startup, a μ C can reprogram the slave address as needed.

Cable Equalizer

By default, the cable equalizer is enabled and set to Adaptive mode. Set AEQ_EN = 0 to switch to manual EQ mode. EQTUNE determines the boost level in manual EQ mode (see Table 9). Set EN_EQ = 0 to disable all equalization (manual or automatic).

The auto-equalization level is determined during serial-link locking. Set AEQ_MAN_TRG_REQ = 1 to re-trigger auto equalization. Set AEQ_PER_MODE = 1 to set up periodic AEQ.

ERRB Output

The deserializer has an open-drain ERRB output. This output asserts low whenever any of the following conditions occur:

- The number of detected errors exceeds the error thresholds during normal operation. Read DET_ERR, set auto-error reset, or re-lock the link to clear.

Table 9. Cable-Equalizer Boost Levels

| BOOST SETTING (MANUAL AND ADAPTIVE EQ) | TYPICAL BOOST GAIN AT 750MHZ (DB) |
|---|--|
| 0000 | 1.6 |
| 0001 | 2.1 |
| 0010 | 2.8 |
| 0011 | 3.5 |
| 0100 | 4.3 |
| 0101 | 5.2 |
| 0110 | 6.3 |
| 0111 | 7.3 |
| 1000 | 8.5 |
| 1001 | 9.7 Power-up default for Manual EQ* |
| 1010 | 11.0 |
| 1011 | 12.2 |

*Automatic EQ is enabled by default.

Additional conditions that set ERRB (disabled by default) include:

- Insufficient boost at maximum boost setting (set UNDERBST_DET_EN = 1). Retrigger the equalization calibration to clear.

Auto-Error Reset

The default method to reset errors is to read the respective error counter registers in the deserializer. Auto-error reset clears the error counters DET_ERR ~1 μ s after ERR goes low. Auto-error reset is disabled on power-up. Enable auto-error reset through ERR_RST. Auto-error reset does not run when the device is in PRBS test mode.

Board Layout

Power-Supply Circuits and Bypassing

The deserializer uses an AVDD and DVDD of 1.7V to 1.9V. All inputs and outputs, except for the serial input, derive power from an IOVDD of 1.7V to 3.6V that scales with IOVDD. Proper voltage-supply bypassing is essential for high-frequency circuit stability.

High-Frequency Signals

Separate the LVCMOS logic signals and CML/coax high-speed signals to prevent crosstalk. Use a four-layer PCB with separate layers for power, ground, CML/coax, and LVCMOS logic signals. Layout STP PCB traces close to each other for a 100Ω differential characteristic impedance. The trace dimensions depend on the type of trace used (microstrip or stripline). Note that two 50Ω PCB traces do not have 100Ω differential impedance when brought close together—the impedance goes down when the traces are brought closer. Use a 50Ω trace for the single-ended output when driving coax. Route the PCB traces for differential CML in parallel to maintain the differential characteristic impedance. Avoid vias. Keep PCB traces that make up a differential pair equal in length to avoid skew within the differential pair.

ESD Protection

ESD tolerance is rated for Human Body Model, IEC 61000-4-2, and ISO 10605. The ISO 10605 and IEC 61000-4-2 standards specify ESD tolerance for electronic systems. The serial outputs are rated for ISO 10605 ESD protection and IEC 61000-4-2 ESD protection. All pins are tested for the Human Body Model. The Human Body Model discharge components are CS = 100pF and RD = 1.5kΩ (Figure 25). The IEC 61000-4-2 discharge components are CS = 150pF and RD = 330Ω (Figure 26). The ISO 10605 discharge components are CS = 330pF and RD = 2kΩ (Figure 27).

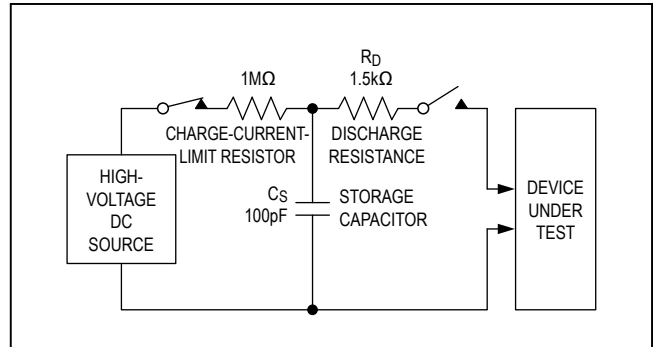


Figure 25. Human Body Model ESD Test Circuit

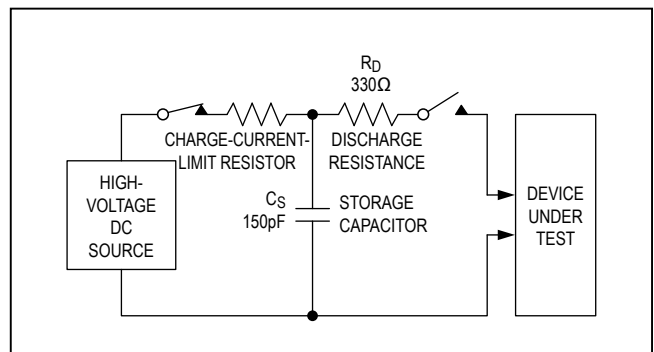


Figure 26. IEC 61000-4-2 Contact Discharge ESD Test Circuit

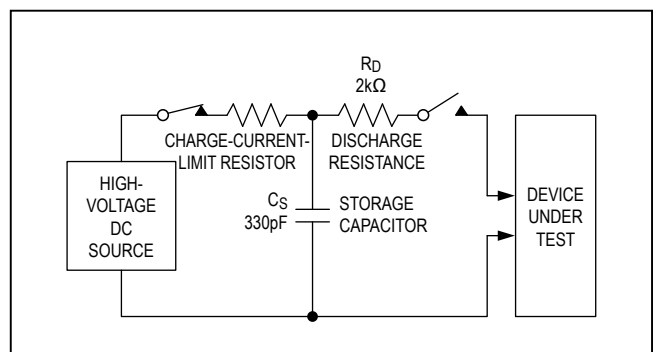


Figure 27. ISO 10605 Contact Discharge ESD Test Circuit

Table 10. Feature Compatibility

| DESERIALIZER FEATURE | GMSL SERIALIZER |
|--------------------------------------|--|
| HSYNC/VSYNC encoding | If feature not supported in the serializer, turn off in the deserializer. |
| I ² C-to-I ² C | If feature not supported in the serializer, use UART-to-I ² C or UART-to-UART. |
| CRC error detection | If feature not supported in the serializer, turn off in the deserializer. |
| Double input | If feature not supported in the serializer, data is output as a single word at half the input frequency. Use Crossbar switch to correct input mapping. |
| Coax | If feature not supported in the serializer, connect unused serial input through 200nF and 50Ω in series to AVDD, and set the reverse control-channel amplitude to 100mV. |
| I ² S encoding | If supported in the serializer, disable I ² S in the serializer |
| High-immunity mode | If feature not supported in the serializer, turn off in the deserializer. |

Compatibility with Other GMSL Devices

The MAX96708 is designed to pair with the MAX96705–MAX96711 family of SerDes devices, but interoperates with any GMSL device. See [Table 10](#) for operating limitations.

Device Configuration and Component Selection

Internal Input Pulldowns

The control and configuration inputs include a pulldown resistor to GND. External pulldown resistors are not needed.

Multifunction Inputs

The device has several inputs/outputs that function both as a parallel input/output and as a configuration pin. On power-up, or when reverting from a power-down state, the pins act as configuration inputs. After latching the input state, the configuration inputs become parallel digital input/outputs. Connect a configuration input through a 30kΩ resistor to IOVDD to set a high level. Leave the configuration input open to set a low level.

I²C/UART Pullup Resistors

The I²C and UART open-drain lines require a pullup resistor to provide a logic-high level. There are tradeoffs between power dissipation and speed, and a compromise may be required when choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when the device is not in operation. I²C specifies 300ns rise times (30% to 70%) for fast mode, which is defined for data rates up to 400kbps. See the I²C specifications in the I²C/UART Port Timing section in the [AC Electrical Characteristics](#) table for details. To meet the fast-mode rise-time requirement, choose the pullup resistors so that rise time $t_R = 0.85 \times R_{PULLUP} \times C_{BUS} <$

300ns. The waveforms are not recognized if the transition time becomes too slow. GMSL supports I²C/UART rates up to 1Mbps (UART-to-I²C mode) and 400kbps (I²C-to-I²C mode).

AC-Coupling Capacitors

Voltage droop and the digital sum variation (DSV) of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is fixed, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level. The RC network for an AC-coupled link consists of the CML/coax receiver termination resistor (R_{TR}), the CML/coax driver termination resistor (R_{TD}), and the series AC-coupling capacitors (C). The RC time constant for four equal-value series capacitors is $(C \times (R_{TD} + R_{TR}))/4$. R_{TD} and R_{TR} are required to match the transmission line impedance (usually 100Ω differential, 50Ω single-ended). This leaves the capacitor selection to change the system time constant. Use 0.22μF or larger high-frequency surface-mount ceramic capacitors, with sufficient voltage rating to withstand a short to battery, to pass the lower-speed reverse control-channel signal. Use capacitors with a case size less than 3.2mm x 1.6mm to have lower parasitic effects to the high-speed signal.

Cables and Connectors

Interconnect for CML typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Coax cables typically have a characteristic impedance of 50Ω (contact the factory for 75Ω operation). [Table 11](#) lists the suggested cables and connectors used in the GMSL link.

Table 11. Suggested Connectors and Cables for GMSL

| VENDOR | CONNECTOR | CABLE | TYPE |
|-------------|----------------|--------------|------|
| Rosenberger | 59S2AX-400A5-Y | Dacar 302 | Coax |
| Rosenberger | D4S10A-40ML5-Z | Dacar 535-2 | STP |
| Nissei | GT11L-2S | F-2WME AWG28 | STP |
| JAE | MX38-FF | A-BW-Lxxxxx | STP |

PRBS

The serializer includes a PRBS pattern generator that works with bit-error verification in the deserializer. To run the PRBS test, set PRBSEN = 1 (0x04, D5) in the deserializer, then in the serializer. To exit the PRBS test, set PRBSEN = 0 (0x04, D5) in the serializer. The deserializer automatically ends PRBS checking and sets the PRBS_OK bit high. Note that during PRBS mode, the remote control channel is not available except to exit PRBS mode if I2C_LOC_ACK = 1; otherwise, the remote control channel is not available at all.

To run the PRBS with a 3Gbps SerDes, first set the PRBS_TYPE bit = 0 in the MAX967XX. Then set PRBSEN = 1 (0x04, D5) in the serializer, then in the deserializer. To exit the PRBS test, set PRBSEN = 0 (0x04, D5) in the deserializer, then in the serializer.

During PRBS test, ERRB function changes to reflect PRBS errors only. ERRB goes low when any PRBS errors occur. ERRB goes high when the PRBS error counter is reset when PRBS_ERR is read. Normal ERRB function resumes when exiting the PRBS test.

GPI/GPO

GPO on the serializer follows GPI transitions on the deserializer. By default, the GPI-to-GPO delay is 0.35ms (max). Keep the time between GPI transitions to a minimum 0.35ms. GPI_IN the deserializer stores the GPI input state. GPO is low after power-up. The μ C can set GPO by writing to the SET_GPO register bit. Do not send a logic-low value on the deserializer RX/SDA input (UART mode) longer than 100 μ s in either base or bypass mode to ensure proper GPO/GPI functionality.

Fast Detection of Loss-of-Lock

A measure of link quality is the recovery time from loss of synchronization. The host can be quickly notified of loss-of-lock by connecting the deserializer's LOCK output to the GPI input. If other sources use the GPI input, such as a touch-screen controller, the μ C can implement a routine to distinguish between interrupts from loss-of-sync and

normal interrupts. Reverse control-channel communication does not require an active forward link to operate and accurately tracks the LOCK status of the GMSL link. LOCK asserts for video link only and not for the configuration link.

Providing a Frame Sync (Camera Applications)

The GPI and GPO provide a simple solution for camera applications that require a frame sync signal from the ECU (e.g., surround-view systems). Connect the ECU frame sync signal to the GPI input and connect the GPO output to the camera-frame sync input. GPI/GPO have a typical delay of 275 μ s. Skew between multiple GPI/GPO channels is 115 μ s (max). If a lower-skew signal is required, connect the camera's frame-sync input to one of the serializer's GPIOs and use an I²C broadcast write command to change the GPIO output state. This has a maximum skew of 1.5 μ s, independent from the used I²C bit rate.

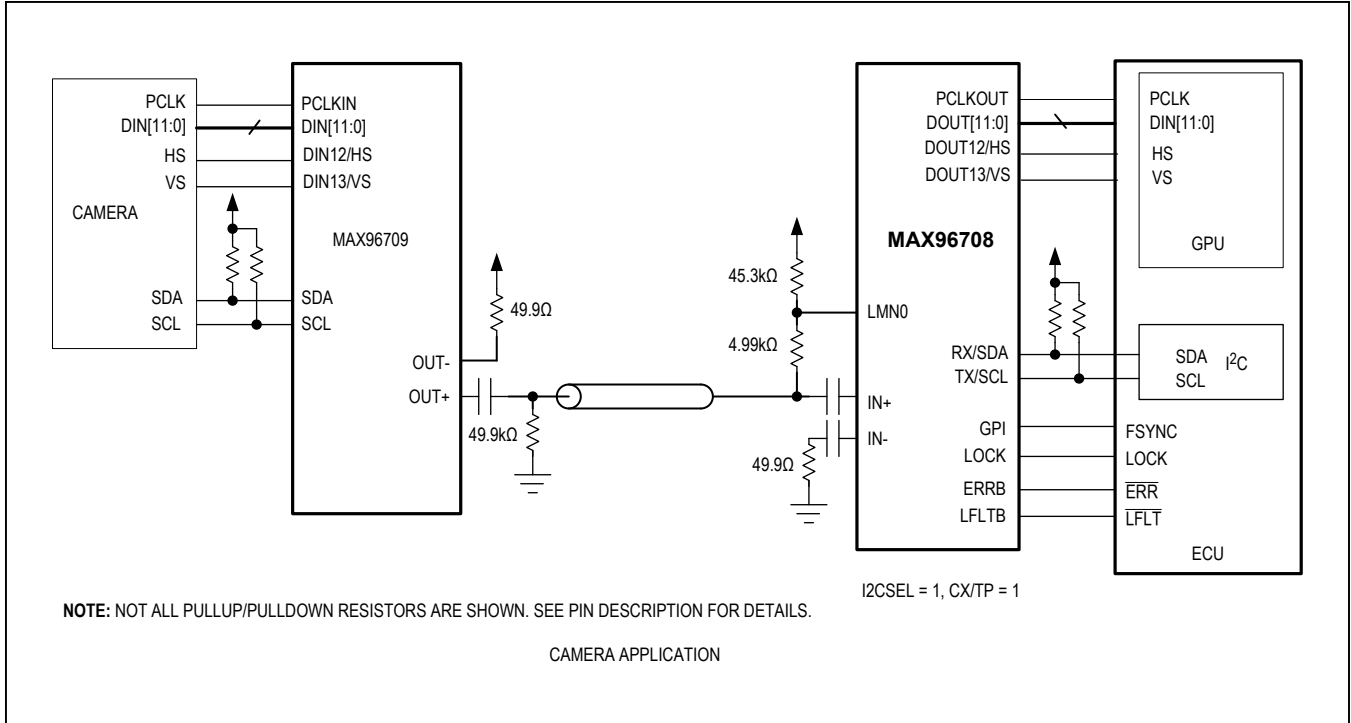
Entering/Exiting Sleep Mode

The procedure for entering and exiting sleep mode depends on the location of the microcontroller, and the type of control-channel interface used. If wake-up from a remote-side (serializer-side) microcontroller is not needed or desired, set the DIS_RWAKE bit = 1 to shut down remote wake-up for further power savings.

When the microcontroller is on the deserializer side, first put the serializer to sleep, or disable serialization. Next, set SLEEP = 1 in deserializer. The device sleeps after 8ms. To wake up the device, send an arbitrary control-channel command to the deserializer (the device will not send an acknowledge), wait for 5ms for the chip to power up and then set SLEEP = 0 to make the wake-up permanent.

When μ C is on the serializer side, set SLEEP = 1 in deserializer. Next, disable serialization. The device sleeps after 8ms. To wake up the deserializer, reenables serialization. The deserializer wakes up and clears its SLEEP bit when it locks to the serializer.

Typical Application Circuit



Ordering Information

| PART NUMBER | TEMP RANGE | PIN-PACKAGE |
|-----------------|-----------------|-------------|
| MAX96708GTJ+ | -40°C to +115°C | 32 TQFN-EP* |
| MAX96708GTJ+T | -40°C to +115°C | 32 TQFN-EP* |
| MAX96708GTJ/V+ | -40°C to +115°C | 32 TQFN-EP* |
| MAX96708GTJ/V+T | -40°C to +115°C | 32 TQFN-EP* |

/V denotes an automotive qualified product.
 +Denotes a lead(Pb)-free/RoHS-compliant package.
 *EP = Exposed pad.
 T = Tape and reel.

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|---|---|
| 0 | 3/16 | Initial release | — |
| 1 | 3/17 | Various updates, beginning with <i>Absolute Maximum Ratings</i> | 7, 29, 33, 38, 40, 62, 63, 65, 66 |

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