## **Power MOSFET**

# 60 V, 9.3 m $\Omega$ , 50 A, Single N-Channel

#### **Features**

- Small Footprint (3.3x3.3 mm) for Compact Design
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Q<sub>G</sub> and Capacitance to Minimize Driver Losses
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

## **MAXIMUM RATINGS** (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	60	V
Gate-to-Source Voltage	Э		$V_{GS}$	±20	V
Continuous Drain		T <sub>C</sub> = 25°C	I <sub>D</sub>	50	Α
Current R <sub>θJC</sub> (Notes 1, 3)	Steady State	T <sub>C</sub> = 100°C		35	
Power Dissipation		$T_C = 25^{\circ}C$	P <sub>D</sub>	46	W
R <sub>θJC</sub> (Note 1)		T <sub>C</sub> = 100°C		23	
Continuous Drain		T <sub>A</sub> = 25°C	I <sub>D</sub>	13	Α
Current R <sub>0JA</sub> (Notes 1, 2, 3)	Steady	T <sub>A</sub> = 100°C		9	
Power Dissipation	State	T <sub>A</sub> = 25°C	P <sub>D</sub>	3.1	W
R <sub>θJA</sub> (Notes 1 & 2)		T <sub>A</sub> = 100°C		1.6	
Pulsed Drain Current	Pulsed Drain Current $T_A = 25^{\circ}C$ , $t_p = 10 \mu s$			290	Α
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Source Current (Body Diode)			I <sub>S</sub>	52	Α
Single Pulse Drain-to-Source Avalanche Energy (I <sub>L(pk)</sub> = 2.3 A)			E <sub>AS</sub>	88	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	3.2	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	48	

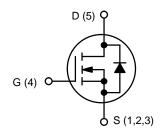
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
- 3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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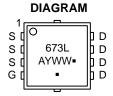
V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
60 V	9.3 mΩ @ 10 V	50 A
60 V	13.3 mΩ @ 4.5 V	50 A



**N-CHANNEL MOSFET** 



WDFN8 (µ8FL) CASE 511AB



**MARKING** 

673L = Specific Device Code A = Assembly Location

Y = Year WW = Work Week

(Note: Microdot may be in either location)

= Pb-Free Package

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

## **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise specified)

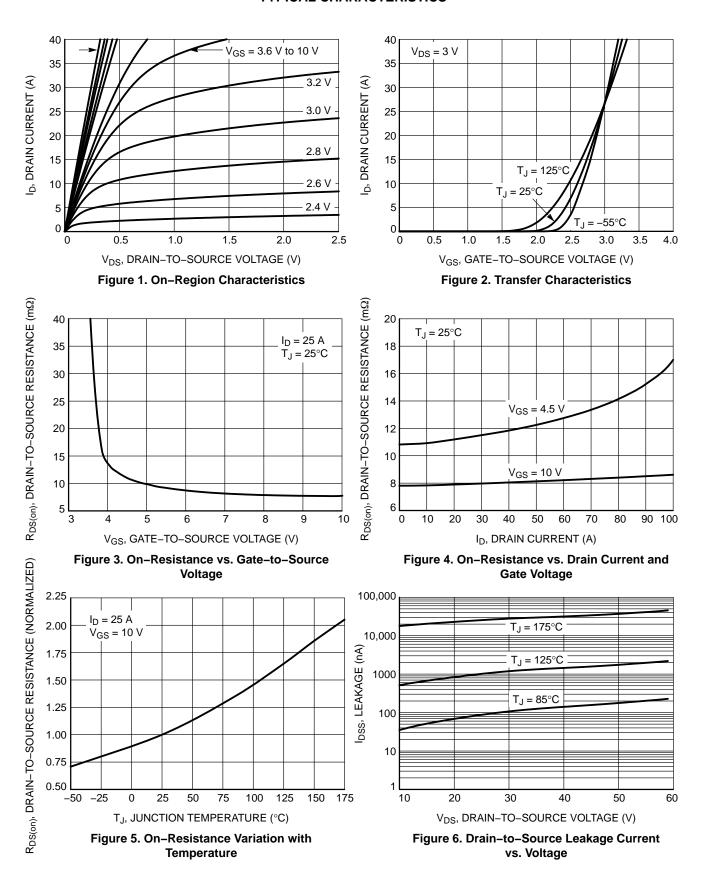
Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	•			•			•
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /				28		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	T <sub>J</sub> = 25°C			10	
		$V_{DS} = 60 \text{ V}$	T <sub>J</sub> = 125°C			250	μΑ
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_{D}$	= 35 μΑ	1.2		2.0	V
Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				-4.5		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 25 A		8.0	9.3	
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 25 A		11	13.3	mΩ
Forward Transconductance	9FS	V <sub>DS</sub> =15 V, I <sub>D</sub>	<sub>0</sub> = 25 A		37		S
CHARGES AND CAPACITANCES	•			•			•
Input Capacitance	C <sub>ISS</sub>				880		
Output Capacitance	C <sub>OSS</sub>	V <sub>GS</sub> = 0 V, f = 1 MH	z, V <sub>DS</sub> = 25 V		450		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>				11		1
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 30 V; I <sub>D</sub> = 25 A			4.5		nC
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 30 V; I <sub>D</sub> = 25 A			9.5		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>				1.0		
Gate-to-Source Charge	Q <sub>GS</sub>	$V_{GS} = 4.5 \text{ V}, V_{DS} = 30 \text{ V}; I_D = 25 \text{ A}$			2.0		nC
Gate-to-Drain Charge	$Q_{GD}$				0.8		
Plateau Voltage	V <sub>GP</sub>				2.9		V
SWITCHING CHARACTERISTICS (Note 5	)				•	•	•
Turn-On Delay Time	t <sub>d(ON)</sub>				9.0		
Rise Time	t <sub>r</sub>	$V_{GS} = 4.5 \text{ V}, V_{D}$	oe = 30 V.		50		1
Turn-Off Delay Time	t <sub>d(OFF)</sub>	$I_D = 25 \text{ A}, R_G = 2.5 \Omega$			13		ns
Fall Time	t <sub>f</sub>				3.0		
DRAIN-SOURCE DIODE CHARACTERIST	TICS			1			
Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V,	T <sub>J</sub> = 25°C		0.9	1.2	
	$I_S = 25 \text{ A}$	I <sub>S</sub> = 25 A	T <sub>J</sub> = 125°C		0.8		
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V, dIs/dt} = 100 \text{ A/}\mu\text{s,}$ $I_{S} = 25 \text{ A}$			28		
Charge Time	t <sub>a</sub>				14		ns
Discharge Time	t <sub>b</sub>				14		1
Reverse Recovery Charge	Q <sub>RR</sub>				18		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width  $\leq 300~\mu s$ , duty cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperatures.

## **TYPICAL CHARACTERISTICS**



#### TYPICAL CHARACTERISTICS

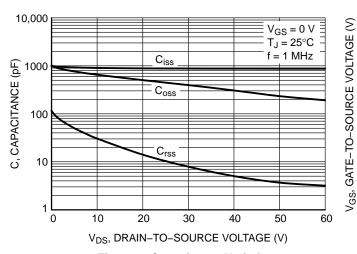


Figure 7. Capacitance Variation

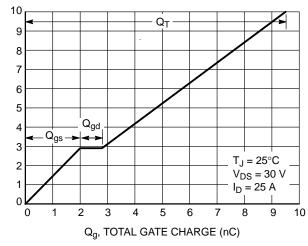


Figure 8. Gate-to-Source vs. Total Charge

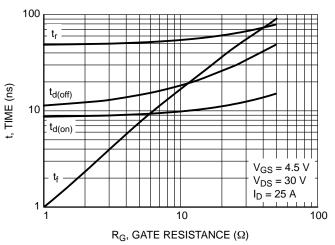


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

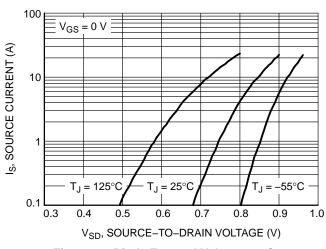


Figure 10. Diode Forward Voltage vs. Current

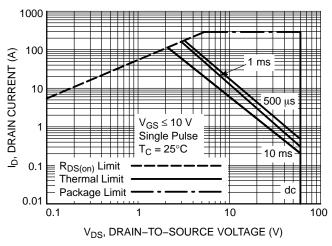


Figure 11. Maximum Rated Forward Biased Safe Operating Area

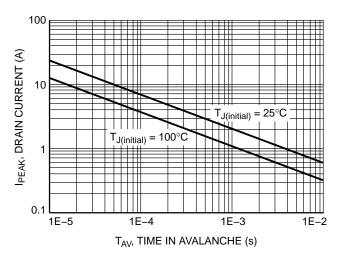


Figure 12. Maximum Drain Current vs. Time in Avalanche

### **TYPICAL CHARACTERISTICS**

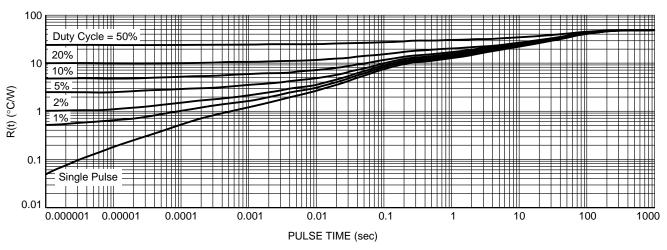


Figure 13. Thermal Response

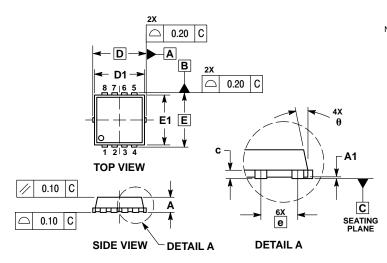
## **DEVICE ORDERING INFORMATION**

Device	Marking	Package	Shipping <sup>†</sup>
NTTFS5C673NLTAG	673L	DFN5 (Pb–Free)	1500 / Tape & Reel
NTTFS5C673NLTWG	673L	DFN5 (Pb-Free)	5000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS

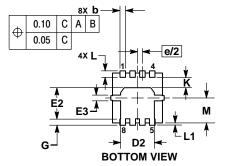
## WDFN8 3.3x3.3, 0.65P CASE 511AB ISSUE D



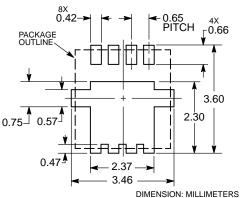
#### NOTES

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α	0.70	0.75	0.80	0.028	0.030	0.031	
A1	0.00		0.05	0.000		0.002	
b	0.23	0.30	0.40	0.009	0.012	0.016	
С	0.15	0.20	0.25	0.006	0.008	0.010	
D		3.30 BSC		0	.130 BSC	)	
D1	2.95	3.05	3.15	0.116	0.120	0.124	
D2	1.98	2.11	2.24	0.078	0.083	0.088	
E	3.30 BSC			0.130 BSC			
E1	2.95	3.05	3.15	0.116	0.120	0.124	
E2	1.47	1.60	1.73	0.058	0.063	0.068	
E3	0.23	0.30	0.40	0.009	0.012	0.016	
е	0.65 BSC			0.026 BSC			
G	0.30	0.41	0.51	0.012	0.016	0.020	
K	0.65	0.80	0.95	0.026	0.032	0.037	
L	0.30	0.43	0.56	0.012	0.017	0.022	
L1	0.06	0.13	0.20	0.002	0.005	0.008	
M	1.40	1.50	1.60	0.055	0.059	0.063	
θ	0 °		12 °	0 °		12 °	



#### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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