

MOSFET – Power, Single N-Channel 60 V, 0.81 mΩ, 398.2 A



NVMTS001N06CL

Features

- Small Footprint (8x8 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Power 88 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- Wettable Flank Plated for Enhanced Optical Inspection
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	60	V
Gate-to-Source Voltage	V _{GS}	±20	V
Continuous Drain Current R _{θJC} (Notes 1, 3)	I _D	398.2	A
		281.6	
Power Dissipation R _{θJC} (Note 1)	P _D	244.0	W
		122.0	
Continuous Drain Current R _{θJA} (Notes 1, 2, 3)	I _D	56.9	A
		40.2	
Power Dissipation R _{θJA} (Notes 1, 2)	P _D	5.0	W
		2.5	
Pulsed Drain Current	I _{DM}	900	A
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C
Source Current (Body Diode)	I _S	203.4	A
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 30 A)	E _{AS}	887	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T _L	260	°C

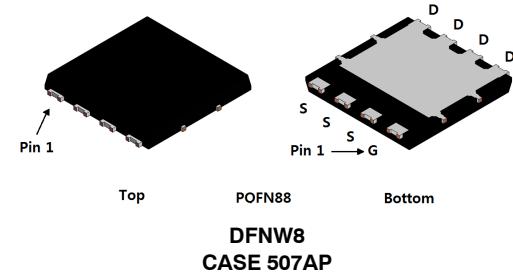
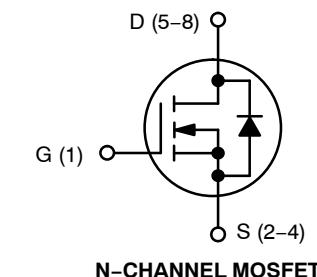
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

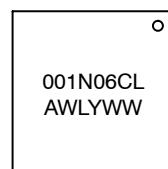
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	R _{θJC}	0.614	°C/W
Junction-to-Ambient – Steady State (Note 2)	R _{θJA}	30.1	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

V _{(BR)DSS}	R _{DS(ON) MAX}	I _{D MAX}
60 V	0.81 mΩ @ 10 V	
	1.05 mΩ @ 4.5 V	398.2 A



MARKING DIAGRAM



A = Assembly Location
 WL = Wafer Lot Code
 Y = Year Code
 WW = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVMTS001N06CL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(\text{BR})\text{DSS}}/T_J$	$I_D = 250 \mu\text{A}$, ref to 25°C			25		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{GS}} = 0 \text{ V}$, $V_{\text{DS}} = 60 \text{ V}$	$T_J = 25^\circ\text{C}$		10		μA
			$T_J = 125^\circ\text{C}$			250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{\text{DS}} = 0 \text{ V}, V_{\text{GS}} = 20 \text{ V}$				100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{\text{GS}(\text{TH})}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 250 \mu\text{A}$		1.2		2.2	V
Threshold Temperature Coefficient	$V_{\text{GS}(\text{TH})}/T_J$	$I_D = 250 \mu\text{A}$, ref to 25°C			-5.53		$\text{mV}/^\circ\text{C}$
Drain-to-Source On Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10 \text{ V}$	$I_D = 50 \text{ A}$		0.73	0.81	$\text{m}\Omega$
Drain-to-Source On Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 4.5 \text{ V}$	$I_D = 50 \text{ A}$		0.94	1.05	$\text{m}\Omega$
Forward Transconductance	g_{FS}	$V_{\text{DS}} = 15 \text{ V}, I_D = 50 \text{ A}$			275		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{\text{GS}} = 0 \text{ V}, f = 1 \text{ MHz}, V_{\text{DS}} = 25 \text{ V}$		12300		pF
Output Capacitance	C_{OSS}			6225		
Reverse Transfer Capacitance	C_{RSS}			130		
Total Gate Charge	$Q_{\text{G}(\text{TOT})}$	$V_{\text{GS}} = 10 \text{ V}, V_{\text{DS}} = 30 \text{ V}; I_D = 50 \text{ A}$		165		nC
Total Gate Charge	$Q_{\text{G}(\text{TOT})}$			74.3		
Threshold Gate Charge	$Q_{\text{G}(\text{TH})}$			15.6		
Gate-to-Source Charge	Q_{GS}			28.7		
Gate-to-Drain Charge	Q_{GD}			14.7		
Plateau Voltage	V_{GP}			2.59		V

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{\text{d}(\text{ON})}$	$V_{\text{GS}} = 4.5 \text{ V}, V_{\text{DS}} = 30 \text{ V}, I_D = 50 \text{ A}, R_G = 2.5 \Omega$		47.2		ns
Rise Time	t_r			25.2		
Turn-Off Delay Time	$t_{\text{d}(\text{OFF})}$			70.7		
Fall Time	t_f			23.3		

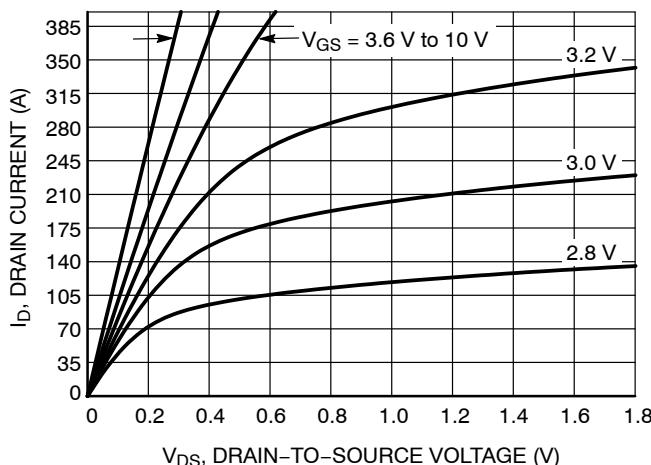
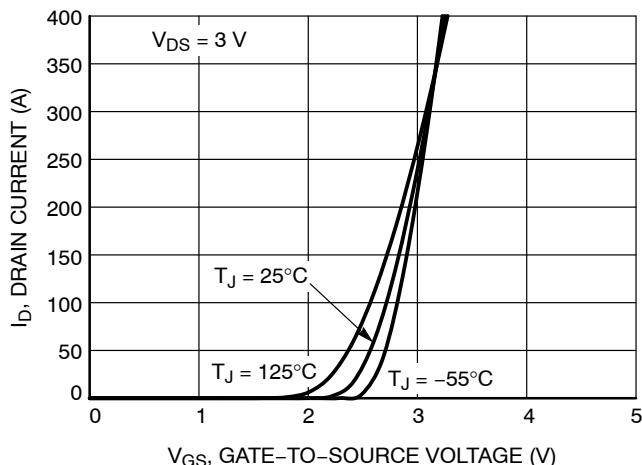
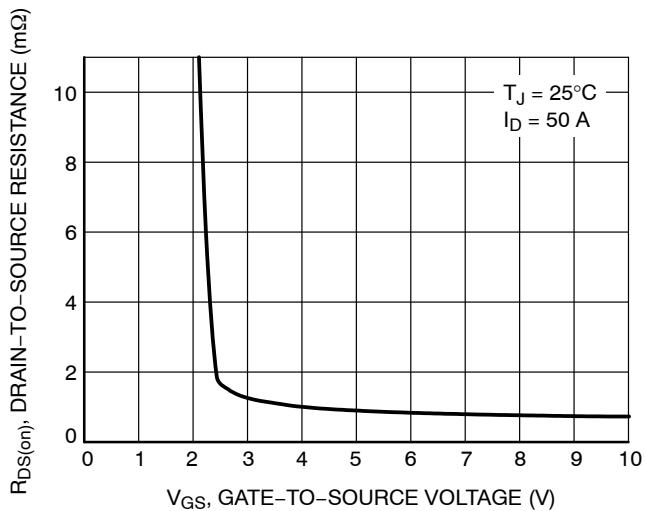
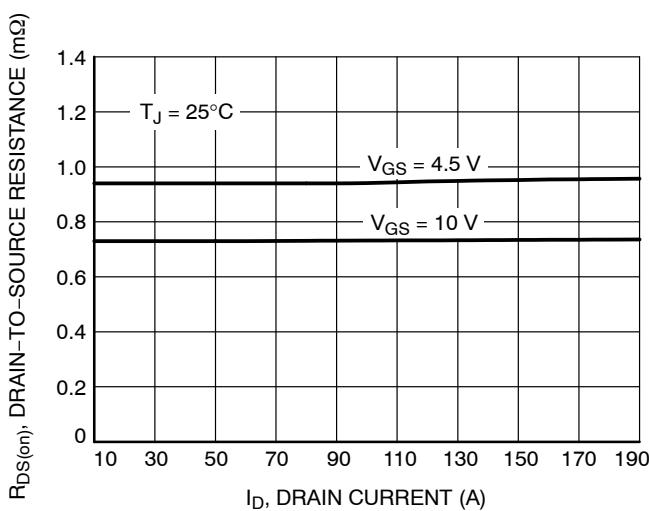
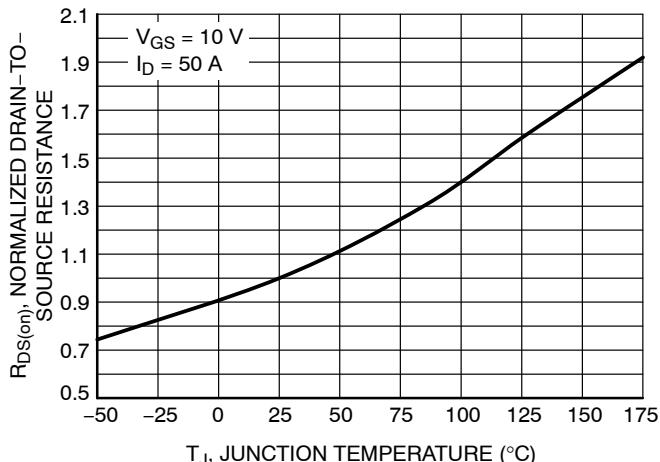
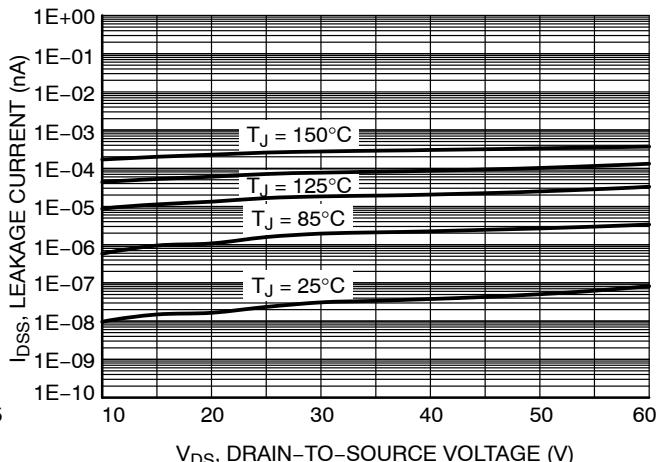
DRAIN-SOURCE DIODE CHARACTERISTICS

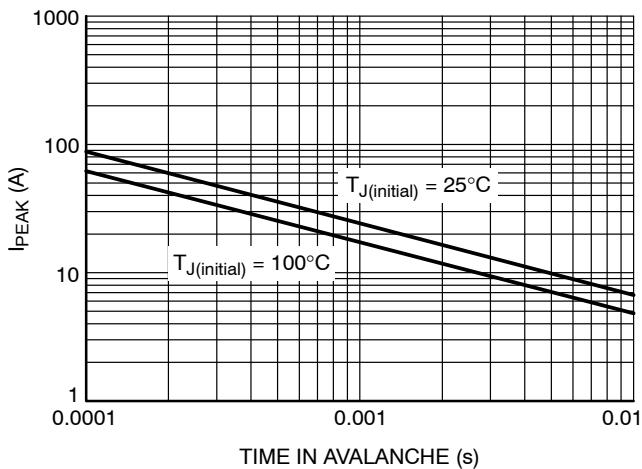
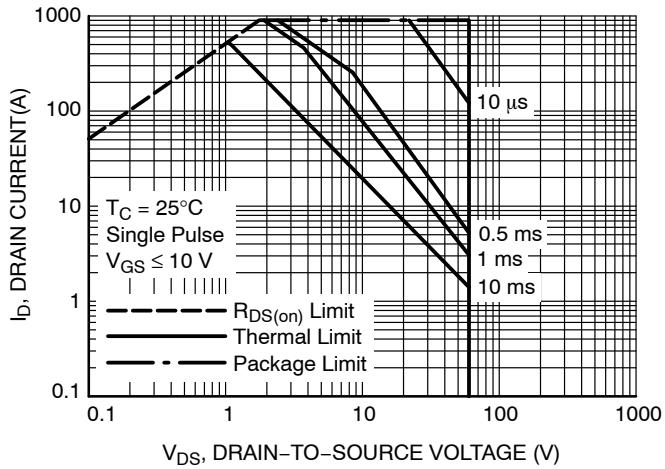
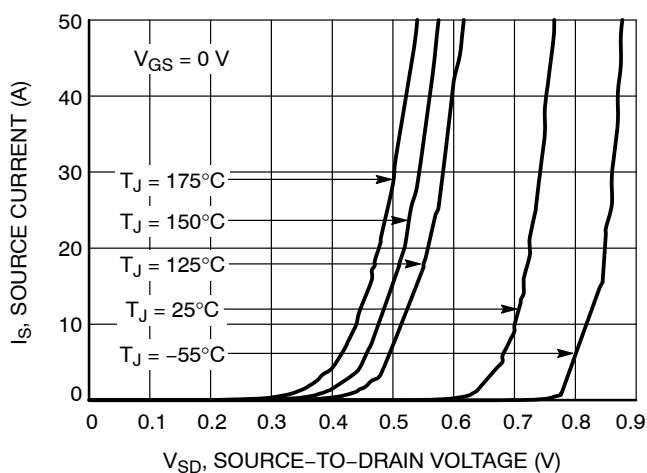
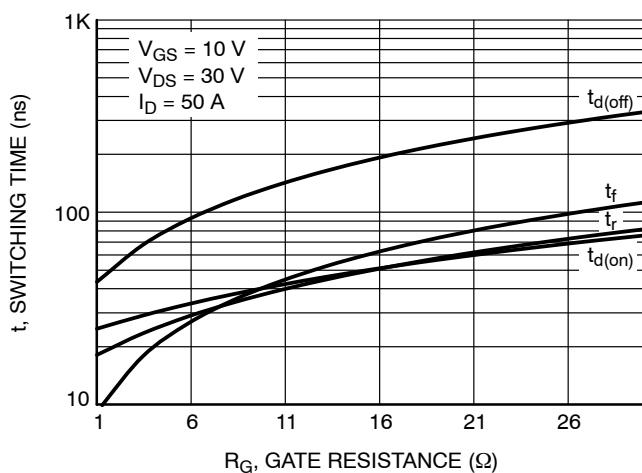
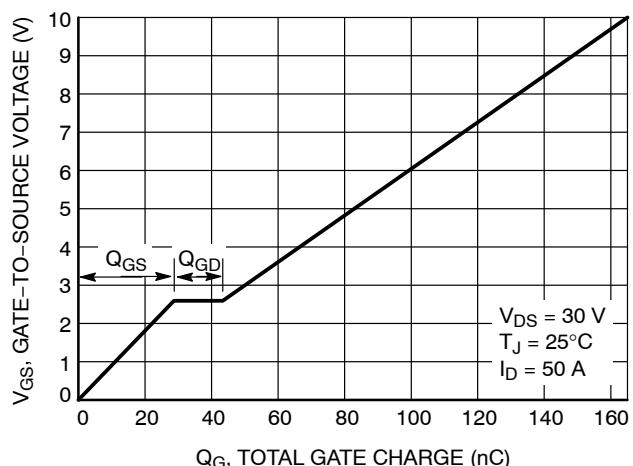
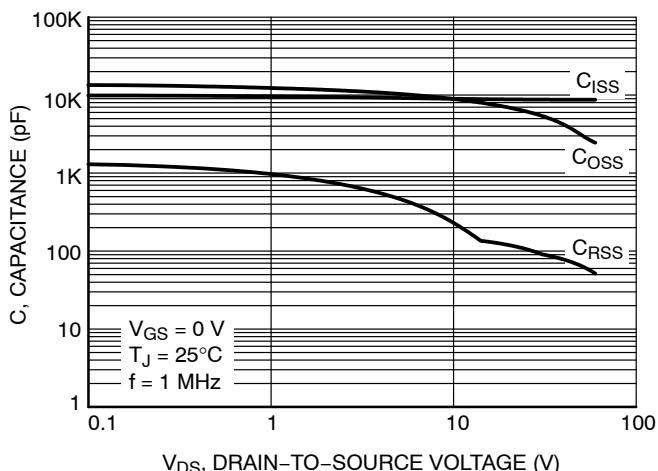
Forward Diode Voltage	V_{SD}	$V_{\text{GS}} = 0 \text{ V}, I_S = 50 \text{ A}$	$T_J = 25^\circ\text{C}$		0.77	1.2	V
			$T_J = 125^\circ\text{C}$		0.63		
Reverse Recovery Time	t_{RR}	$V_{\text{GS}} = 0 \text{ V}, dI_S/dt = 100 \text{ A}/\mu\text{s}, I_S = 50 \text{ A}$			98.9		ns
Charge Time	t_a				66.8		
Discharge Time	t_b				32.1		
Reverse Recovery Charge	Q_{RR}				229		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics

Figure 3. On-Resistance vs. Gate-to-Source Voltage

Figure 4. On-Resistance vs. Drain Current and Gate Voltage

Figure 5. On-Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS


NVMTS001N06CL

TYPICAL CHARACTERISTICS

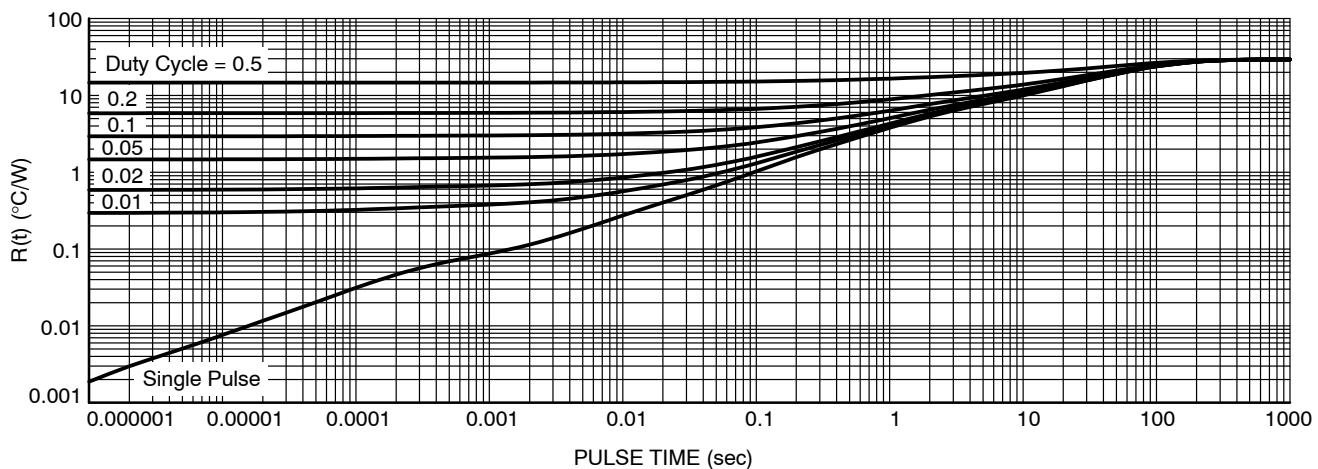


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMTS001N06CLTXG	001N06CL	DFNW8 (Pb-Free)	3000 / Tape & Reel

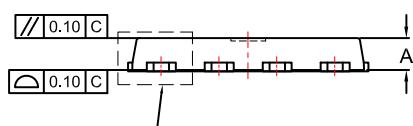
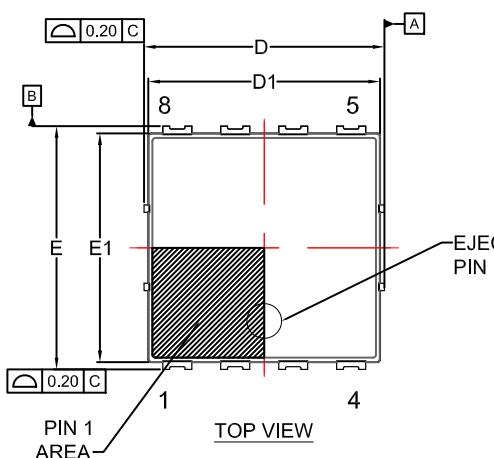
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

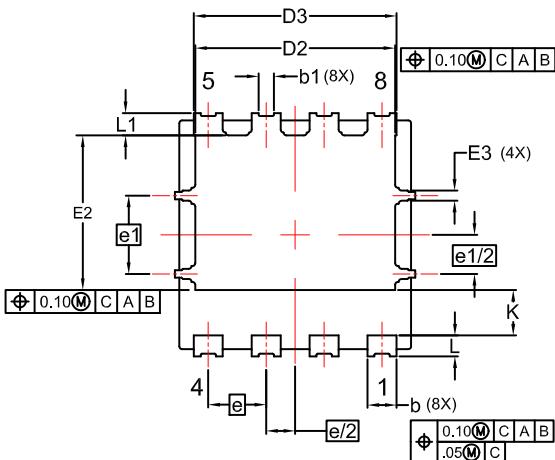
DFNW8 8.3x8.4, 2P

CASE 507AP

ISSUE B



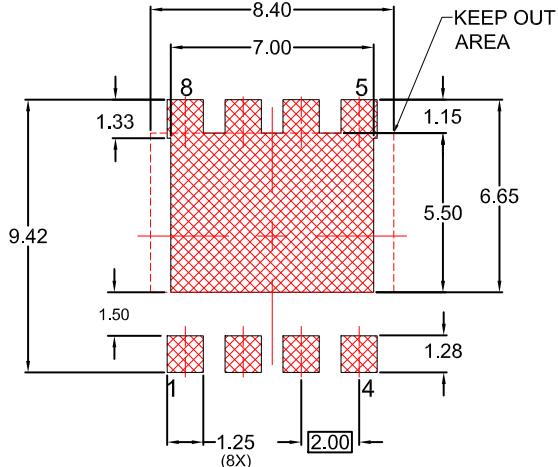
FRONT VIEW

DETAIL A
SCALE: 2X

BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS.
"A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



RECOMMENDED LAND PATTERN*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A1	0.00	—	0.05
b	0.90	1.00	1.10
b1	0.43	0.53	0.63
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	7.90	8.00	8.10
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
E	8.30	8.40	8.50
E1	7.80	7.90	8.00
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
e	2.00 BSC		
e/2	1.00 BSC		
e1	2.70 BSC		
e1/2	1.35 BSC		
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
Θ	0°	—	12°

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