VMusic3 Version 1.0



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Future Technology Devices International Ltd

Datasheet

VMusic3 Vinculum-II Application Module



VMusic3 is a USB host and MP3/WMA Player application module with an enclosure. The default firmware of the VMusic3 supports audio playback and UART/SPI communications with the embedded USB host controller and USB host port. VMusic3 can be used to read MP3 and other audio format files from a USB flash disk process the data and output the stereo audio through the line-out header and headphone jack.

1 Introduction

VMusic3 is designed to support quick and easy integration of a UART/SPI application with a USB client device. VMusic3 also supports playback of MP3 and WMA. The VMusic3 is packaged in a neat enclosure displaying a bicolour LED, making it suitable for incorporating into finished product designs.

The VMusic3 utilises FTDI's Vinculum-II (VNC2-48L1B) dual USB host controller IC. This IC is a microcontroller and USB host controller; it can be reprogrammed using the UART interface or the Vinculum-II debugger module interface connecter. The default firmware used is V2MSC, this firmware supports the UART/SPI to USB host interface and MP3 playback. This firmware can be modified or replace with another firmware.

The VMusic3 also utilises VLSI Solution's VS1053b compressed audio codec to provide the audio play back feature. This chip operates with the Vinculum-II and supporting firmware when reading MP3 and WMA files from a USB flash drive. The VS1053b processes this data and outputs the stereo audio to the headphone jack and line-out header. Connecting headphones or speakers to either of these ports transduces the audio data into sound.

For details on the Vinculum-II collateral please click

http://www.ftdichip.com/Products/ICs/VNC2.htm.

1.1 Features

VMusic3 has the following features:

- MP3 and WMA playback
- Vinculum-II microcontroller/USB host controller IC.
- USB "A" type socket to connect to USB client devices.
- 2mm (0.08") pitch 8 pin header used for the UART/SPI interface.
- Connects directly and communicates with a FTDI TTL-232R-3V3-2mm USB-UART cable.
- Jumper selectable UART and SPI interfaces, both operating 3.3V TTL/CMOS.
- Pre-programmed with V2MSC firmware.
- Vinculum-II debugger module port under the enclosure, for changing the firmware and debugging.
- UART programming mode control pins PROG# and RESET# are connected to an internal header.
- Reprogrammable over USB Port from flash drive.
- The VMusic3 and all components used are Pb-free (RoHS compliant).

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2 Ordering Information

Module Code	Utilised IC Code	Description
VMUSIC3	VNC2-48L1B	USB host application module with MP3 playback and enclosure.

3 VMusic3 Signals and Configurations

3.1 VMusic3 Pin-Out



Figure 3.1 – VMusic3 Pin Out (in UART mode)

The pin-out is illustrated in Figure 3.1.

3.2 VMusic3 Jumper Configuration

The VMusic3 comes preloaded with the V2MSC firmware and the jumper is set to UART mode by default. Adjusting the jumpers accordingly configures the module to operate in SPI mode.

The interface modes of the VMusic3 running on a V2MSC firmware are given in Table 3.1

UART/SPI	Interface Mode
Pull-Up	UART
Pull-Down	SPI

Table 3.1 - VMusic3 Jumper Box



3.3 Interface Discriptions

Pin No.	Name	Туре	Description
1	GND	PWR	Signal ground
2	RTS#	Output	Request To Send control output – Handshake signal
3	5V0	PWR	5V supply input
4	RXD	Input	Receive asynchronous data input
5	TXD	Output	Transmit asynchronous data output
6	CTS#	Input	Clear To Send control input - Handshake signal
7	NC	-	No Connect
8	RI#/WU	Input	Ring Indicator control input / Wake Up

Table 3.2 – 3.3V TTL/CMOS UART Pin Out

Pin No.	Name	Туре	Description
5	CLK	Input	SPI clock input. Maximum frequency: 24MHz.
4	MOSI	Input	SPI slave serial data input
2	MISO	Output	SPI slave serial data output
6	SS#	Input	SPI slave select input

Table 3.3 – 3.3V TTL/CMOS SPI Pin Out

For further details see VNC2 datasheet.

4 VMusic2 and VMusic3 comparisons

The VMusic3 is a drop in replacement for the VMusic2 for the majority of VMusic2 applications. VMusic3 uses firmware called V2MSC which is similar to V2DAP (used in VDRIVE3) with an additional module for controlling MP3 playback. However for a small number of applications that use SPI, differences exists between VMUSIC firmware and V2MSC firmware which would require some changes to be made to the application software. For further details on this discrepancy please see <u>AN 176 - Vinculum Comparison of VDAP and V2DAP</u>.

Additional features of the VMusic3:

- Vinculum-II can be configured by a user defined firmware
- VMusic3 has an SPI master interface available (not enabled in V2MSC firmware).
- VMusic3's SPI interface can be clocked up to 24MHz
- VMusic3 can be programmed using the debugger-module port in addition to programming using the UART interface port.
- VMusic3 can utilise many of the Vinculum-II sample firmware available on the FTDI website.



5 VMusic3 Application Example

VMusic3 can be used to play audio from a flash disk. An example is given where a PIC is used to send commands to the VMusic3 select playing option such as play, pause and skip.

It is also possible to control the VMusic3 from a PC using a <u>TTL-232R-3V3-2mm</u> and a terminal. See <u>Vinculum Firmware User Manual</u> for details on the control commands.

Out Rid 3.5mm Stereo a Line Out Le /DC GNE RAS ICSPDAT fic Ind Ir LEC RA4 ICSPCLK RA2 MCLR RA2 RTS RC тхр RX RCO RC RXD тх RC1 RTS# CTS RC3 RC2 PIC16F688 USB Flash D Skip Forward

5.1 UART Interface to PIC Example

Figure 5.1 – MP3 playback using VMusic3 controlled by a PIC MCU

A VMusic2 compatible example is given in Figure 5.1. This example shows a VMusic3 interfacing with an external PIC MCU and supporting components. In this example four push buttons are used to control play / pause, stop, skip forward / volume up and skip back / volume down of the MP3 player.

For more information on this application see VMUSIC SPI PIC Sample on the following web page:

http://www.ftdichip.com/Support/SoftwareExamples/VinculumProjects.htm



6 VMusic3 Commands Details

The command set for the VMusic3 is given in Table 6.1.

For more details on Vinculum commands please see: <u>http://www.ftdichip.com/Firmware/Precompiled/UM_VinculumFirmware_V205.pdf</u>

Extended Command Set	Short Command Set (Hexadecimal Codes)	Function
VPF·file 4	1D 20 file OD	Plays a single file
VRF·file 4	89 20 file OD	Repeatedly plays a single file
VST 4	20 OD	Stops playback
V3A 🖌	21 OD	Plays all MP3 files
VRA 🗸	8A 0D	Repeatedly plays all MP3 files
VRR 4	8F 0D	Repeatedly plays random MP3 files
VSF 4	25 OD	Skip forward one track
VSB 🗸	26 OD	Skip back one track
VSD 4	8E 0D	Skip forward on whole directory
VP 4	8B 0D	Pause playback
AL 4	8C 0D	Fast forward 5 seconds
VB 4	8D 0D	Rewind 5 seconds
VRD·byte 4	1F 20 byte OD	Reads command register
VWR·byte+word 4	1E 20 byte word 0D	Writes command register
VSV·byte 4	88 20 byte 0D	Sets playback volume

Table 6.1 – V2MSC Command Set



7 VMusic3 Electrical Details

7.1 SPI Interface Timing

The following timing diagrams are for the VNC1L Legacy Interface mode of SPI slave.



Figure 7.1 – SPI

To start the data transfer process SS# needs to be set high, and remain high for the entire read cycle. Once the read cycle completes SS# needs to be set low for at least one clock cycle to allow another data transfer cycle to occur.

The first bit of MOSI is the R/W bit, receiving a logic high for this bit allows data to be read from the VMusic3. The second bit is the address bit, ADD, this bit is used to select reading data from the data register when set to logic high, or from the status register when set to logic low. During an SPI Read cycle a package of data is transmitted from the VMusic3 on the MISO line from the time of the first clock cycle after the SPI ADD bit, with the MSB transmitted first.

After the data has been transferred the status of MISO can be checked to determine if the data read is new data that has not been read before, which is indicated by a transmitted logic low. Otherwise if old data is being transmitted, which is indicated by a transmitted logic high, the read cycle needs to be repeated to get new data.



Figure 7.2 – VMusic3 SPI Waveforms

To start the data transfer process SPI SS# needs to be set high, and remain high for the entire write cycle. Once the write cycle SPI completes SS# needs to be set low for at least one clock cycle to allow another data transfer cycle to occur. The first bit of MOSI is the R/W bit, receiving a logic low for this bit allows data to be written to the VMusic3.



The second bit is the address bit, ADD, this bit is used to select a data write to the data register when set to logic high, and to the status register when set to logic low. During an SPI Write cycle a package of data is transmitted to the VMusic3 on the MOSI line from the first clock cycle after the SPI ADD bit, with the MSB transmitted first.

After the data has been transferred the status of MISO can be checked to determine if the data written has been accepted. If a logic low is given for the status bit, it can be determined from this that the data write was successful. If logic high is given for the status bit, the internal buffer of the device receiving data is full, and the same write cycle should be repeated.



Figure 7.3 – VMusic3 SPI Timing

Time	Description	Min	Typical	Max	Unit
T1	SCLK Period	83	-	-	ns
T2	SCLK High	20	-	-	ns
Т3	SCLK Low	20	-	-	ns
T4	Input Setup Time	10	-	-	ns
T5	Input Setup Time	10	-	-	ns
T6	Input Hold Time	2	-	-	ns
T7	Output Valid Time	-	-	20	ns
Table 7	1 – SPI Timing Table				



8 VMusic3 Max-Ratings

The absolute maximum ratings for the VDrive3 devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Unit	Conditions
Storage Temperature	-40°C to 85°C	Degrees C	
Ambient Operating Temperature (Power Applied)	-30°C to 85°C	Degrees C	
VCC Supply Voltage	-0.3 to +5.5	V	
DC Input Voltage – USBDP and USBDM	-0.5 to +3.63	V	

Table 8.1 – Absolute Maximum Ratings

9 VMusic3 Mechanical Details











Figure 9.1 – VMusic3 Dimensions



10 VMusic3 Circuit Schematic



Figure 10.1 – Module Circuit Schematic



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Appendix B – Revision History

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