EVE3 TFT Module

Hardware Manual

Revision 1.0

Revision History

Revision	Date	Description	Author
1.0	March 13, 2019	Initial Release	Divino

Contents

Revision History 1

1. Introduction 1

    1.1. Key Features 1

    1.2. Block Diagram 1

2. Bridgetek EVE BT81x Graphics Engine 2

3. Ordering 3

    3.1. Ordering Part Numbering Scheme 3

    3.2. Options 3

    3.3. Recommend Parts 4

        EVE2-USB2SPI-KIT-A 4

        EVE2-SHIELD 4

        EVE2-SPI2BBC 4

4. EVE3 Headers 5

    4.1. SPI Communication and Power Header Pinout 5

    4.2. BT81x Communication Pads 6

5. Communication Interface 7

    5.1. SPI Interface Timing Specification 7

    5.2. SPI and QSPI communication 7

    5.3. Serial Data Protocol 9

6. BT81x Peripherals 9

    6.1. Audio Engine 9

    6.2. Sound Synthesizer 9

    6.3. Audio Playback 11

    6.4. General Purpose Input Output 11

    6.5. SPI NOR Flash Interface 12

    6.6. Backlight Driver 12

    6.7. Touch Configuration File 12

7. TFT Display 13

    7.1. EVE3 Module Displays 13

    7.2. EVE3 TFT Display Timings 13

8. Mounting 14

    8.1. Mounting TFT Panels 14

    8.2. 3D Printed Cases/Mounts 14

9. Electrical Characteristics 15

    9.1. Absolute Maximum Ratings 15

    9.2. EVE3 DC Characteristics 15

    9.3. EVE3 Digital I/O Pin Characteristics 15

    9.4. Power Specifications 15

    9.5. Touch Sense Characteristics 16

10. Dimensional Drawing 17

11. EVE3 Schematic 18

12. Contact 18

1. Introduction

The Matrix Orbital EVE3 lineup utilizes Bridgetek's third generation BT81x Embedded Video Engine to control, render, manage and display complex graphics on a full color TFT touch screen. By taking advantage of the 1 megabyte of graphics RAM, motion-JPEG encoded AVI videos can be played back in both portrait and landscape mode. Data can be displayed through a set of widgets such as gauges, spinners, sliders, and bar graphs.

Additional features include compatibility with capacitive or resistive touch panels and support for up to 255 touch objects on screen. Mono 8-bit linear audio wave playback at sampling frequencies from 8 kHz to 48 kHz is made possible by the built-in sound synthesizer and digital filter. Up to 256Megabits of high speed QSPI NOR Flash can be added to the EVE3 TFT Module allowing image, font, audio, and video assets to be stored on the EVE3 board.

The EVE3 communicates using SPI protocol, and can be configured for quad SPI communication. Using SPI communication protocol makes the EVE3 compatible with many microcontrollers available on the market, including the Bridgetek FT900, NXP 17XX, Arduino, and many more. With built-in graphics operations, and support for multiple widgets, development of high-quality Human Machine Interfaces (HMI) screens is simplified.

1.1. Key Features

- Advanced Embedded Video Engine(EVE) BT81x with high resolution graphics and video playback
- Support multiple widgets for simplified design development
- Support for Resistive and Capacitive Touch Screen Technology
- Support capacitive touch screen with up to 5 touches detection
- Support for LCD display with resolution up to SVGA (800x600) and formats with data enable (DE) mode or VSYNC/HSYNC mode
- Support landscape and portrait orientations
- Support playback of motion-JPEG encoded AVI videos
- -20°C to 70°C extended operating temperature range
- Up to 256 Megabits of QSPI NOR Flash memory

1.2. Block Diagram

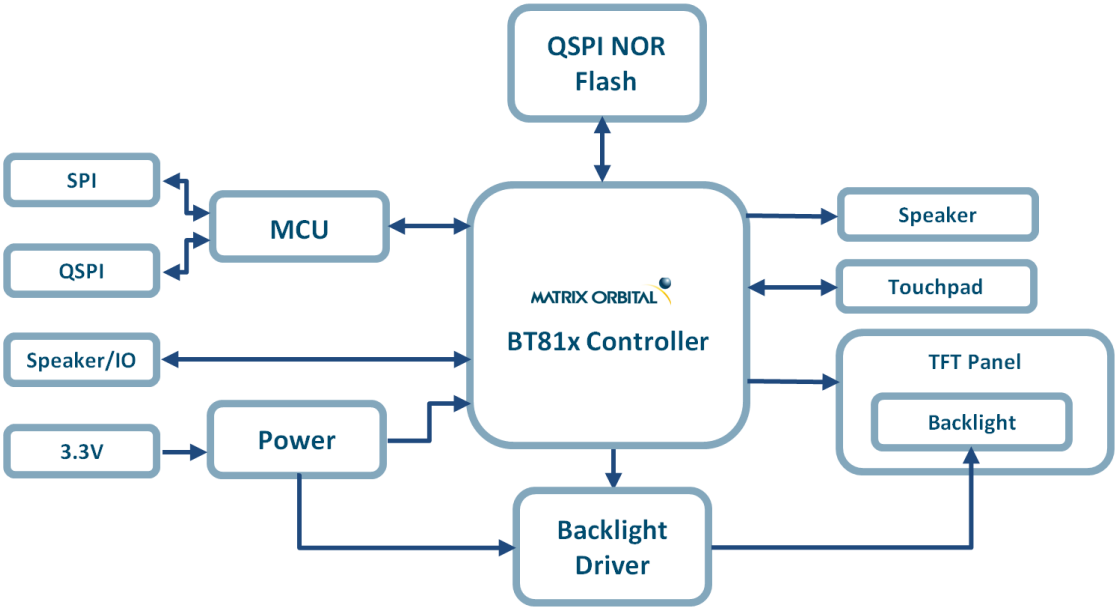

Figure 1: EVE3 Block Diagram

2. Bridgetek EVE BT81x Graphics Engine

The BT81x series chips are graphics controllers with add-on features such as audio playback and touch capabilities, and contain a rich set of graphic objects (primitive and widgets) that can be used for displaying various menus and screens for a range of products including home appliances, toys, industrial machinery, home automation, elevators, and many more.

The BT81x EVE graphics controller ICs combine display, touch and audio functionality within a single chip and take an innovative object-oriented approach to HMI implementation that is proving highly effective. The third generation EVE devices at the heart of the EVE3 TFT Module has a greater pixel resolution than previous EVE ICs, resulting in sharper image rendering and greater colour depth. The BT81x also has accelerated data transfer and image/video loading capabilities, enhanced video playback, plus expanded memory resources.

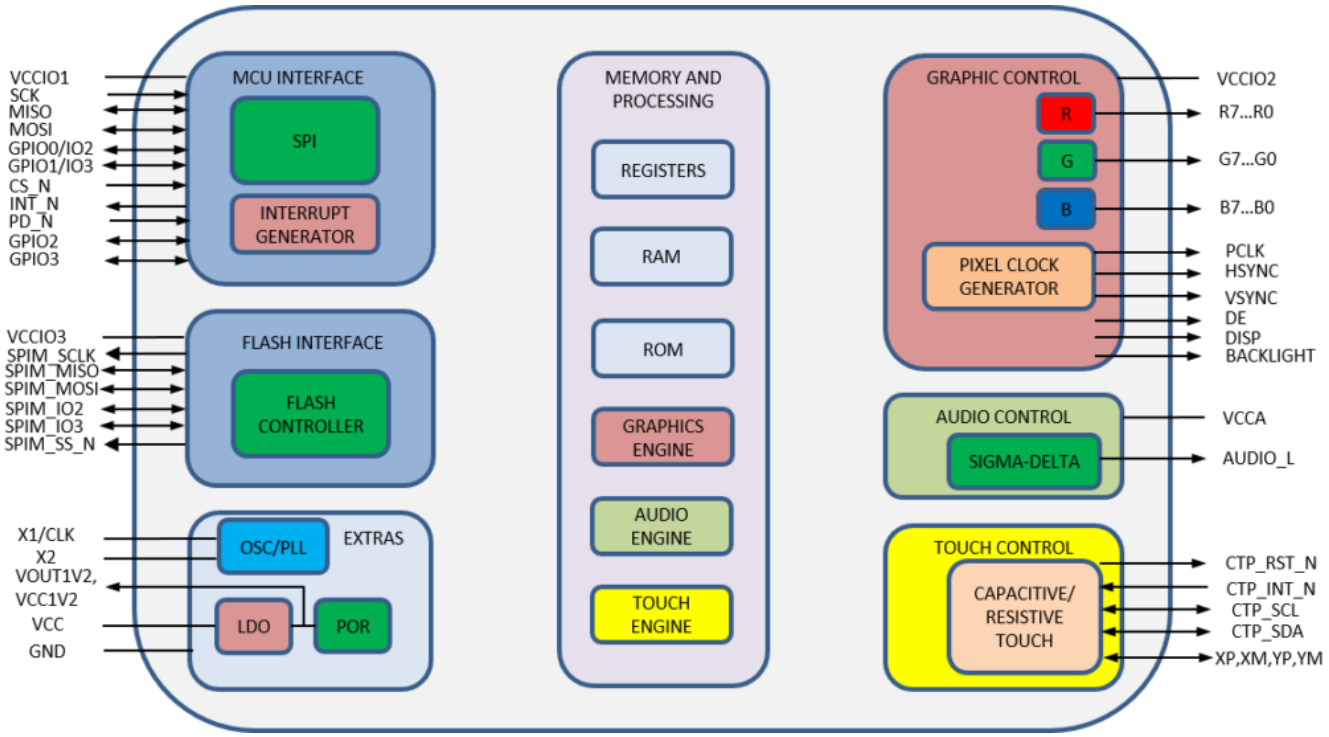

Figure 2: EVE3 Embedded Video Engine

More details regarding the BT81x, and how to control it can be found on the official Bridgetek website, http://www.brtchip.com/bt81x

3. Ordering

The EVE3 has multiple size and touch variants, to ensure that there is an option for every application. Resistive and capacitive touch panels are also available, allowing interactive touch functionality for all applications.

3.1. Ordering Part Numbering Scheme

Table 1: EVE3 Part Numbering Scheme

EVE3	-35	A	-BLM	-TPN	-F256
1	2	3	4	5	6

3.2. Options

Table 2: EVE3 Display Options

#	Designator	Options
1	Product Type	EVE3: BT81X TFT Display
2	Display Size	35: 3.5” 43:4.3” 50:5.0” 70:7.0”
3	Screen Type	A: Standard TFT G: Extended Bezel touch panel
4	Backlight	-BLM: 300 Nit < Brightness < 600 Nit -BLH: 600 Nit < Brightness < 1000 Nit -BLD: Brightness > 1000 Nit
5	Touch	-TPC: Capacitive -TPR: Resistive -TPN: None
6	Memory	-F0: 0 Mb QSPI NOR Flash memory -F32: 32 Mb QSPI NOR Flash memory -F64: 64 Mb QSPI NOR Flash memory -F128: 128 Mb QSPI NOR Flash memory -F256: 256 Mb QSPI NOR Flash memory

3.3. Recommend Parts

EVE2-USB2SPI-KIT-A

Figure 3: EVE2-USB2SPI-KIT-A

The Matrix Orbital USB to SPI Bridge utilizes the FTDI FT232H IC, allowing users to communicate to their SPI devices through a USB interface. Made specifically to be used with the Matrix Orbital EVE series of displays, the USB to SPI Bridge can help decrease development time and reduce development hardware complexity.

EVE2-SHIELD

Figure 4: EVE2-SHIELD

The Scoodo is an interface module for Matrix Orbital EVE SPI TFT displays to Arduino Uno and Parallax Propeller Shield products.

EVE2-SPI2BBC

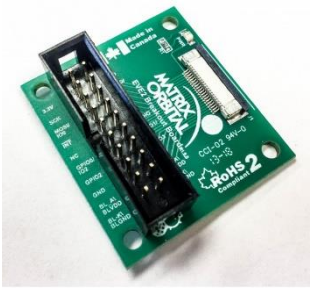

Figure 5: EVE2-SPI2BBC

A simple breakout board that allows converts the EVE's 20 pin FFC cable to a 20 position 2.54mm 2 row straight pin header.

4. EVE3 Headers

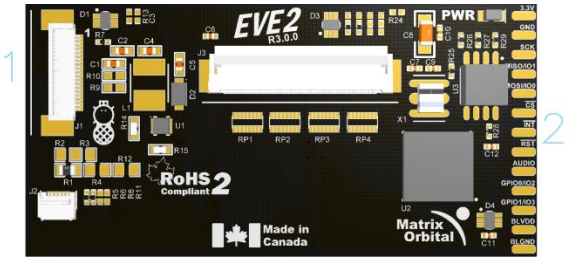

Figure 6: EVE3 TFT Module Header Locations

Table 3: List of available Headers

#	Header	Standard Mate
1	SPI Communication and Power	FFC-20P
2	BT81x Communication pads	None

4.1. SPI Communication and Power Header Pinout

The 20 pin FFC header on the EVE3 is used to interface with an SPI controller, and is compatible with a number of 20 pin ribbon cables. Any 20 pin FFC cable with a 0.5mm pitch and bottom contacts, such as the Wurth Electronics INC 687620050002 series ribbon cable will be compatible with the EVE3 TFT Module.

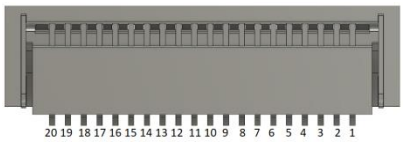

Figure 7: EVE3 TFT Module 20 pin FFC communication header

Table 4: EVE3 TFT Module 20 pin FFC communication header pinout

Pin	Symbol	Type	Function
1	VCC	Power	Logic Voltage (3.3V)
2	GND	Ground	Ground Connection
3	SCK	Input	SPI clock input
4	MISO	Input/output	SPI Single mode: SPI MISO output SPI Dual/Quad mode: SPI data line 1
5	MOSI	Input/output	SPI Single mode: SPI MISO input SPI Dual/Quad mode: SPI data line 0
6	CS	Input	SPI slave select input.*
7	$\overline{\text{INT}}$	Open Drain Output	Interrupt to host**
8	RST		BT81x Reset pin
9	N/C	No connection	No connection
10	AUDIO	Output	Audio PWM out
11	IO2	Input/output	SPI Single/Dual mode: General purpose IO 0 SPI Quad mode: SPI data line 2
12	IO3	Input/output	SPI Single/Dual mode: General purpose IO 1 SPI Quad mode: SPI data line 3
13	GPIO2	Input/output	General purpose IO 2
14	GPIO3	Input/output	General purpose IO 3
15	GND	Ground	Ground connection
16	VCC	Power	Logic Voltage (3.3V)
17	BLVDD	VDD	No Connect (Optional Backlight Voltage)
18	BLVDD	VDD	No Connect (Optional Backlight Voltage)
19	BLGND	Ground	Ground
20	BLGND	Ground	Ground

***Note:** The CS pin signifies when a SPI transaction occurs by going active low. When the pin goes inactive high, the write operation is considered complete.

****Note:** Open drain output (default) or push-pull output, active low

4.2. BT81x Communication Pads

All of the BT81x Communication pins are extended out and made available through the BT81x solder pads on the module. These solder pads offer an alternative method of connecting to the BT81x and provides the same functionality as their SPI Communication Header counterparts.

Each pad is 1 mm wide, 3mm in length, and follows a 2.54 mm pitch. It is recommended that 18 gauge wire or greater is used when soldering to these pads.

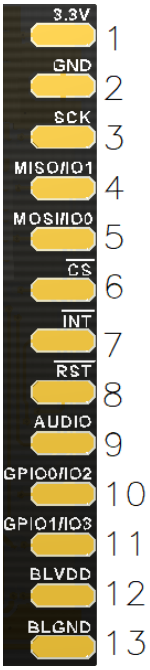

Figure 8: BT81x Solder Pads

Table 5: BT81x Solder Pad pinout

Pin	Symbol	Type	Function
1	3.3V	Power	Logic Voltage (3.3V)
2	GND	Ground	Ground Connection
3	SCK	Input	SPI clock input
4	MISO/IO1	Input/output	SPI Single mode: SPI MISO output SPI Dual/Quad mode: SPI data line 1
5	MOSI/ IO0	Input/output	SPI Single mode: SPI MISO input SPI Dual/Quad mode: SPI data line 0
6	$\overline{CS}$	Input	SPI slave select input.*
7	$\overline{INT}$	Open Drain Output	Interrupt to host**
8	$\overline{RST}$		BT81x Reset pin
9	AUDIO	Output	Audio PWM out
10	GPIO0/IO2	Input/output	SPI Single/Dual mode: General purpose IO 0 SPI Quad mode: SPI data line 2
11	GPIO1/IO3	Input/output	SPI Single/Dual mode: General purpose IO 1 SPI Quad mode: SPI data line 3
12	BLVDD	VDD	No Connect (Optional Backlight Voltage)
13	BLGND	Ground	Ground

***Note:** The CS pin signifies when a SPI transaction occurs by going active low. When the pin goes inactive high, the write operation is considered complete.

****Note:** Open drain output (default) or push-pull output, active low

5. Communication Interface

5.1. SPI Interface Timing Specification

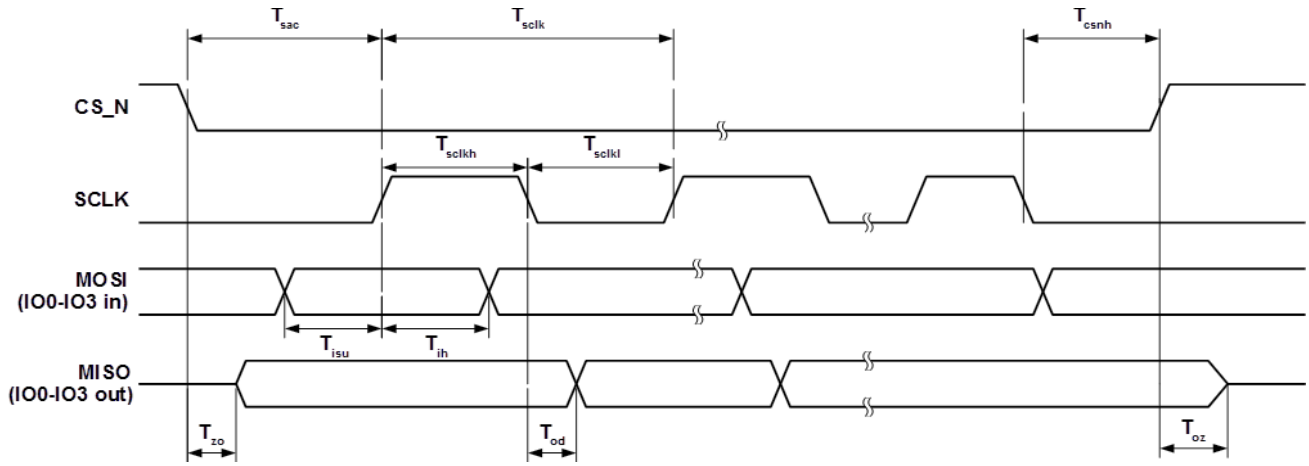

Figure 9: SPI Timing Diagram

Table 6: SPI Timing Signals

Parameter	Description	VCCIO = 3.3V		Units
		Min	Max	
Tsclk	SPI Clock Period (SINGLE/DUAL mode)	33.3		ns
Tslck	SPI clock Period (QUAD mode)	40		ns
Tsclkl	SPI clock low duration	13		ns
Tsclkh	SPI clock high duration	13		ns
Tsac	SPI access time	3		ns
Tisu	Input Setup	3		ns
Tih	Input hold	0		ns
Tzo	Output enable delay		11	ns
Toz	Output disable delay		10	ns
Tod	Output data delay		11	ns
Tcsnh	CSN hold time	0		ns

5.2. SPI and QSPI communication

The EVE3 is capable of communicating to hosts and microcontrollers through a quad serial parallel interface (QSPI). Only SPI mode 0 is supported. The QSPI slave interface can operate up to 30MHZ, and can be configured in SINGLE, DUAL or QUAD channel modes.

The SPI slave defaults to SINGLE channel mode operation, using MISO as output to the master and MOSI as input from the master. The SPI slave can be configured to allow DUAL and QUAD channel modes by writing to register REG_SPI_WIDTH while in single channel mode.

Table 7: SPI/QSPI Communication Configuration

REG_SPI_WIDTH[1:0]	Channel Mode	Data pins	Max bus speed
00	SINGLE - default mode	MISO, MOSI	30 MHz
01	DUAL	IO0, IO1	30 MHz
10	QUAD	IO0, IO1, IO2, IO3	25 MHz
11	Reserved	-	-

When DUAL/QUAD channel modes are enabled, the SPI data ports become unidirectional. SPI transactions will be signified by CS going active low when DUAL/QUAD modes are active, and data ports are set as inputs.

Hence, for writing to the BT81x, the protocol is “WR-Command/Addr2, Addr1, Addr0, DataX, DataY, DataZ …” The write operation is considered complete when CS goes inactive high.

For reading from the BT81x, the protocol is “RD-Command/Addr2, Addr1, Addr0, Dummy-Byte, DataX, DataY, DataZ”. However as the data ports are now unidirectional, a change of port direction will occur before DataX is clocked out of the BT81x. Therefore it is important that the firmware controlling the SPI master changes the SPI master data port direction to “input” after transmitting Addr0. The BT81x will not change the port direction till it starts to clock out DataX. Hence, the Dummy-Byte cycles will be used as a change-over period when neither the SPI master nor slave will be driving the bus; the data paths thus must have pull-ups/pull-downs. The SPI slave from the BT81x will reset all its data ports’ direction to input once CS goes inactive high (i.e. at the end of the current SPI master transaction).

The below diagram depicts the behaviour of both the SPI master and slave in the master read case.

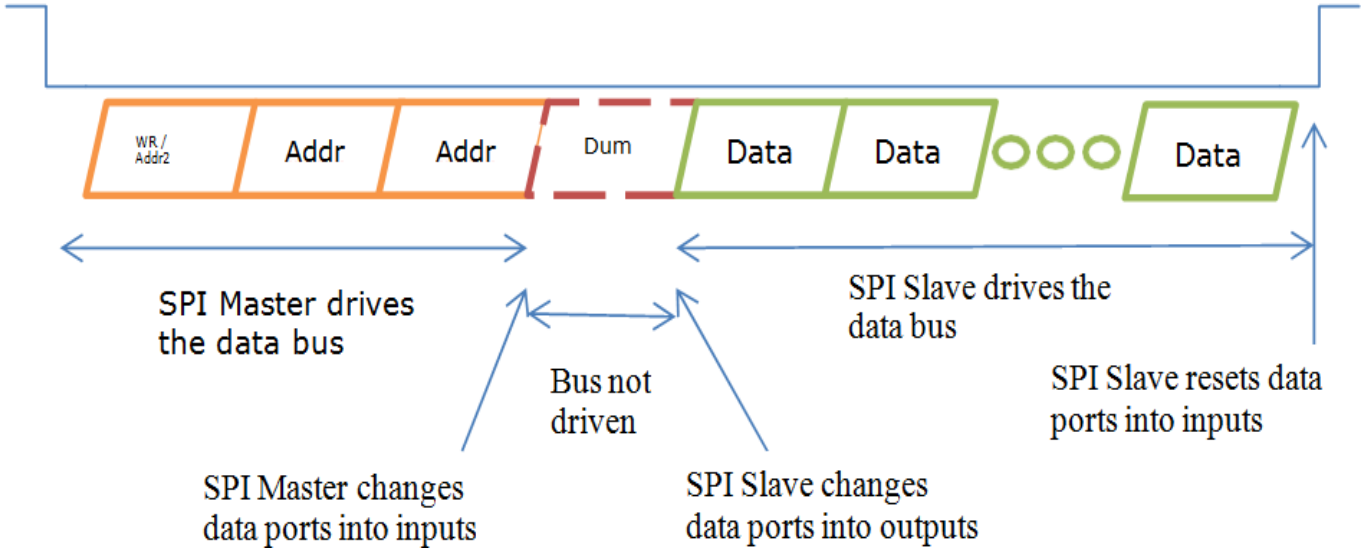

Figure 10: SPI Master and Slave bus behaviour

For DUAL channel operation, MISO(MSB) and MOSI are used. In Quad channel operation, IO3(MSB), IO2, MISO, and MOSI are used.

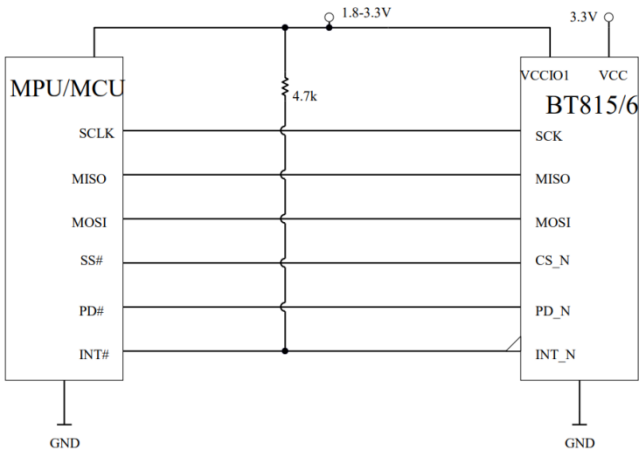

Figure 11: Single/Dual Channel SPI Interface connection

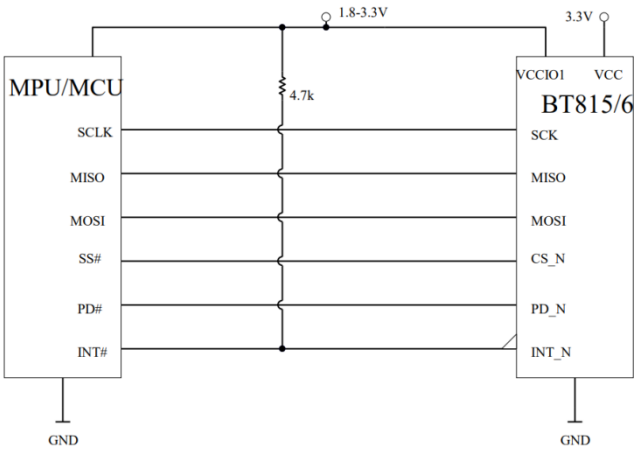

Figure 12: Quad channel SPI Interface connection

5.3. Serial Data Protocol

When interfaced with a host, the BT81x will appear as a memory-mapped SPI device. Communication between the host and the BT81x is accomplished through a series of reads and writes to a large (4 megabyte) address space. Within this address space are dedicated areas for graphics, audio and touch control.

The BT81x address space is read and written to using SPI transactions. Memory read, memory write and command write transactions are sent by the most significant bit first.

Each transaction starts with CS going low, and ends when CS going high. Data transactions have no limit regarding data length, so long as the memory address is continuous.

When initiating an SPI memory read transaction, the host will send two zero bits, followed by the 22-bit address. A dummy byte follows the address, and the BT81x will respond to each host byte with read data bytes.

Table 8: SPI Memory read transaction

7	6	5	4	3	2	1	0	
0	0	Address [21:16]						Write Address
Address [15:8]								
Address [7:0]								
Dummy byte								
Byte 0								Read Address
Byte n								

For SPI memory write transactions, a ‘1’ bit and ‘0’ bit is sent by the host, followed by the 22-bit address. The write data follows.

Table 9: SPI Memory write transaction

7	6	5	4	3	2	1	0	
1	0	Address [21:16]						Write Address
Address [15:8]								
Address [7:0]								
Dummy byte								
Byte 0								Read Address
Byte n								

6. BT81x Peripherals

6.1. Audio Engine

BT81x provides mono audio output through a PWM output pin, AUDIO_L. It outputs two audio sources; the sound synthesizer and audio file playback.

6.2. Sound Synthesizer

A sound processor, AUDIO ENGINE, generates the sound effects from a small ROM library of waves table. To play a sound effect listed in the Sound Effect table, load the REG_SOUND register with a code value and write 1 to the REG_PLAY register. The REG_PLAY register reads 1 while the effect is playing and returns a ‘0’ when the effect ends. Some sound effects play continuously until interrupted or instructed to play the next sound effect. To interrupt an effect, write a new value to REG_SOUND and REG_PLAY registers; e.g. write 0 (Silence) to REG_SOUND and 1 to PEG_PLAY to stop the sound effect.

The sound volume is controlled by register REG_VOL_SOUND. The 16-bit REG_SOUND register takes an 8-bit sound in the low byte. For some sounds, marked "pitch adjust" in the table below, the high 8 bits contain a MIDI note value. For these sounds, a note value of zero indicates middle C. For other sounds the high byte of REG_SOUND is ignored.

Table 10: Sound Effect

Value	Effect	Continuous	Pitch Adjust
00h	Silence	Y	N
01h	Square Wave	Y	Y
02h	Sine Wave	Y	Y
03h	Sawtooth Wave	Y	Y
04h	Triangle Wave	Y	Y
05h	Beeping	Y	Y
06h	Alarm	Y	Y
07h	Warble	Y	Y
08h	Carousel	Y	Y
10h	1 short pip	N	Y
11h	2 short pips	N	Y
12h	3 short pips	N	Y
13h	4 short pips	N	Y
14h	5 short pips	N	Y
15h	6 short pips	N	Y
16h	7 short pips	N	Y
17h	8 short pips	N	Y
18h	9 short pips	N	Y
19h	10 short pips	N	Y
1Ah	11 short pips	N	Y
1Bh	12 short pips	N	Y
1Ch	13 short pips	N	Y
1Dh	14 short pips	N	Y
1Eh	15 short pips	N	Y
1Fh	16 short pips	N	Y
23h	DTMF #	Y	N
2Ch	DTMF *	Y	N
30h	DTMF 0	Y	N
31h	DTMF 1	Y	N
32h	DTMF 2	Y	N
33h	DTMF 3	Y	N
34h	DTMF 4	Y	N
35h	DTMF 5	Y	N
36h	DTMF 6	Y	N
37h	DTMF 7	Y	N
38h	DTMF 8	Y	N
39h	DTMF 9	Y	N
40h	Harp	N	Y
41h	Xylophone	N	Y
42h	Tuba	N	Y
43h	Glockenspiel	N	Y
44h	Organ	N	Y
45h	Trumpet	N	Y
46h	Piano	N	Y
47h	Chimes	N	Y
48h	Music Box	N	Y
49h	Bell	N	Y
50h	Click	N	N
51h	Switch	N	N
52h	Cowbell	N	N
53h	Notch	N	N
54h	Hihat	N	N
55h	Kickdrum	N	N
56h	Pop	N	N
57h	Clack	N	N
58h	Chack	N	N
60h	Mute	N	N
61h	Unmute	N	N

Table 11: MIDI Note Effect

MIDI note	ANSI note	Freq (Hz)	MIDI note	ANSI note	Freq (Hz)	MIDI note	ANSI note	Freq (Hz)	MIDI note	ANSI note	Freq (Hz)
21	A0	27.5	43	G2	98.0	65	F4	349.2	87	D#6	1244.5
22	A#0	29.1	44	G#2	103.8	66	F#4	370.0	88	E6	1318.5
23	B0	30.9	45	A2	110.0	67	G4	392.0	89	F6	1396.9
24	C1	32.7	46	A#2	116.5	68	G#4	415.3	90	F#6	1480.0
25	C#1	34.6	47	B2	123.5	69	A4	440.0	91	G6	1568.0
26	D1	36.7	48	C3	130.8	70	A#4	466.2	92	G#6	1661.2
27	D#1	38.9	49	C#3	138.6	71	B4	493.9	93	A6	1760.0
28	E1	41.2	50	D3	146.8	72	C5	523.3	94	A#6	1864.7
29	F1	43.7	51	D#3	155.6	73	C#5	554.4	95	B6	1975.5
30	F#1	46.2	52	E3	164.8	74	D5	587.3	96	C7	2093.0
31	G1	49.0	53	F3	174.6	75	D#5	622.3	97	C#7	2217.5
32	G#1	51.9	54	F#3	185.0	76	E5	659.3	98	D7	2349.3
33	A1	55.0	55	G3	196.0	77	F5	698.5	99	D#7	2489.0
34	A#1	58.3	56	G#3	207.7	78	F#5	740.0	100	E7	2637.0
35	B1	61.7	57	A3	220.0	79	G5	784.0	101	F7	2793.8
36	C2	65.4	58	A#3	233.1	80	G#5	830.6	102	F#7	2960.0
37	C#2	69.3	59	B3	246.9	81	A5	880.0	103	G7	3136.0
38	D2	73.4	60	C4	261.6	82	A#5	932.3	104	G#7	3322.4
39	D#2	77.8	61	C#4	277.2	83	B5	987.8	105	A7	3520.0
40	E2	82.4	62	D4	293.7	84	C6	1046.5	106	A#7	3729.3
41	F2	87.3	63	D#4	311.1	85	C#6	1108.7	107	B7	3951.1
42	F#2	92.5	64	E4	329.6	86	D6	1174.7	108	C8	4186.0

6.3. Audio Playback

The BT81x can play back recorded sound through its audio output. To do this, load the original sound data into the BT81x's RAM, and set registers to start the playback.

The registers controlling audio playback are:

REG_PLAYBACK_START:	The start address of the audio data
REG_PLAYBACK_LENGTH:	The length of the audio data, in bytes
REG_PLAYBACK_FREQ:	The playback sampling frequency, in Hz
REG_PLAYBACK_FORMAT:	The playback format, one of LINEAR SAMPLES, uLAW SAMPLES, or ADPCM SAMPLES
REG_PLAYBACK_LOOP:	If zero, the sample is played once. If one, the sample is repeated indefinitely
REG_PLAYBACK_PLAY:	A write to this location triggers the start of audio playback, regardless of writing '0' or '1'. Read back '1' when playback is ongoing, and '0' when playback finishes
REG_VOL_PB:	Playback volume, 0-255

The mono audio formats supported are 8-bits PCM, 8-bits uLAW and 4-bits IMA-ADPCM. For ADPCM_SAMPLES, each sample is 4 bits, so two samples are packed per byte, the first sample is in bits 0-3 and the second is in bits 4-7.

The current audio playback read pointer can be queried by reading the REG_PLAYBACK_READPTR. Using a large sample buffer, looping, and this read pointer, the host MPU/MCU can supply a continuous stream of audio.

6.4. General Purpose Input Output

Depending on the package, the BT81x can be configured to use up to 4 GPIO pins. These GPIO pins are controlled by the REG_GPIOX_DIR and REG_GPIOX registers. Alternatively the GPIO0 and GPIO1 pins can also be controlled by REG_GPIO_DIR and REG_GPIO to maintain backward compatibility with the FT800/FT801.

6.5. SPI NOR Flash Interface

NOR flash memory has been included with the EVE3 TFT Module, and can be accessed through SPI. The on-board flash memory will allow you to store audio files, images, animations and videos on your EVE, reducing the amount of flash memory taken up on the host side.

A specific set of commands are available to access the on-board flash. In addition, the BT81x can be configured for full speed communication with the on-board flash.

6.6. Backlight Driver

The EVE3 TFT Module comes equipped with its own backlight driver and integrated backlight control circuit, but if you are running a high brightness or 7" inch display variant, more power may need to be supplied to the display. The EVE3 Module can be configured to provide additional current through pins 17, 18, 19, and 20 by populating the R1 and R2 resistor pads with 0 Ohm resistors. With R1 and R2 populated, additional 3.3V power can be supplied to pins 17 and 18, doubling the amount of current that can be fed to the display.

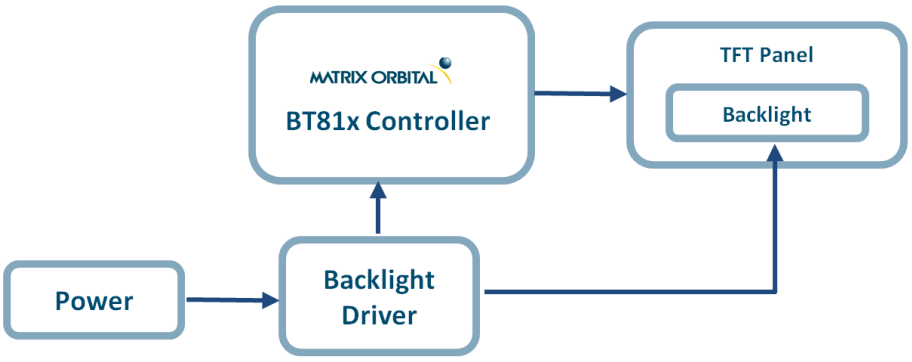

Figure 13: Backlight Driver Block Diagram

6.7. Touch Configuration File

The EVE3 TFT Module can be ordered with a resistive or capacitive touch panel. Both touch variants require minimal setup in order to operate properly.

Resistive touch panel sensitivity can be increased by adjusting the resistive pressure threshold. The pressure threshold is specified through the REG_TOUCH_RZ register. A lower pressure value indicates a higher pressure threshold. It is recommended to set the pressure threshold to 1200 for testing, and adjust the value accordingly to suit your application.

The capacitive touch panel that comes with the EVE3-TPC uses a GT911 touch controller. The capacitive touch panel can be configured easily by setting the REG_TOUCH_CONFIG register to 0x05D0.

7. TFT Display

7.1. EVE3 Module Displays

The EVE3 Module is paired with a Matrix Orbital Parallel TFT display. Information about Matrix Orbital's Parallel TFT lineup, including drawings, dimensions, and tolerances can be found online at:

https://www.matrixorbital.com/index.php?route=download/download_category&dpath=178_85_229

Table 12: EVE3 Parallel Display Datasheet

EVE3 Display	Parallel TFT Datasheet
EVE3-29A	MOP-TFT320102-29A
EVE3-35A	MOP-TFT320240-35A
EVE3-43A	MOP-TFT480272-43A
EVE3-50A	MOP-TFT800480-50A
EVE3-70A	MOP-TFT800480-70A

7.2. EVE3 TFT Display Timings

Table 13: EVE3 TFT Display Timings

Display Timings	Display				
	EVE3-29	EVE3-35	EVE3-43	EVE3-50	EVE3-70
REG_HSIZE	320	320	480	800	800
REG_VSIZE	102	240	272	480	480
REG_HCYCLE	408	408	548	928	928
REG_HOFFSET	70	68	43	88	88
REG_HSYNC0	0	0	0	0	0
REG_HSYNC1	10	10	41	48	48
REG_VCYCLE	262	262	292	525	525
REG_VOFFSET	156	18	12	32	32
REG_VSYNC0	0	0	0	0	0
REG_VSYNC1	2	2	10	3	3
REG_ PCLK	8	8	5	2	2
REG_SWIZZLE	0	0	0	0	0
REG_PCLK_POL	0	0	1	1	1
REG_CSPREAD	1	1	1	0	0
REG_DITHER	1	1	1	1	1

8. Mounting

8.1. Mounting TFT Panels

Our G series extended capacitive touch EVE3 TFT Module units will come with a double sided adhesive already applied on the exposed back side of the over-sized cover glass. A 3M 93010LE tape with 300LSE adhesive is used, allowing the display to be easily mounted on flat surfaces. In addition, the tape can maintain its bond in environments of 100% relative humidity at 38°C, and can withstand temperatures up to 149°C.

Figure 14: EVE3-38G Installation

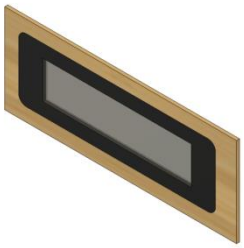

Figure 15: Completed Assembly

Resistive and Non-touch EVE modules can be mounted to panels using 3M adhesives, similar to what is applied on our G series extended capacitive touch panels. An extended metal plate with mounting points could be applied to the back of the EVE panel using adhesives to expand mounting options.

8.2. 3D Printed Cases/Mounts

A collection of 3D case designs can be found on our Matrix Orbital Thingiverse page. These designs can be downloaded and modified to suit you project needs and specifications, and then printed using a 3D printer.

If you don't have access to a 3D printer, our designs are also available for purchase from our Matrix Orbital Shapeways page.

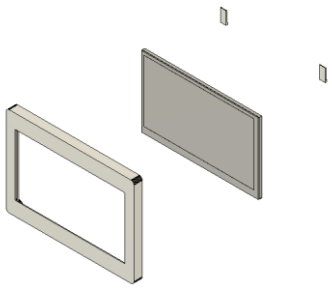

Figure 16: Display Assembly

Figure 17: Hole Guide

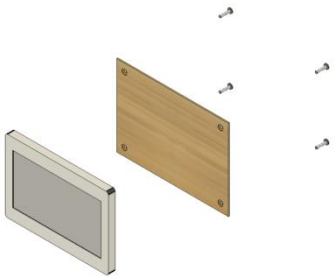

Figure 18: Display Assembly Installation

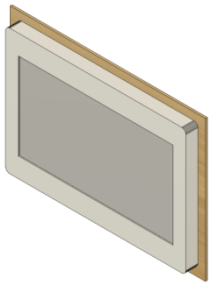

Figure 19:Completed Assembly

9. Electrical Characteristics

9.1. Absolute Maximum Ratings

Table 14: EVE3 Module Limiting Values

Item	Value	Unit
Storage Temperature	-30 to 80	°C
Ambient Temperature (Power Applied)	-20 to +70	°C
VCC Supply Voltage	0 to +4	V
DC Input Voltage	-0.5 to + (VCCIO + 0.3)	V

9.2. EVE3 DC Characteristics

Table 15: BT81x DC characteristics

Item	Description	Min.	Typ.	Max.	Unit	Conditions
VCC	VCC operating supply voltage	2.97	3.30	3.63	V	Normal Operation
Icc1	Power Down Current	-	0.2	-	mA	Power down mode
Icc2	Sleep Current	-	0.6	-	mA	Sleep Mode
Icc3	Standby Current	-	3.0	-	mA	Standby Mode
Icc4	Operating Current	-	22	-	mA	Normal Operations

9.3. EVE3 Digital I/O Pin Characteristics

Table 16: Digital I/O Specifications

Parameter	Description	Min	Typ.	Max	Units	Conditions
Voh	Output Voltage High	VCCIO- 0.4	3.3V-	-	V	Ioh=5mA
Vol	Output Voltage Low	-	-	0.4	V	Iol=5mA
Vih	Input High Voltage	2.0	-	-	V	
Vil	Input Low Voltage	-	-	0.8	V	
Vth	Schmitt Hysteresis Voltage	0.22	-	0.3	V	
Iin	Input leakage current	-10	-	10	uA	Vin = VCCIO or 0
Ioz	Tri-state output leakage current	-10	-	10	uA	Vin = VCCIO or 0
Rpu	Pull-up resistor	-	42	-	kΩ	
Rpd	Pull-down resistor	-	44	-	kΩ	

9.4. Power Specifications

Table 17: Power Characteristics

Parameter		EVE3-29A	EVE3-35A	EVE3-43A	EVE3-50A	EVE3-70A	Units
EVE3 Logic		40	40	40	40	40	mA
TFT Power Supply (max)		40	20	24	199.2	140	mA
TFT Backlight	Min	0	0	0	0	0	mA
	Typ	120	124	206	240	465	mA
	Max	144	149	247	288	558	mA

9.5. Touch Sense Characteristics

Table 18: Touch Panel characteristics

Parameter	Description	Min	Typ.	Max	Units	Conditions
Rsw-on	X-,X+,Y- and Y+ Drive On resistance	-	6	10	Ω	VCCIO=3.3V
Rsw-off	X-,X+,Y- and Y+ Drive Off resistance	10	-	-	MΩ	
Rpu	Touch sense pull up resistance	78	100	125	kΩ	
Vth+	Touch Detection rising-edge threshold on XP pin	1.59	-	2.04	V	VCCIO=3.3V
Vth-	Touch Detection falling-edge threshold on XP pin	1.23	-	1.55	V	VCCIO=3.3V
Rl	X-axis and Y-axis drive load resistance	200	-	-	Ω	

10. Dimensional Drawing

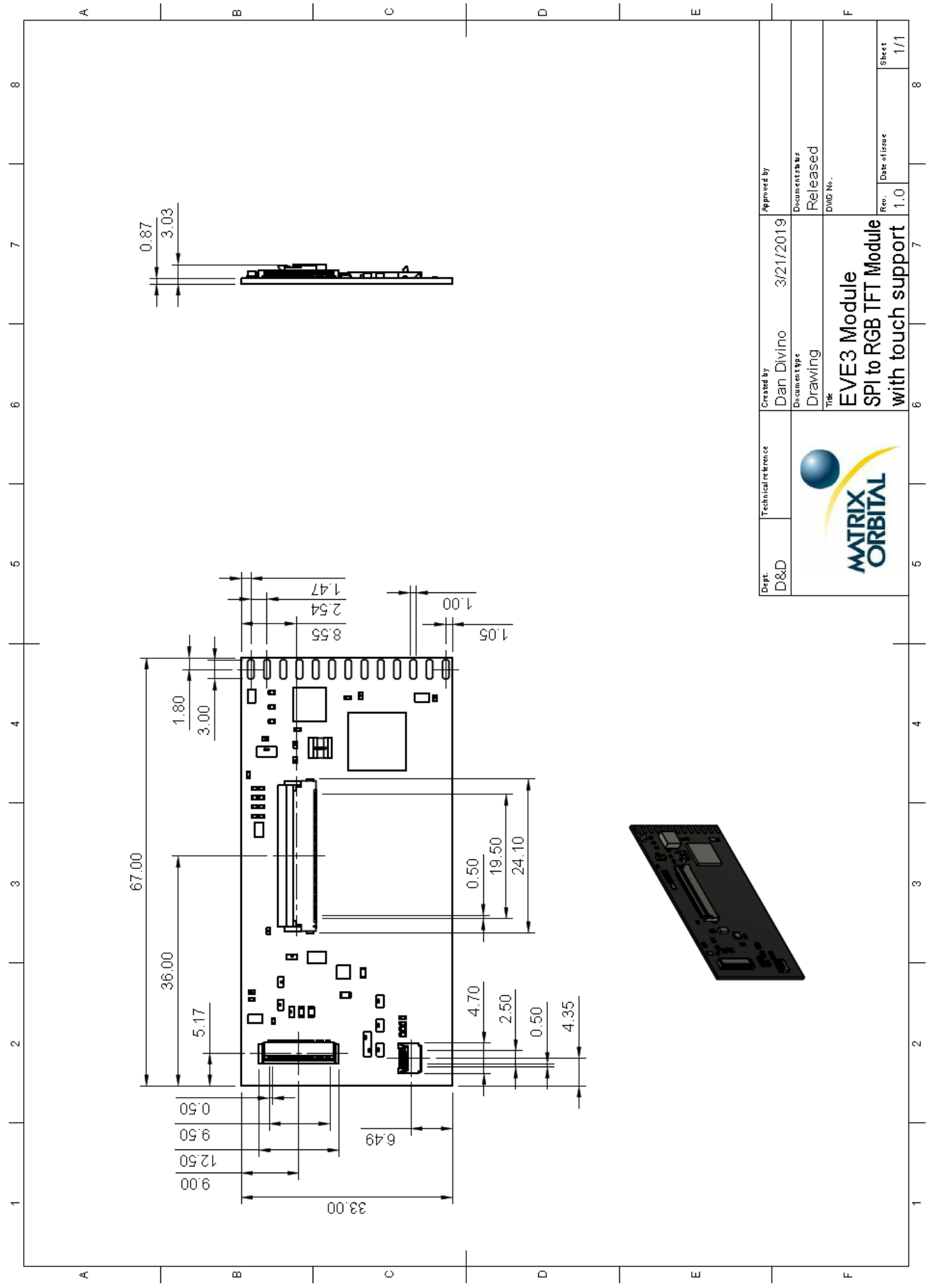

Figure 20: EVE3 Technical Drawing

11. EVE3 Schematic

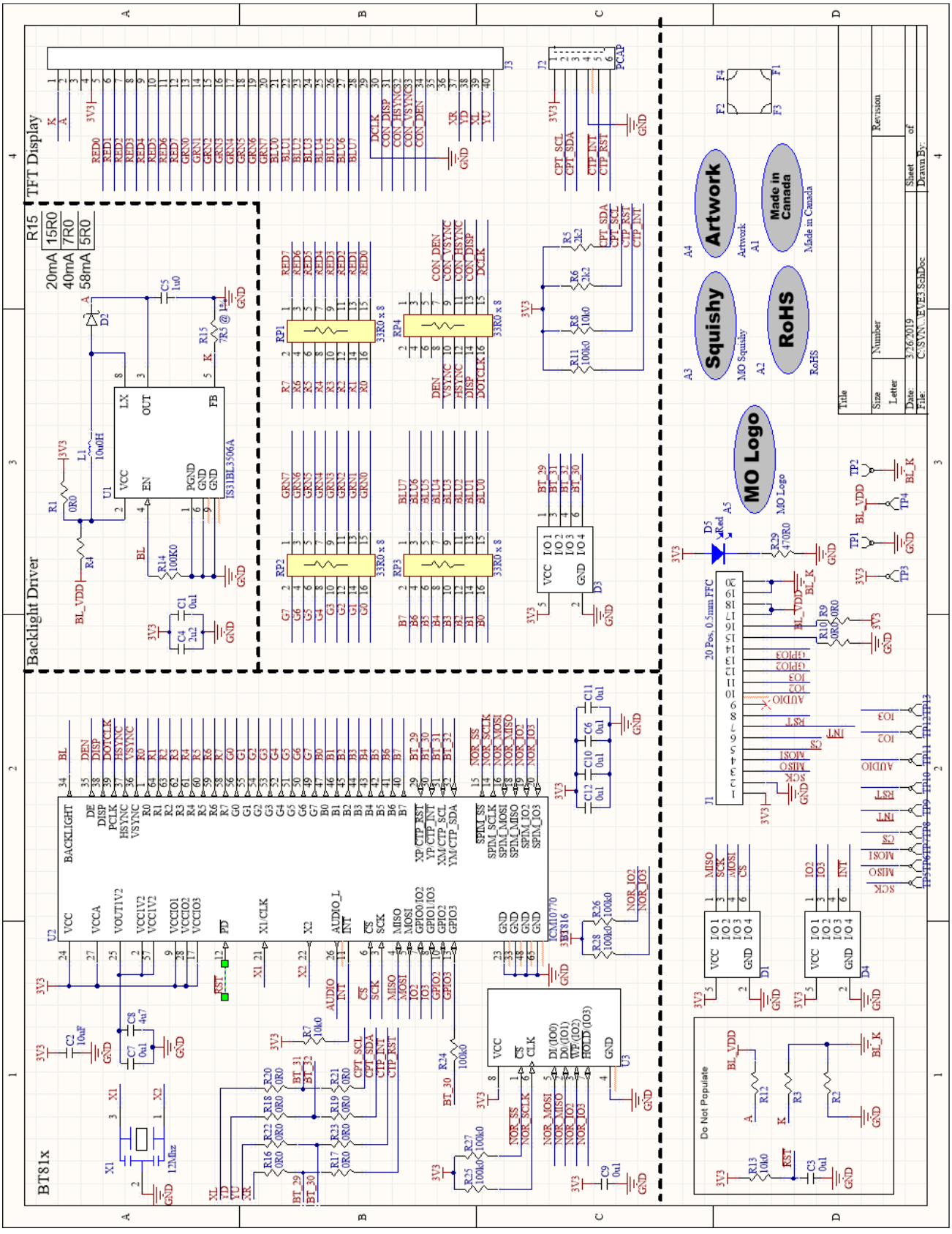

Figure 21: EVE3 Schematic

12. Contact

Sales

Phone: 403.229.2737

Email: sales@matrixorbital.ca

Support

Phone: 403.204.3750

Email: support@matrixorbital.ca

Online

Purchasing: www.matrixorbital.com

Support: www.matrixorbital.ca