



# BUK9K22-80E

Dual N-channel 80 V, 22 mΩ logic level MOSFET

11 May 2018

Product data sheet

## 1. General description

Dual Logic level N-channel MOSFET in an LFPK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC-Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- Dual MOSFET
- AEC-Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with  $V_{GS(th)}$  rating of greater than 0.5 V at 175 °C

## 3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

## 4. Quick reference data

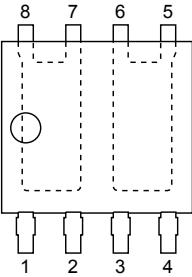
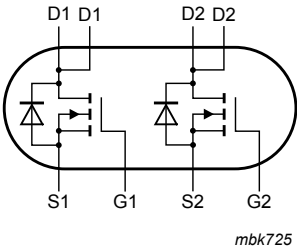
Table 1. Quick reference data

Table 17. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Limiting values FET1 and FET2							
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	-	80	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>		-	-	21	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>		-	-	64	W
T <sub>j</sub>	junction temperature			-55	-	175	°C
Static characteristics FET1 and FET2							
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 175 °C; <a href="#">Fig. 12</a>		-	-	54.5	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a>		-	15.7	21.7	mΩ
Dynamic characteristics FET1 and FET2							
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 64 V; V <sub>GS</sub> = 5 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>		-	8.4	-	nC
Q <sub>G(tot)</sub>	total gate charge			-	23.1	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 LFPAK56D (SOT1205)	 mbk725
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9K22-80E	LFPAK56D	plastic, single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K22-80E	92280E

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

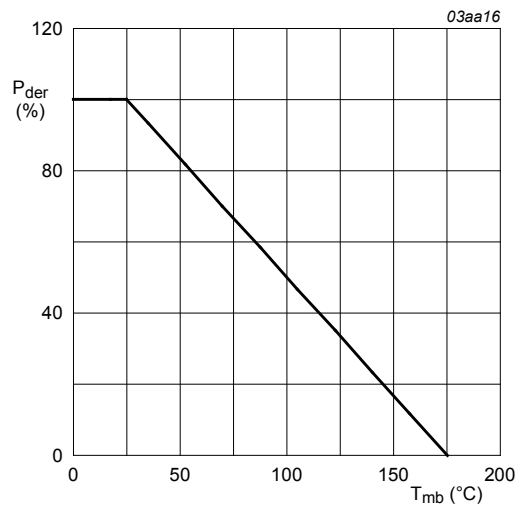
Symbol	Parameter	Conditions		Min	Max	Unit
<b>Limiting values FET1 and FET2</b>						
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	80	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$		-	80	V
$V_{GS}$	gate-source voltage	DC; $T_j \leq 175\text{ °C}$		-10	10	V
		Pulsed; $T_j \leq 175\text{ °C}$	[1] [2]	-15	15	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; Fig. 1		-	64	W
$I_D$	drain current	$V_{GS} = 5\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 2		-	21	A
		$V_{GS} = 5\text{ V}$ ; $T_{sp} = 100\text{ °C}$ ; Fig. 2		-	15	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 3		-	84	A
$T_{stg}$	storage temperature			-55	175	°C
$T_j$	junction temperature			-55	175	°C
<b>Source-drain diode FET1 and FET2</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$		-	21	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$		-	84	A
<b>Avalanche ruggedness FET1 and FET2</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 21\text{ A}$ ; $V_{sup} \leq 80\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 5\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped; Fig. 4	[3] [4]	-	116	mJ

[1] Accumulated pulse duration up to 50 hours delivers zero defect ppm

[2] Significantly longer life times are achieved by lowering  $T_j$  and or  $V_{GS}$

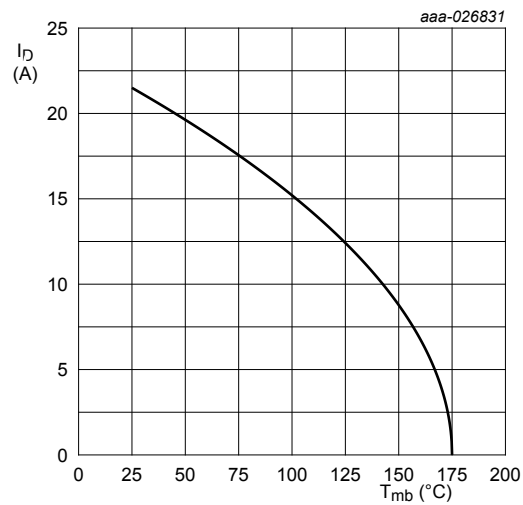
[3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

[4] Refer to application note AN10273 for further information



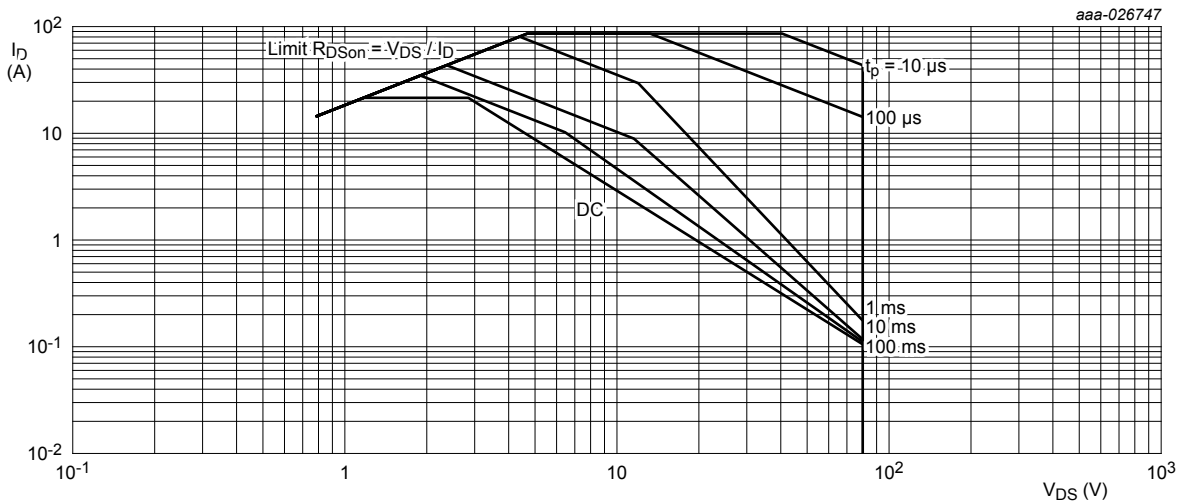
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



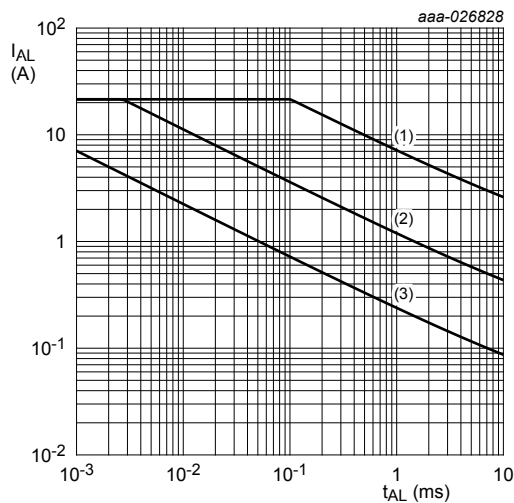
$V_{GS} \geq 5$  V

Fig. 2. Continuous drain current as a function of mounting base temperature, FET1 and FET2



$T_{mb} = 25$  °C;  $I_{DM}$  is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage, FET1 and FET2



(1)  $T_{j\text{ (init)}} = 25^{\circ}\text{C}$ ; (2)  $T_{j\text{ (init)}} = 150^{\circ}\text{C}$ ; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	-	2.36	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

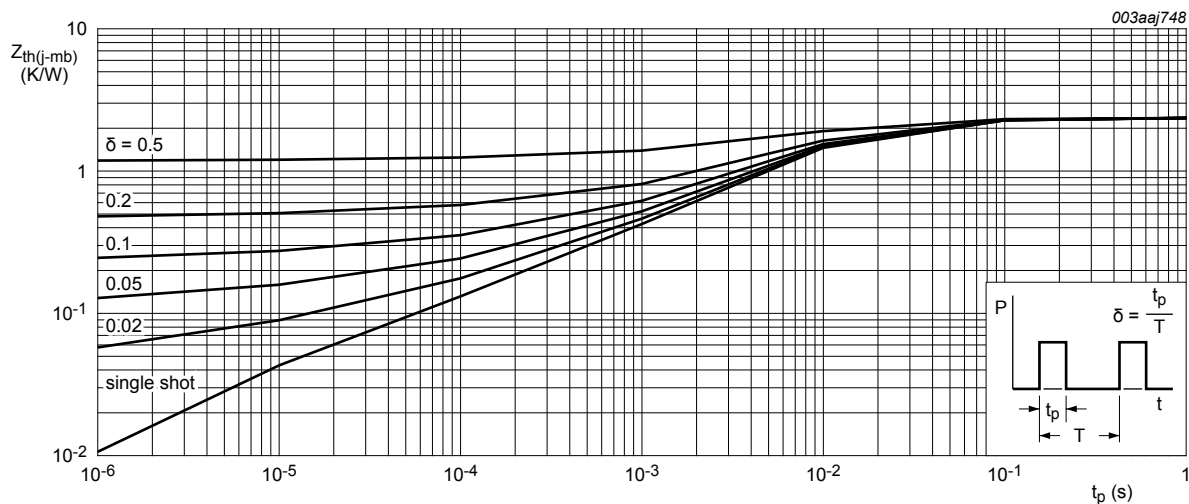


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration, FET1 and FET2

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics FET1 and FET2							
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		80	-	-	V
		I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C		72	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = 25 °C; <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>		1.4	1.7	2.1	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = -55 °C; <a href="#">Fig. 10</a>		-	-	2.45	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = 175 °C; <a href="#">Fig. 10</a>		0.5	-	-	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 80 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	0.01	1	μA
		V <sub>DS</sub> = 80 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C		-	-	500	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	2	100	nA
		V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a>		-	15.7	21.7	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a>		-	14.4	19	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 175 °C; <a href="#">Fig. 12</a>		-	-	54.5	mΩ
Dynamic characteristics FET1 and FET2							
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 64 V; V <sub>GS</sub> = 5 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>		-	23.1	-	nC
Q <sub>GS</sub>	gate-source charge			-	5.4	-	nC
Q <sub>GD</sub>	gate-drain charge			-	8.4	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; <a href="#">Fig. 15</a>		-	2342	3115	pF
C <sub>oss</sub>	output capacitance			-	170	204	pF
C <sub>rss</sub>	reverse transfer capacitance			-	89	122	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 60 V; R <sub>L</sub> = 5 Ω; V <sub>GS</sub> = 5 V; R <sub>G(ext)</sub> = 5 Ω; T <sub>j</sub> = 25 °C		-	13.9	-	ns
t <sub>r</sub>	rise time			-	24.9	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	28.6	-	ns
t <sub>f</sub>	fall time			-	20.6	-	ns
Source-drain diode FET1 and FET2							
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 10 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 16</a>		-	0.8	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 10 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; T <sub>j</sub> = 25 °C		-	28.4	-	ns
Q <sub>r</sub>	recovered charge			-	33	-	nC

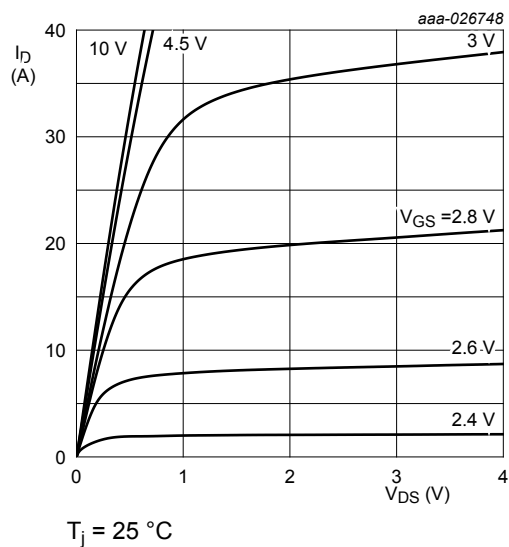


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values, FET1 and FET2

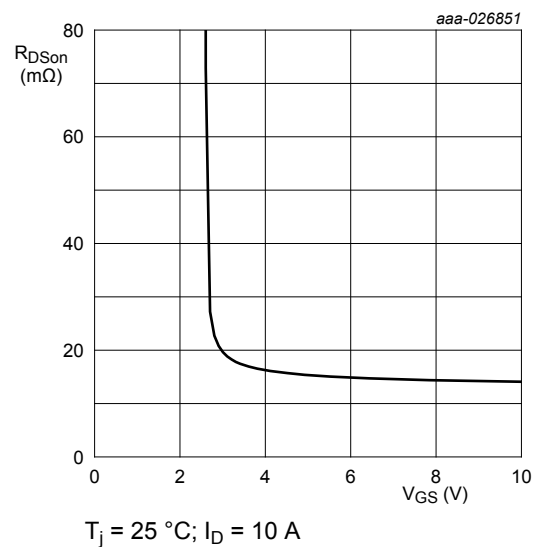


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values, FET1 and FET2

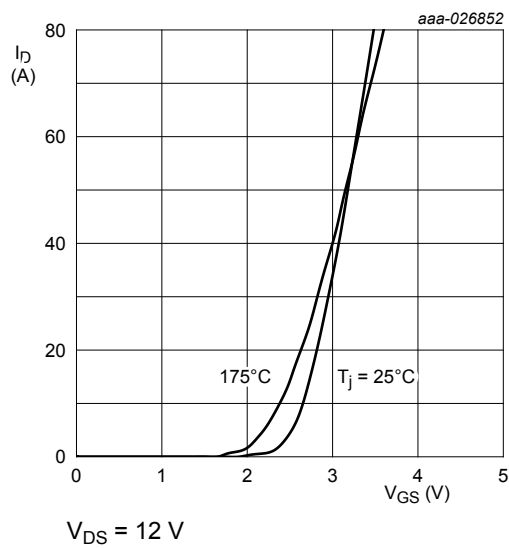


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2

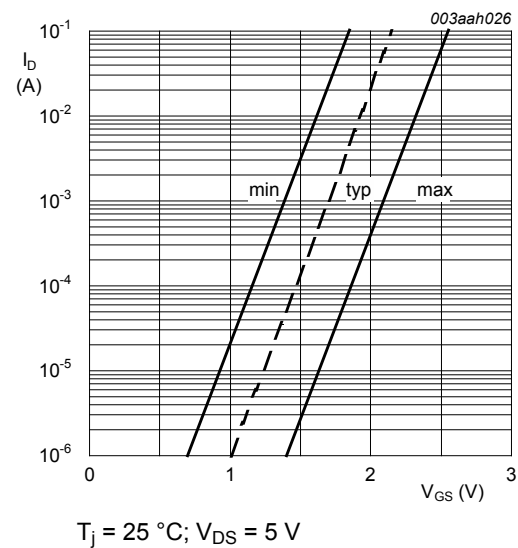


Fig. 9. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2

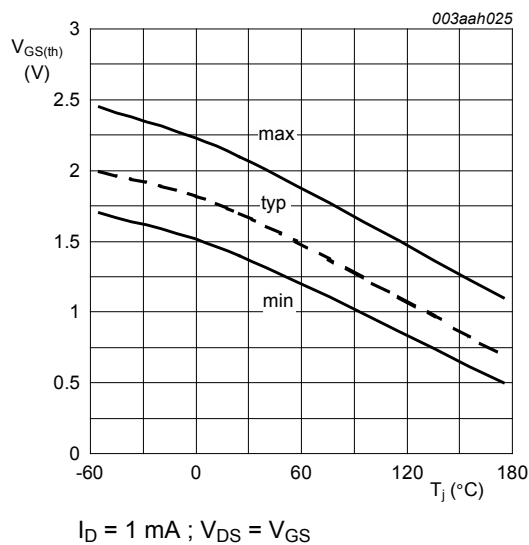


Fig. 10. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2

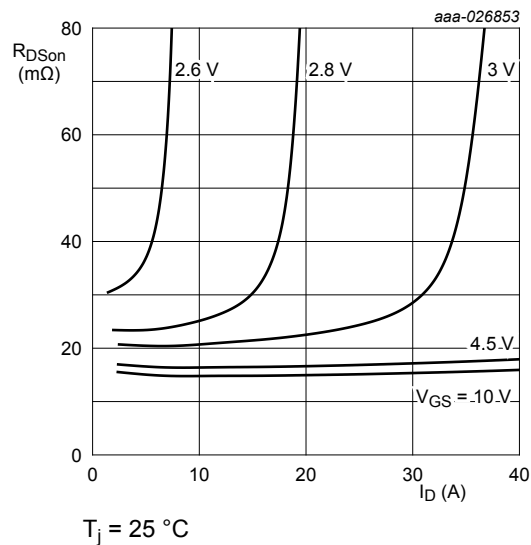


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2

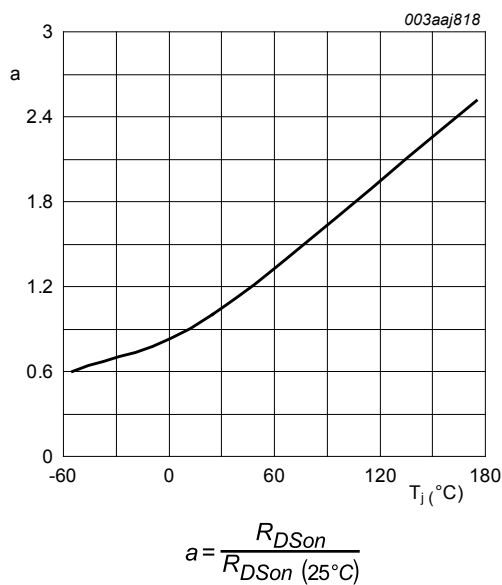


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2

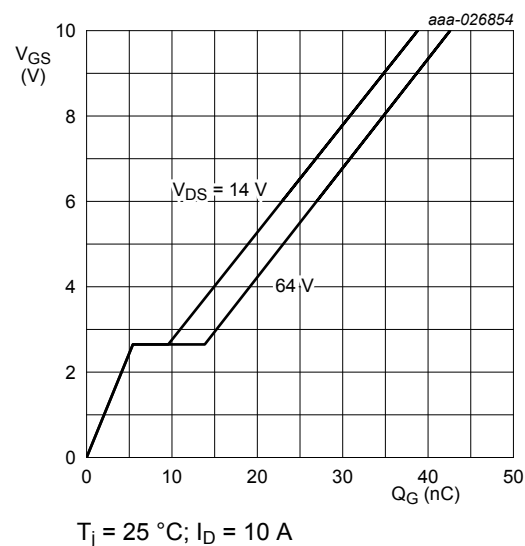


Fig. 13. Gate-source voltage as a function of gate charge; typical values, FET1 and FET2



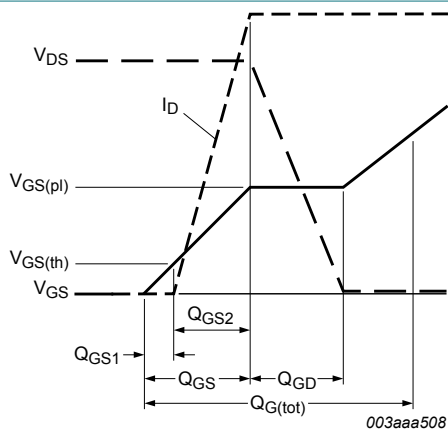
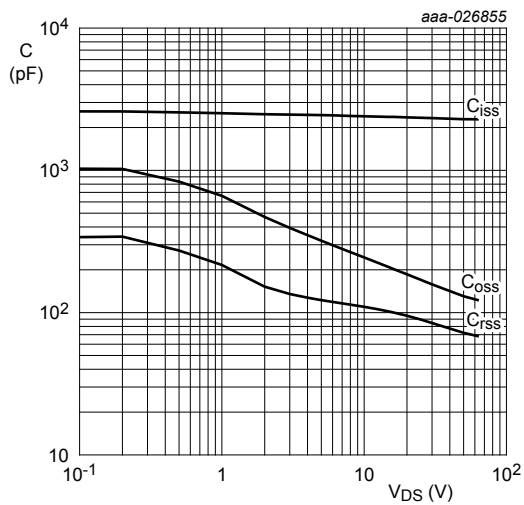
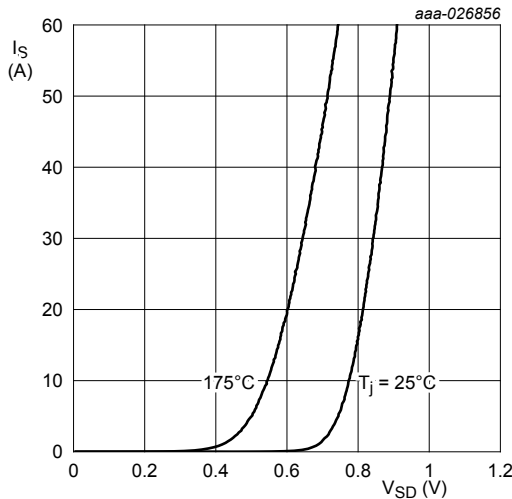


Fig. 14. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$ ;  $f = 1 \text{ MHz}$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2



$V_{GS} = 0 \text{ V}$

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2

11. Package outline

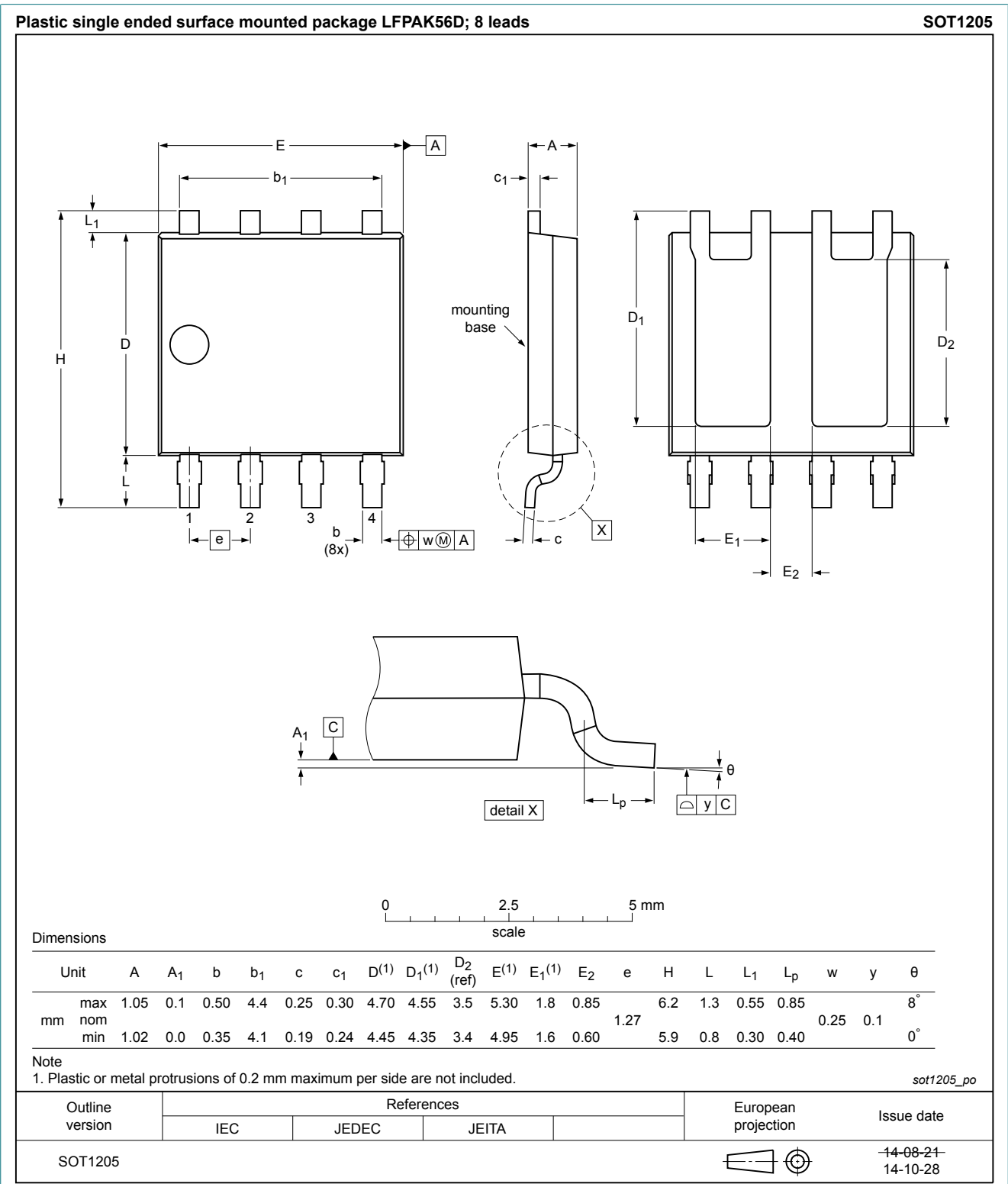


Fig. 17. Package outline LPAK56D (SOT1205)

## 12. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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