



## An Ultra-small, 4 mΩ, 5 A Integrated Power Switch with PG Output

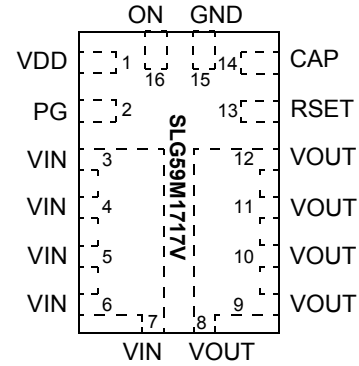
### General Description

Operating from a 2.5 V to 5.5 V power supply and fully specified over the -40 °C to 85 °C Industrial temperature range, the SLG59M1717V is a high-performance 4 mΩ, 5 A single-channel nFET integrated power switch designed for all 0.8 V to 5.5 V power rail applications. The SLG59M1717V features adjustable inrush current control which is achieved by adjusting the  $V_{OUT}$  slew rate with an external capacitor. Using a proprietary MOSFET design, the SLG59M1717V achieves a stable 4 mΩ  $R_{DS_{ON}}$  across a wide input/supply voltage range. The SLG59M1717V also incorporates resistor-adjustable current limiting as well as thermal protection. Using Silego's proprietary CuFET™ technology for high-current operation, the SLG59M1717V is packaged in a space-efficient, low thermal resistance, RoHS-compliant 1.6mm x 2.5 mm STQFN package.

### Features

- Low Typical  $R_{DS_{ON}}$  nFET Block: 4 mΩ
- Maximum Continuous Switch Current: Up to 5 A
- Supply Voltage: 2.5 V ≤  $V_{DD}$  ≤ 5.5 V
- Wide Input Voltage Range: 0.8 V ≤  $V_{IN}$  ≤  $V_{DD}$
- Capacitor adjustable Start-up and In-rush Current Control
- Two-stage Overcurrent Protection:
  - Resistor-adjustable Active Current Limit
  - Fixed 1.6 A Short-circuit Current Limit
- Thermal Shutdown Protection
- Open-drain PG Signaling
- Operating Temperature: -40 °C to 85 °C
- Low  $\theta_{JA}$ , 16-pin 1.6 mm x 2.5 mm STQFN
  - Pb-Free / Halogen-Free / RoHS compliant

### Pin Configuration

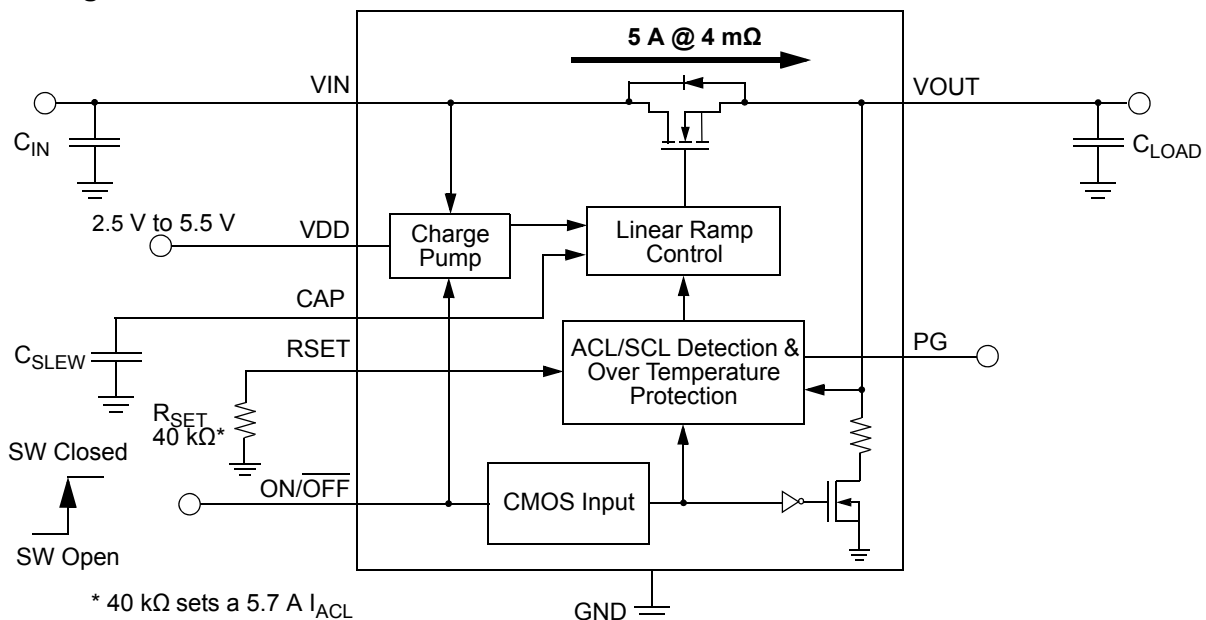


16-pin FC-STQFN (Top View)

### Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

### Block Diagram





### Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	Power	With an internal 1.9 V UVLO threshold, VDD supplies the power for the operation of the power switch and internal control circuitry where its range is $2.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ . Bypass the VDD pin to GND with a 0.1 $\mu\text{F}$ (or larger) capacitor
2	PG	Output	An open drain output. PG is asserted when $V_{OUT}$ reaches 90% of $V_{IN}$ . Connect an external 10-k $\Omega$ resistor from the PG pin to local system logic supply.
3-7	VIN	MOSFET	Drain terminal of Power MOSFET (Pins 3-7 fused together). Connect a 10 $\mu\text{F}$ (or larger) low ESR capacitor from this pin to GND. Capacitors used at VIN should be rated at 10 V or higher.
8-12	VOUT	MOSFET	Source terminal of Power MOSFET (Pins 8-12 fused together). Connect a capacitor (up to 600 $\mu\text{F}$ ) from this pin to GND. Capacitors used at VOUT should be rated at 10 V or higher.
13	RSET	Input	A 1%-tolerance, metal-film resistor between 38 k $\Omega$ and 80 k $\Omega$ sets the IPS's active current limit. A 38 k $\Omega$ resistor sets the SLG59M1717V's active current limit to 6 A and a 80 k $\Omega$ resistor sets the active current limit to 2.85 A.
14	CAP	Input	A capacitor connected from CAP pin to GND sets the VOUT slew rate and overall turn-on time of the SLG59M1717V. For best performance, the range for $C_{SLEW}$ values are $2\text{ nF} \leq C_{SLEW}$ . Capacitors used at the CAP pin should be rated at 10 V or higher.
15	GND	GND	Ground
16	ON	Input	A low-to-high transition on this pin closes the power switch. ON is an asserted-HIGH, level-sensitive CMOS input with $V_{IL} < 0.3\text{ V}$ and $V_{IH} > 0.85\text{ V}$ . Connect this pin to the output of a general-purpose output (GPO) from a microcontroller or other application processor. While there is an internal pull down circuit to ground ( $\sim 4\text{ M}\Omega$ ), do not allow this pin to be open-circuited.

### Ordering Information

Part Number	Type	Production Flow
SLG59M1717V	STQFN 16L	Industrial, -40 °C to 85 °C
SLG59M1717VTR	STQFN 16L (Tape and Reel)	Industrial, -40 °C to 85 °C



## Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Power Supply Pin to GND		--	--	6	V
V <sub>IN</sub> to GND	Power Switch Input Voltage to GND		-0.3	--	6	V
V <sub>OUT</sub> to GND	Power Switch Output Voltage to GND		-0.3	--	V <sub>IN</sub>	V
ON, RSET, CAP, and to PG GND	ON, RSET, CAP, and PG Pin Voltages to GND		-0.3	--	6	V
T <sub>S</sub>	Storage Temperature		-65	--	150	°C
ESD <sub>HBM</sub>	ESD Protection	Human Body Model	2000	--	--	V
ESD <sub>CDM</sub>	ESD Protection	Charged Device Model	500	--	--	V
MSL	Moisture Sensitivity Level		1			
θ <sub>JA</sub>	Package Thermal Resistance, Junction-to-Ambient	1.6mm x 2.5mm STQFN; Determined using 1 in <sup>2</sup> , 1.2 oz. copper pads under each VIN and VOUT on FR4 pcb material, with airflow	--	35	--	°C/W
W <sub>DIS</sub>	Package Power Dissipation		--	--	1.2	W
ID <sub>S</sub> <sub>MAX</sub>	Max Continuous Switch Current		--	--	5	A
MOSFET ID <sub>S</sub> <sub>PK</sub>	Peak Current from Drain to Source	Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	--	--	6	A

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Electrical Characteristics

T<sub>A</sub> = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Power Supply Voltage		2.5	--	5.5	V
V <sub>DD(UVLO)</sub>	V <sub>DD</sub> Undervoltage Lockout Threshold	V <sub>DD</sub> ↑	1.6	1.9	2.2	V
		V <sub>DD</sub> ↓	1.5	1.8	2.2	V
I <sub>DD</sub>	Power Supply Current when OFF	V <sub>DD</sub> = V <sub>IN</sub> = 5.5 V; ON = 0	--	--	1	μA
	Power Supply Current, ON (Steady State)	V <sub>DD</sub> = V <sub>IN</sub> = ON = 5.5 V; No Load, R <sub>SET</sub> = 80 kΩ	--	160	200	μA
RDS <sub>ON</sub>	ON Resistance	T <sub>A</sub> 25°C MOSFET @100 mA; V <sub>DD</sub> = V <sub>IN</sub> = 5 V	--	4	5.5	mΩ
		T <sub>A</sub> 85°C MOSFET @100 mA; V <sub>DD</sub> = V <sub>IN</sub> = 5 V	--	5	6.8	mΩ
		T <sub>A</sub> 85°C MOSFET @ 5 A; V <sub>DD</sub> = 5 V, V <sub>IN</sub> = 1 V <sup>2</sup>	--	5.1	7.0	mΩ
MOSFET ID <sub>S</sub>	Current from V <sub>IN</sub> to V <sub>OUT</sub>	Continuous	--	--	5	A
I <sub>FET_OFF</sub>	MOSFET OFF Leakage Current	V <sub>DD</sub> = V <sub>IN</sub> = 5.5 V; V <sub>OUT</sub> = 0 V; ON = 0 V	--	0.1	2	μA
V <sub>IN</sub>	Drain Voltage		0.8	--	V <sub>DD</sub>	V



## Electrical Characteristics (continued)

T<sub>A</sub> = -40 °C to 85 °C (unless otherwise stated)

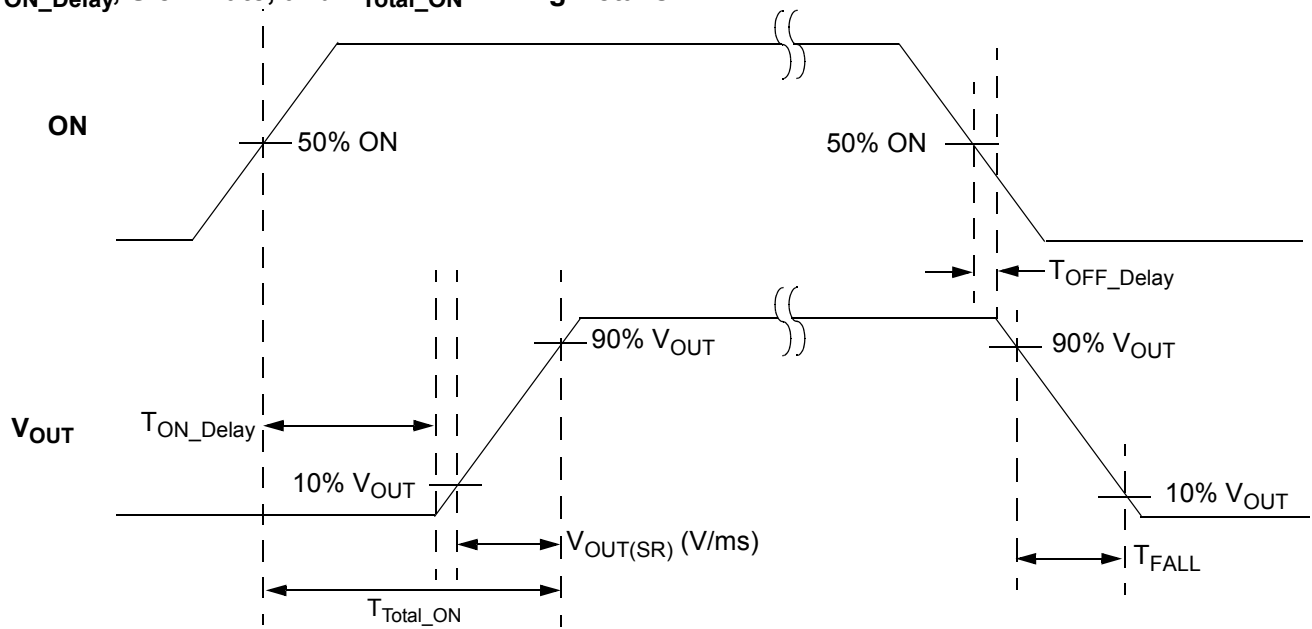
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T <sub>ON_Delay</sub>	ON pin Delay Time	50% ON to Ramp Begin, V <sub>DD</sub> = V <sub>IN</sub> = 5 V; C <sub>SLEW</sub> = 12 nF; R <sub>LOAD</sub> = 20 Ω, C <sub>LOAD</sub> = 10 μF	--	200	--	μs
V <sub>OUT(SR)</sub>	V <sub>OUT</sub> Slew Rate <sup>3</sup>	10% V <sub>OUT</sub> to 90% V <sub>OUT</sub> ↑;	Set by External C <sub>SLEW</sub> <sup>1</sup>			V/ms
		Example: C <sub>SLEW</sub> = 12 nF; V <sub>DD</sub> = V <sub>IN</sub> = 5 V; R <sub>LOAD</sub> = 20 Ω, C <sub>LOAD</sub> = 10 μF	0.8	1	1.2	V/ms
T <sub>Total_ON</sub>	Total Turn-on Time	50% ON to 90% V <sub>OUT</sub> ↑;	Set by External C <sub>SLEW</sub> <sup>1</sup>			ms
		Example: C <sub>SLEW</sub> = 12 nF; V <sub>DD</sub> = V <sub>IN</sub> = 5 V; R <sub>LOAD</sub> = 20 Ω, C <sub>LOAD</sub> = 10 μF	--	4.7	--	ms
T <sub>OFF_Delay</sub>	OFF Delay Time	50% ON to V <sub>OUT</sub> Fall Start; V <sub>DD</sub> = V <sub>IN</sub> = 5 V, R <sub>LOAD</sub> = 20 Ω, no C <sub>LOAD</sub>	--	8	15	μs
C <sub>LOAD</sub>	Output Load Capacitance	C <sub>LOAD</sub> connected from V <sub>OUT</sub> to GND	1	10	600	μF
I <sub>LIMIT</sub>	Active Current Limit (I <sub>ACL</sub> ) <sup>2</sup>	V <sub>OUT</sub> > 0.25 V; R <sub>SET</sub> = 80 kΩ	2.28	2.85	3.42	A
	Short-circuit Current Limit (I <sub>SCL</sub> ) <sup>3</sup>	V <sub>OUT</sub> < 0.25 V	--	1.6	--	A
PG <sub>VOH</sub>	Power Good Pull-up Voltage	Open Drain Output Buffer	--	--	5.5	V
PG	Power Good level	V <sub>OUT</sub> reaches 90% of V <sub>IN</sub>	87	90	93	%
PG <sub>HYS</sub>	Power Good Hysteresis	V <sub>OUT</sub> below V <sub>PG</sub> level 5%	--	5	--	%
ON_V <sub>IH</sub>	High Input Voltage on ON pin		0.85	--	V <sub>DD</sub>	V
ON_V <sub>IL</sub>	Low Input Voltage on ON pin		-0.3	0	0.3	V
R <sub>DISCHRG</sub>	Output Discharge Resistance	V <sub>DD</sub> = 5 V, V <sub>OUT</sub> = 0.4 V, ON = 0 V	70	93	150	Ω
THERM <sub>ON</sub>	Thermal shutoff turn-on temperature		--	150	--	°C
THERM <sub>OFF</sub>	Thermal shutoff turn-off temperature		--	130	--	°C

### Notes:

1. Refer to typical Timing Parameter vs. C<sub>SLEW</sub> performance charts for additional information when available.
2. Based on bench characterization
3. Please consult SLG59M1717V Start-up Inrush Current Considerations with Capacitive Loads section starting on Page 14.



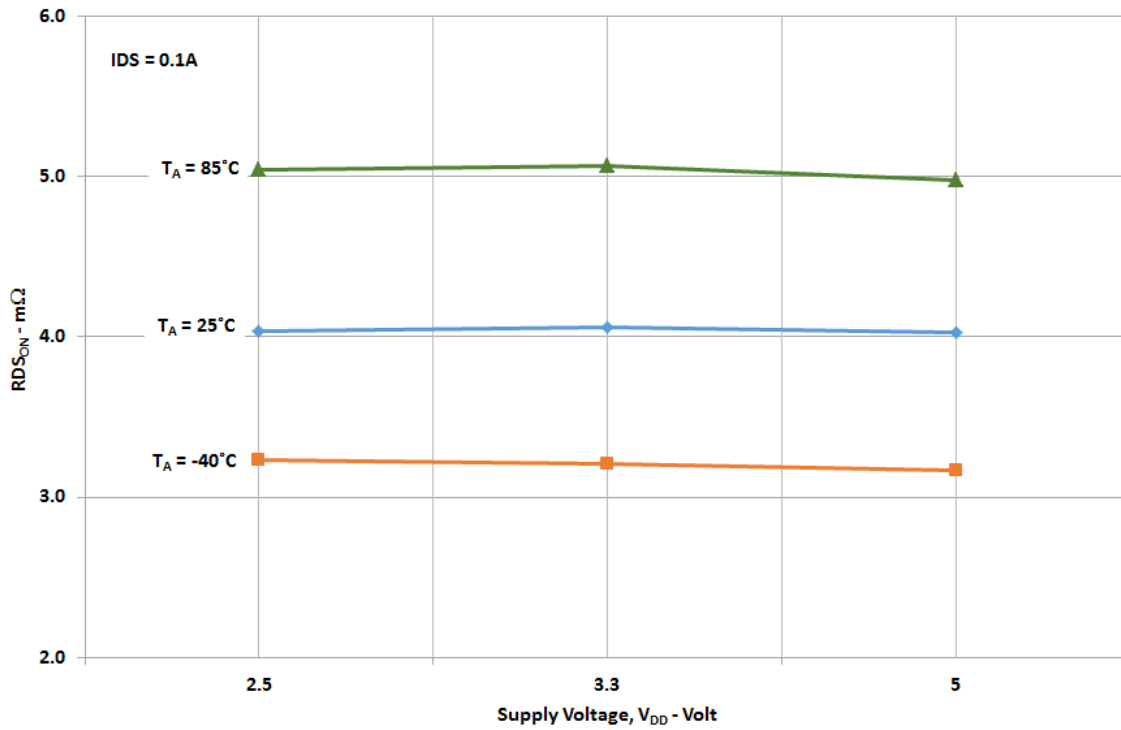
### $T_{ON\_Delay}$ , Slew Rate, and $T_{Total\_ON}$ Timing Details



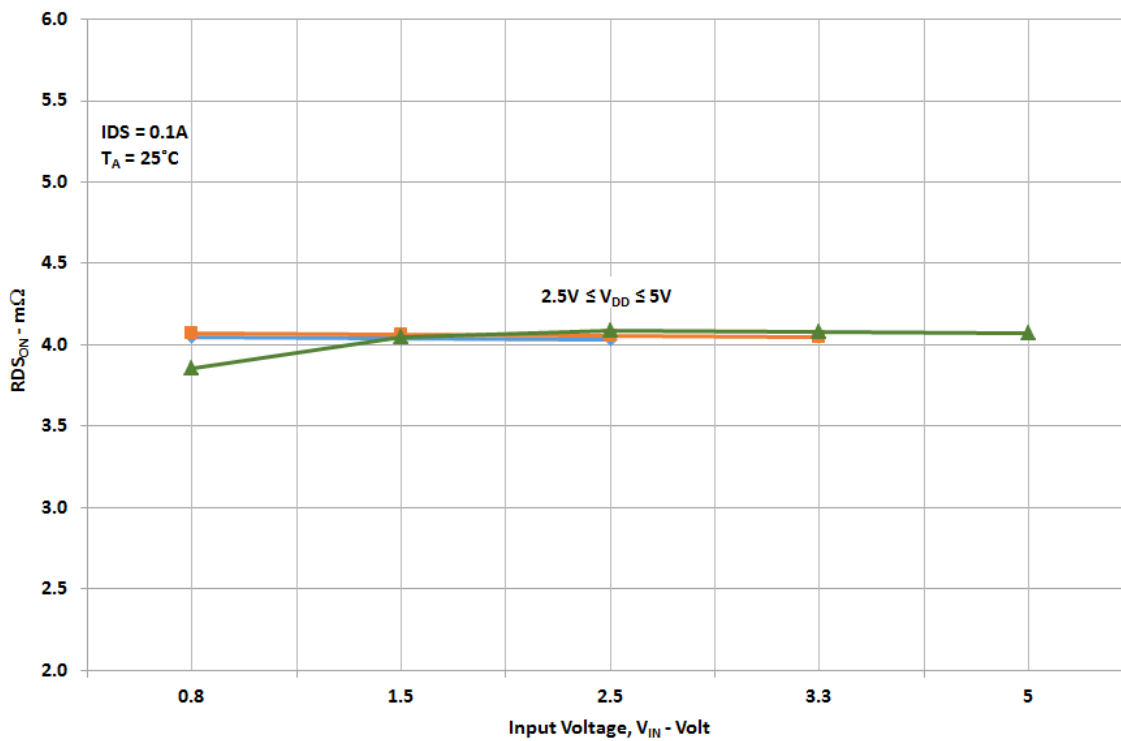


### Typical Performance Characteristics

#### $R_{DS(ON)}$ vs. $V_{DD}$ , and Temperature

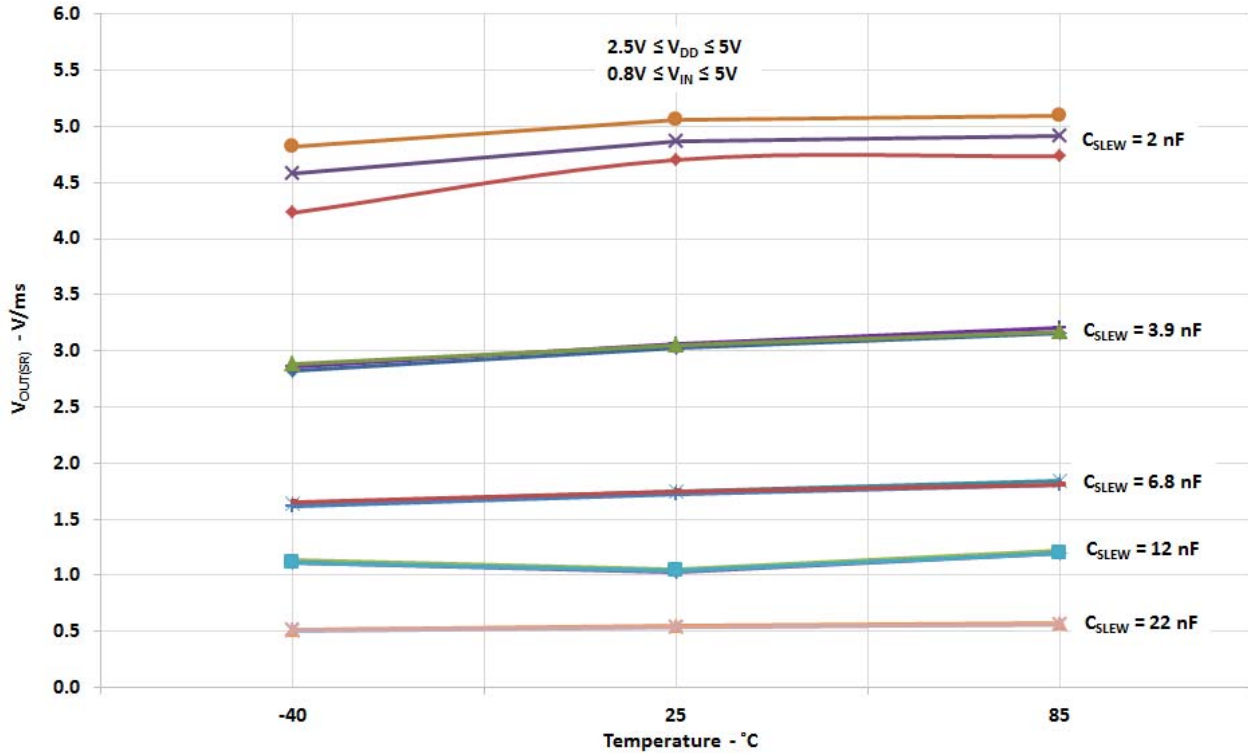


#### $R_{DS(ON)}$ vs. $V_{IN}$ and $V_{DD}$

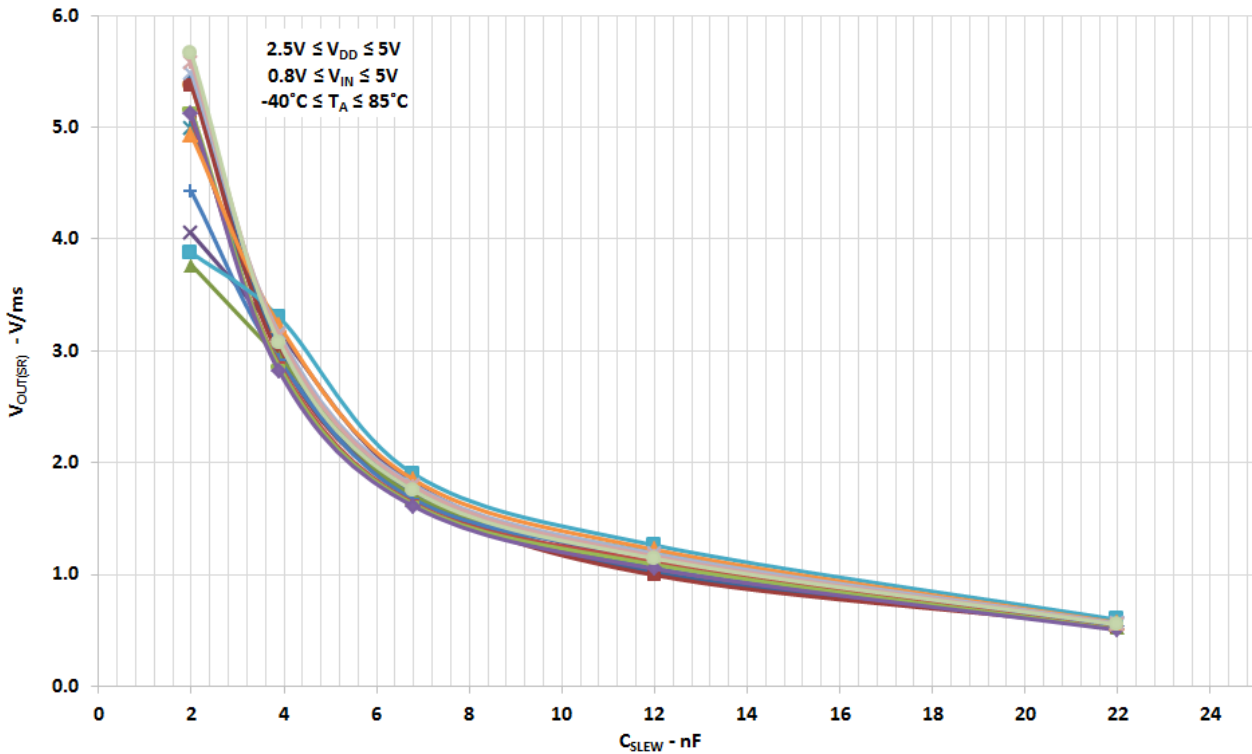




$V_{OUT(SR)}$  vs. Temperature,  $V_{IN}$ ,  $V_{DD}$ , and  $C_{SLEW}$

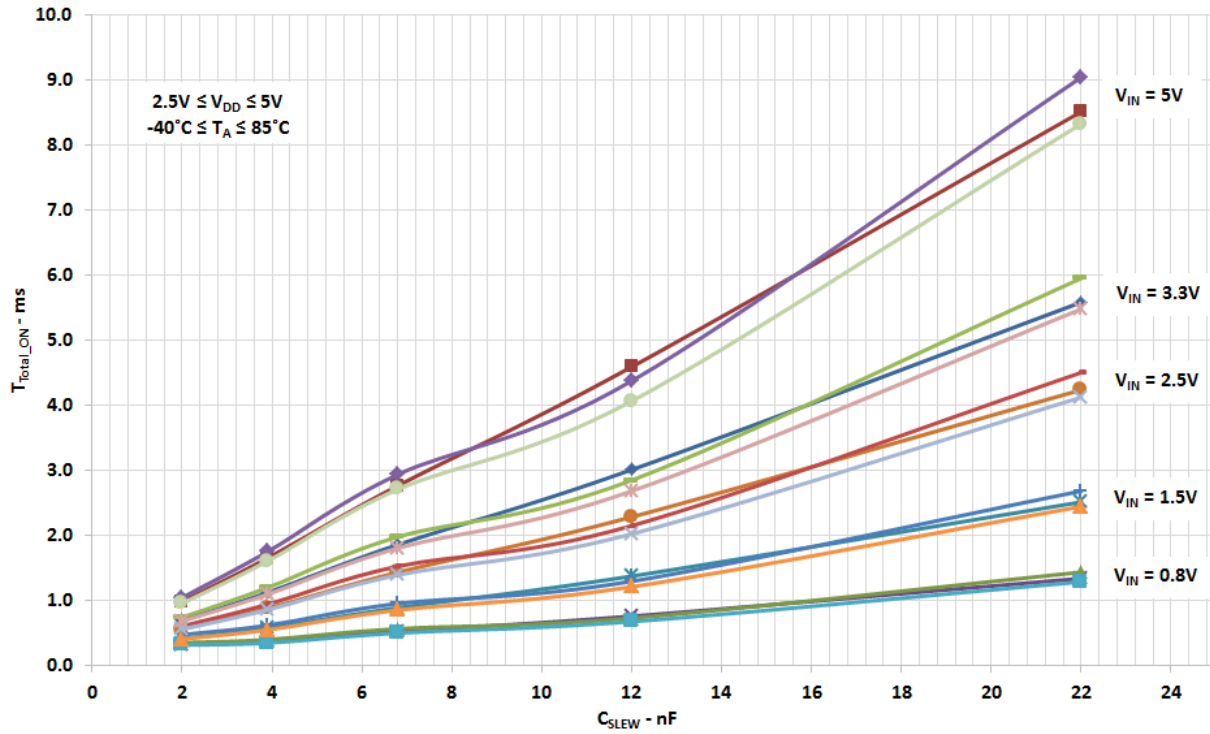


$V_{OUT(SR)}$  vs.  $C_{SLEW}$ ,  $V_{IN}$ ,  $V_{DD}$ , and Temperature

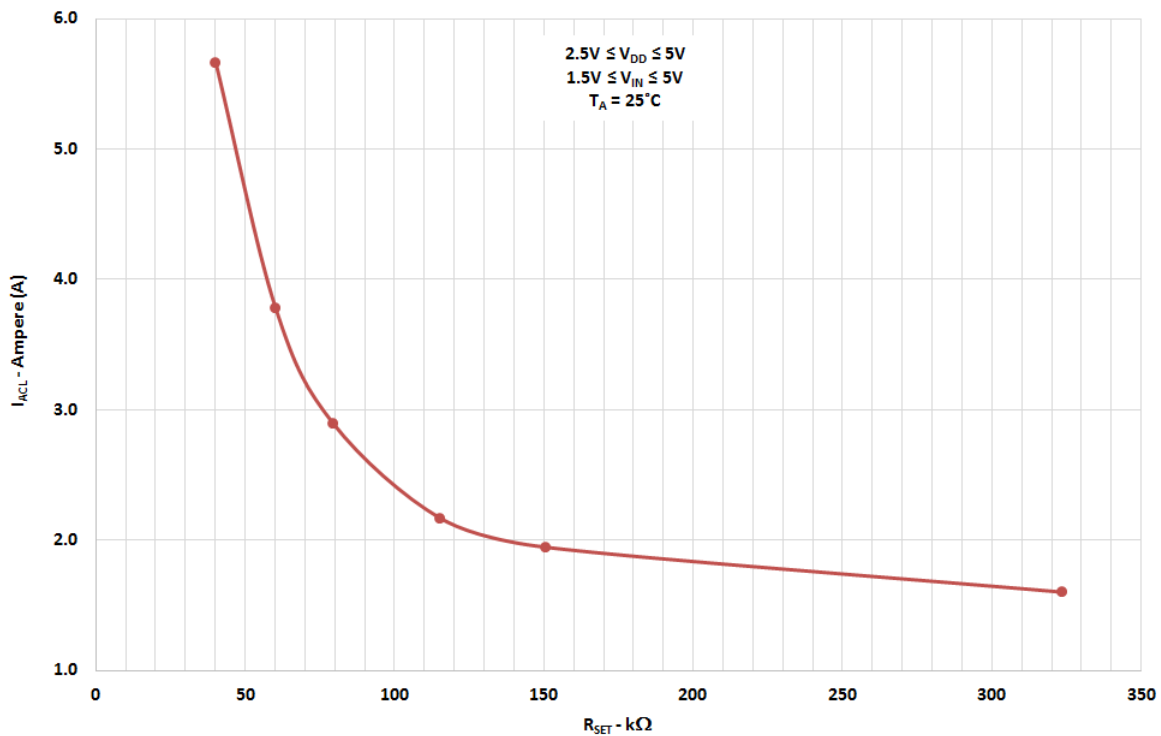




### $T_{Total\_ON}$ vs. $C_{SLEW}$ , $V_{IN}$ , $V_{DD}$ , and Temperature



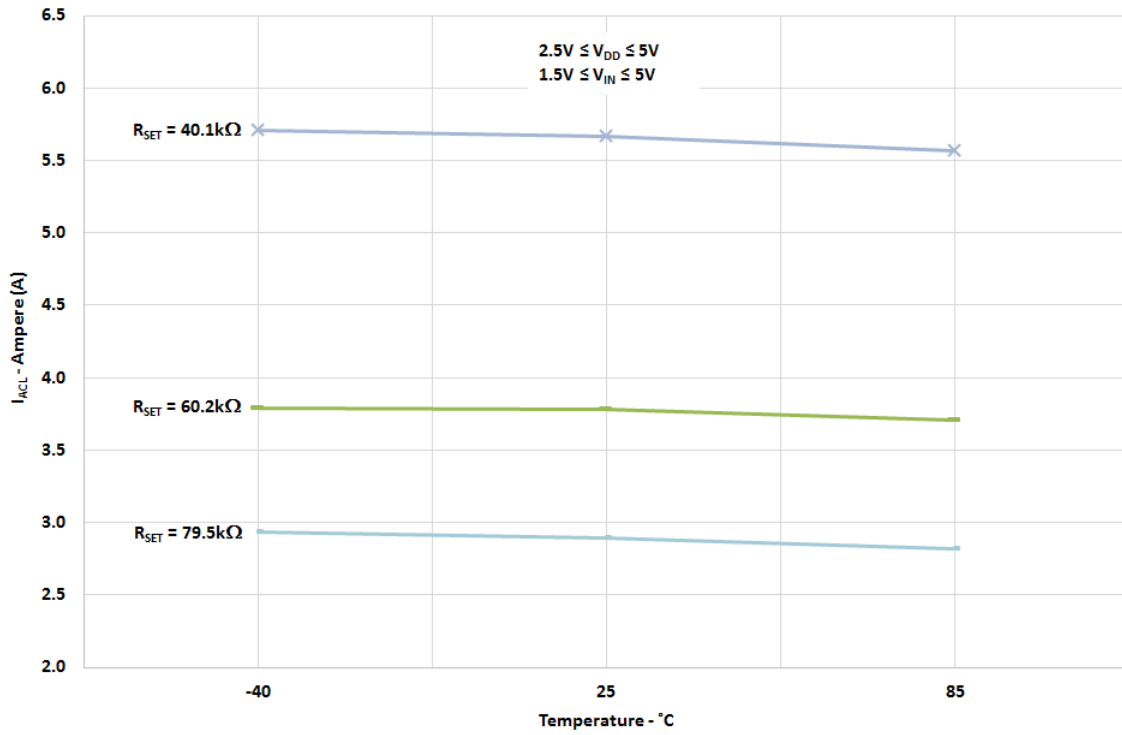
### I<sub>ACL</sub> vs. R<sub>SET</sub>, V<sub>DD</sub>, and V<sub>IN</sub>







$I_{ACL}$  vs. Temperature,  $V_{DD}$ , and  $V_{IN}$





## Typical Turn-on Waveforms - $V_{DD} = V_{IN} = 5\text{ V}$

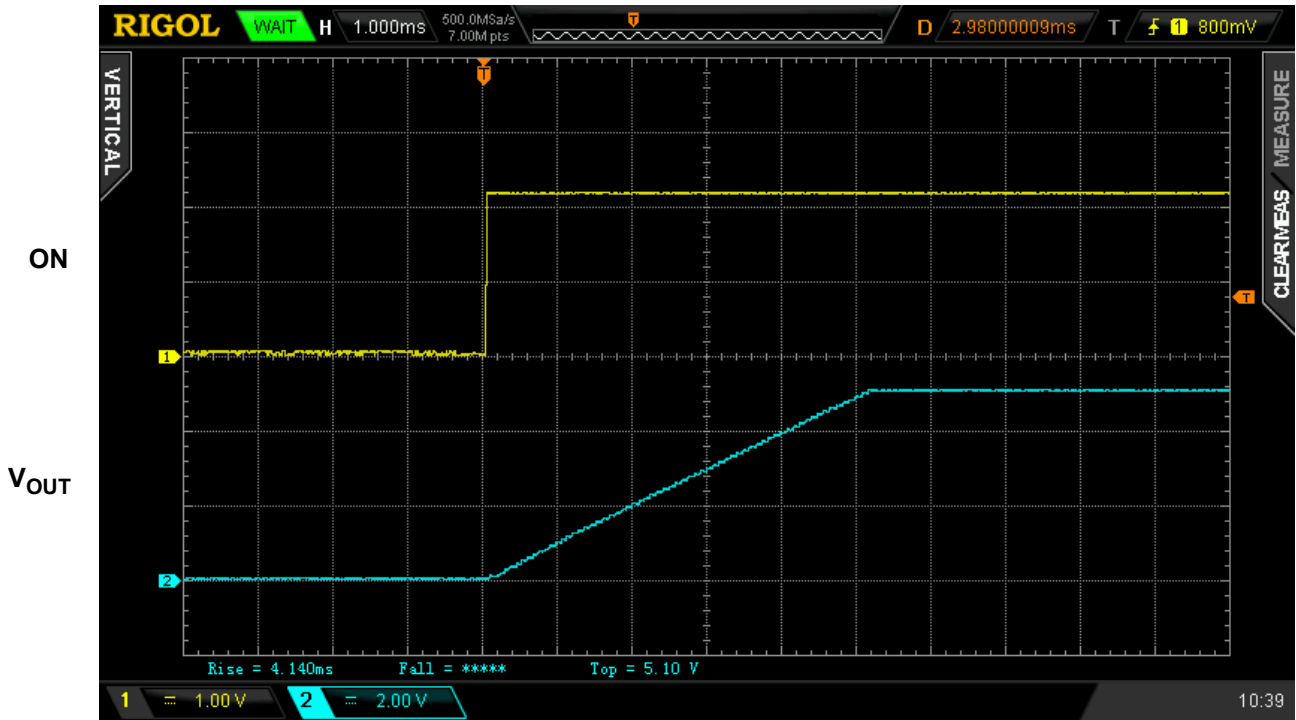


Figure 1. Typical Turn ON operation waveform for  $V_{DD} = V_{IN} = 5\text{ V}$ ,  $C_{SLEW} = 12\text{ nF}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{LOAD} = 20\text{ }\Omega$

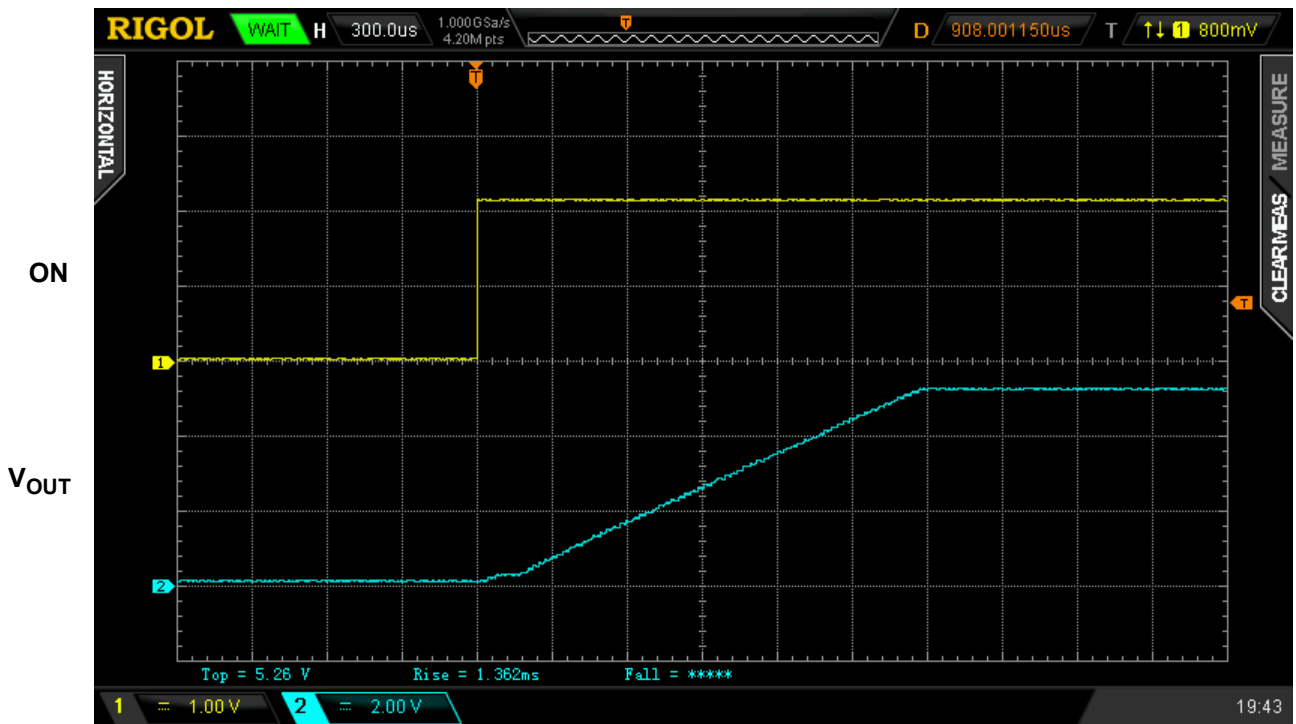


Figure 2. Typical Turn ON operation waveform for  $V_{DD} = V_{IN} = 5\text{ V}$ ,  $C_{SLEW} = 4\text{ nF}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{LOAD} = 20\text{ }\Omega$



### Typical Turn-off Waveforms - $V_{DD} = V_{IN} = 5\text{ V}$

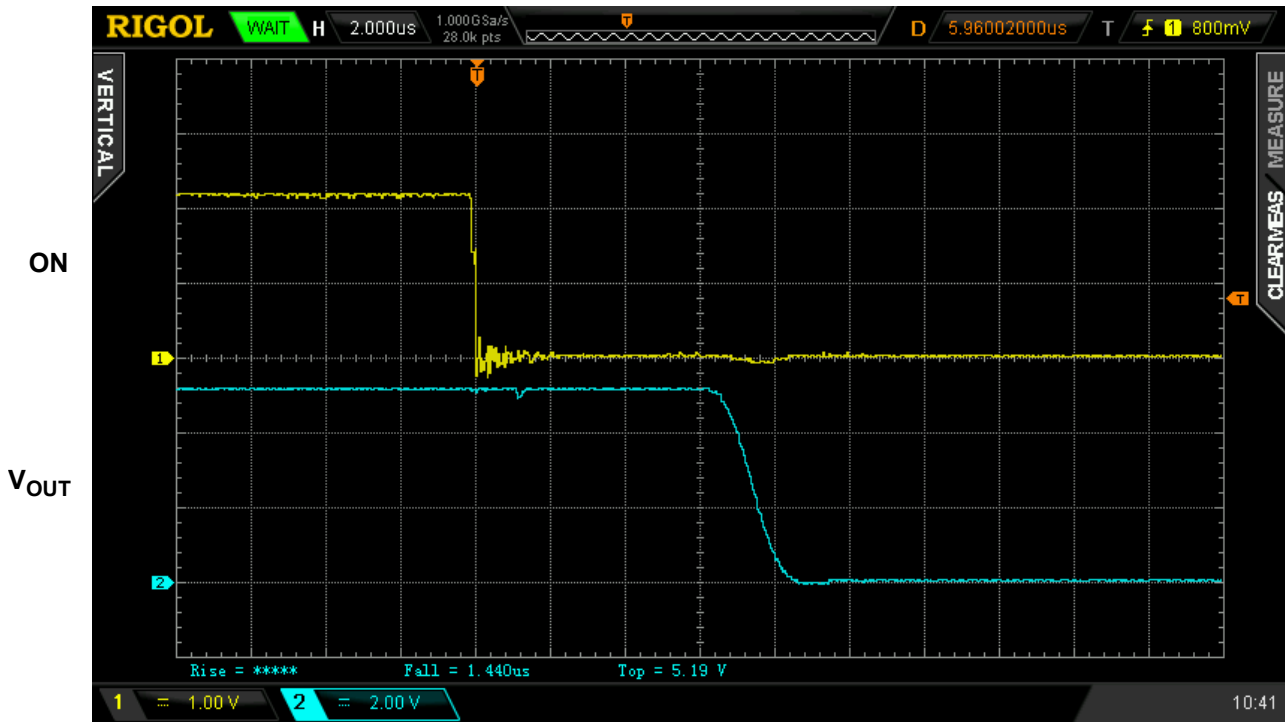


Figure 3. Typical Turn OFF operation waveform for  $V_{DD} = V_{IN} = 5\text{ V}$ ,  $C_{SLEW} = 12\text{ nF}$ , no  $C_{LOAD}$ ,  $R_{LOAD} = 20\ \Omega$

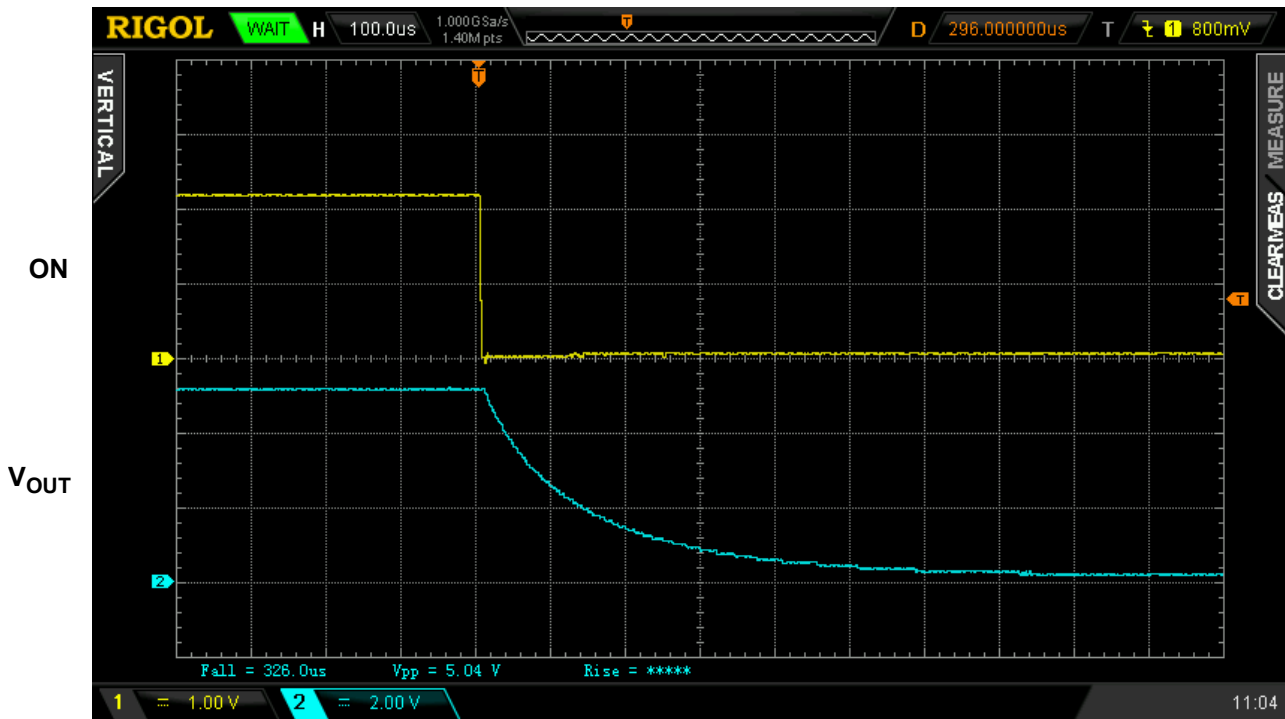
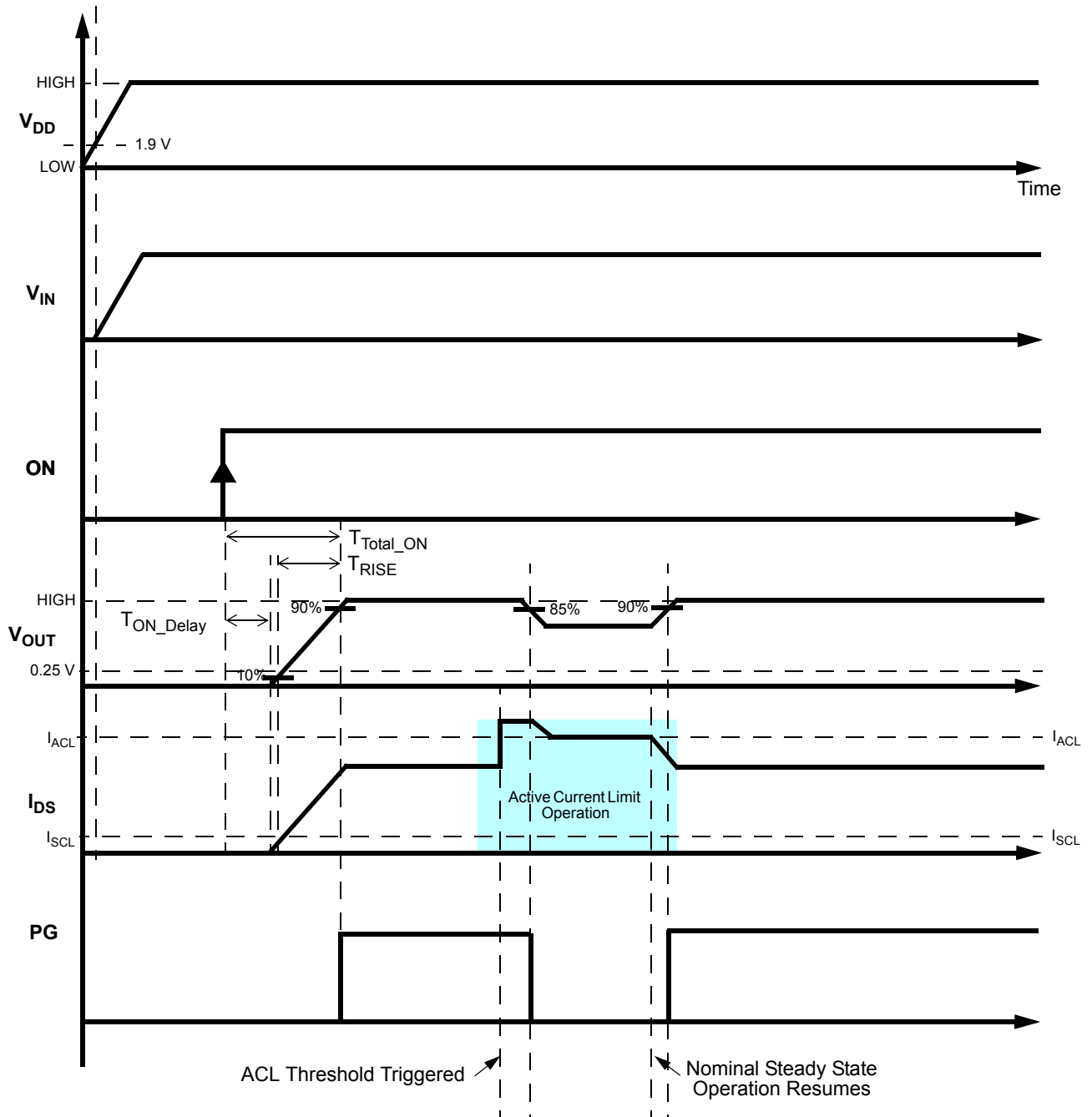


Figure 4. Typical Turn OFF operation waveform for  $V_{DD} = V_{IN} = 5\text{ V}$ ,  $C_{SLEW} = 12\text{ nF}$ ,  $C_{LOAD} = 10\ \mu\text{F}$ ,  $R_{LOAD} = 20\ \Omega$

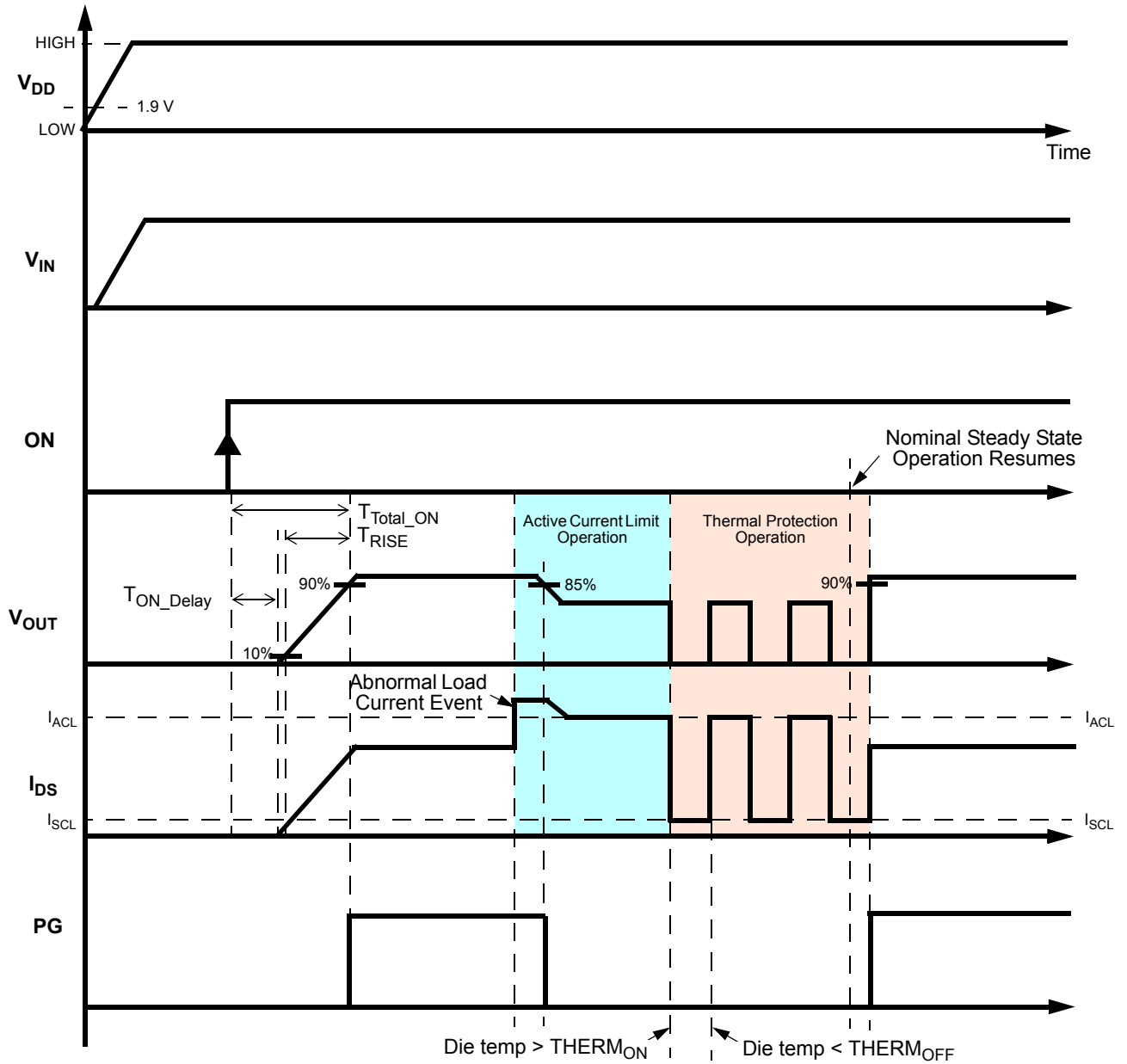


Timing Diagram - Basic Operation including Active Current Limit Protection





### Timing Diagram - Active Current Limit & Thermal Protection Operation





### SLG59M1717V Power-Up/Power-Down Sequence Considerations

To ensure glitch-free power-up under all conditions, apply  $V_{DD}$  first, followed by  $V_{IN}$  after  $V_{DD}$  exceeds 1.9 V. Then allow  $V_{IN}$  to reach 90% of its max value before toggling the ON pin from Low-to-High. Likewise, power-down in reverse order.

If  $V_{DD}$  and  $V_{IN}$  need to be powered up simultaneously, glitching can be minimized by having a suitable load capacitor. A 10  $\mu\text{F}$   $C_{LOAD}$  will prevent glitches for rise times of  $V_{DD}$  and  $V_{IN}$  less than 2 ms.

If the ON pin is toggled HIGH before  $V_{DD}$  and  $V_{IN}$  have reached their steady-state values, the IPS timing parameters may differ from datasheet specifications.

The slew rate of output  $V_{OUT}$  follows a linear ramp set by a capacitor connected to the CAP pin. A larger capacitor value at the CAP pin produces a slower ramp, reducing inrush current from capacitive loads.

### SLG59M1717V Current Limiting Operation

The SLG59M1717V has two types of current limiting triggered by the output  $V_{OUT}$  voltage.

#### 1. Standard Current Limiting Mode (with Thermal Shutdown Protection)

When the  $V_{OUT}$  voltage  $> 250$  mV, the output current is initially limited to the Active Current Limit ( $I_{ACL}$ ) specification listed in the Electrical Characteristics table. The ACL monitor's response time is very fast and is triggered within a few microseconds to sudden (transient) changes in load current. When a load current overload is detected, the ACL monitor increases the FET resistance to keep the current from exceeding the power switch's  $I_{ACL}$  threshold. During active current-limit operation,  $V_{OUT}$  is also reduced by  $I_{ACL} \times RDS_{ON(ACL)}$ . This observed behavior is illustrated in the timing diagrams on Pages 12 and 13.

However, if a load-current overload condition persists where the die temperature rises because of the increased FET resistance, the power switch's internal Thermal Shutdown Protection circuit can be activated. If the die temperature exceeds the listed  $THERM_{ON}$  specification, the FET is shut OFF completely, thereby allowing the die to cool. When the die cools to the listed  $THERM_{OFF}$  temperature threshold, the FET is allowed to turn back on. This process may repeat as long as the output current overload condition persists.

#### 2. Short Circuit Current Limiting Mode (with Thermal Shutdown Protection)

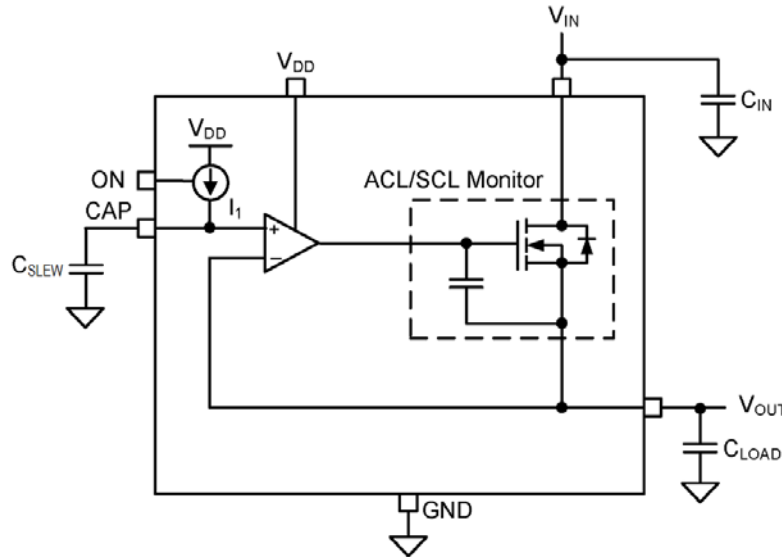
When the  $V_{OUT}$  voltage  $< 250$  mV (which is the case with a hard short, such as a solder bridge on the power rail), the power switch's internal Short-circuit Current Limit (SCL) monitor limits the FET current to approximately 1.6 A (the  $I_{SCL}$  threshold). While the internal Thermal Shutdown Protection circuit remains enabled and since the  $I_{SCL}$  threshold is much lower than the  $I_{ACL}$  threshold, thermal shutdown protection may become activated only at higher ambient temperatures.

### SLG59M1717V Start-up Inrush Current Considerations with Capacitive Loads

In distributed power applications, the SLG59M1717V is generally implemented on the outboard or downstream side of switching regulator dc/dc converters with internal overcurrent protection. As an adjustable output voltage slew-rate, integrated power switch, it is important to understand the start-up operation of the SLG59M1717V with capacitive loads. An equivalent circuit of the SLG59M1717V's slew-rate control loop with capacitors at its VIN and VOUT pins is shown in *Figure 1*:



### SLG59M1717V Start-up Inrush Current Considerations with Capacitive Loads (continued)



**Figure 1. SLG59M1717V's Equivalent Slew-rate Control Loop Circuit.**

For a desired  $V_{OUT}$  slew-rate ( $V_{OUT(SR)}$ ), a corresponding  $C_{SLEW}$  value is selected. At the  $V_{OUT}$  pin and with  $ON = LOW$ , the internal FET is OFF,  $V_{OUT}$  is initially at 0V, and there is no stored charge on  $C_{LOAD}$ . When a low-to-high transition is applied to the IC's  $ON$  pin, an internal current source ( $I_1$ ) is enabled which, in turn, charges the external slew-rate capacitor,  $C_{SLEW}$ . The SLG59M1717V's internal micropower op amp sets the circuit's  $V_{OUT(SR)}$  based on the slew rate of the nodal voltage at its non-inverting pin (the voltage at the  $CAP$  pin).

As a function of  $V_{OUT(SR)}$  and  $C_{LOAD}$ , a 1st-order expression for the circuit's FET current (and inrush current) when a low-to-high transition on the  $ON$  pin is applied becomes:

$$\text{Start-up Current } I_{DS} \text{ or } I_{INRUSH} = V_{OUT(SR)} \times C_{LOAD}$$

From the expression above and for a given  $V_{OUT(SR)}$ ,  $C_{LOAD}$  determines the magnitude of the inrush current; that is, for large values of  $C_{LOAD}$ , large inrush currents can result. If the inrush currents are large enough to trigger the overcurrent protection of an upstream dc/dc converter, the system can be shut down.

In applications where the desired  $V_{OUT(SR)}$  is fast and  $C_{LOAD}$  is very large ( $>200\mu F$ ), there is a secondary effect on the observed  $V_{OUT(SR)}$  attributed to the SLG59M1717V's internal short-circuit current limit monitor (its SCL monitor). If the resultant inrush current is larger than the IC's  $I_{SCL}$  threshold, the SCL current monitor limits the inrush current and the current to charge  $C_{LOAD}$  until the SCL OFF threshold is crossed ( $\sim 0.25V$ ). During the time the SCL monitor's been activated, the inrush current profile may exhibit an observable reduction in  $V_{OUT(SR)}$  as shown in *Figure 2* where  $C_{SLEW}$  was set to 4nF and 470 $\mu F$  was chosen for  $C_{LOAD}$ .



### SLG59M1717V Start-up Inrush Current Considerations with Capacitive Loads (continued)



**Figure 2.** A SLG59M1717V with  $C_{SLEW}$  set to 4nF and 470 $\mu$ F for  $C_{LOAD}$ .  $C_{LOAD}$ -to- $C_{SLEW}$  ratio is greater than 33,600. Note that the internal SCL monitor's been triggered and  $V_{OUT(SR)}$  is reduced until  $V_{OUT}$  reaches  $\sim$ 0.25V.

A closer analysis of the IC's internal slew-control large-scale yields the following:

$$\frac{I_{SCL}}{C_{LOAD}} = M_{SR} \times \frac{I_1}{C_{SLEW}}$$

where

$I_{SCL}$  = IC's short-circuit current limit threshold, typically 1.6 A;

$M_{SR}$  = An internal slew-rate multiplier from the IC's CAP pin to the VOUT pin;

$I_1$  = An internal current source to charge the external  $C_{SLEW}$ .

Rearranging the equation to isolate both  $C_{LOAD}$  and  $C_{SLEW}$  yields the following:

$$\frac{C_{LOAD}}{C_{SLEW}} = \frac{I_{SCL}}{I_1 \times M_{SR}}$$

For the SLG59M1717V device, the right-hand side of the expression is approximately 33,600 after taking into account part-to-part variations because of process, voltage, and temperature.

Referring to the configuration of *Figure 2's* scope capture, the  $C_{LOAD}$ -to- $C_{SLEW}$  ratio is 117,500 (470 $\mu$ F/4nF) where it is evident that the SCL monitor circuit is charging  $C_{LOAD}$  shortly after a low-to-high ON transition. If it is desired to avoid a reduction in  $V_{OUT(SR)}$ , the choices are decreasing  $C_{LOAD}$  and/or increasing  $C_{SLEW}$  so that the ratio is always less than 33,600 including taking into account external capacitor tolerances for initial accuracy and temperature.

As shown in *Figure 3*, it was chosen to reduce  $V_{OUT(SR)}$  by increasing  $C_{SLEW}$  to 15nF while keeping  $C_{LOAD}$  at 470 $\mu$ F. With this configuration, the ratio of  $C_{LOAD}$  to  $C_{SLEW}$  is about 31,333 (smaller than 33,600). Upon a low-to-high transition on the ON pin, the  $V_{OUT}$  increases smoothly with no evidence of SCL monitor's interaction.





## SLG59M1717V Start-up Inrush Current Considerations with Capacitive Loads (continued)

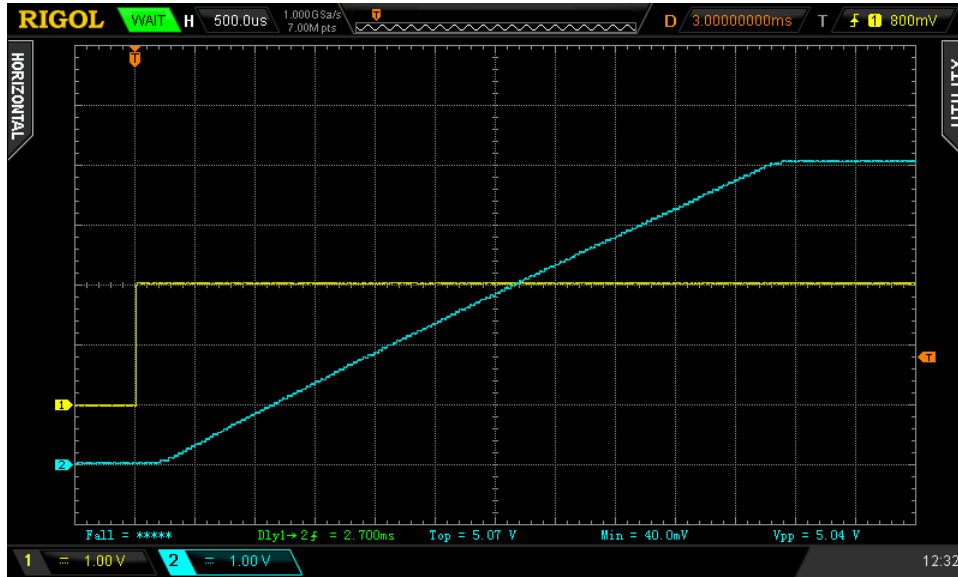


Figure 3. A SLG59M1717V with  $C_{SLEW}$  set to 15nF and 470 $\mu$ F retained for  $C_{LOAD}$ .  $C_{LOAD}$ -to- $C_{SLEW}$  ratio is smaller than 33,600. Note smooth  $V_{OUT}$  transition.

### Setting the SLG59M1717V Output Current Limit with $R_{SET}$

The current-limit operation of the SLG59M1717V begins by choosing the appropriate  $\pm 1\%$ -tolerance  $R_{SET}$  value for the application. The recommended range for  $R_{SET}$  is:

$$38 \text{ k}\Omega \leq R_{SET} \leq 80 \text{ k}\Omega$$

which corresponds to an output constant current limit in the following range:

$$2.85 \text{ A} \leq I_{ACL} \leq 6 \text{ A}$$

Table 1: Setting Current Limit Threshold vs.  $R_{SET}$

Constant Current Limit	$R_{SET}$
2.85 A	80 k $\Omega$
3.8 A	60 k $\Omega$
6 A	38 k $\Omega$



### Power Dissipation

The junction temperature of the SLG59M1717V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG59M1717V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = RDS_{ON} \times I_{DS}^2$$

where:

PD = Power dissipation, in Watts (W)

$RDS_{ON}$  = Power MOSFET ON resistance, in Ohms ( $\Omega$ )

$I_{DS}$  = Output current, in Amps (A)

and

$$T_J = PD \times \theta_{JA} + T_A$$

where:

$T_J$  = Junction temperature, in Celsius degrees ( $^{\circ}C$ )

$\theta_{JA}$  = Package thermal resistance, in Celsius degrees per Watt ( $^{\circ}C/W$ )

$T_A$  = Ambient temperature, in Celsius degrees ( $^{\circ}C$ )

During active current-limit operation, the SLG59M1717V's power dissipation can be calculated by taking into account the voltage drop across the power switch ( $V_{IN} - V_{OUT}$ ) and the magnitude of the output current in active current-limit operation ( $I_{ACL}$ ):

$$PD = (V_{IN} - V_{OUT}) \times I_{ACL} \text{ or}$$

$$PD = (V_{IN} - (R_{LOAD} \times I_{ACL})) \times I_{ACL}$$

where:

PD = Power dissipation, in Watts (W)

$V_{IN}$  = Input Voltage, in Volts (V)

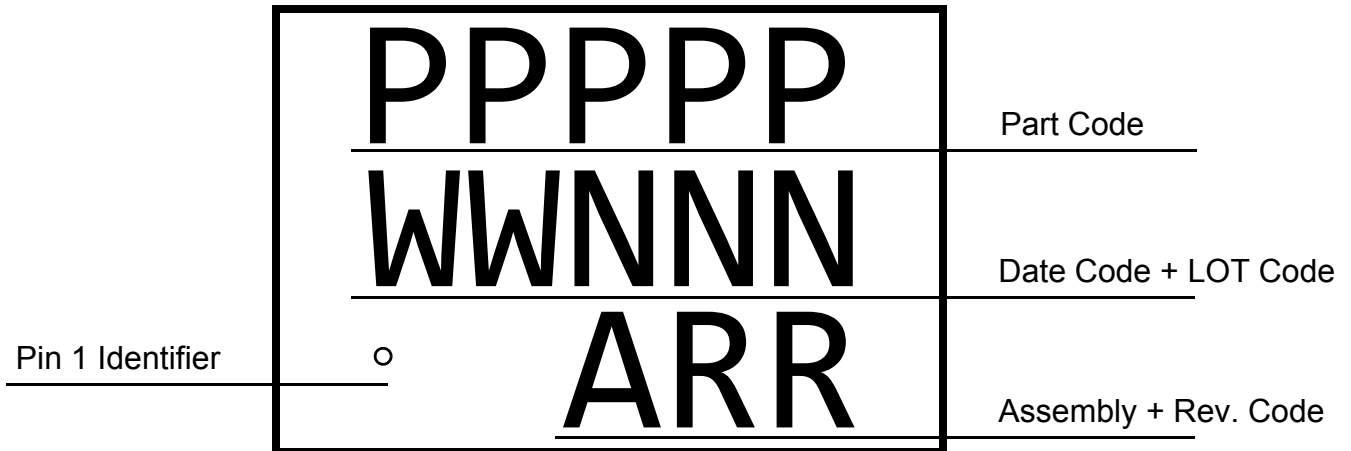
$R_{LOAD}$  = Load Resistance, in Ohms ( $\Omega$ )

$I_{ACL}$  = Output limited current, in Amps (A)

$V_{OUT} = R_{LOAD} \times I_{ACL}$



Package Top Marking System Definition



- PPPPP - Part ID Field
- WW - Date Code Field<sup>1</sup>
- NNN - Lot Traceability Code Field<sup>1</sup>
- A - Assembly Site Code Field<sup>2</sup>
- RR - Part Revision Code Field<sup>2</sup>

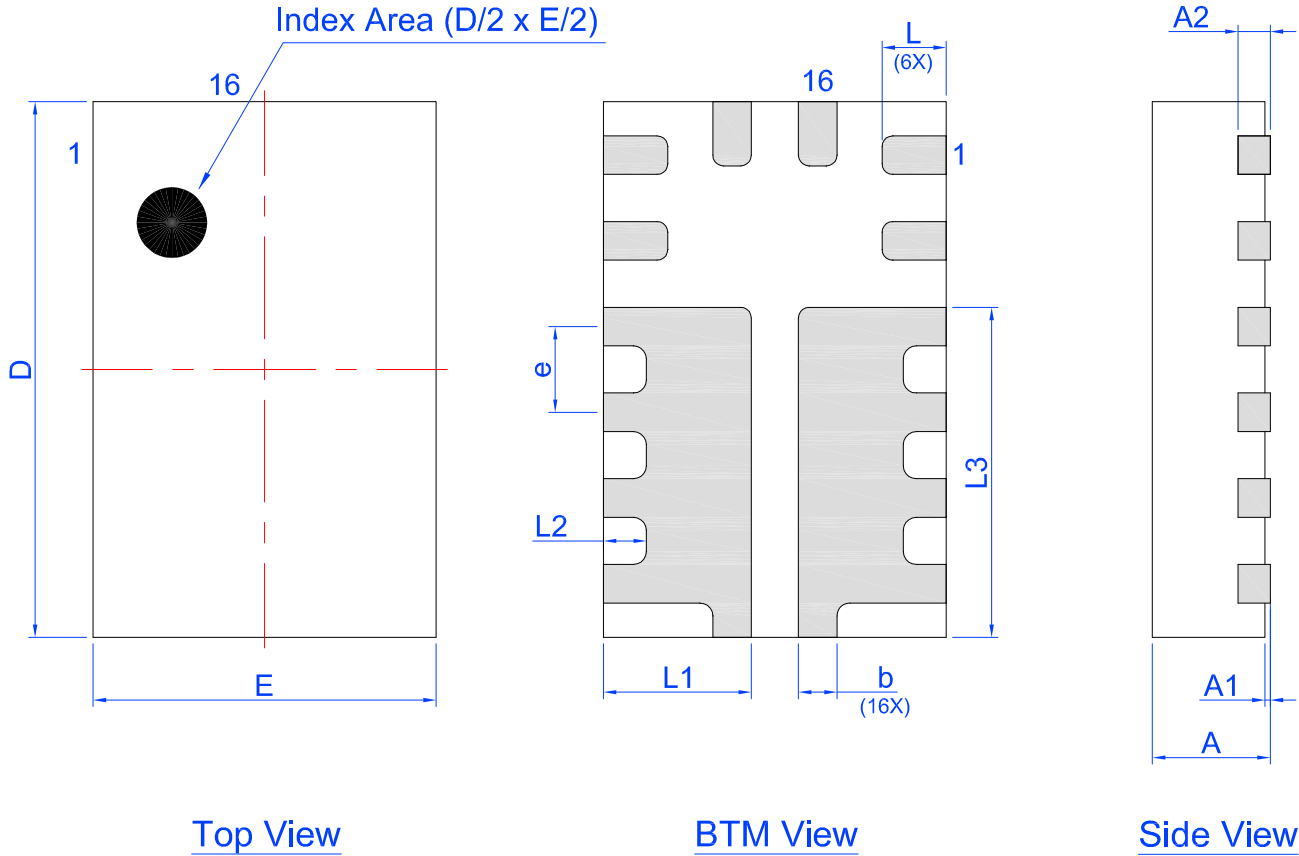
Note 1: Each character in code field can be alphanumeric A-Z and 0-9

Note 2: Character in code field can be alphabetic A-Z



**Package Drawing and Dimensions**

16 Lead STQFN Package 1.6 mm x 2.5 mm (Fused Lead)



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.45	2.50	2.55
A1	0.005	-	0.05	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.64	0.69	0.74
e	0.40 BSC			L2	0.15	0.20	0.25
				L3	1.49	1.54	1.59

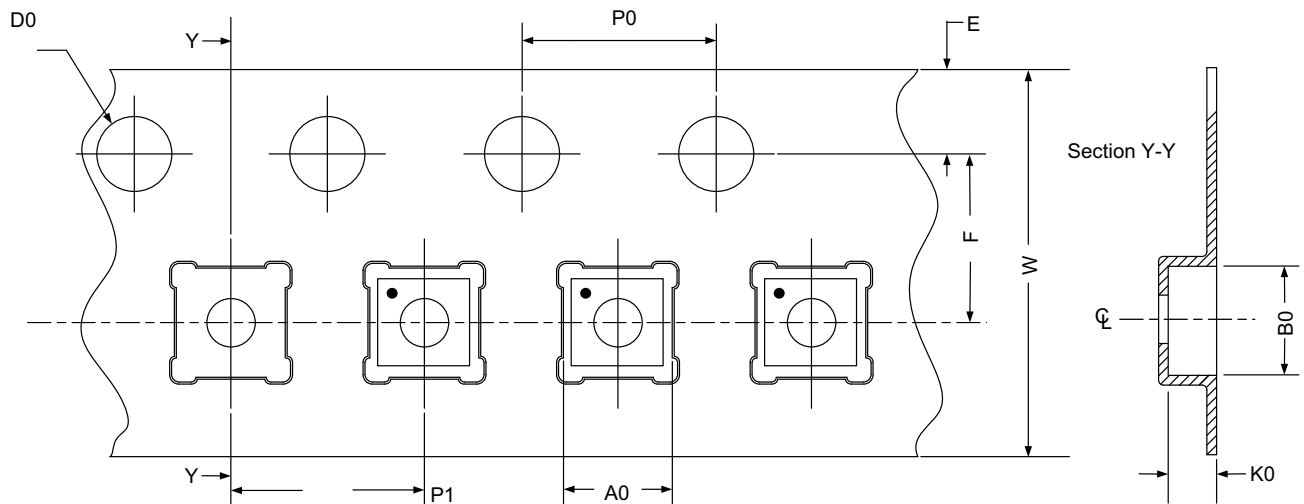


**Tape and Reel Specifications**

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 16L 1.6x2.5mm 0.4P FCA Green	16	1.6x2.5x 0.55mm	3000	3000	178/60	100	400	100	400	8	4

**Carrier Tape Drawing and Dimensions**

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 16L 1.6x2.5mm 0.4P FCA Green	1.8	2.8	0.7	4	4	1.55	1.75	3.5	8



Refer to EIA-481 specification

**Recommended Reflow Soldering Profile**

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.2 mm<sup>3</sup> (nominal). More information can be found at [www.jedec.org](http://www.jedec.org).



**Revision History**

Date	Version	Change
2/23/2017	1.00	Production Release