19-4145; Rev 6; 11/11

Low-Power µP Supervisory Circuits with Battery-Backup Circuit and Chip-Enable Gating

General Description

The MAX16016/MAX16020/MAX16021 supervisory circuits monitor power supplies, provide battery-backup control, and chip-enable (CE) gating to write protect memory in microprocessor (µP)-based systems. These low-power devices improve system reliability by providing several supervisory functions in a small, single integrated solution.

The MAX16016/MAX16020/MAX16021 perform four basic system functions:

1) Provide a µP reset output during V_{CC} supply power-up, power-down, and brownout conditions.
2) Control V_{CC} to battery-backup switching internally to maintain data or low-power operation for memories, real-time clocks (RTCs), and other digital logic when the main power is removed.
3) Provide memory write protection through internal chip-enable gating during brownout.
4) Provide a combination of additional supervisory functions listed in the *Features* section.

The MAX16016/MAX16020/MAX16021 operate from a 1.53V to 5.5V supply voltage and offer fixed reset thresholds for monitoring 5V, 3.3V, 3V, 2.5V, and 1.8V systems. Each device is available with either a push-pull or open-drain reset output.

The MAX16016/MAX16020/MAX16021 are available in small TDFN/TQFN packages and are fully specified for an operating temperature range of -40°C to +85°C.

Applications

Main/Backup Power for RTCs, CMOS Memories

Industrial Control

GPS Systems

Set-Top Boxes

Point-of-Sale Equipment

Portable/Battery Equipment

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Features

- **System Monitoring for 5V, 3.3V, 3V, 2.5V, or 1.8V Power-Supply Voltages**
- **1.53V to 5.5V Operating Voltage Range**
- **Low 1.2µA Supply Current (0.25µA in Battery-Backup Mode)**
- **145ms (min) Reset Timeout Period**
- **Battery Freshness Seal**
- **On-Board Gating of CE Signals, 1.5ns Propagation Delay (MAX16020/MAX16021)**
- **Debounced Manual Reset Input**
- **Watchdog Timer, 1.2s (typ) Timeout**
- **Power-Fail Comparator and Low-Line Indicator for Monitoring Voltages Down to 0.6V**
- **Battery-On, Battery-OK, and Battery Test Indicators**
- **Small 10-Pin TDFN or 16-Pin TQFN Packages**
- **UL®-Certified to Conform to IEC 60950-1**

Ordering Information

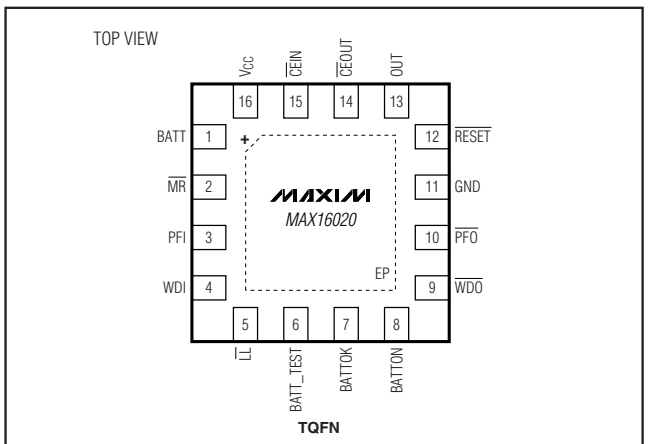
PART	TEMP RANGE	PIN-PACKAGE
MAX16016_TB_+T	-40°C to +85°C	10 TDFN-EP*

The first placeholder "_" designates all output options. Letter "L" indicates push-pull outputs and letter "P" indicates open-drain outputs. The last placeholder "_" designates the reset threshold (see Table 1).
T = Tape and reel.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Ordering Information continued at end of data sheet.

Selector Guide located at end of data sheet.

Pin Configurations



Pin Configurations continued at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Low-Power µP Supervisory Circuits with Battery-Backup Circuit and Chip-Enable Gating

ABSOLUTE MAXIMUM RATINGS

V_{CC}, BATT, OUT, BATT_TEST to GND .....-0.3V to +6V
$\overline{RESET}$, RESET, $\overline{PFO}$, BATTOK, $\overline{WDO}$, BATTON, BATT_TEST, $\overline{LL}$, (all open-drain) to GND .....-0.3V to +6V
$\overline{RESET}$, RESET, BATTOK, $\overline{WDO}$, BATTON, $\overline{LL}$ (all push-pull) to GND .....-0.3V to (V_{OUT} + 0.3V)
WDI, $\overline{PFI}$ to GND .....-0.3V to (V_{OUT} + 0.3V)
$\overline{CE}$IN, $\overline{CE}$OUT to GND .....-0.3V to (V_{OUT} + 0.3V)
$\overline{MR}$ to GND .....-0.3V to (V_{CC} + 0.3V)
Input Current
V_{CC} Peak Current 1A
V_{CC} Continuous Current 250mA
BATT Peak Current 500mA
BATT Continuous Current 70mA
Output Current
OUT Short Circuit to GND Duration 10s
$\overline{RESET}$, RESET, BATTON 20mA
Continuous Power Dissipation (T_A = +70°C)
10-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
16-Pin TQFN (derate 25mW/°C above +70°C) 2000mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow)
TDFN .....+260°C
TQFN .....+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TDFN
Junction-to Ambient Thermal Resistance (θ_{JA}) .....41°C/W
Junction-to Case Thermal Resistance (θ_{JC}) .....9°C/W

TQFN
Junction-to Ambient Thermal Resistance (θ_{JA}) .....40°C/W
Junction-to Case Thermal Resistance (θ_{JC}) .....6°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.53V to 5.5V, V_{BATT} = 3V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range (Note 3)	V_{CC}, V_{BATT}	V_{CC} or V_{BATT} > V_{TH}		0		5.5	V
Supply Current	I_{CC}	V_{CC} > V_{TH}	V_{CC} = 1.62V		1.2	2	µA
			V_{CC} = 2.8V		1.9	3	
			V_{CC} = 3.6V		2.3	3.5	
			V_{CC} = 5.5V		3.4	5	
Supply Current in Battery-Backup Mode	I_{BATT}	V_{CC} = 0V			0.25	0.5	µA
V_{CC} Switchover Threshold Voltage		V_{CC} rising, V_{CC} - V_{BATT}			0.1 x V_{CC}		V
BATT Switchover Threshold Voltage		V_{CC} falling, V_{CC} < V_{TH}, V_{CC} - V_{BATT}			0		mV
BATT Standby Current		V_{CC} > V_{BATT} + 0.2V		-10		+10	nA
BATT Freshness Leakage Current		V_{BATT} = 5.5V				20	nA
V_{CC} to OUT On-Resistance	R_{ON}	V_{CC} = 4.75V, I_{OUT} = 150mA			1.4	4.5	Ω
		V_{CC} = 3.15V, I_{OUT} = 65mA			1.7	4.5	
		V_{CC} = 2.35V, I_{OUT} = 25mA			2.1	5.0	
		V_{CC} = 1.91V, I_{OUT} = 10mA			2.6	5.5	
Output Voltage in Battery-Backup Mode	V_{OUT}	V_{BATT} = 4.5V, I_{OUT} = 20mA		V_{BATT} - 0.1			V
		V_{BATT} = 2.5V, I_{OUT} = 20mA		V_{BATT} - 0.15			

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 1.53V to 5.5V, V_{BATT} = 3V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RESET OUTPUT (RESET, $\overline{RESET}$)						
Reset Threshold	V_{TH}			(see Table 1)		V
V_{CC} Falling to Reset Delay	t_{RD}	V_{CC} falling at 10V/ms		20		µs
Reset Timeout Period	t_{RP}		145	215	285	ms
$\overline{RESET}$ Output Low Voltage	V_{OL}	V_{CC} ≥ 3.3V, I_{SINK} = 3.2mA, $\overline{RESET}$ asserted			0.3	V
		V_{CC} ≥ 1.6V, I_{SINK} = 1mA, $\overline{RESET}$ asserted			0.3	
		V_{CC} ≥ 1.2V, I_{SINK} = 100µA, $\overline{RESET}$ asserted			0.3	
$\overline{RESET}$ Output High Voltage (Push-Pull Output)	V_{OH}	V_{CC} = 1.1 x V_{TH}, I_{SOURCE} = 100µA, $\overline{RESET}$ deasserted	V_{OUT} - 0.3			V
$\overline{RESET}$ Output Leakage Current (Open-Drain Output)		$V_{\overline{RESET}}$ = 5.5V, $\overline{RESET}$ deasserted			1	µA
RESET Output Low Voltage	V_{OL}	V_{CC} ≥ 3.3V, I_{SINK} = 3.2mA, RESET deasserted			0.3	V
		V_{CC} ≥ 1.8V, I_{SINK} = 1.0mA, RESET deasserted			0.3	
RESET Output High Voltage (Push-Pull Output)	V_{OH}	V_{CC} = 0.9 x V_{TH}, I_{SOURCE} = 100µA, RESET asserted	V_{OUT} - 0.3			V
RESET Output Leakage Current (Open-Drain Output)		V_{RESET} = 5.5V, RESET asserted			1	µA
POWER-FAIL COMPARATOR						
PFI, Input Threshold	V_{PFT}	V_{IN} falling, 1.6V ≤ V_{CC} ≤ 5.5V	0.572	0.590	0.611	V
PFI, Hysteresis	$V_{PFT-HYS}$			30		mV
PFI Input Current		V_{CC} = 5.5V	-1		+1	µA
$\overline{PFO}$ Output Low Voltage	V_{OL}	V_{CC} ≥ 1.6V, I_{SINK} = 1mA, output asserted			0.3	V
		V_{CC} ≥ 1.2V, I_{SINK} = 100µA, output asserted			0.3	
PFO Output Voltage High (Push-Pull Output)	V_{OH}	V_{CC} = 1.1 x V_{TH}, I_{SOURCE} = 100µA, output asserted	V_{OUT} - 0.3			V
$\overline{PFO}$, Leakage Current (Open-Drain Output)		$V_{\overline{PFO}}$ = 5.5V, output deasserted			1	µA
$\overline{PFO}$, Delay Time		V_{PFT} + 100mV to V_{PFT} - 100mV		20		µs
MANUAL RESET ($\overline{MR}$)						
Input Low Voltage	V_{IL}				0.3 x V_{CC}	V
Input High Voltage	V_{IH}		0.7 x V_{CC}			V
Pullup Resistance			20	30		kΩ
Glitch Immunity		V_{CC} = 3.3V		100		ns
$\overline{MR}$ to Reset Delay				120		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 1.53V to 5.5V, V_{BATT} = 3V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WATCHDOG TIMER (WDI, $\overline{WDO}$)						
Watchdog Timeout Period	t_{WD}		0.83	1.235	1.64	s
Minimum WDI Input Pulse Width	t_{WDI}		320			ns
WDI Input Low Voltage	V_{IL}	(Note 6)			0.3 x V_{CC}	V
WDI Input High Voltage	V_{IH}	(Note 6)	0.7 x V_{CC}			V
WDI Input Current (Note 7)		V_{WDI} = 0V or 5.5V, time average	-1		+1	µA
$\overline{WDO}$ Output Low Voltage	V_{OL}	V_{CC} = 5.0V, I_{SINK} = 1mA, $\overline{WDO}$ asserted			0.3	V
$\overline{WDO}$ Output High Voltage (Push-Pull Output)	V_{OH}	V_{CC} = 1.1 x V_{TH}, I_{SOURCE} = 100µA, $\overline{WDO}$ deasserted	V_{OUT} - 0.3			V
$\overline{WDO}$ Leakage Current (Open-Drain Output)		$V_{\overline{WDO}}$ = 5.5V, $\overline{WDO}$ deasserted			1	µA
BATTERY-ON INDICATOR (BATTON)						
Output Low Voltage	V_{OL}	I_{SINK} = 3.2mA, V_{BATT} = 2.1V			0.3	V
BATTON Leakage Current		V_{BATTON} = 5.5V			1	µA
BATTON Output High Voltage	V_{OH}	V_{CC} = 0.9 x V_{TH}, I_{SOURCE} = 100µA, BATTON asserted	V_{OUT} - 0.3			V
Output Short-Circuit Current (Note 4)		Sink current, V_{CC} = 5V		60		mA
CE GATING ($\overline{CEIN}$, $\overline{CEOUT}$)						
$\overline{CEIN}$ Leakage Current		Reset asserted, V_{CC} = 0.9 x V_{TH} or 0V	-1		+1	µA
$\overline{CEIN}$ to $\overline{CEOUT}$ Resistance		Reset not asserted (Note 5)		8	50	Ω
$\overline{CEOUT}$ Short-Circuit Current		Reset asserted, $\overline{CEOUT}$ = 0, V_{CC} = 0.9 x V_{TH}		0.75	2	mA
$\overline{CEIN}$ to $\overline{CEOUT}$ Propagation Delay		50Ω source, C_{LOAD} = 50pF, V_{CC} = 4.75V		1.5	7	ns
Output High Voltage		V_{CC} = 5V, V_{CC} ≥ V_{BATT}, I_{SOURCE} = 100µA	0.8 x V_{CC}			V
		V_{CC} = 0V, V_{BATT} ≥ 2.2V, I_{SOURCE} = 1µA	V_{BATT} - 0.1			
Reset to $\overline{CEOUT}$ Delay				12		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 1.53V to 5.5V, V_{BATT} = 3V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOW LINE ($\overline{LL}$)						
Low Line to Reset Threshold Voltage		V_{CC} falling		(see Table 2)		mV
V_{CC} Falling to $\overline{LL}$ Delay		V_{CC} falling at 10V/ms		20		µs
$\overline{LL}$ Output Low Voltage	V_{OL}	V_{CC} ≥ 1.6V, I_{SINK} = 1mA, $\overline{LL}$ asserted			0.3	V
		V_{CC} ≥ 1.2V, I_{SINK} = 100µA, $\overline{LL}$ asserted			0.3	
$\overline{LL}$ Output High Voltage (Push-Pull Output)	V_{OH}	V_{CC} = 0.9 x $V_{TH_\overline{LL}}$, I_{SOURCE} = 100µA, $\overline{LL}$ deasserted	V_{OUT} - 0.3			V
Output Leakage Current		$V_{\overline{LL}}$ = 5.5V, $\overline{LL}$ deasserted			1	µA
BATTERY-OK INDICATOR (BATTOK, BATT_TEST)						
BATTOK Threshold		Inferred internally from BATT	2.508	2.6	2.673	V
BATTOK Output Voltage Low	V_{OL}	V_{CC} = 1.1 x V_{TH}, I_{SINK} = 1mA, reset asserted			0.3	V
BATTOK Output High Voltage	V_{OH}	V_{CC} = 1.1 x V_{TH}, I_{SOURCE} = 100µA, BATTOK asserted	V_{OUT} - 0.3			V
BATTOK Output Leakage Current		V_{BATTOK} = 5.5V, deasserted			1	µA
BATT_TEST Output Low Voltage		V_{CC} = 1.1 x V_{TH}, I_{SINK} = 1mA			0.3	V

Note 2: All devices are 100% production tested at T_A = +25°C and T_A = +85°C. Limits to -40°C are guaranteed by design.
Note 3: V_{BATT} can be 0V anytime, or V_{CC} can go down to 0V if V_{BATT} is active (except at startup).
Note 4: Use external current-limit resistor to limit current to 20mA (max).
Note 5: $\overline{CE}$IN/$\overline{CE}$OUT resistance is tested with V_{CC} = 5V and $V_{\overline{CE}IN}$ = 0V or 5V.
Note 6: WDI is internally serviced within the watchdog period if WDI is left unconnected.
Note 7: The WDI input current is specified as the average input current when the WDI input is driven high or low. The WDI input is designed for a three-stated output device with a 10µA maximum leakage current and capable of driving a maximum capacitive load of 200pF. The three-state device must be able to source and sink at least 200µA when active.

Table 1a. Reset Threshold Ranges (MAX16016)

SUFFIX	RESET THRESHOLD RANGES (V)		
	MIN	TYP	MAX
L	4.508	4.63	4.906
M	4.264	4.38	4.635
T	2.991	3.08	3.239
S	2.845	2.93	3.080
R	2.549	2.63	2.755
Z	2.243	2.32	2.425
Y	2.117	2.19	2.288
W	1.603	1.67	1.733
V	1.514	1.575	1.639

Table 1b. Reset Threshold Ranges (MAX16020/MAX16021)

SUFFIX	RESET THRESHOLD RANGES (V)		
	MIN	TYP	MAX
L	4.520	4.684	4.852
M	4.275	4.428	4.585
T	3.010	3.100	3.190
S	2.862	2.946	3.034
R	2.568	2.640	2.716
Z	2.260	2.323	2.390
Y	2.133	2.192	2.255
W	1.616	1.661	1.710
V	1.528	1.571	1.618

Low-Power µP Supervisory Circuits with Battery-Backup Circuit and Chip-Enable Gating

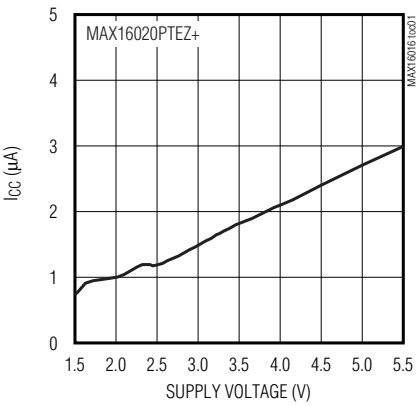
Table 2. Low-Line Threshold Ranges

SUFFIX	LOW-LINE THRESHOLD RANGES (V)		
	MIN	TYP	MAX
L	4.627	4.806	4.955
M	4.378	4.543	4.683
T	3.075	3.181	3.274
S	2.922	3.023	3.111
R	2.620	2.409	2.787
Z	2.309	2.383	2.450
Y	2.180	2.246	2.311
W	1.653	1.704	1.752
V	1.563	1.612	1.657

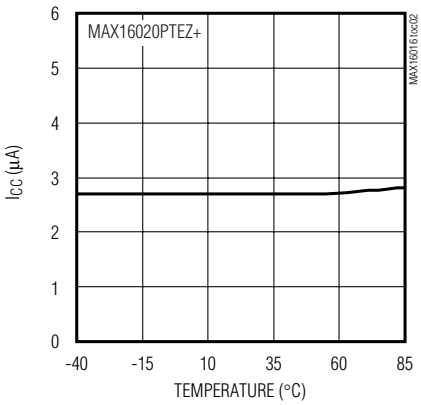
Typical Operating Characteristics

(V_{CC} = 5V, V_{BATT} = 0V, T_A = +25°C, unless otherwise noted.)

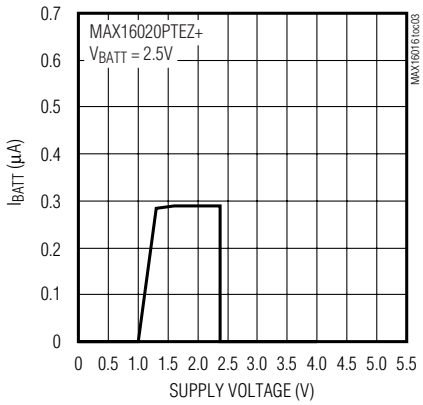
V_{CC} SUPPLY CURRENT vs. SUPPLY VOLTAGE



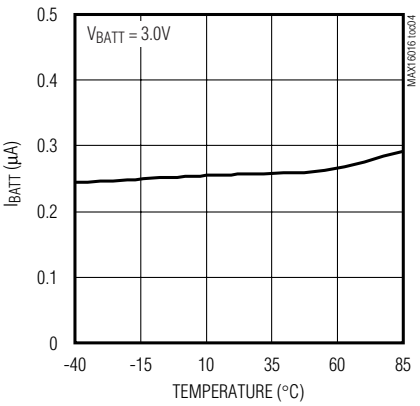
V_{CC} SUPPLY CURRENT vs. TEMPERATURE (I_{OUT} = 0mA)



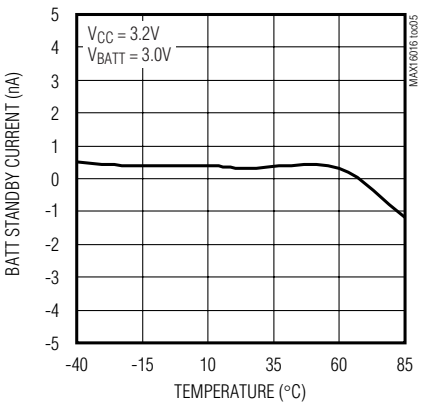
BATT SUPPLY CURRENT vs. SUPPLY VOLTAGE



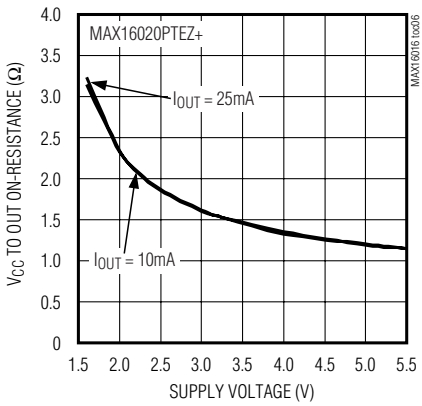
BATTERY SUPPLY CURRENT vs. TEMPERATURE (V_{CC} = 0V)



BATT STANDBY CURRENT vs. TEMPERATURE



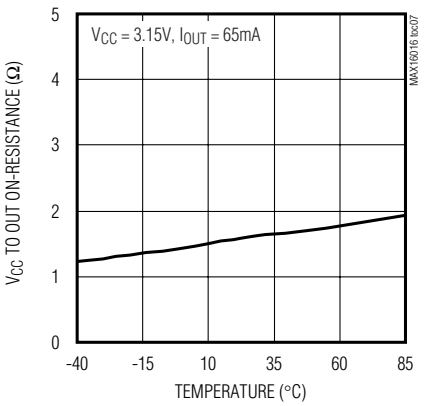
V_{CC} TO OUT ON-RESISTANCE vs. SUPPLY VOLTAGE



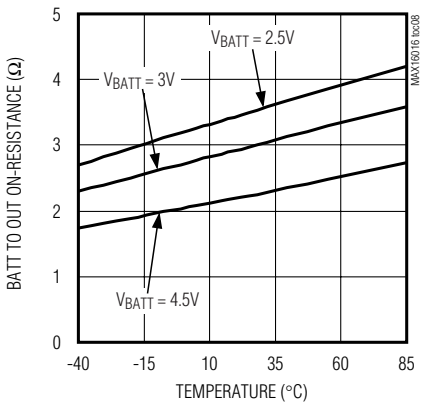
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{BATT} = 0V, T_A = +25°C, unless otherwise noted.)

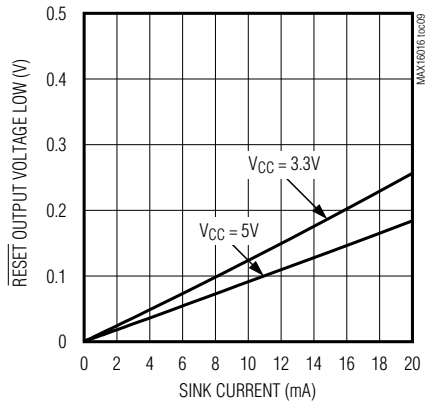
V_{CC} TO OUT ON-RESISTANCE vs. TEMPERATURE



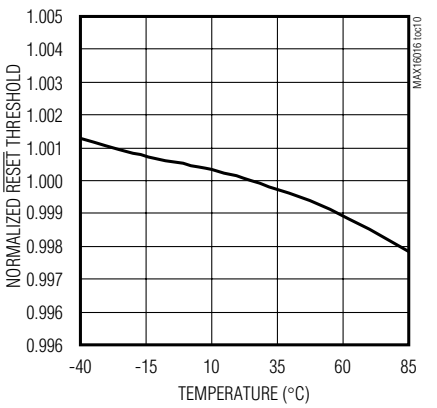
BATT TO OUT ON-RESISTANCE vs. TEMPERATURE (V_{CC} = 0V, I_{OUT} = 20mA)



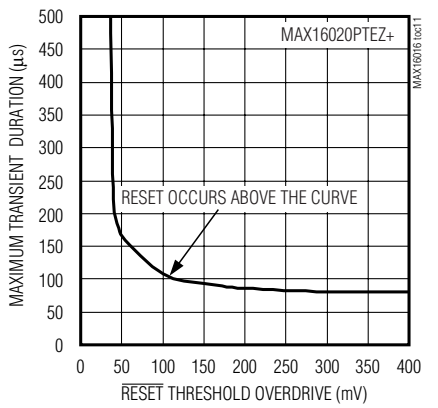
$\overline{RESET}$ OUTPUT VOLTAGE LOW vs. SINK CURRENT



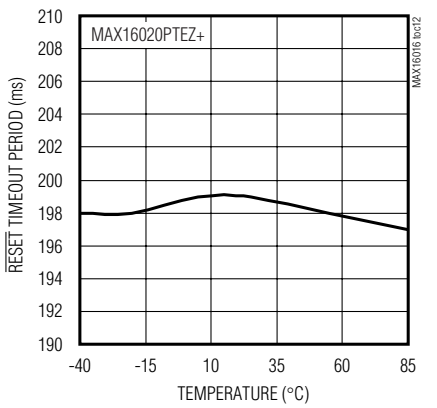
NORMALIZED $\overline{RESET}$ THRESHOLD vs. TEMPERATURE



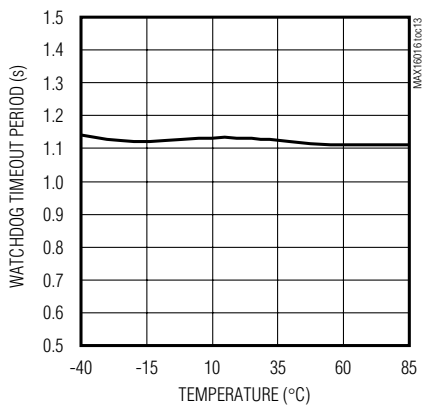
MAXIMUM TRANSIENT DURATION vs. $\overline{RESET}$ THRESHOLD OVERDRIVE



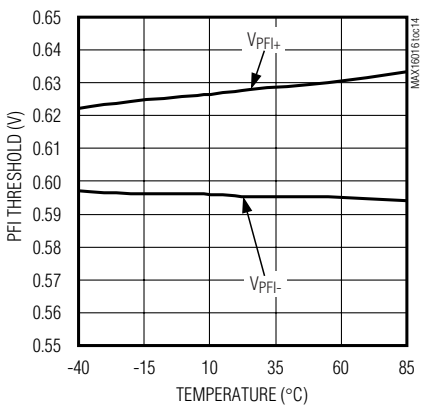
$\overline{RESET}$ TIMEOUT PERIOD vs. TEMPERATURE



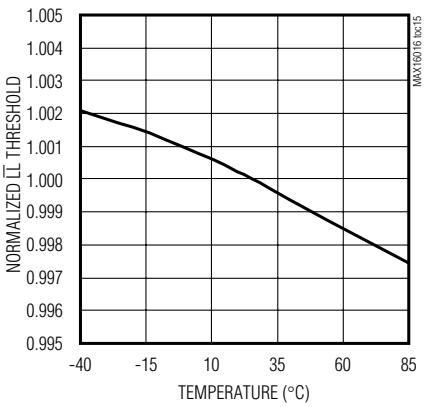
WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



PFI THRESHOLD vs. TEMPERATURE



NORMALIZED $\overline{LL}$ THRESHOLD vs. TEMPERATURE

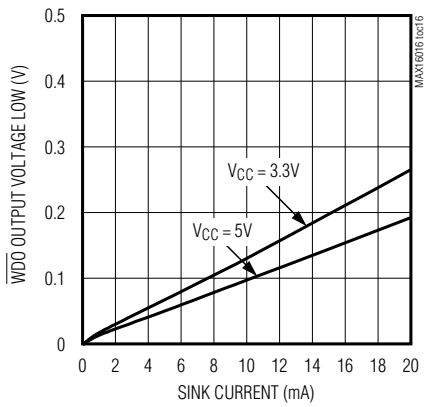


Low-Power µP Supervisory Circuits with Battery-Backup Circuit and Chip-Enable Gating

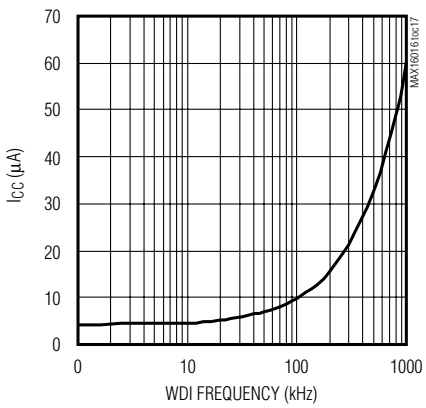
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{BATT} = 0V, T_A = +25°C, unless otherwise noted.)

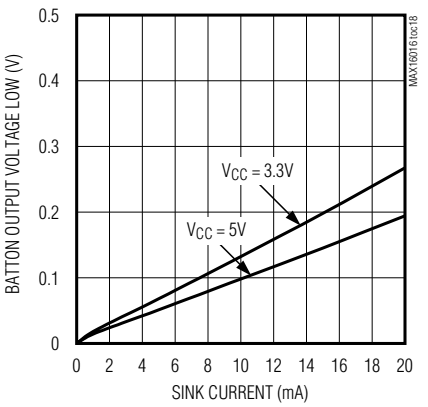
$\overline{WDO}$ OUTPUT VOLTAGE LOW vs. SINK CURRENT



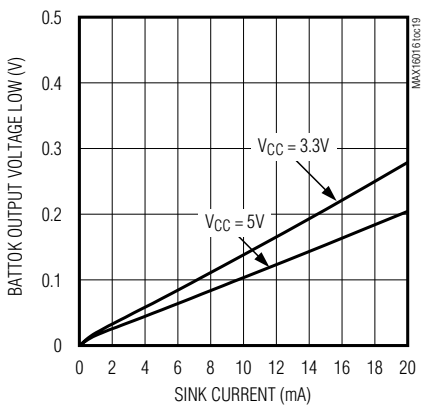
V_{CC} SUPPLY CURRENT vs. WDI FREQUENCY



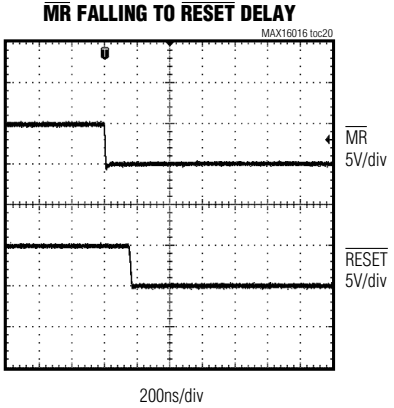
BATTON OUTPUT VOLTAGE LOW vs. SINK CURRENT



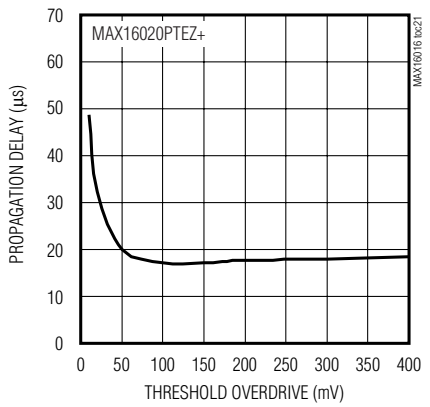
BATTOK OUTPUT VOLTAGE LOW vs. SINK CURRENT



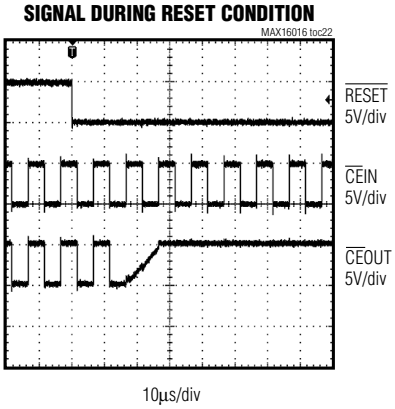
$\overline{MR}$ FALLING TO $\overline{RESET}$ DELAY



$\overline{RESET}$ PROPAGATION DELAY vs. THRESHOLD OVERDRIVE



CHIP-ENABLE GATING LOCKING OUT SIGNAL DURING RESET CONDITION



Pin Description—MAX16016

PIN	NAME	FUNCTION
1	V_{CC}	Supply Voltage Input. Bypass V_{CC} to GND with a 0.1µF capacitor.
2	BATT	Backup Battery Input. If V_{CC} falls below its reset threshold, and if $V_{BATT} > V_{CC}$, OUT connects to BATT. If V_{CC} rises above 1.01 x V_{BATT}, OUT connects to V_{CC}. Bypass BATT to GND with a 0.1µF capacitor.
3	$\overline{MR}$	Active-Low Manual Reset Input. $\overline{RESET}$ asserts when $\overline{MR}$ is pulled low. $\overline{RESET}$ remains low for the duration of reset timeout period after $\overline{MR}$ transitions from low to high. Connect $\overline{MR}$ to V_{CC} or leave unconnected if not used. $\overline{MR}$ is internally connected to V_{CC} through a 30kΩ pullup resistor.
4	PFI	Power-Fail Comparator Input. Connect PFI to a resistive divider to set the desired PFI threshold. The PFI input is referenced to an internal V_{PFT} threshold. A $V_{PFT-HYS}$ internal hysteresis provides noise immunity. The power-fail comparator is powered from OUT.
5	WDI	Watchdog Timer Input. If WDI remains high or low for longer than the watchdog timeout period (t_{WD}), the internal watchdog timer runs out and a reset pulse is triggered for the reset timeout period. The internal watchdog clears when reset asserts or whenever WDI sees a rising or falling edge. To disable the watchdog feature, leave WDI unconnected or three-state the driver connected to WDI.
6	BATTON	Active-High Battery-On Output. BATTON goes high when in battery-backup mode.
7	$\overline{PFO}$	Active-Low Power-Fail Comparator Output. $\overline{PFO}$ goes low when V_{PFI} falls below the internal V_{PFT} threshold and goes high when V_{PFI} rises above $V_{PFT} + V_{PFT-HYS}$ hysteresis.
8	GND	Ground
9	$\overline{RESET}$	Active-Low Reset Output. $\overline{RESET}$ asserts when V_{CC} falls below the reset threshold or $\overline{MR}$ is pulled low. $\overline{RESET}$ remains low for the duration of the reset timeout period after V_{CC} rises above the reset threshold and $\overline{MR}$ goes high. $\overline{RESET}$ also asserts low when the internal watchdog timer runs out.
10	OUT	Switched Output. OUT is connected to V_{CC} when the reset output is not asserted or when V_{CC} is greater than V_{BATT}. OUT connects to BATT when $\overline{RESET}$ is asserted and V_{BATT} is greater than V_{CC}. Bypass OUT to GND with a 0.1µF (min) capacitor.

Low-Power µP Supervisory Circuits with Battery-Backup Circuit and Chip-Enable Gating

Pin Description—MAX16020/MAX16021

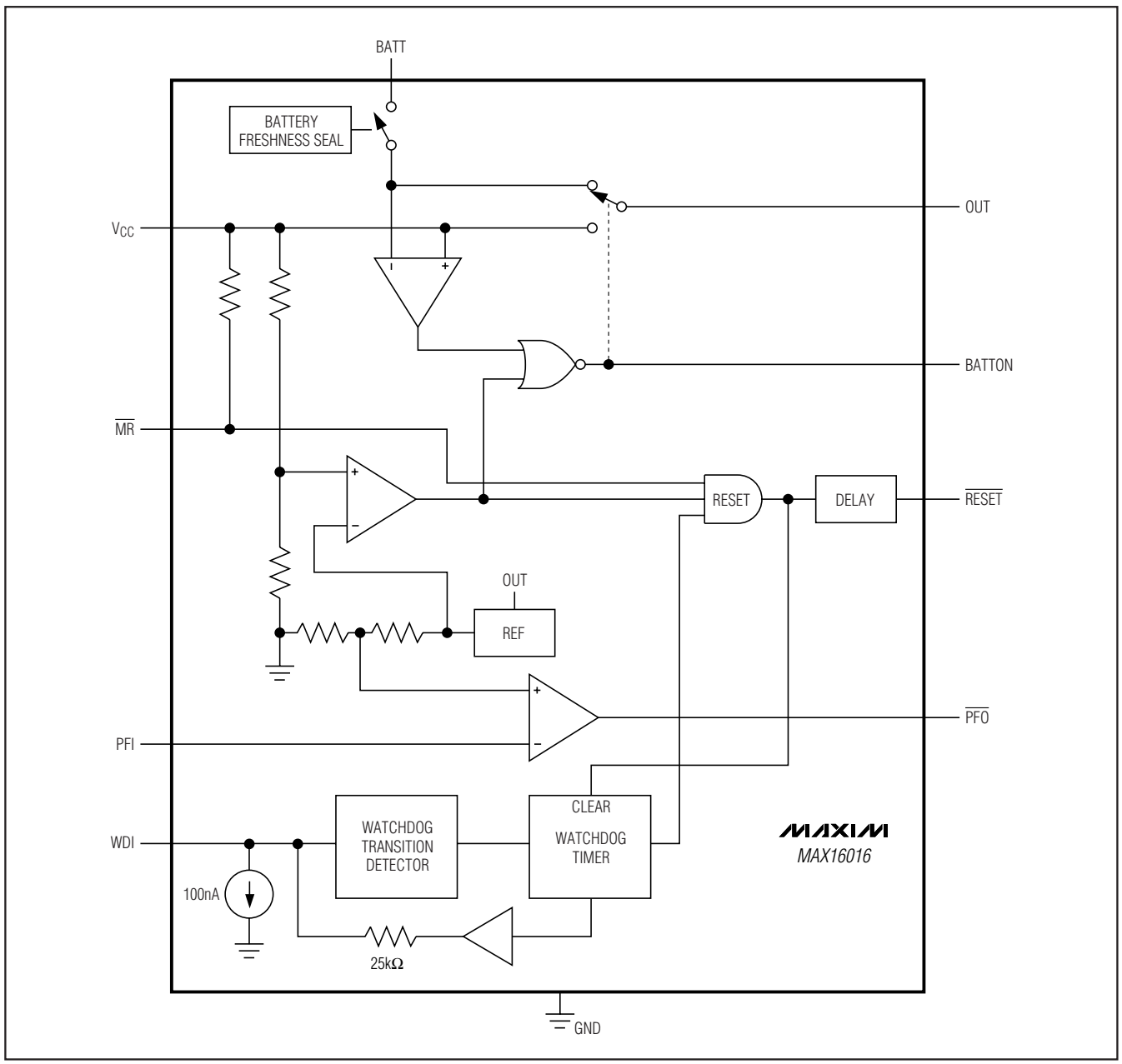
PIN		NAME	FUNCTION
MAX16020	MAX16021		
1	1	BATT	Backup Battery Input. If V_{CC} falls below its reset threshold, and if $V_{BATT} > V_{CC}$, OUT connects to BATT. If V_{CC} rises above 1.01 x V_{BATT}, OUT connects to V_{CC}. Bypass BATT to GND with a 0.1µF capacitor.
2	2	$\overline{MR}$	Active-Low Manual Reset Input. $\overline{RESET}$ asserts when $\overline{MR}$ is pulled low. $\overline{RESET}$ remains low for the duration of reset timeout period after $\overline{MR}$ transitions from low to high. Connect $\overline{MR}$ to V_{CC} or leave unconnected if not used. $\overline{MR}$ is internally connected to V_{CC} through a 30kΩ pullup resistor.
3	3	PFI	Power-Fail Comparator Input. Connect PFI to a resistive divider to set the desired PFI threshold. The PFI input is referenced to an internal threshold V_{PFT}, $V_{PFT-HYS}$ internal hysteresis provides noise immunity. The power-fail comparator is powered from OUT.
4	4	WDI	Watchdog Timer Input. If WDI remains high or low for longer than the watchdog timeout period (t_{WD}), the internal watchdog timer runs out and asserts $\overline{WDO}$. The internal watchdog clears when reset asserts or whenever WDI sees a rising or falling edge. To disable the watchdog feature, leave WDI unconnected or three-state the driver connected to WDI.
5	5	$\overline{LL}$	Active-Low Low-Line Output. $\overline{LL}$ goes low when V_{CC} falls to 2.5% above the reset threshold (Table 2). $\overline{LL}$ provides an early warning of V_{CC} failure before reset asserts. Use this output to generate a nonmaskable interrupt (NMI) to initiate an orderly shutdown routine when V_{CC} is falling.
6	—	BATT_TEST	Open-Drain Battery-Test Output. Pulses low for 1.3s every 24 hours during the battery voltage test. If $V_{BATT} < 2.6V$, BATTOK deasserts low. See Figure 6 for providing additional load during the battery test.
—	6	RESET	Active-High Reset Output. RESET asserts when V_{CC} falls below the reset threshold or when $\overline{MR}$ asserts and stays asserted for the reset timeout period after V_{CC} rises above the reset threshold and $\overline{MR}$ deasserts.
7	7	BATTOK	Battery-OK Output. BATTOK goes low when the battery voltage falls below the BATTOK threshold (BATTOK is low when in battery-backup mode).
8	8	BATTON	Active-High Battery-On Output. BATTON goes high when in battery-backup mode.

Pin Description—MAX16020/MAX16021 (continued)

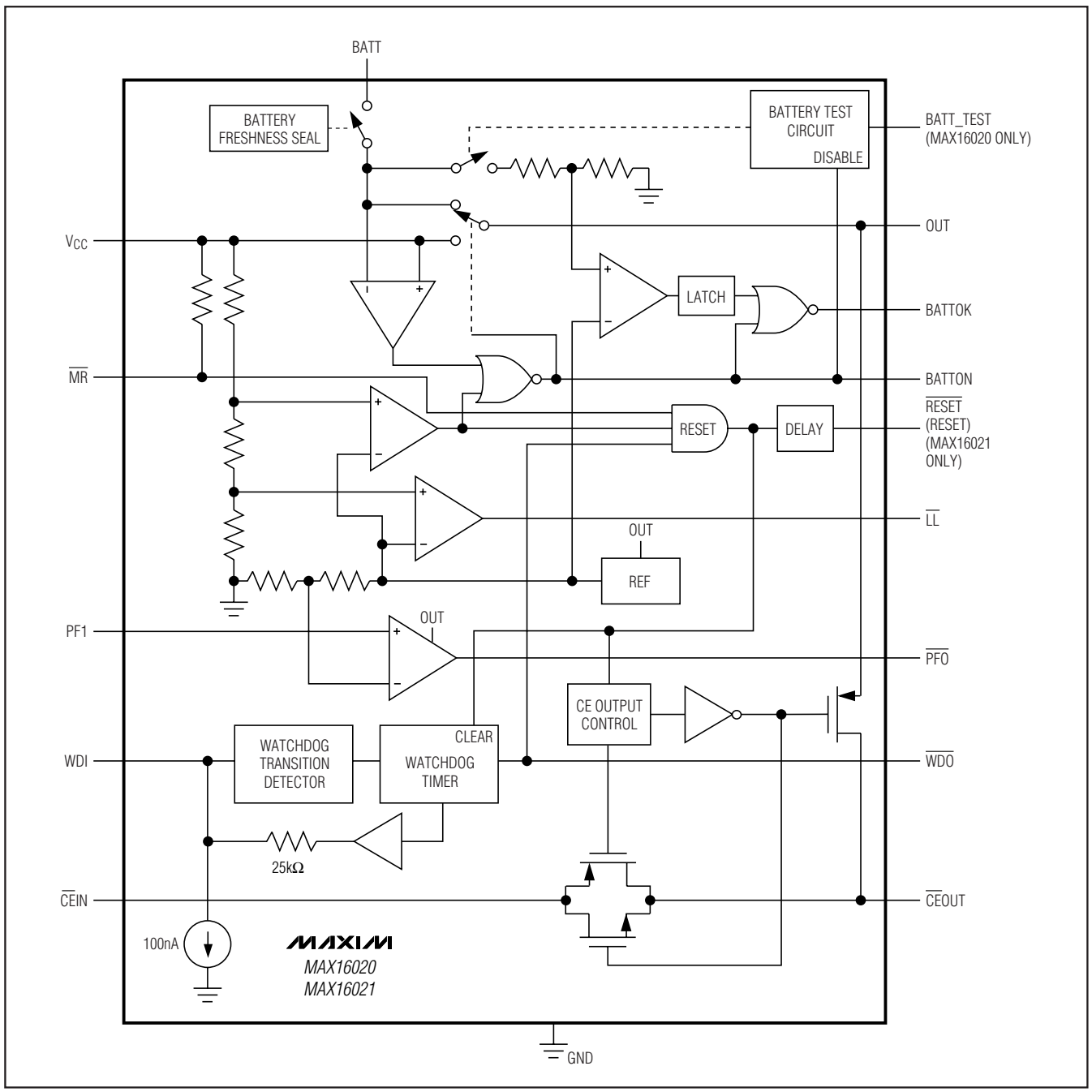
PIN		NAME	FUNCTION
MAX16020	MAX16021		
9	9	$\overline{WDO}$	Active-Low Watchdog Output. $\overline{WDO}$ asserts when WDI remains high or low longer than the watchdog timeout period. $\overline{WDO}$ returns high on the next WDI transition or when a reset is asserted.
10	10	$\overline{PFO}$	Active-Low Power-Fail Comparator Output. $\overline{PFO}$ goes low when V_{PFI} falls below the internal 0.6V V_{PFT} threshold and goes high when V_{PFI} rises above V_{PFT} + $V_{PFT-HYS}$ hysteresis.
11	11	GND	Ground
12	12	$\overline{RESET}$	Active-Low Reset Output. $\overline{RESET}$ asserts when V_{CC} falls below the reset threshold or $\overline{MR}$ is pulled low. $\overline{RESET}$ remains low for the duration of the reset timeout period after V_{CC} rises above the reset threshold and $\overline{MR}$ goes high.
13	13	OUT	Switched Output. OUT is connected to V_{CC} when the reset output is not asserted or when V_{CC} is greater than V_{BATT}. OUT connects to BATT when $\overline{RESET}$ is asserted and V_{BATT} is greater than V_{CC}. Bypass OUT to GND with a 0.1µF (min) capacitor.
14	14	$\overline{CE}$OUT	Active-Low Chip-Enable Output. $\overline{CE}$OUT goes low only when $\overline{CE}$IN is low and reset is not asserted. If $\overline{CE}$IN is low when reset is asserted, $\overline{CE}$OUT stays low for 12µs (typ) or until $\overline{CE}$IN goes high, whichever occurs first.
15	15	$\overline{CE}$IN	Chip-Enable Input. The input to CE gating circuitry. Connect to GND or OUT if not used.
16	16	V_{CC}	Supply Voltage Input. Bypass V_{CC} to GND with a 0.1µF capacitor.
—	—	EP	Exposed Pad. Internally connected to GND. Connect EP to a large ground plane to aid heat dissipation. Do not use EP as the only ground connection for the device.

Low-Power µP Supervisory Circuits with Battery-Backup Circuit and Chip-Enable Gating

Functional Diagrams



Functional Diagrams (continued)



Low-Power µP Supervisory Circuits with Battery-Backup Circuit and Chip-Enable Gating

Detailed Description

The *Typical Application Circuit* shows a typical connection using the MAX16020. OUT powers the static random-access memory (SRAM). If V_{CC} is greater than the reset threshold (V_{TH}), or if V_{CC} is lower than V_{TH}, but higher than V_{BATT}, V_{CC} connects to OUT. If V_{CC} is lower than V_{TH} and V_{CC} is less than V_{BATT}, BATT connects to OUT (see the *Functional Diagrams*). In battery-backup mode, an internal MOSFET connects the backup battery to OUT. The on-resistance of the MOSFET is a function of backup-battery voltage and temperature.

Backup-Battery Switchover

In a brownout or power failure, it may be necessary to preserve the contents of the RAM. With a backup battery installed at BATT, the MAX16016/MAX16020/MAX16021 automatically switch the RAM to the backup power when V_{CC} falls. The MAX16016/MAX16020/MAX16021 have a BATTON output that goes high when in battery-backup mode. These devices require two conditions before switching to battery-backup mode:

1) V_{CC} must be below the reset threshold.

2) V_{CC} must be below V_{BATT}.

Table 3 lists the status of the inputs and outputs in battery-backup mode. The device does not power up if the only voltage source is on BATT. OUT only powers up from V_{CC} at startup.

CE Signal Gating

The MAX16020/MAX16021 provide internal gating of CE signals to prevent erroneous data from being written to CMOS RAM in the event of a power failure or brownout. During normal operation, the CE gate is enabled and passes all CE transitions. When the reset output asserts, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. $\overline{CE}$OUT is pulled up to OUT through an internal current source. The 1.5ns propagation delay from $\overline{CE}$IN to $\overline{CE}$OUT allows the devices to be used with most µPs and high-speed DSPs.

During normal operation (reset not asserted), $\overline{CE}$IN is connected to $\overline{CE}$OUT through a low on-resistance transmission gate. If $\overline{CE}$IN is high when a reset asserts, $\overline{CE}$OUT remains high regardless of any subsequent transition on $\overline{CE}$IN during the reset event.

If $\overline{CE}$IN is low when reset asserts, $\overline{CE}$OUT is held low for 12µs to allow completion of the read/write operation. After the 12µs delay expires, $\overline{CE}$OUT goes high and stays high regardless of any subsequent transitions on $\overline{CE}$IN during the reset event. When $\overline{CE}$OUT is disconnected from $\overline{CE}$IN, $\overline{CE}$OUT is actively pulled up to OUT.

The propagation delay through the CE circuitry depends on both the source impedance of the drive to $\overline{CE}$IN and the capacitive loading at $\overline{CE}$OUT. Minimize the capacitive load at $\overline{CE}$OUT to minimize the propagation delay, and use a low output-impedance driver.

Low-Line Output ($\overline{LL}$)

The low-line comparator monitors V_{CC} with a threshold voltage typically 2.5% higher than the reset threshold (see Table 2). $\overline{LL}$ asserts prior to a reset condition during a brownout condition. On power-up, $\overline{LL}$ deasserts after the reset output. $\overline{LL}$ can be used to provide a nonmaskable interrupt (NMI) to the µP when the voltage begins to fall to initiate an orderly software shutdown routine.

Manual Reset Input

Many µP-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. For the MAX16016/MAX16020/MAX16021, a logic-low on $\overline{MR}$ asserts RESET/$\overline{RESET}$. RESET/$\overline{RESET}$ remains asserted while $\overline{MR}$ is low. When $\overline{MR}$ goes high RESET/$\overline{RESET}$ deasserts after a minimum of 145ms (t_{RP}). $\overline{MR}$ has an internal 30kΩ pullup resistor to V_{CC}. $\overline{MR}$ can be driven with TTL/CMOS logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual reset function; external debounce circuitry is not required. If $\overline{MR}$ is driven from a long cable or the device is used in a noisy environment, connect a 0.1µF capacitor from $\overline{MR}$ to GND to provide additional noise immunity.

Table 3. Input and Output Status in Battery-Backup Mode

PIN	STATUS
V_{CC}	Disconnected from OUT
OUT	Connected to BATT
BATT	Connected to OUT. Current drawn from the battery is less than 0.55µA (at V_{BATT} = 3V, excluding I_{OUT}) when V_{CC} = 0V.
RESET/$\overline{RESET}$	Asserted
BATTON, $\overline{WDO}$	High state (push-pull), high impedance (open-drain)
BATTOK, $\overline{LL}$	Low state
$\overline{CE}$IN	Disconnected from $\overline{CE}$OUT
$\overline{CE}$OUT	Pulled up to V_{OUT}
$\overline{PFO}$	Not affected

Watchdog Timer

Watchdog Input

The watchdog monitors µP activity through the input WDI. If the µP becomes inactive, either the reset output is asserted in pulses (MAX16016) or the watchdog output goes low (MAX16020/MAX16021). To use the watchdog function, connect WDI to a bus line or µP I/O line. If WDI remains high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and $\overline{RESET}$ asserts for the reset timeout period (MAX16016) or $\overline{WDO}$ goes low (MAX16020/MAX16021). The internal watchdog timer clears whenever the reset output asserts or the WDI sees a rising or falling edge within the watchdog timeout period. The WDI input is designed for a three-stated output device with a 10µA maximum leakage current and the capability of driving a maximum capacitive load of 200pF. The three-state device must be able to source and sink at least 200µA when active. Disable the watchdog timer by leaving WDI unconnected or by three-stating the driver connected to WDI. The watchdog timer periodically attempts to pulse WDI to the opposite logic-level through a 25kΩ resistor for 40µs to determine whether WDI is either unconnected or latched to a logic state. The watchdog function is also disabled when in battery-backup mode.

Watchdog Output

$\overline{WDO}$ remains high if there is a transition or pulse at WDI during the watchdog-timeout period. $\overline{WDO}$ goes low if no transition occurs at WDI during the watchdog timeout period and remains low until the next transition at WDI or when a reset is asserted. Connect $\overline{WDO}$ to $\overline{MR}$ to generate a system reset on every watchdog fault. When a watchdog fault occurs in this mode, $\overline{WDO}$ goes low, which pulls $\overline{MR}$ low, causing a reset pulse to be issued. As soon as the reset output is asserted, the watchdog timer clears and $\overline{WDO}$ returns high. With $\overline{WDO}$ connected to $\overline{MR}$, a continuous high or low on WDI causes 145ms (min) reset pulses to be issued every 1.235s.

Battery Testing Function/BATTOK Indicator (MAX16020/MAX16021)

The MAX16020/MAX16021 feature a battery testing function that works in conjunction with the BATTOK output. The battery voltage is tested for 1.235s after V_{CC} is applied and once every 24 hours thereafter. During this test, an internal 100kΩ resistor is connected from BATT to ground and the battery is monitored to ensure that the battery voltage is above 2.6V. If the battery voltage is below 2.6V, the BATTOK output deasserts low to indicate a weak battery condition. The MAX16020 has a BATT_TEST output that pulses high during the battery voltage test. Connect a resistor and FET as shown in Figure 6 to provide an additional load during the battery test. In battery-backup mode, the battery testing function is disabled and BATTOK goes low.

Battery Freshness Seal Mode

The MAX16016/MAX16020/MAX16021 battery freshness seal disconnects the backup battery from internal circuitry and OUT until V_{CC} is applied. This ensures the backup battery connected to BATT is fresh when the final product is used for the first time.

The internal freshness seal latch prevents BATT from powering OUT until V_{CC} has come up for the first time, setting the latch. When V_{CC} subsequently turns off, BATT begins to power OUT.

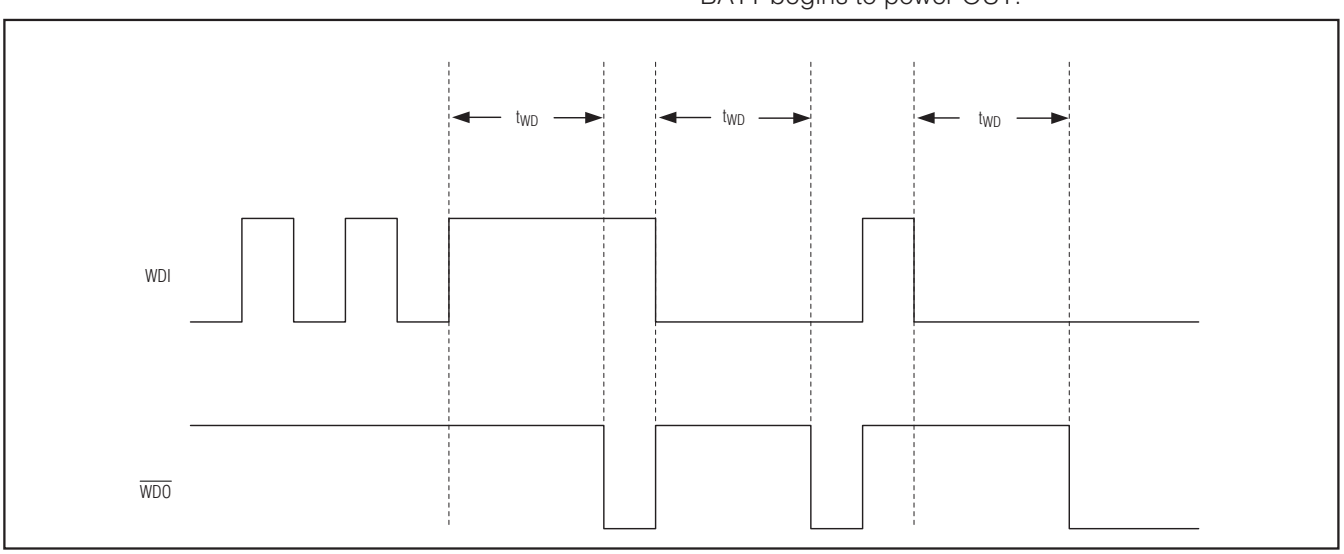


Figure 1. Watchdog Timing (MAX16016/MAX16020)

Low-Power µP Supervisory Circuits with Battery-Backup Circuit and Chip-Enable Gating

To reenable the freshness seal:

1) Connect a battery to BATT.
2) Bring V_{CC} to 0V.
3) Drive $\overline{MR}$ higher than V_{BATT} + 1.2V for at least 3µs.
4) Pull OUT to 0V.

Reset Output

A µP's reset input starts the µP in a known state. The µP supervisory circuits assert a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. Reset output is guaranteed to be a logic-low or logic-high depending on the device chosen. $\overline{RESET}$ or RESET asserts when V_{CC} is below the reset threshold and remains asserted for at least 145ms (t_{RP}) after V_{CC} rises above the reset threshold. $\overline{RESET}$ or RESET also asserts when $\overline{MR}$ is low. The MAX16016 watchdog function causes $\overline{RESET}$ to assert in pulses following a watchdog timeout. The reset output is available in both push-pull and open-drain configurations.

Power-Fail Comparator

The MAX16016/MAX16020/MAX16021 offer an undervoltage comparator that the output $\overline{PFO}$ goes low when the voltage at PFI falls below its V_{PFT} threshold.

Common uses for the power-fail comparator include monitoring the power supply (such as a battery) before any voltage regulation to provide an early power-fail warning, so software can conduct an orderly system shutdown. The power-fail comparator has a typical input hysteresis of $V_{PFT-HYS}$ and is powered from OUT, making it independent of the reset circuit. Connect the PFI input to GND if not used.

Applications Information

Monitoring an Additional Supply

The MAX16016/MAX16020/MAX16021 µP supervisors can monitor either positive or negative supplies using a resistive voltage-divider to PFI. $\overline{PFO}$ can be used to generate an interrupt to the µP or to trigger a reset (Figures 2 and 3). To monitor a negative supply, connect the top of the resistive divider to V_{CC}. Connect the bottom of the resistive divider to the negative voltage to be monitored.

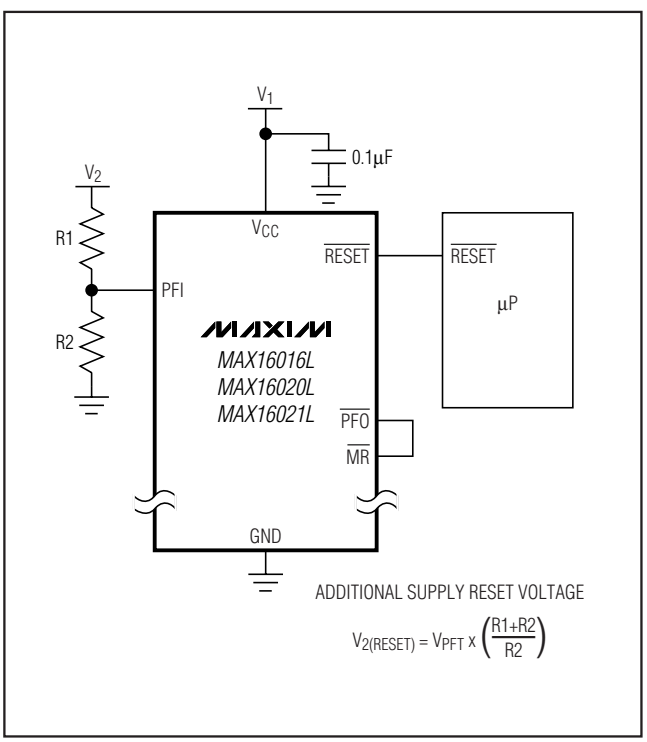


Figure 2. Monitoring an Additional Supply by Connecting $\overline{PFO}$ to $\overline{MR}$

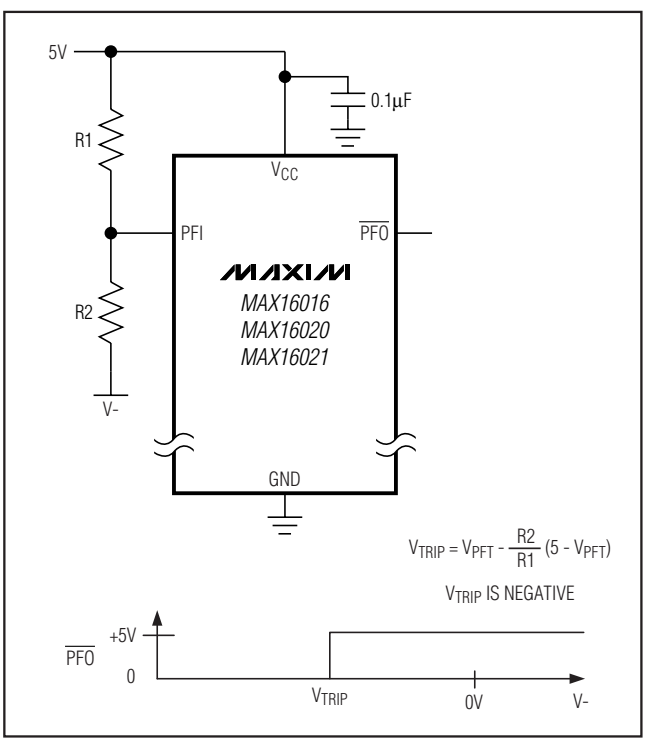


Figure 3. Monitoring a Negative Supply

Adding Hysteresis to PFI

The power-fail comparators have a typical input hysteresis of $V_{PFT-HYS}$. This is sufficient for most applications where a power-supply line is being monitored through an external voltage-divider (see the *Monitoring an Additional Supply* section). Figure 4 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 so that PFI sees V_{PFT} when V_{IN} falls to the desired trip point (V_{TRIP}). Resistor R3 adds hysteresis. R3 is typically an order of magnitude greater than R1 or R2. R3 should be larger than 50kΩ to prevent it from loading down $\overline{PFO}$. Capacitor C1 adds additional noise rejection.

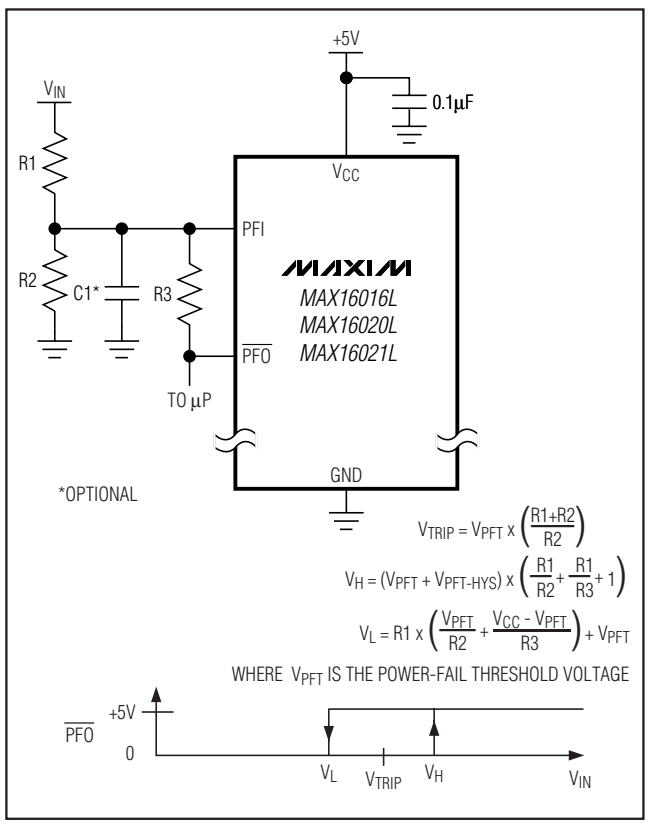


Figure 4. Adding Hysteresis to the Power-Fail Comparator

Battery-On Indicator (Push-Pull Version)

BATTON goes high when in battery-backup mode. Use BATTON to indicate battery-switchover status or to supply base drive to an external pass transistor for higher current applications (Figure 5).

Operation Without a Backup Power Source

The MAX16016/MAX16020/MAX16021 provide a battery-backup function. If a backup power source is not used, connect BATT to GND and OUT to V_{CC}.

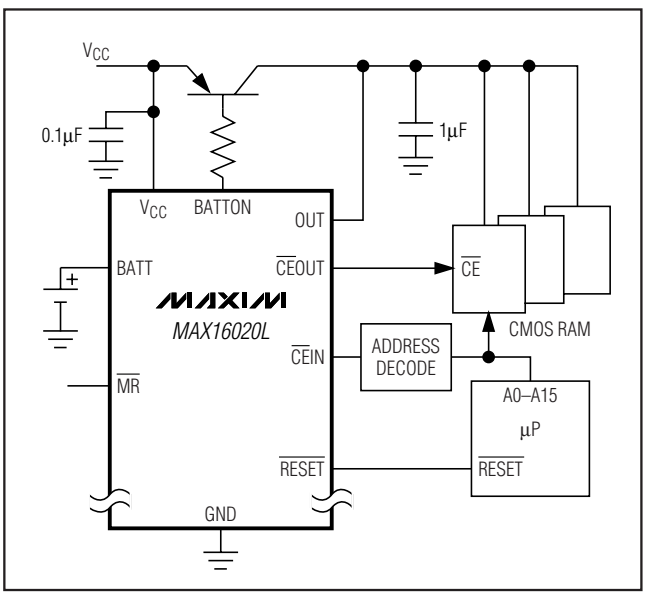


Figure 5. BATTON Driving an External Pass Transistor

Low-Power µP Supervisory Circuits with Battery-Backup Circuit and Chip-Enable Gating

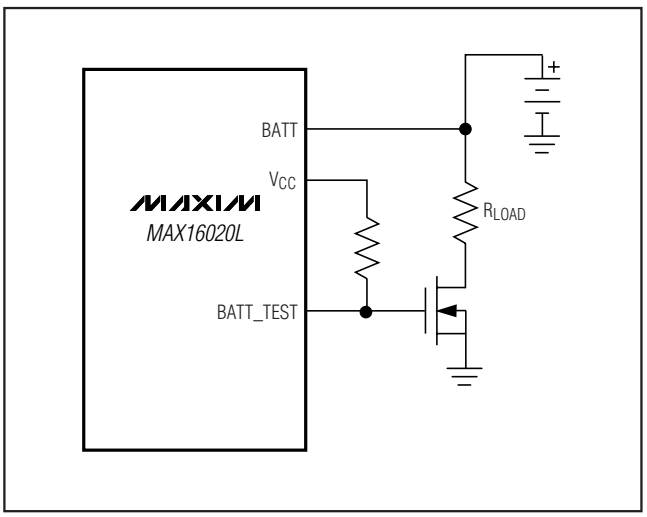


Figure 6. Adjustable BATT_TEST Load

Replacing the Backup Battery

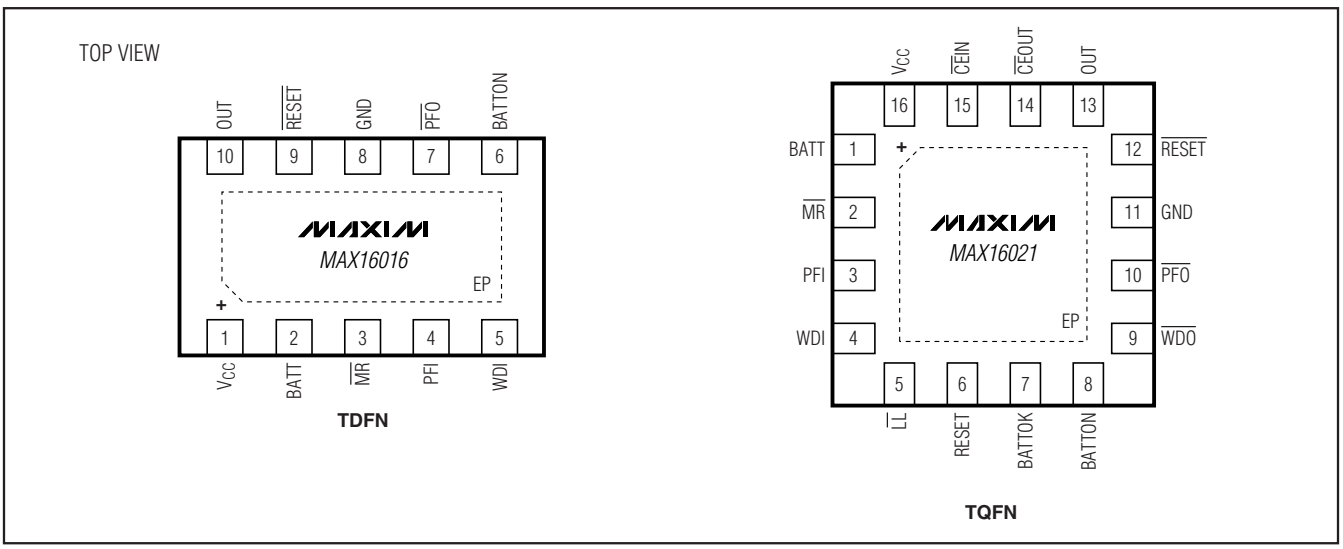
When V_{CC} is above V_{TH}, the backup power source can be removed without danger of triggering a reset pulse. The device does not enter battery-backup mode when V_{CC} stays above the reset threshold voltage.

Negative-Going V_{CC} Transients

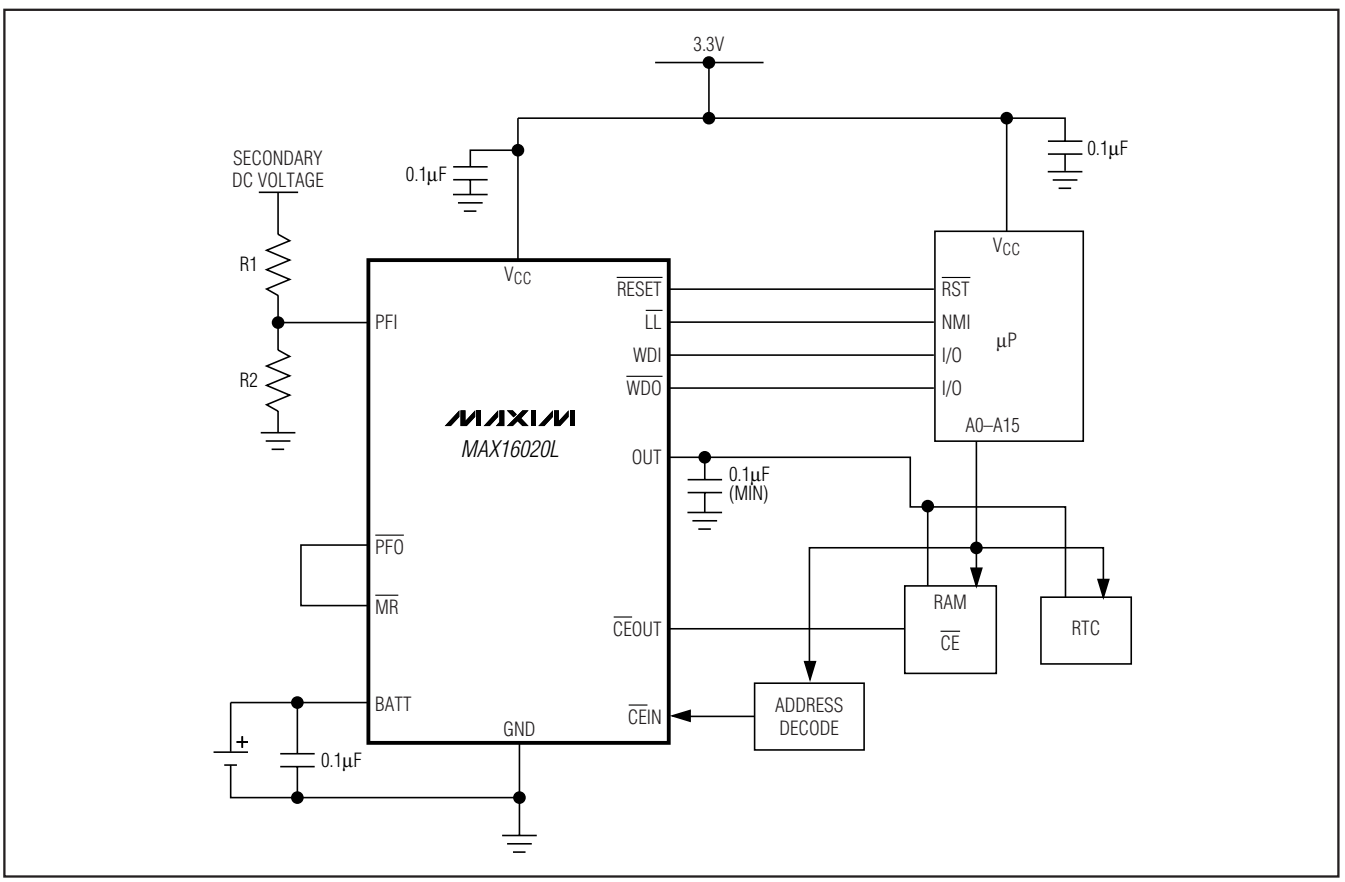
The MAX16016/MAX16020/MAX16021 are relatively immune to short duration, negative going V_{CC} transients. Resetting the µP when V_{CC} experiences only small glitches is usually not desirable. A 0.1µF bypass capacitor mounted close to V_{CC} provides additional transient immunity.

Low-Power µP Supervisory Circuits with Battery-Backup Circuit and Chip-Enable Gating

Pin Configurations (continued)



Typical Application Circuit



Low-Power µP Supervisory Circuits with Battery-Backup Circuit and Chip-Enable Gating

Selector Guide

PART	ALL LOGIC OUTPUTS (EXCEPT BATT_TEST)	$\overline{MR}$	POWER-FAIL COMPARATOR	WATCHDOG TIMER	BATTON	LOW-LINE OUTPUT	BATTOK/ BATT_TEST/ RESET	CHIP-ENABLE
MAX16016LTB_	Push-pull	√	√	WDI	√	—	—	—
MAX16016PTB_	Open-drain	√	√	WDI	√	—	—	—
MAX16020LTE_	Push-pull	√	√	WDI/$\overline{WDO}$	√	√	BATTOK/ BATT_TEST	√
MAX16020PTE_	Open-drain	√	√	WDI/$\overline{WDO}$	√	√	BATTOK/ BATT_TEST	√
MAX16021LTE_	Push-pull	√	√	WDI/$\overline{WDO}$	√	√	BATTOK/ RESET	√
MAX16021PTE_	Open-drain	√	√	WDI/$\overline{WDO}$	√	√	BATTOK/ RESET	√

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX16020_TE_+T	-40°C to +85°C	16 TQFN-EP*
MAX16021_TE_+T	-40°C to +85°C	16 TQFN-EP*

The first placeholder "_" designates all output options. Letter "L" indicates push-pull outputs and letter "P" indicates open-drain outputs. The last placeholder "_" designates the reset threshold (see Table 1).

T = Tape and reel.

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 TDFN-EP	T1033+1	**21-0137**	**90-0093**
16 TQFN-EP	T1644+4	**21-0139**	**90-0070**

Low-Power µP Supervisory Circuits with Battery-Backup Circuit and Chip-Enable Gating

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/08	Initial release	—
1	7/08	Released the MAX16016. Updated *Ordering Information*, *Electrical Characteristics*, Tables 1 and 2, *Pin Description*, and *Detailed Description*.	1, 3, 4, 5, 9, 10, 12, 13, 15, 16, 19, 20
2	10/08	Released the MAX16021.	20
3	12/08	Updated *Electrical Characteristics*, *Pin Description*, Table 3, and the *Power-Fail Comparator* section.	3, 9, 10, 11, 14, 16
4	1/10	Updated *Electrical Characteristics*.	4
5	4/11	Updated *Pin Description*.	9, 10
6	11/11	Updated *Pin Description*.	9, 10

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