Revision History AS4C64M32MD1 - 90-ball FBGA PACKAGE

Revision	Details	Date
Rev 1.0	Preliminary datasheet	September 2014

64M x 32 bit MOBILE DDR Synchronous DRAM (SDRAM)

Confidential **Advanced (Rev. 1.0, Sep. /2014)**

Feature

- 4 banks x 16M x 32 organization
- Two Die-stacked 4 banks x 16M x 16
- Data Mask for Write Control (DM)
- Four Banks controlled by BA0 & BA1
- Programmable CAS Latency: 2, 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length: 2, 4, 8, for Sequential Type
- 2, 4, 8, for Interleave Type
- Automatic and Controlled Precharge Command
- Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 8192 cycles/64ms
- Available in 90-ball BGA
- Double Data Rate (DDR)
- Bidirectional Data Strobe (DQS) for input and output data, active on both edges
- Differential clock inputs CLK and /CLK
- Power Supply 1.7V - 1.95V
- Drive Strength (DS) Option:Full, 1/2, 1/4, 1/8
- Auto Temperature-Compensated Self Refresh (Auto TCSR)
- Partial-Array Self Refresh (PASR) Option: Full, 1/2, 1/4, 1/8, 1/16
- Deep Power Down (DPD) mode
- Operating Temperature Range
  - Commercial -25°C to 85°C
  - Industrial -40°C to 85°C

All parts are ROHS Compliant

Description

The AS4C64M32MD1 is a four bank mobile DDR DRAM organized as 4 banks x 16M x 32. It achieves high speed data transfer rates by employing a chip architecture that pre-fetches multiple bits and then synchronizes the output data to a system clock.

All of the controls, address, circuits are synchronized with the positive edge of an externally supplied clock. I/O transactions are possible on both edges of DQS.

Operating the four memory banks in an inter-leaved fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, CAS latency and speed grade of the device.

Additionally, the device supports low power saving features like PASR, Auto-TCSR, DPD as well as options for different drive strength. It's ideally suitable for mobile application.

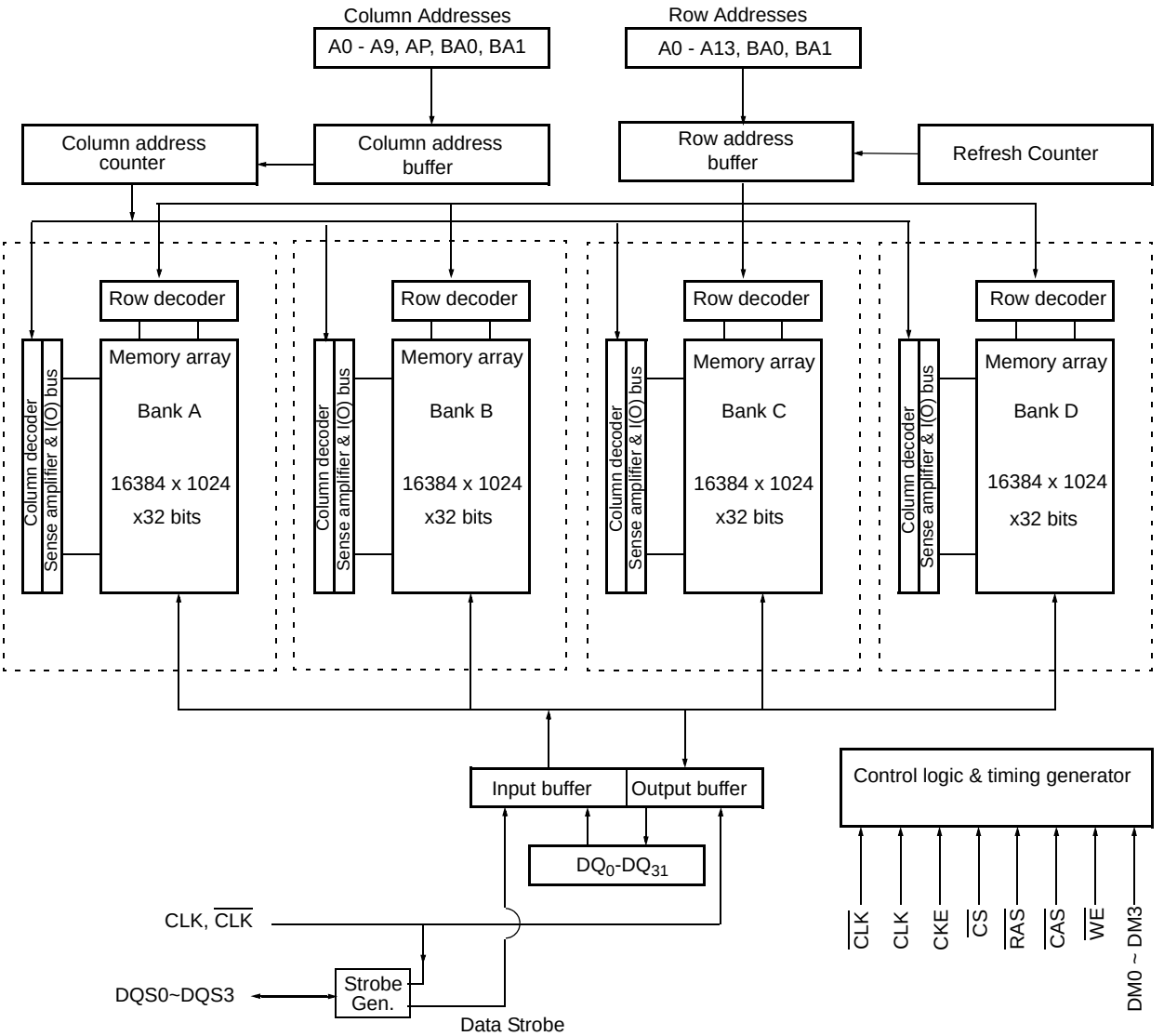
Table 1. Speed Grade Information

Speed Grade – Data rate	Clock Frequency	CAS Latency	t_{RCD} (ns)	t_{RP} (ns)
400Mbps (max)	200 MHz (max)	3	15	15

Table 2 – Ordering Information for ROHS Compliant Products

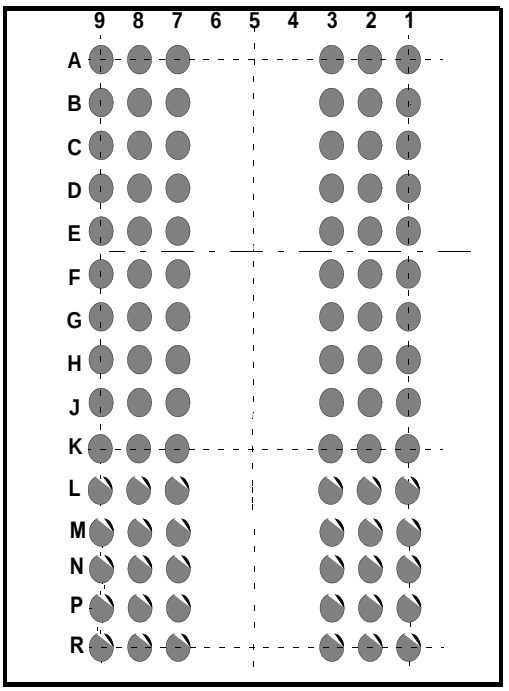
Product part No	Org	Temperature	Package
AS4C64M32MD1-5BCN	**64M x 32**	**Commercial - 25°C to 85°C (Extended)**	**90-ball FBGA**
AS4C64M32MD1-5BIN	**64M x 32**	**Industrial -40°C to 85°C**	**90-ball FBGA**

Block Diagram



90 BALL BGA CONFIGURATION

Top View



90Ball(6X15)CSP						
	1	2	3	7	8	9
A	VSS	DQ31	VSSQ	VDDQ	DQ16	VDD
B	VDDQ	DQ29	DQ30	DQ17	DQ18	VSSQ
C	VSSQ	DQ27	DQ28	DQ19	DQ20	VDDQ
D	VDDQ	DQ25	DQ26	DQ21	DQ22	VSSQ
E	VSSQ	DQS3	DQ24	DQ23	DQS2	VDDQ
F	VDD	DM3	NC	A13	DM2	VSS
G	CKE	CK	$\overline{CK}$	$\overline{WE}$	$\overline{CAS}$	$\overline{RAS}$
H	A9	A11	A12	$\overline{CS}$	BA0	BA1
J	A6	A7	A8	A10/AP	A0	A1
K	A4	DM1	A5	A2	DM0	A3
L	VSSQ	DQS1	DQ8	DQ7	DQS0	VDDQ
M	VDDQ	DQ9	DQ10	DQ5	DQ6	VSSQ
N	VSSQ	DQ11	DQ12	DQ3	DQ4	VDDQ
P	VDDQ	DQ13	DQ14	DQ1	DQ2	VSSQ
R	VSS	DQ15	VSSQ	VDDQ	DQ0	VDD

Pin Names

CLK, $\overline{CLK}$	Differential Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQS0, DQS1 DQS2, DQS3	Data Strobe (Bidirectional)
A_0–A_{13}	Address Inputs

BA0, BA1	Bank Select
DQ_0–DQ_{31}	Data Input/Output
DM0, DM1 DM2, DM3	Data Mask
V_{DD}	Power (1.7V - 1.95V)
V_{SS}	Ground
V_{DDQ}	Power for I/O's (1.7V - 1.95V)
V_{SSQ}	Ground for I/O's

Signal Pin Description

Pin	Type	Signal	Polarity	Function
CLK $\overline{CLK}$	Input	Pulse	Positive Edge	The system clock input. All inputs except DQs and DMs are sampled on the rising edge of CLK.
CKE	Input	Level	Active High	Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiates either the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{CS}$	Input	Pulse	Active Low	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the command to be executed by the SDRAM.
A0 - A13	Input	Level	—	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, A10 is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10(=AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will be pre-charged simultaneously regardless of state of BA0 and BA1.
DQx	Input/ Output	Level		Data Input/Output pins operate in the same manner as conventional DRAMs.
BA0, BA1	Input	Level	—	Selects which bank is to be active.
DQS0,DQS1 DQS2,DQS3	Input/ Output	Level	—	Data Strobes : Output with read data, input with write data. Edge-aligned with read data, centered in write data. it is used to fetch write data. For the x32, DQS0 corresponds to the data on DQ0-DQ7; DQS1 corresponds to the data on DQ8-DQ15, DQS2 corresponds to the data on DQ16-DQ23, DQS3 corresponds to the data on DQ24-DQ31
DM0,DM1 DM2,DM3	Input	Pulse	Active High	Input Data Mask : DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. DM pins include dummy loading inter-nally, to match the DQ and DQS loading. For the x32, DM0 corresponds to the data on DQ0-DQ7; DM1 corresponds to the data on DQ8-DQ15, DM2 corresponds to the data on DQ16-DQ23, DM3 corresponds to the data on DQ24-DQ31
VDD, VSS	Supply			Power and ground for the input buffers and the core logic.
VDDQ,VSSQ	Supply	—	—	Isolated power supply and ground for the output buffers to provide improved noise immunity.

Mode Register Set

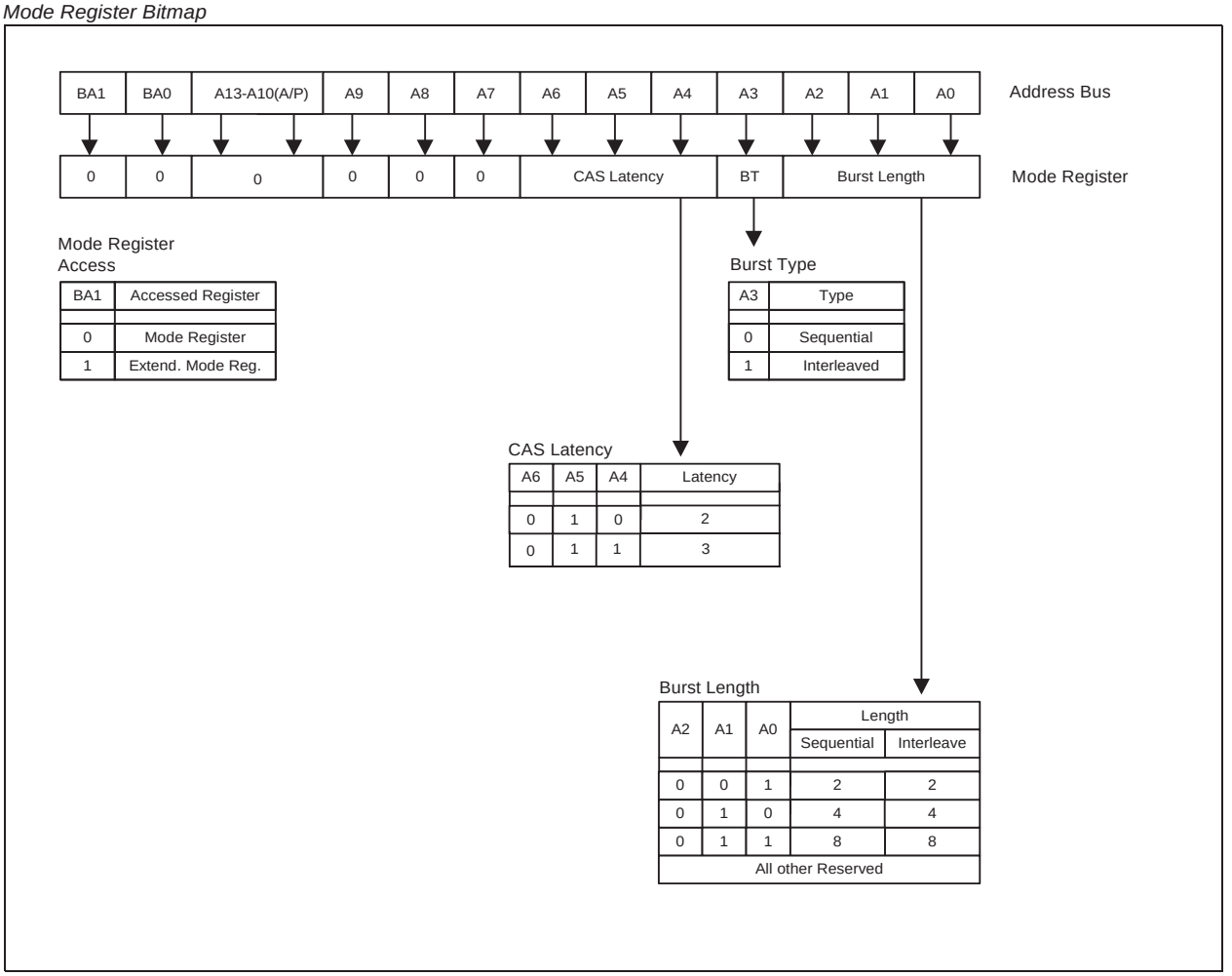
The mode register stores the data for controlling the various operating modes of the mobile DDR, includes CAS latency, addressing mode, burst length, test mode, and various vendor specific options. The default value of the mode register is not defined. Therefore the mode register must be written after power up to operate the mobile DDR. The device should be activated with the CKE already high prior to writing into the Mode Register.

The Mode Register is written by using the MRS command. The state of the address signals registered in the same cycle as MRS command is written in the mode register. The value can be changed as long as all banks are in the idle state.

The mode register is divided into various fields depending on functionality. The burst length uses A2.. A0, CAS latency (read latency from column address) uses A6.. A4. BA0 must be set to low for normal operation. A9.. A13 is reserved for future use.

BA1 selects Extended Mode Register Setup operation when set to 1. Refer to the table for specific codes for various burst length, addressing modes and CAS latencies.

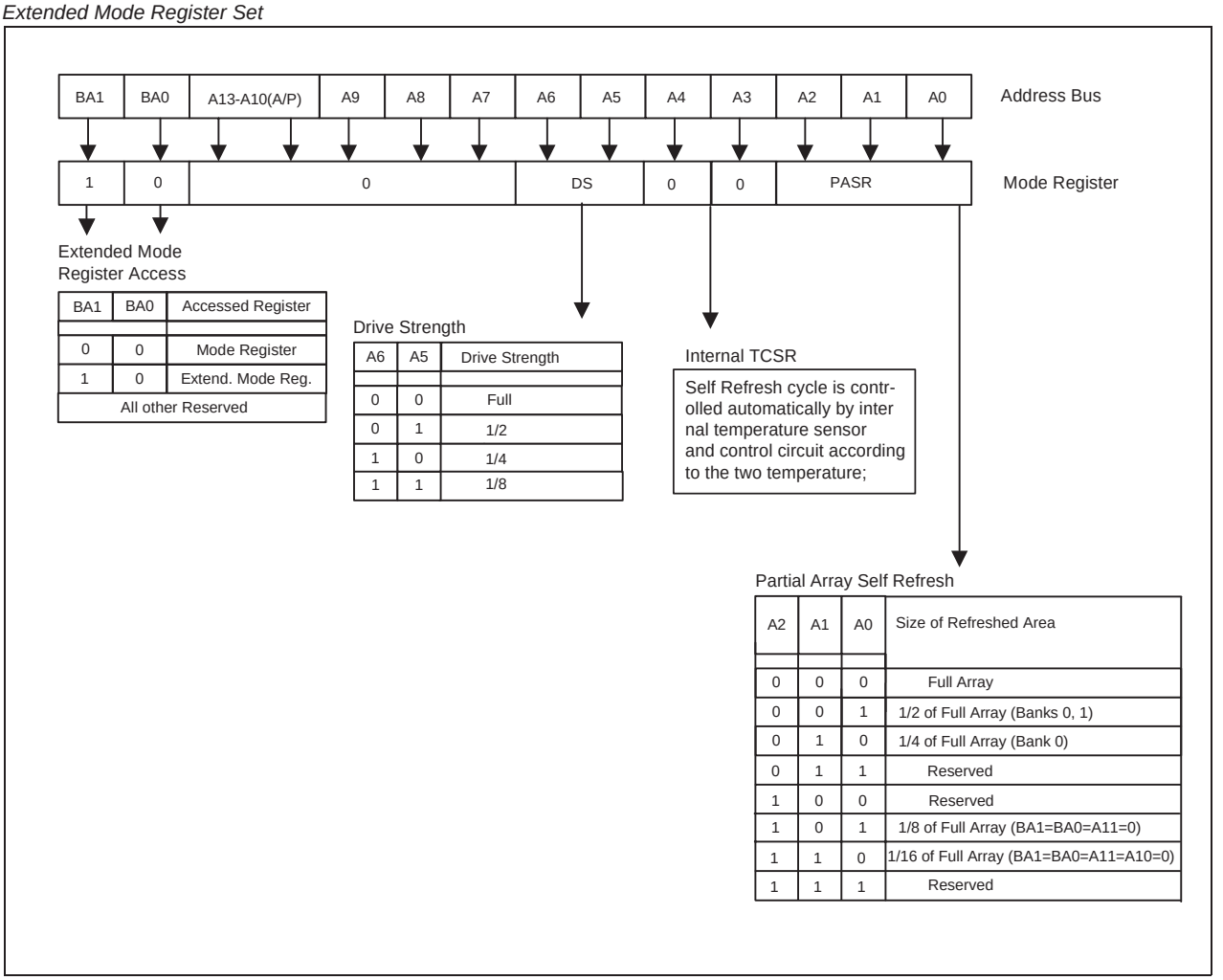
Mode Register Bitmap



EMRS

The Extended Mode Register is responsible for setting the Drive strength options and Partial array Self Refresh. The EMRS can be programmed by performing a normal Mode Register Setup operation and setting the BA1=1 and BA0=0. In order to save power consumption, the mobile DDR Sdram has five (PASR) options: Full array, 1/2, 1/4 ,1/8, 1/16 of Full Array. Additionally, the device has internal temperature sensor to control self refresh cycle atuomatically according to the two temperature range; Max. 40 deg C, and Max. 85 deg C. This is the device internal Temperature Compensated Self Refresh(TCSR). The device has four drive strength options: Full, 1/2, 1/4 or 1/8.

Extended Mode Register Set



BA1	BA0	Accessed Register
0	0	Mode Register
1	0	Extend. Mode Reg.
All other Reserved		

A6	A5	Drive Strength
0	0	Full
0	1	1/2
1	0	1/4
1	1	1/8

A2	A1	A0	Size of Refreshed Area
0	0	0	Full Array
0	0	1	1/2 of Full Array (Banks 0, 1)
0	1	0	1/4 of Full Array (Bank 0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	1/8 of Full Array (BA1=BA0=A11=0)
1	1	0	1/16 of Full Array (BA1=BA0=A11=A10=0)
1	1	1	Reserved

Signal and Timing Description

General Description

The 2G bit mobile DDR is a 256M byte mobile DDR SDRAM. It consists of four banks. Each bank is organized as 16384 rows x 1024 columns x 32 bits.
Read and Write accesses are burst oriented. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address bits registered coincident with the Activate command are used to select the bank and the row to be accessed. BA1 and BA0 select the bank, address bits A13.. A0 select the row. Address bits A9.. A0 registered coincident with the Read or Write command are used to select the starting column location for the burst access.

The regular Single Data Rate SDRAM read and write cycles only use the rising edge of the external clock input. For the mobile SDRAM the special signals DQSx (Data Strobe) are used to mark the data valid window. During read bursts, the data valid window coincides with the high or low level of the DQSx signals. During write bursts, the DQSx signal marks the center of the valid data window. Data is available at every rising and falling edge of DQSx, therefore the data transfer rate is doubled.
For Read accesses, the DQSx signals are aligned to the clock signal CLK.

Special Signal Description

Clock Signal

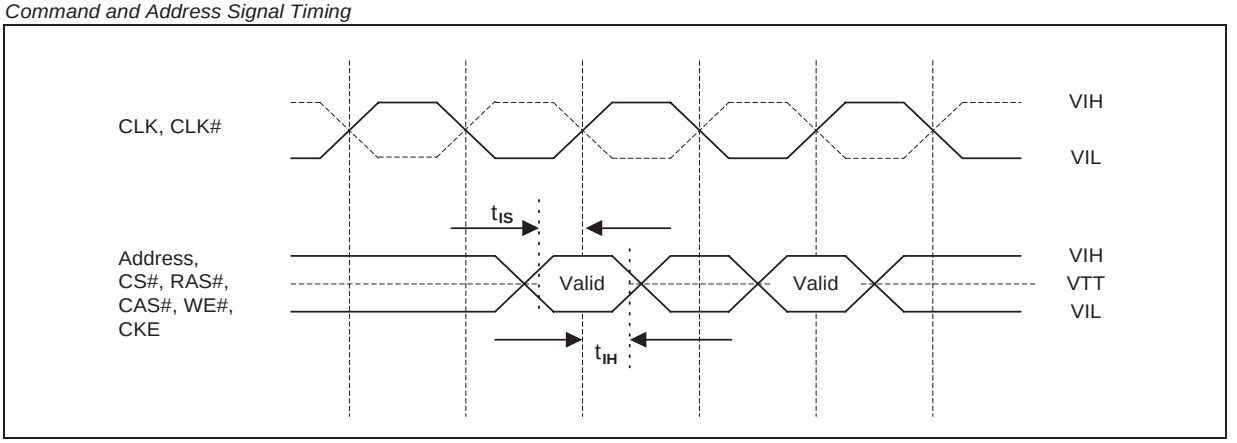
The mobile DDR operates with a differential clock (CLK and $\overline{CLK}$) input. CLK is used to latch the address and command signals. Data input and DMx signals are latched with DQSx. The minimum and maximum clock cycle time is defined by t_{CK}.

The minimum and maximum clock duty cycle are specified using the minimum clock high time t_{CH} and the minimum clock low time t_{CL} respectively.

Command Inputs and Addresses

Like single data rate SDRAMs, each combination of $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ input in conjunction with $\overline{CS}$ input at a rising edge of the clock determines a mobile DDR command.

Command and Address Signal Timing



Data Strobe and Data Mask

Operation at Burst Reads

The Data Strobes provide a 3-state output signal to the receiver circuits of the controller during a read burst. The data strobe signal goes 1 clock cycle low before data is driven by the mobile DDR and then toggles low to high and high to low till the end of the burst. CAS latency is specified to the first low to high transition. The edges of the Output Data signals and the edges of the data strobe signals during a read are nominally coincident with edges of the input clock.
The tolerance of these edges is specified by the parameters t_{AC} and t_{DQSCK} and is referenced to the crossing point of the CLK and /CLK signal. The t_{DQSQ} timing parameter describes the skew between the data strobe edge and the output data edge.

The following table summarizes the mapping of DQS0 ~ DQS3 and DM0 ~ DM3 signals to the data bus.

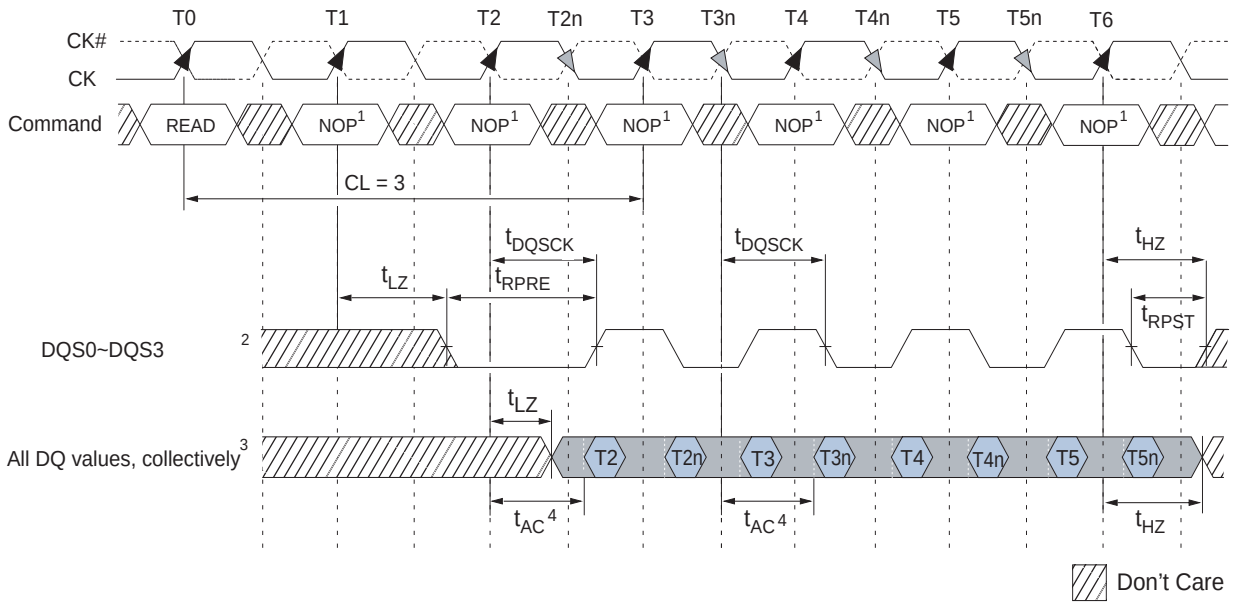
Mapping of DQS0~DQS3 and DM0~DM3

Data strobe signal	Data mask signal	Controlled data bus
DQS0	DM0	DQ7 .. DQ0
DQS1	DM1	DQ8 .. DQ15
DQS2	DM2	DQ16 .. DQ23
DQS3	DM3	DQ24 .. DQ31

The minimum time during which the output data is valid is critical for the receiving device. This also applies to the Data Strobe DQS during a read since it is tightly coupled to the output data. The parameters t_{QH} and t_{DQSQ} define the minimum output data valid window. Prior to a burst of read data, given that the device is not currently in burst read mode, the data strobe signals transit from Hi-Z to a valid logic low. This is referred to as the data strobe “read preamble” t_{RPRE}. This transition happens one clock prior to the first edge of valid data.

Once the burst of read data is concluded, given that no subsequent burst read operation is initiated, the data strobe signals transit from a valid logic low to Hi-Z. This is referred to as the data strobe “read postamble” t_{RPST}.

Data Output Timing - t_{AC} and t_{DQSCK}

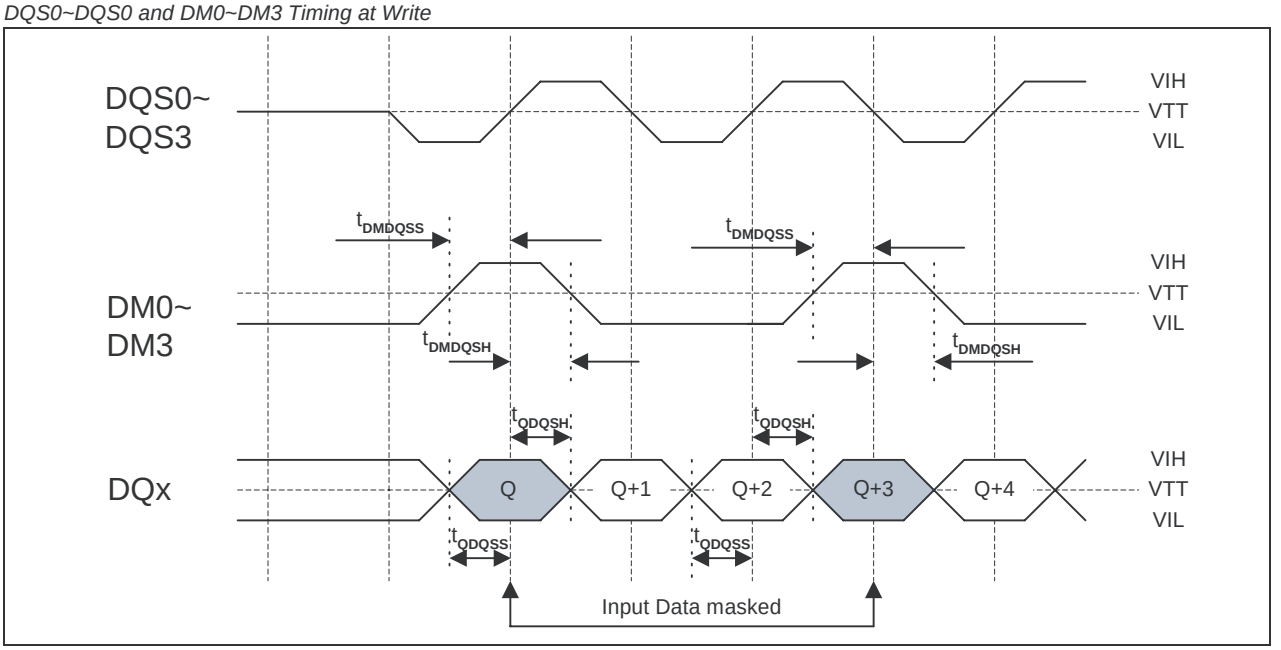


Notes:
1. Commands other than NOP can be valid during this cycle.
2. DQ transitioning after DQS transitions define t_{DQSQ} window.
3. All DQ must transition by t_{DQSQ} after DQS transitions, regardless of t_{AC}.
4. t_{AC} is the DQ output window relative to CK and is the long-term component of DQ skew.

Operation at Burst Write

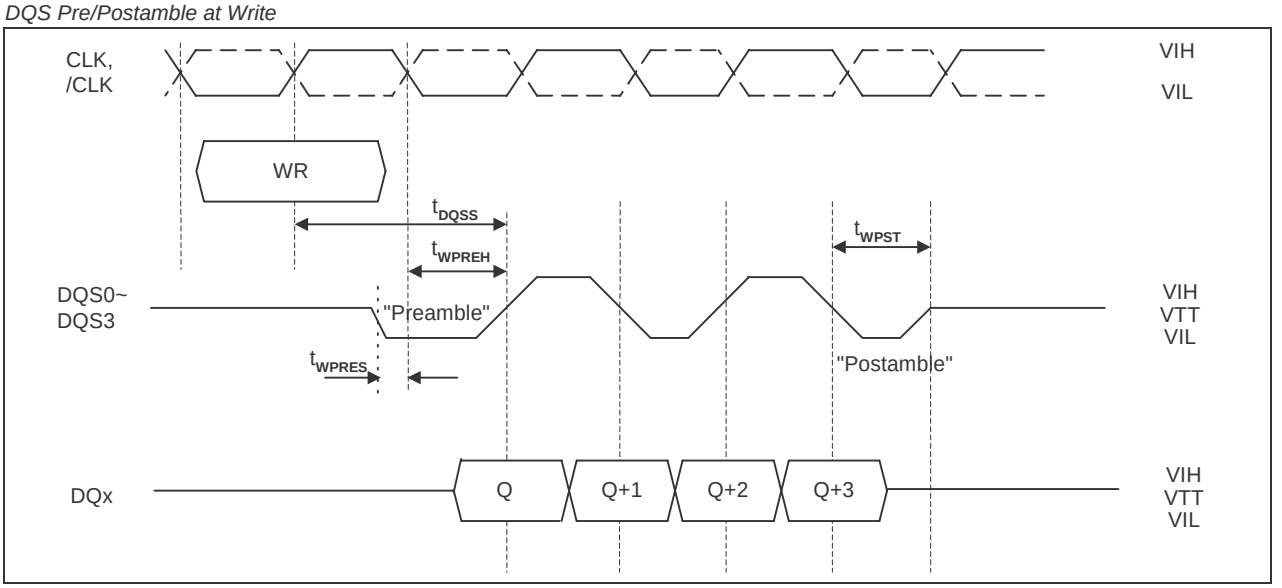
During a write burst, control of the data strobe is driven by the memory controller. The DQS0~DQS3 signals are centered with respect to data and data mask. The tolerance of the data and data mask edges versus the data strobe edges during writes are specified by the setup and hold time parameters of data (t_{QDQSS} & t_{QDQSH}) and data mask (t_{DMDQSS} & t_{DMDQSH}). The input data is masked in the same cycle when the corresponding DM0~DM3 signal is high (i.e. the DM0~DM3 mask to write latency is zero.)

DQS0~DQS0 and DM0~DM3 Timing at Write



Prior to a burst of write data, given that the controller is not currently in burst write mode, the data strobe signal DQS0~DQS3 changes from Hi-Z to a valid logic low. This is referred to as the data strobe Write Preamble. Once the burst of write data is concluded, given no subsequent burst write operation is initiated, the data strobe signal DQS0~DQS3 transits from a valid logic low to Hi-Z. This is referred the data strobe Write Postamble, t_{WPST}. For mobile DDR data is written with a delay which is defined by the parameter t_{DQSS}, write latency). This is different than the single data rate SDRAM where data is written in the same cycle as the Write command is issued.

DQS Pre/Postamble at Write

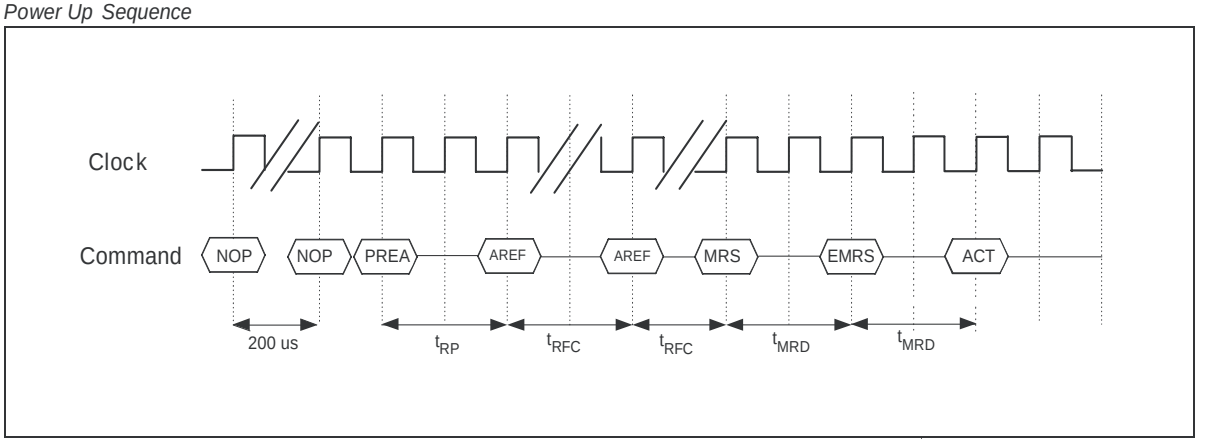


Power-Up Sequence

The following sequence is highly recommended for Power-Up :

1. Apply power and start clock. Maintain CKE and the other pins are in NOP conditions at the input
2. Apply V_{DD} before or at the same time as V_{DDQ}, apply V_{DDQ} before or at the same time as V_{REF}, V_{TT}
3. Start clock, maintain stable conditions for 200 us
4. Apply NOP and set CKE to high
5. Apply All Bank Precharge command
6. Issue Auto Refresh command twice and must satisfy minimum t_{RFC}
7. Issue MRS (Mode Register Set command)
8. Issue a EMRS (Extended Mode Register Set command), not necessary

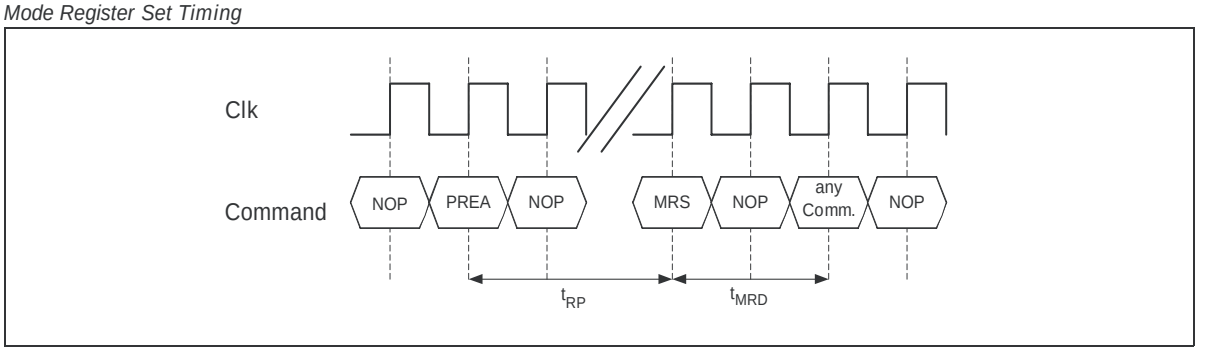
Power Up Sequence



Mode Register Set Timing

The mobile DDR should be activated with CKE already high prior to writing into the mode register. Two clock cycles are required complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state.

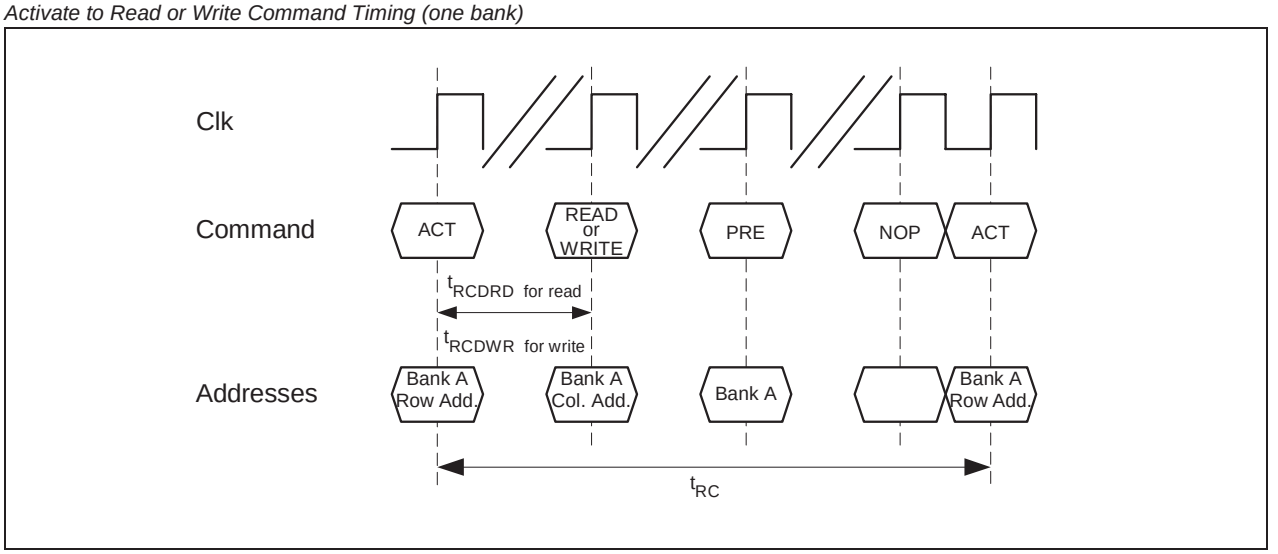
Mode Register Set Timing



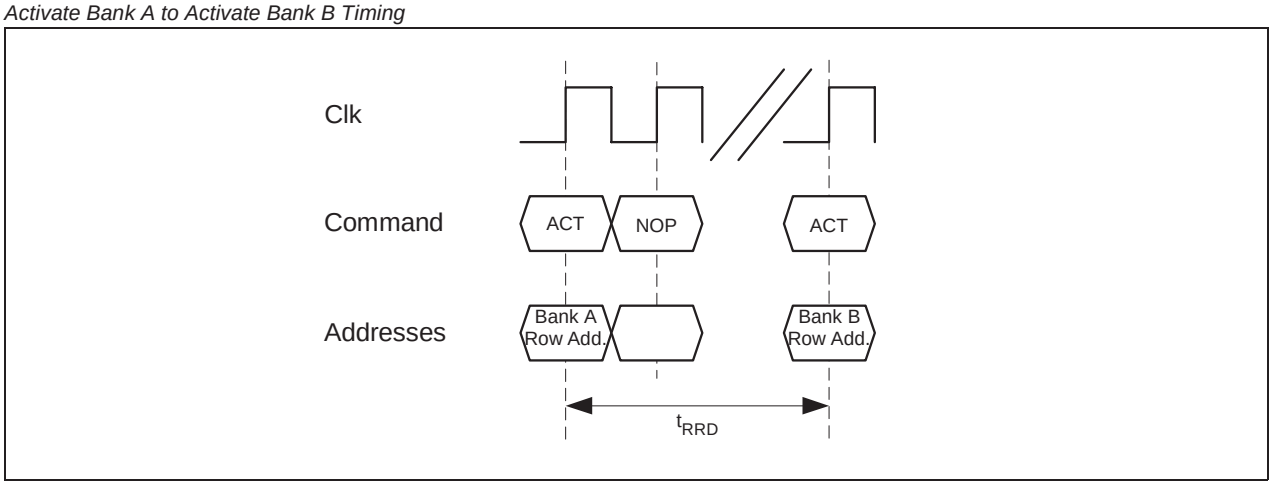
Bank Activation Command (ACT)

The Bank Activation command is initiated by issuing an ACT command at the rising edge of the clock. The mobile DDR has 4 independent banks which are selected by the two Bank select Addresses (BA0, BA1). The Bank Activation command must be applied before any Read or Write operation can be executed. The delay from the Bank Activation command to the first read or write command must meet or exceed the minimum of RAS to CAS delay time (t_{RCDRD} min. for read commands and t_{RCDWR} min. for write commands). Once a bank has been activated, it must be precharged before another Bank Activate command can be applied to the same bank. The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank to Bank activation delay time (t_{RRD} min).

Activate to Read or Write Command Timing (one bank)



Activate Bank A to Activate Bank B Timing



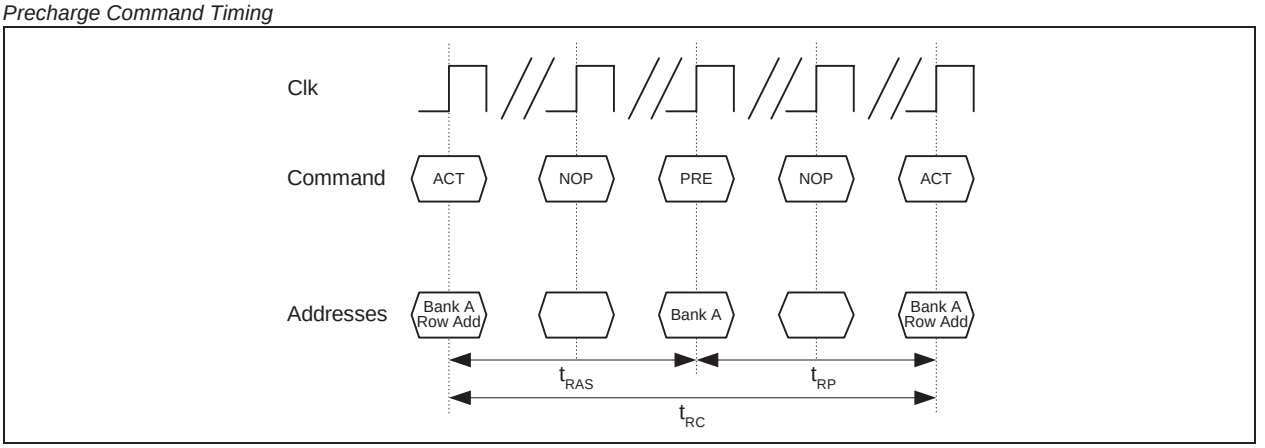
Precharge Command

This command is used to precharge or close a bank that has been activated. Precharge is initiated by issuing a Precharge command at the rising edge of the clock. The Precharge command can be used to precharge each bank respectively or all banks simultaneously. The Bank addresses BA0 and BA1 select the bank to be precharged. After a Precharge command, the analog delay t_{RP} has to be met until a new Activate command can be initiated to the same bank.

Table
Precharge Control

A10/ AP	BA1	BA0	Precharged
0	0	0	Bank A Only
0	0	1	Bank B Only
0	1	0	Bank C Only
0	1	1	Bank D Only
1	X	X	All Banks

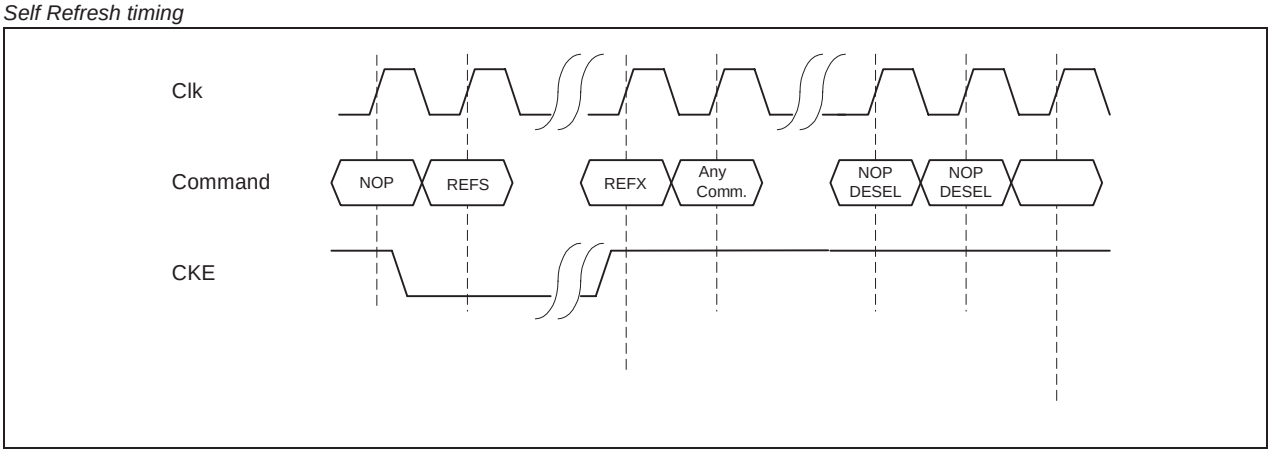
Precharge Command Timing



Self Refresh

The Self Refresh mode can be used to retain the data in the mobile DDR if the chip is powered down. To set the mobile DDR into a Self Refreshing mode, a Self Refresh command must be issued and CKE held low at the rising edge of the clock. Once the Self Refresh command is initiated, CKE must stay low to keep the device in Self Refresh mode. During the Self Refresh mode, all of the external control signals are disabled except CKE. The clock is internally disabled during Self Refresh operation to reduce power. An internal timing generator guarantees the self refreshing of the memory content.

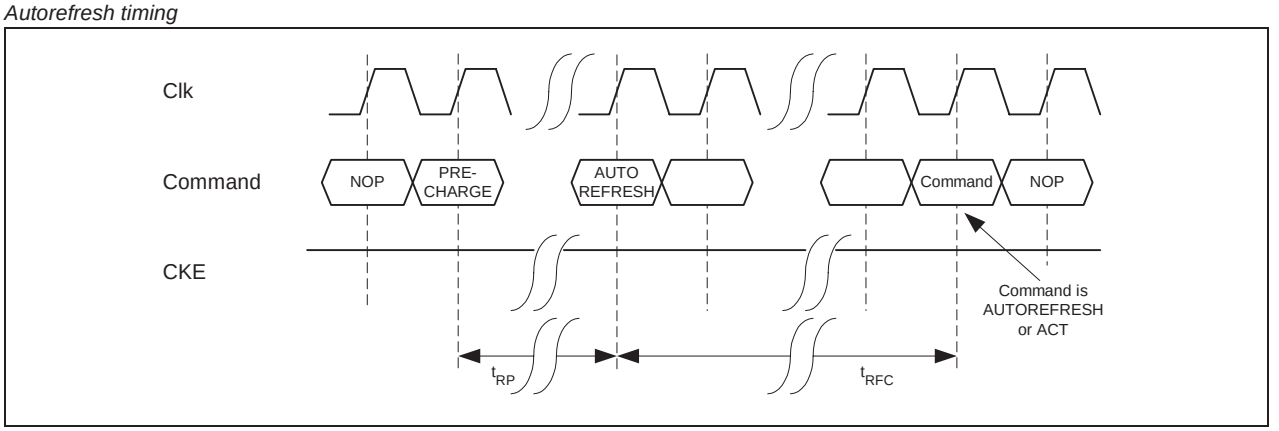
Self Refresh timing



Auto Refresh

The auto refresh function is initiated by issuing an Auto Refresh command at the rising edge of the clock. All banks must be precharged and idle before the Auto Refresh command is applied. No control of the external address pins is required once this cycle has started. All necessary addresses are generated in the device itself. When the refresh cycle has completed, all banks will be in the idle state. A delay between the Auto Refresh command and the next Activate Command or subsequent Auto Refresh Command must be greater than or equal to the t_{RFC}(min).

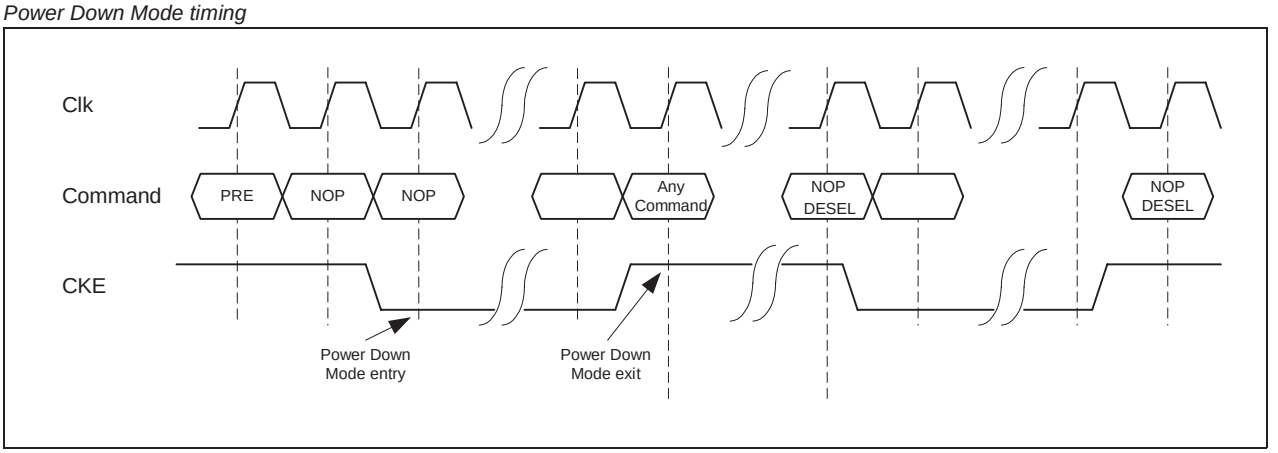
Autorefresh timing



Power Down Mode

The Power Down Mode is entered when CKE is set low and exited when CKE is set high. The CKE signal is sampled at the rising edge of the clock. Once the Power Down Mode is initiated, all of the receiver circuits except CLK and the CKE circuits are gated off to reduce power consumption. All banks can be set to idle state or stay activate during Power Down Mode, but burst activity may not be performed. After exiting from Power Down Mode, at least one clock cycle of command delay must be inserted before starting a new command. During Power Down Mode, refresh operations cannot be performed; therefore, the device cannot remain in Power Down Mode longer than the refresh period (t_{REF}) of the device.

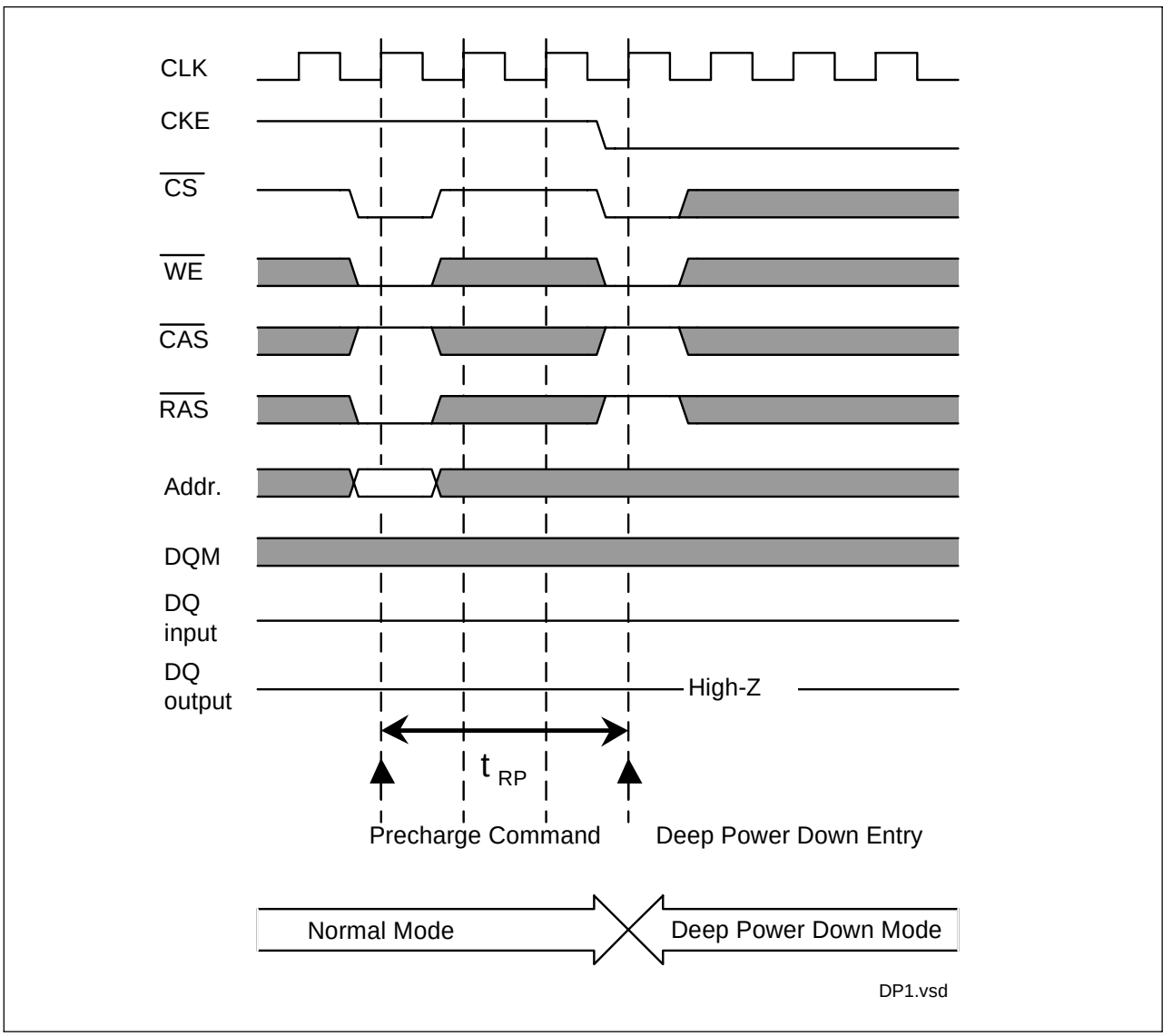
Power Down Mode timing



Deep Power Down Mode

The Deep Power Down mode is an unique function with very low standby currents. All internal volatge generators inside the mobile DDR are stopped and all memory data is lost in this mode. To enter the Deep Power Down mode all banks must be precharged.

Deep Power Down Mode Entry



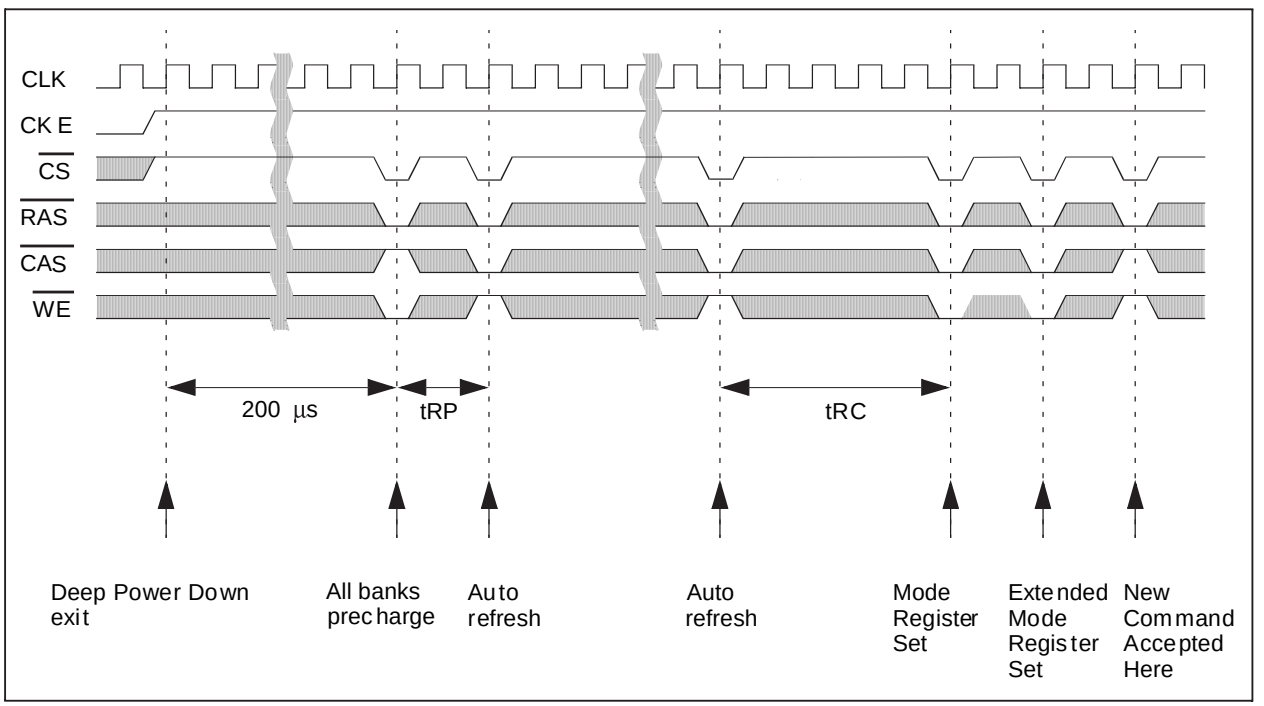
The deep power down mode has to be maintained for a minimum of 100µs.

Deep Power Down Exit

The deep power down mode is exited by asserting CKE high.

After the exit, the following sequence is needed to enter a new command :

1. Maintain NOP input conditions for a minimum of 200 us
2. Issue precharge commands for all banks of the device
3. Issue two or more auto refresh commands and satisfy minimum t_{RFC}
4. Issue a mode register set command to initialize the mode register
5. Issue an extended mode register set command to initialize the extende mode register



Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to the memory (write cycle) or from the memory (read cycle). The burst length is programmable and set by address bits A0 - A3 during the Mode Register Setup command. The burst length controls the number of words that will be output after a read command or the number of words to be input after a write command. One word is 32 bits wide. The sequential burst length can be set to 2, 4, 8 or 16 data words.

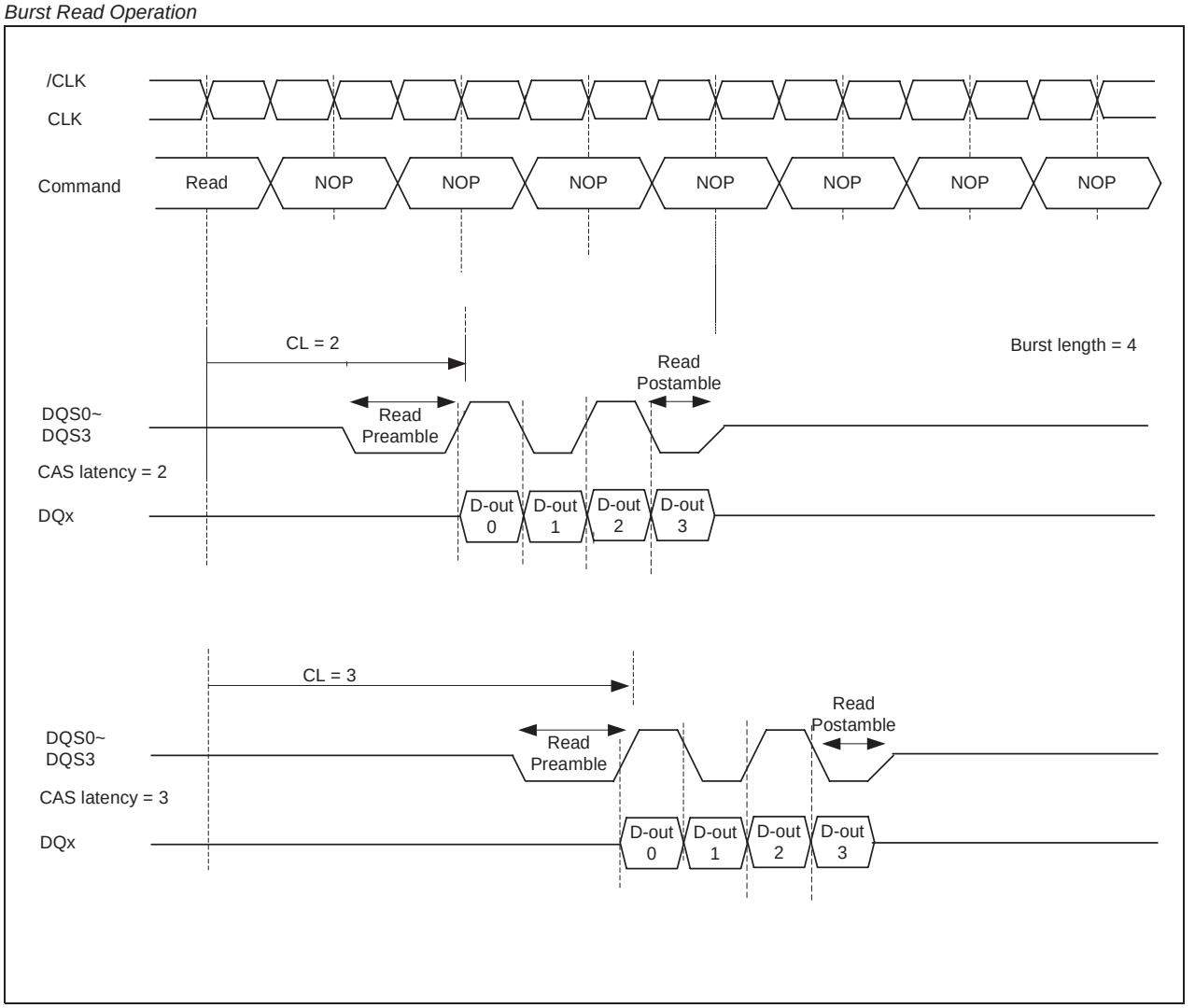
Burst Mode and Sequence

Burst Length	Starting Column Address				Order of Access within a Burst	
	A3	A2	A1	A0	Type = Sequential	Type = Interleaved
2				0	0 - 1	0 - 1
				1	1 - 0	1 - 0
4			0	0	0 - 1 - 2 - 3	0 - 1 - 2 - 3
			0	1	1 - 2 - 3 - 0	1 - 0 - 3 - 2
			1	0	2 - 3 - 0 - 1	2 - 3 - 0 - 1
			1	1	3 - 0 - 1 - 2	3 - 2 - 1 - 0
8		0	0	0	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7
		0	0	1	1 - 2 - 3 - 4 - 5 - 6 - 7 - 0	1 - 0 - 3 - 2 - 5 - 4 - 7 - 6
		0	1	0	2 - 3 - 4 - 5 - 6 - 7 - 0 - 1	2 - 3 - 0 - 1 - 6 - 7 - 4 - 5
		0	1	1	3 - 4 - 5 - 6 - 7 - 0 - 1 - 2	3 - 2 - 1 - 0 - 7 - 6 - 5 - 4
		1	0	0	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3
		1	0	1	5 - 6 - 7 - 0 - 1 - 2 - 3 - 4	5 - 4 - 7 - 6 - 1 - 0 - 3 - 2
		1	1	0	6 - 7 - 0 - 1 - 2 - 3 - 4 - 5	6 - 7 - 4 - 5 - 2 - 3 - 0 - 1
		1	1	1	7 - 0 - 1 - 2 - 3 - 4 - 5 - 6	7 - 6 - 5 - 4 - 3 - 2 - 1 - 0
16	0	0	0	0	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F
	0	0	0	1	1-2-3-4-5-6-7-8-9-A-B-C-D-E-F-0	1-0-3-2-5-4-7-6-9-8-B-A-D-C-F-E
	0	0	1	0	2-3-4-5-6-7-8-9-A-B-C-D-E-F-0-1	2-3-0-1-6-7-4-5-A-B-8-9-E-F-C-D
	0	0	1	1	3-4-5-6-7-8-9-A-B-C-D-E-F-0-1-2	3-2-1-0-7-6-5-4-B-A-9-8-F-E-D-C
	0	1	0	0	4-5-6-7-8-9-A-B-C-D-E-F-0-1-2-3	4-5-6-7-0-1-2-3-C-D-E-F-8-9-A-B
	0	1	0	1	5-6-7-8-9-A-B-C-D-E-F-0-1-2-3-4	5-4-7-6-1-0-3-2-D-C-F-E-9-8-B-A
	0	1	1	0	6-7-8-9-A-B-C-D-E-F-0-1-2-3-4-5	6-7-4-5-2-3-0-1-E-F-C-D-A-B-8-9
	0	1	1	1	7-8-9-A-B-C-D-E-F-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0-F-E-D-C-B-A-9-8
	1	0	0	0	8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7	8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7
	1	0	0	1	9-A-B-C-D-E-F-0-1-2-3-4-5-6-7-8	9-8-B-A-D-C-F-E-1-0-3-2-5-4-7-6
	1	0	1	0	A-B-C-D-E-F-0-1-2-3-4-5-6-7-8-9	A-B-8-9-E-F-C-D-2-3-0-1-6-7-4-5
	1	0	1	1	B-C-D-E-F-0-1-2-3-4-5-6-7-8-9-A	B-A-9-8-F-E-D-C-3-2-1-0-7-6-5-4
	1	1	0	0	C-D-E-F-0-1-2-3-4-5-6-7-8-9-A-B	C-D-E-F-8-9-A-B-4-5-6-7-0-1-2-3
	1	1	0	1	D-E-F-0-1-2-3-4-5-6-7-8-9-A-B-C	D-C-F-E-9-8-B-A-5-4-7-6-1-0-3-2
	1	1	1	0	E-F-0-1-2-3-4-5-6-7-8-9-A-B-C-D	E-F-C-D-A-B-8-9-6-7-4-5-2-3-0-1
	1	1	1	1	F-0-1-2-3-4-5-6-7-8-9-A-B-C-D-E	F-E-D-C-B-A-9-8-7-6-5-4-3-2-1-0

Burst Read Operation: (READ)

The Burst Read operation is initiated by issuing a READ command at the rising edge of the clock after t_{RCD} from the bank activation. The address inputs (A8.. A0) determine the starting address for the burst. The burst length (2, 4 or 8) must be defined in the Mode Register. The first data after the READ command is available depending on the CAS latency. The subsequent data is clocked out on the rising and falling edge of DQS0~DQS3 until the burst is completed. The DQS0~DQS3 signals are generated by the mobile DDR during the Burst Read Operation.

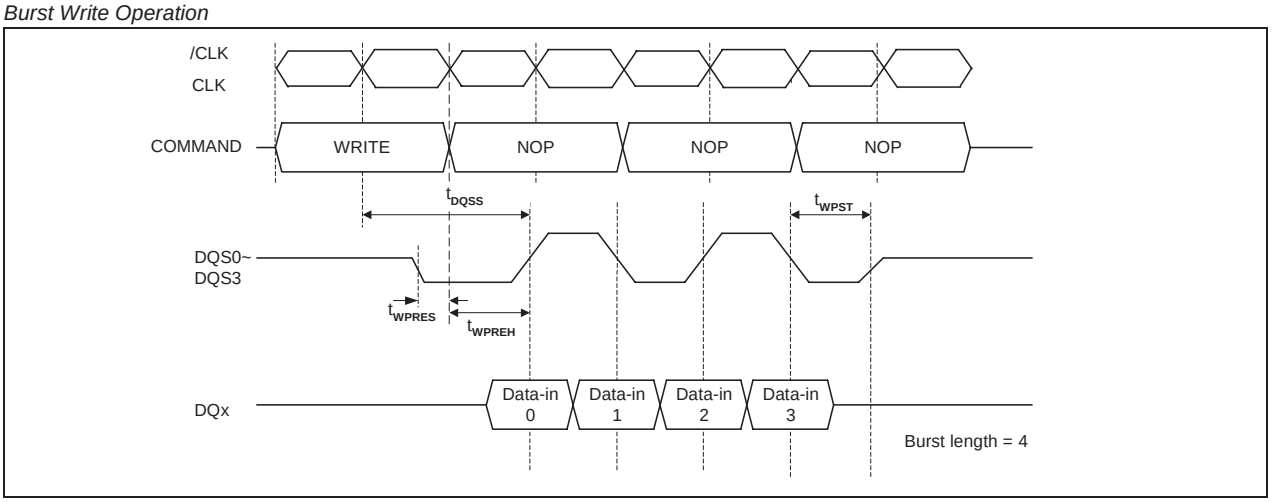
Burst Read Operation



Burst Write Operation (WRITE)

The Burst Write is initiated by issuing a WRITE command at the rising edge of the clock. The address inputs (A9 .. A0) determine starting column address. Data for the first burst write cycle must be applied on the DQ pins on the first rise edge of DQS0~DQS3 follow WRITE command. The time between the WRITE command and the first corresponding edge of the data strobe is t_{DQSS}. The remaining data inputs must be supplied on each subsequent rising and falling edge of the data strobe until the burst length is completed. When the burst has been finished, any additional data supplied to the DQ pins will be ignored.

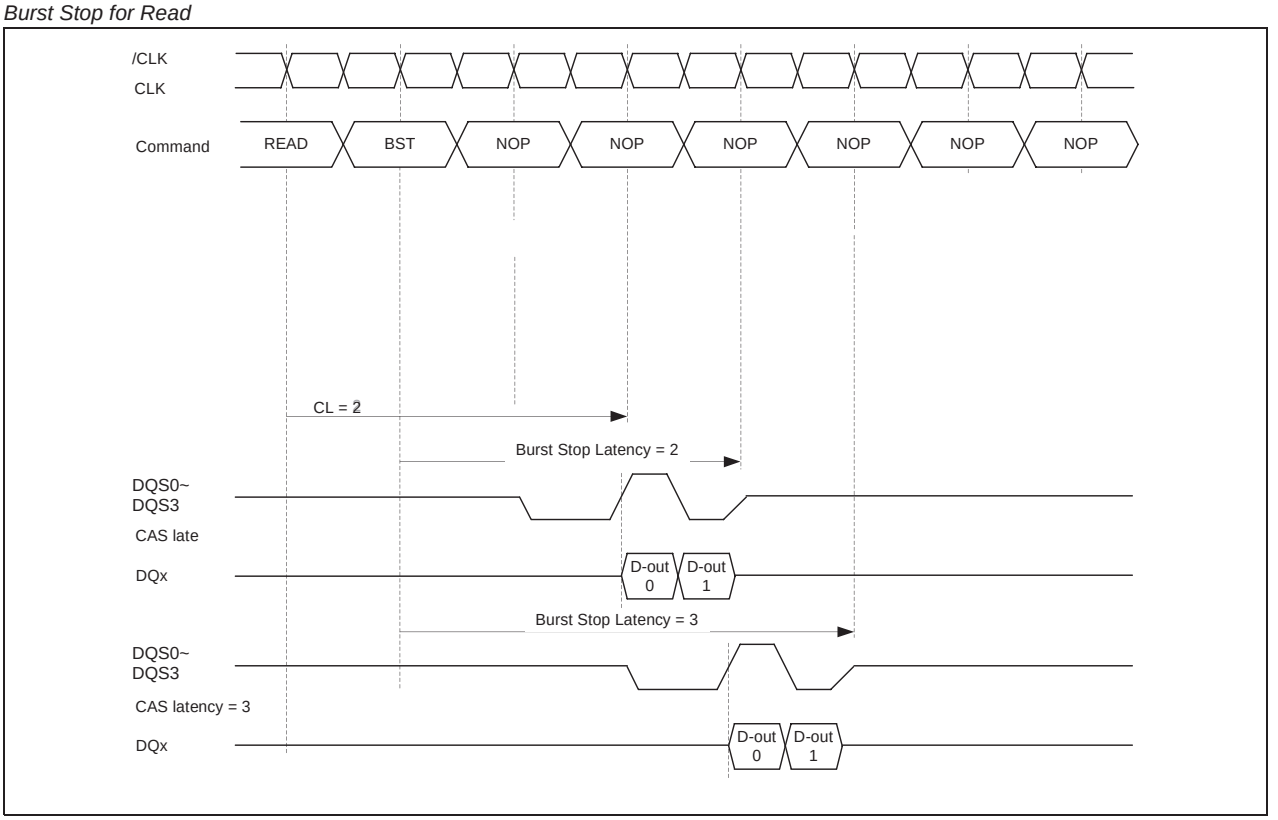
Burst Write Operation



Burst Stop Command (BST)

A Burst Stop is initiated by issuing a BURST STOP command at the rising edge of the clock. The Burst Stop Command has the fewest restrictions, making it the easiest method to terminate a burst operation before it has been completed. When the Burst Stop Command is issued during a burst read cycle, read data and LDQS, UDQS go to a high-Z state after a delay which is equal to the CAS latency set in the Mode Register. The Burst Stop latency is equal to the CAS latency CL.The Burst Stop command is not supported during a write burst operation. Burst Stop is also illegal during Read with Auto-Precharge.

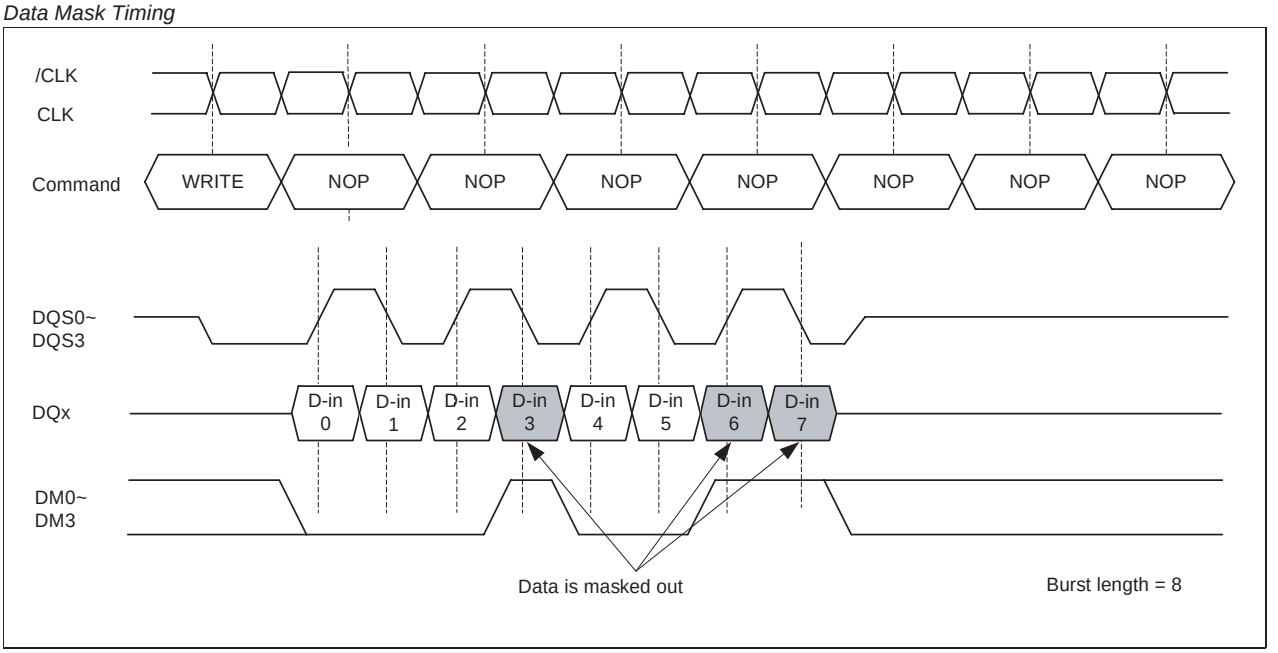
Burst Stop for Read



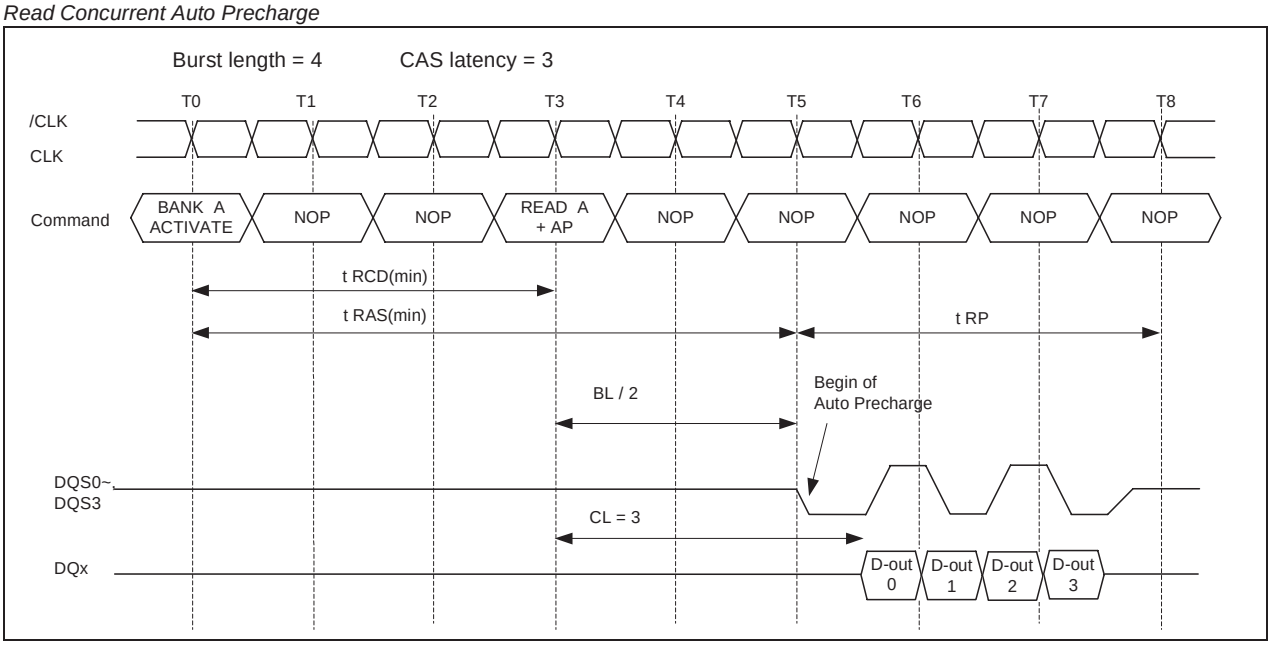
Data Mask (DM0 ~ DM3) Function

The mobile DDR has a Data Mask function that can be used only during write cycles. When the Data Mask is activated, active high during burst write, the write operation is masked immediately. The DM0~DM3 to data-mask latency zero. DM0~DM3 can be issued at the rising or negative edge of Data Strobe.

Data Mask Timing



Read Concurrent Auto Precharge



Concurrent Read Auto Precharge Support

Asserted Command	For same Bank			For different Bank		
	T4	T5	T6	T4	T5	T6
READ	NO	NO	NO	NO	YES	YES
READ+AP	YES	YES	NO	NO	YES	YES
ACTIVATE	NO	NO	NO	YES	YES	YES
PRECHARGE	YES	YES	NO	YES	YES	YES

Note: This table is for the case of Burst Length = 4, CAS Latency =3 and t_{WR}=2 clocks

When READ with Auto Precharge is asserted, new commands can be asserted at T4,T5 and T6 as shown in Table

An Interrupt of a running READ burst with Auto Precharge i.e. at T4 and T5 to the same bank with another READ+AP command is allowed, it will extend the begin of the internal Precharge operation to the last READ+AP command.

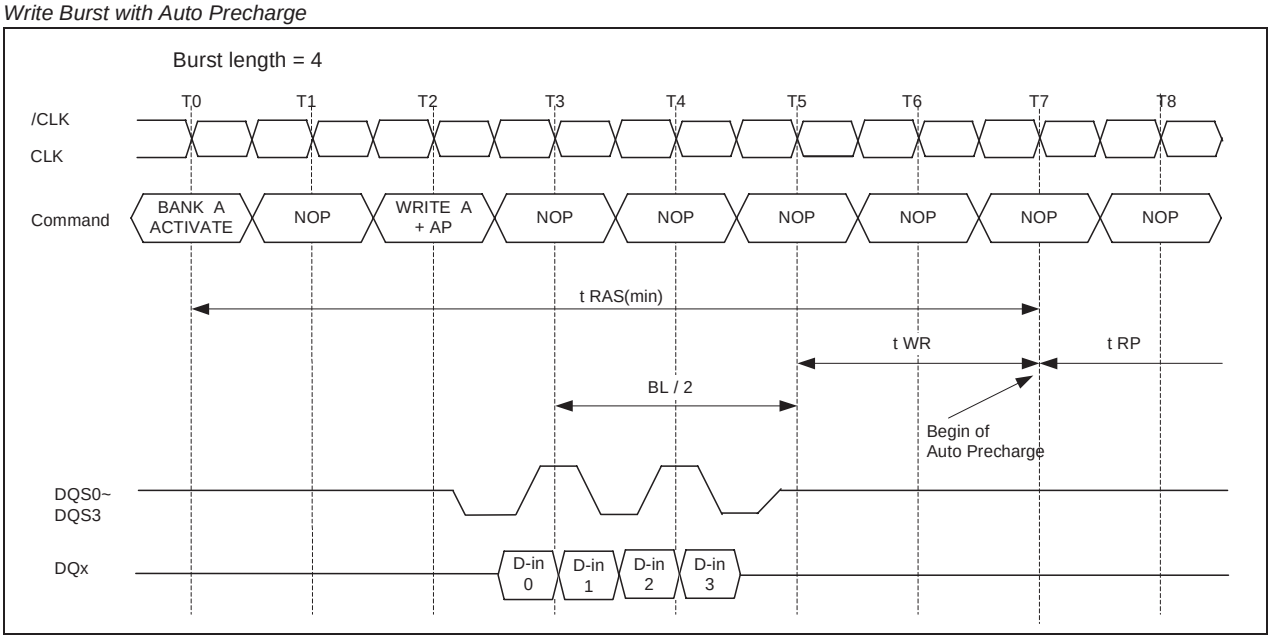
Interrupts of a running READ burst with Auto Precharge i.e. at T4 are not allowed when doing concurrent command to another active bank. ACTIVATE or PRECHARGE commands to another bank are always possible while a READ with Auto Precharge operation is in progress.

Write with Autoprecharge (WRITEA)

If A8 is high when a Write command is issued, the Write with Auto-Precharge function is performed. The internal precharge begins after the write recovery time t_{WR} and t_{RAS}(min) are satisfied.

If a Write with Auto Precharge command is initiated, the mobile DDR automatically enters the precharge operation at the first rising edge of CLK after the last valid edge of DQS (completion of the burst) plus the write recovery time t_{WR}. Once the precharge operation has started, the bank cannot be reactivated and the new command can not be asserted until the Precharge time (t_{RP}) has been satisfied. If t_{RAS}(min) has not been satisfied yet, an internal interlock will delay the precharge operation until it is satisfied.

Write Burst with Auto Precharge



Note: t_{WR} starts at the first rising edge of clock after the last valid edge of the 4 DQSx.

Table
Concurrent Write Auto Precharge Support

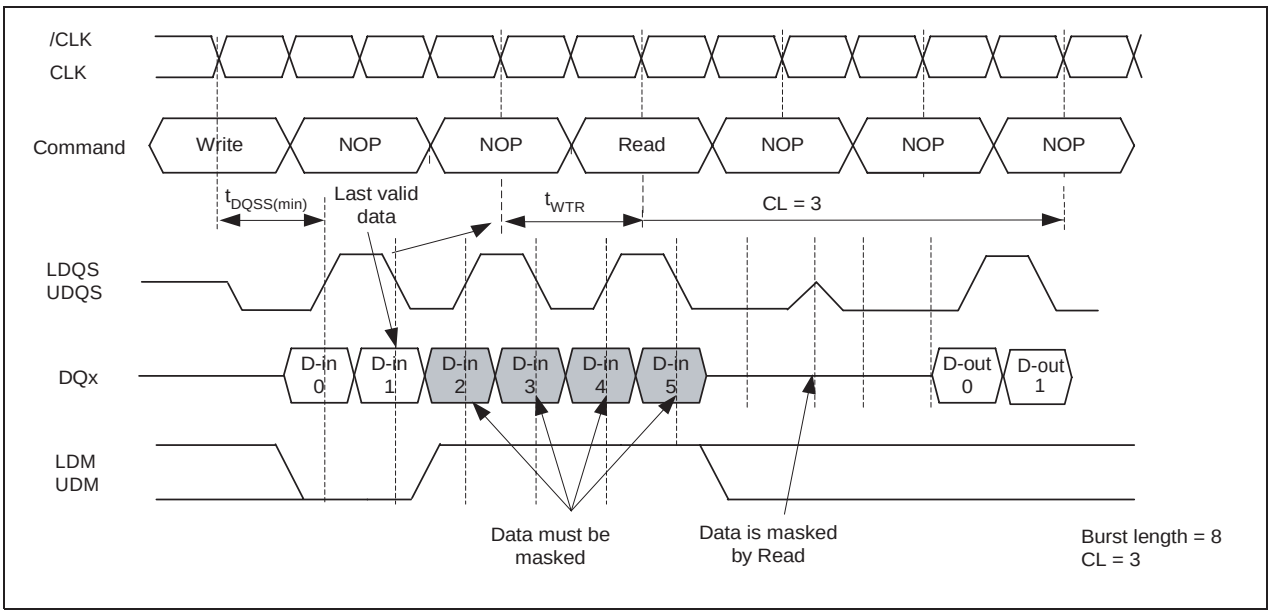
Asserted Command	For same Bank						For different Bank				
	T3	T4	T5	T6	T7	T8	T3	T4	T5	T6	T7
WRITE	NO	NO	NO	NO	NO	NO	NO	YES	YES	YES	YES
WRITE+AP	YES	NO	NO	NO	NO	NO	NO	YES	YES	YES	YES
READ	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	YES
READ+AP	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	YES
ACTIVATE	NO	NO	NO	NO	NO	NO	YES	YES	YES	YES	YES
PRECHARGE	NO	NO	NO	NO	NO	NO	YES	YES	YES	YES	YES

When Write with Auto Precharge is asserted, new commands can be asserted at T3.. T8 as shown in Table .

An Interrupt of a running WRITE burst with Auto Precharge i.e. at T3 to the same bank with another WRITE+AP command is allowed as long as the burst is running, it will extend the begin of the internal Precharge operation to the last WRITE+AP command.

Interrupts of a running WRITE burst with Auto Precharge i.e. at T3 are not allowed when doing concurrent WRITE's to another active bank. Consecutive WRITE or WRITE+AP bursts (T4.. T7) to other open banks are possible. ACTIVATE or PRECHARGE commands to another bank are always possible while a WRITE with Auto Precharge operation is in progress.

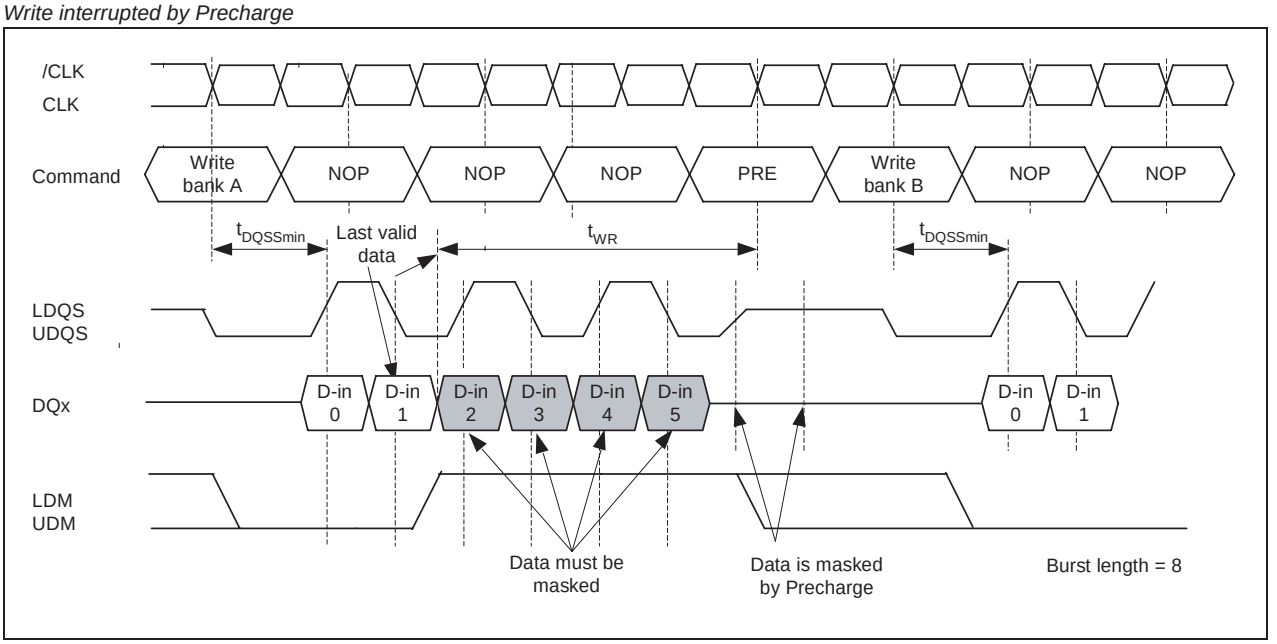
Write interrupted by Read



Write Interrupted by a Precharge

A Burst Write operation can be interrupted before completion of the burst by a Precharge of the same bank. Random column access is allowed. A Write Recovery time (t_{WR}) is required from the last data to Precharge command. When Precharge command is asserted, any residual data from the burst write cycle must be masked by LDM, UDM.

Write interrupted by Precharge



Command Table

Table Command Overview

Operation	Code	CKE n-1	CKE n	CS#	RAS#	CAS#	WE#	BA0	BA1	A10	A0-9 A11,12
Device Deselect	DESEL	H	X	H	X	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X	X
Mode Register Setup	MRS	H	X	L	L	L	L	0	0	OPCODE	
Extended Mode Register Setup	EMRS	H	X	L	L	L	L	0	1	OPCODE	
Bank Activate	ACT	H	X	L	L	H	H	BA	BA	Row Address	
Read	READ	H	X	L	H	L	H	BA	BA	L	Col.
Read with Auto Precharge	READA	H	X	L	H	L	H	BA	BA	H	Col.
Write Command	WRITE	H	X	L	H	L	L	BA	BA	L	Col.
Write Command with Auto Precharge	WRITEA	H	X	L	H	L	L	BA	BA	H	Col.
Burst Stop	BST	H	X	L	H	H	L	X	X	X	X
Precharge Single Bank	PRE	H	X	L	L	H	L	BA	BA	L	X
Precharge All Banks	PREAL	H	X	L	L	H	L	X	X	H	X
Autorefresh	REF	H	H	L	L	L	H	X	X	X	X
Self Refresh Entry	REFX	H	L	L	L	L	H	X	X	X	X
Self Refresh Exit	SREFEX	L L	H H	H L	X H	X H	X H	X X	X X	X X	X X
Power Down Mode Entry *(Note 1)*	PWDNEN	H H	L L	H L	X H	X H	X H	X X	X X	X X	X X
Power Down Mode Exit	PWDNEX	L	H	H L	X valid	X valid	X valid	X	X	X	X
Deep Power Down Mode Entry	Idle	H	L	L	H	H	L	X	X	X	X
Deep Power Down Mode Exit	Deep pow-er down	L	H	X	X	X	X	X	X	X	X

Note: 1: The Power Down Mode Entry command is illegal during Burst Read or Burst Write operations.

Function Truth Table I

Current State	Command	Address	Action	Notes
IDLE	DESEL	X	NOP	3
	NOP	X	NOP	3
	BST	X	NOP	3
	READ / READA	BA,CA,A10	ILLEGAL	1
	WRITE / WRITEA	BA,CA,A10	ILLEGAL	1
	ACT	BA, RA	Bank Active	
	PRE / PREAL	BA, A10	NOP	
	AREF / SREF	X	AUTO-Refresh or Self-Refresh	4
	MRS / EMRS	Op-Code	Mode Register Set or Extended Mode Register Set	
ROW ACTIVE	DESEL	X	NOP	
	NOP	X	NOP	
	BST	X	NOP	
	READ / READA	BA, CA, A10	Begin Read, Determine Auto Precharge	9
	WRITE / WRITEA	BA, CA, A10	Begin Write, Determine Auto Precharge	9
	ACT	BA, RA	ILLEGAL	1, 5
	PRE / PREAL	BA, A10	Precharge / Precharge All	6
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
READ	DESEL	X	Continue burst to end	
	NOP	X	Continue burst to end	
	BST	X	Terminate Burst	
	READ / READA	BA, CA, A10	Terminate burst, Begin New Read, Determine Auto-Prechgarge	7
	WRITE / WRITEA	BA, CA, A10	ILLEGAL	2, 7
	ACT	BA, RA	ILLEGAL	1
	PRE / PREAL	BA ,A10	Terminate Burst / Precharge	
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	Op-Code	ILLEGAL	
READ with Auto Precharge	DESEL	X	Continue burst to end, Precharge	
	NOP	X	Continue burst to end, Precharge	
	BST	X	ILLEGAL	
	READ / READA	BA, CA, A10	ILLEGAL	
	WRITE / WRITEA	BA, CA, A10	ILLEGAL	
	ACT	BA, RA	ILLEGAL	1
	PRE / PREAL	BA ,A10	ILLEGAL	1
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	Op-Code	ILLEGAL	

Function Truth Table I

Current State	Command	Address	Action	Notes
WRITE	DESEL	X	Continue burst to end	
	NOP	X	Continue burst to end	
	BST	X	ILLEGAL	
	READ / READA	BA, CA, A10	Terminate Burst, Begin Read, Determine Auto-Precharge.	7, 8
	WRITE / WRITEA	BA, CA, A10	Terminate Burst, Begin new Write, Determine Auto-Precharge	2, 7
	ACT	BA, RA	ILLEGAL	1
	PRE / PREAL	BA, A10	Terminate Burst , Precharge	8
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
WRITE with Auto Precharge	DESEL	X	Continue burst to end, Precharge	
	NOP	X	Continue burst to end, Precharge	
	BST	X	ILLEGAL	
	READ / READA	BA, CA, A10	ILLEGAL	
	WRITE / WRITEA	BA, CA, A10	ILLEGAL	
	ACT	BA, RA	ILLEGAL	1
	PRE / PREAL	BA , A10	ILLEGAL	1
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
ROW ACTIVATING	DESEL	X	NOP (Row Active after t_{RCD})	
	NOP	X	NOP (Row Active after t_{RCD})	
	BST	X	NOP (Row Active after t_{RCD})	
	READ / READA	BA, CA, A10	ILLEGAL	1, 9
	WRITE / WRITEA	BA, CA, A10	ILLEGAL	1, 9
	ACT	BA, RA	ILLEGAL	1, 5
	PRE / PREAL	BA, A10	ILLEGAL	1, 6
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
PRECHARGE	DESEL	X	NOP (Row Idle after t_{RP})	
	NOP	X	NOP (Row Idle after t_{RP})	
	BST	X	NOP (Row Idle after t_{RP})	
	READ / READA	BA, CA, A10	ILLEGAL	1
	WRITE / WRITEA	BA, CA, A10	ILLEGAL	1
	ACT	BA, RA	ILLEGAL	1
	PRE / PREAL	BA, A10	NOP (Row Idle after t_{RP}) 1	
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	

Function Truth Table I

Current State	Command	Address	Action	Notes
WRITE RECOVERING	DESEL	X	NOP (Row Active after t_{WR})	
	NOP	X	NOP (Row Active after t_{WR})	
	BST	X	NOP (Row Active after t_{WR})	
	READ / READA	BA, CA, A10	Begin Read, Determine Auto-Prechgarge	2
	WRITE / WRITEA	BA, CA, A10	Begin Write, Determine Auto-Prechgarge	
	ACT	BA, RA	ILLEGAL	2
	PRE / PREAL	BA ,A10	ILLEGAL	1, 10
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
WRITE RECOVERING with AUTO-PRECHARGE	DESEL	X	NOP (Precharge after t_{WR})	
	NOP	X	NOP (Precharge after t_{WR})	
	BST	X	NOP (Precharge after t_{WR})	
	READ / READA	BA, CA, A10	ILLEGAL	1, 2
	WRITE / WRITEA	BA, CA, A10	ILLEGAL	1
	ACT	BA, RA	ILLEGAL	1
	PRE / PREAL	BA ,A10	ILLEGAL	1
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
REFRESH	DESEL	X	NOP (Idle after t_{RC})	
	NOP	X	NOP (Idle after t_{RC})	
	BST	X	NOP (Idle after t_{RC})	
	READ / READA	BA, CA, A10	ILLEGAL	
	WRITE / WRITEA	BA, CA, A10	ILLEGAL	
	ACT	BA, RA	ILLEGAL	11
	PRE / PREAL	BA ,A10	ILLEGAL	
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
(EXTENDED) MODE REGISTER SET	DESEL	X	NOP (Idle after two clocks)	
	NOP	X	NOP (Idle after two clocks)	
	BST	X	NOP (Idle after two clocks)	
	READ / READA	BA, CA, A10	ILLEGAL	
	WRITE / WRITEA	BA, CA, A10	ILLEGAL	
	ACT	BA, RA	ILLEGAL	
	PRE / PREAL	BA ,A10	ILLEGAL	
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	

Note: All entries assume the CKE was High during the preceding clock cycle
Note: 1. Illegal to bank specified states; function may be legal in the bank indicated by BAx, depending on the state of that bank
Note: 2. Must satisfy bus contention, bus turn around, write recovery requirements.
Note: 3. If both banks are idle, and CKE is inactive, the device will enter Power Down Mode. All input buffers except CKE, CLK and CLK# will be disabled.
Note: 4. If both banks are idle, and CKE is deactivated coincidentally with an AutoRefresh command, the device will enter SelfRefresh Mode. All input buffers except CKE will be disabled.
Note: 5. Illegal, if t_{RRD} is not satisfied.
Note: 6. Illegal, if t_{RAS} is not satisfied.
Note: 7. Must satisfy burst interrupt condition.
Note: 8. Must mask two preceding data bits with the DM pin.
Note: 9. Illegal, if t_{RCD} is not satisfied.
Note: 10. Illegal, if t_{WR} is not satisfied.
Note: 11. Illegal, if t_{RC} is not satisfied.

Abbreviations:

H	High Level
L	Low Level
X	Don t Care
V	Valid Data Input
RA	Row Address
BA	Bank Address
PA	Precharge All
NOP	No Operation
CA	Column Address
Ax	Address Line x

FUNCTION TRUTH TABLE for CKE

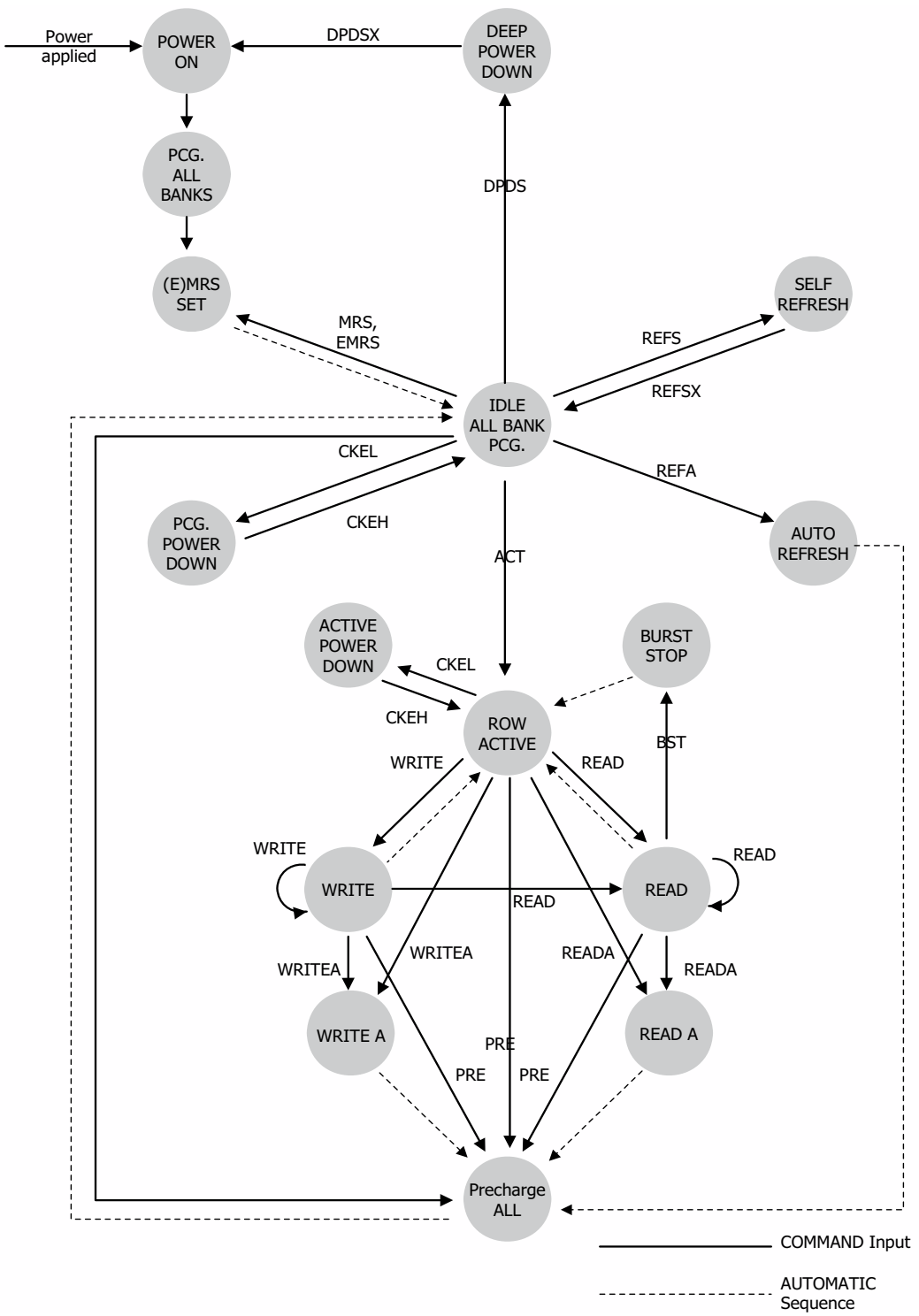
Current State	CKE n-1	CKE n	CS#	RAS#	CAS#	WE#	Address	Action	Notes
SELF REFRESH	H	L	L	L	L	H	X	Self Refresh Entry	1
	L	H	H	X	X	X	X	Exit Self-Refresh	1
	L	H	L	H	H	H	X	Exit Self-Refresh	1
	L	H	L	H	H	L	X	ILLEGAL	1
	L	H	L	H	H	X	X	ILLEGAL	1
	L	H	L	L	L	X	X	ILLEGAL	1
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)	1
POWER DOWN	H	X	X	X	X	X	X	INVALID	
	L	H	X	X	X	X	X	Exit Power Down (Idle after t_{PDEX})	1
	L	L	X	X	X	X	X	NOP (Maintain Power Down)	
ALL BANKS IDLE	H	H	X	X	X	X	X	Refer to Function Truth Table	2
	H	L	L	L	L	H	X	Enter Self Refresh	3
	H	L	H	X	X	X	X	Enter Power-Down	2
	H	L	L	H	H	H	X	Enter Power-Down	2
	H	L	L	H	H	L		ILLEGAL	2
	H	L	L	H	L	X		ILLEGAL	2
	H	L	L	L	X	X		ILLEGAL	2
	L	X	X	X	X	X	X	Refer to Power Down in this table	
All other states	H	H	X	X	X	X	X	Refer to Funtion Truth Table	

Note: 1. CKE low-to-high transition re-enables inputs asynchronously. A minimum setup time to CLK must be satisfied before any commands other than EXIT are executed.
Note: 2. Power Down can be entered when all banks are idle (banks can be active or precharged)
Note: 3. Self Refresh can be entered only from the Precharge / Idle state.

Abbreviations:

H	High Level
L	Low Level
X	Don tCare
V	Valid Data Input
RA	Row Address
BA	Bank Address
PA	Precharge All
NOP	No Operation
CA	Column Address

Mobile DDR SDRAM operation
State Diagram



ACT :
Active

BST :
Burst

CKEL :
Enter Power-Down

CKEH :
Exit Power-Down

DPDS :
Enter Deep Power-Down

DPDSX :
Exit Deep Power-DownEMRS

EMRS :
Ext. Mode Reg. Set

MRS :
Mode Register Set

PRE :
Precharge

PREALL :
Precharge All Banks

REFA :
Auto Refresh

REFS :
Enter Self Refresh

REFSX :
Exit Self Refresh

READ :
Read w/o Auto Precharge

READA :
Read with Auto Precharge

WRITE :
Write w/o Auto Precharge

WRITEA :
Write with Auto Precharge

IDD Max Specifications and Conditions

Conditions	Version		
	Symbol	-5	Unit
Operating current - One bank Active-Precharge; tRC = tRC (min); tCK = tCK (min); CKE = High; CS = High between valid command; Address inputs are switching every 2 clock cycles; Data bus inputs are stable	IDD0	190	mA
Precharge power-down standby current; All banks idle; CKE = Low; CS = High; tCK = tCK (min); Address and control inputs are switching; Data bus inputs are stable	IDD2P	10	mA
Precharge power-down standby current; Clock stopped; All banks idle; CKE = Low; CS = High; CK = Low; $\overline{CK}$ = High; Address and control inputs are switching; Data bus inputs are stable	IDD2PS	10	mA
Precharge nonpower-down standby current; All banks idle; CKE = High; CS = High; tCK = tCK (min); Address and control inputs are switching; Data bus inputs are stable	IDD2N	70	mA
Precharge nonpower-down standby current; Clock stopped; All banks idle; CKE = High; CS = High; CK = Low; $\overline{CK}$ = High; Address and control inputs are switching; Data bus inputs are stable	IDD2NS	60	mA
Active power-down standby current; One bank active; CKE = Low; CS = High; tCK = tCK (min); Address and control inputs are switching; Data bus inputs are stable	IDD3P	10	mA
Active power-down standby current; Clock stopped; One bank active; CKE =Low; CS = High; CK = Low; $\overline{CK}$ = High; Address and control inputs are switching; Data bus inputs are stable	IDD3PS	10	mA
Active nonpower-down standby current; One bank active; CKE = High; CS = High; tCK = tCK (min); Address and control inputs are switching; Data bus inputs are stable	IDD3N	70	mA
Active nonpower-down standby current; Clock stopped; One bank active; CKE = High; CS = High; CK = Low; $\overline{CK}$ = High; Address and control inputs are switching; Data bus inputs are stable	IDD3NS	54	mA
Operating current - burst read; One bank active; Burst length = 4; tCK = tCK (min); Continuous Read burst; Address inputs are switching every 2 clock cycles; 50% of data changing at every burst; lout = 0 m A	IDD4R	180	mA
Operating current - burst write; One bank active; Burst length = 4; tCK = tCK (min); Continuous Write burst; Address inputs are switching every 2 clock cycles; 50% of data changing at every burst	IDD4W	180	mA
Auto refresh current; Burst refresh; CKE = High; Address and control inputs are switching; Data bus inputs are stable	IDD5	160	mA
Deep Power Down Current; Address and control inputs are stable; Data bus inputs are stable	IDD8	20	uA

Partial Array Self Refresh Current (PASR)

Parameter & Test Condition	Extended Mode Register A[2:0] Tcase [^{o}C]	Symb.	max.	Unit	Note
Self Refresh Current Self Refresh Mode CKE = 0.2V, tck = infinity, full array activations, all banks	85^{o}C max.	ICC6	3	mA	
Self Refresh Current Self Refresh Mode CKE = 0.2V, tck = infinity, 1/2 array activations	85^{o}C max.	ICC6	2.4	mA	
Self Refresh Current Self Refresh Mode CKE = 0.2V, tck = infinity, 1/4 array activation	85^{o}C max.	ICC6	2.2	mA	
Self Refresh Current Self Refresh Mode CKE = 0.2V, tck = infinity, 1/8 array activation	85^{o}C max.	ICC6	2	mA	
Self Refresh Current Self Refresh Mode CKE = 0.2V, tck = infinity, 1/16 array activation	85^{o}C max.	ICC6	2	mA	

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 2.7	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-0.5 ~ 2.7	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.0	W
Short circuit current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

Capacitance (V_{DD} = 1.8V, T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0~A_{13}, BA_0~BA_1,CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN1}	1.5	3.0	pF
Input capacitance (CK, $\overline{CK}$)	C_{IN2}	1.5	3.0	pF
Data & DQS input/output capacitance (DQ_0~DQ_{15})	C_{OUT}	3.0	5.0	pF
Input capacitance (DMs)	C_{IN3}	3.0	5.0	pF

Power & DC Operating Conditions (LVCMOS In/Out)

Recommended operating conditions (Voltage referenced to V_{SS} = 0V)

Parameter	Symbol	Min	Typ	Max	Unit
Device Supply voltage	V_{DD}	1.7	1.8	1.95	V
Output Supply voltage	V_{DDQ}	1.7	1.8	1.95	V
Input logic high voltage	V_{IH}	0.7*V_{DDQ}	-	V_{DDQ}+0.30	V
Input logic low voltage	V_{IL}	-0.3	-	0.3*V_{DDQ}	V
Input Leakage current	I_I	-2	-	2	uA
Output Leakage current	IOZ	-5	-	5	uA

AC Input Operating Conditions

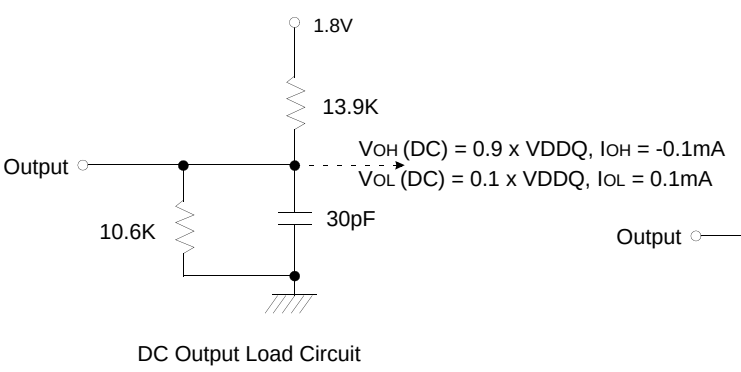
Recommended operating conditions (Voltage referenced to V_{SS} = 0V, V_{DD} = 1.7V ~1.95V)

Parameter	Symbol	Min	Typ	Max	Unit
Input High (Logic 1) Voltage; DQ	V_{IH}	V_{CCQ}*0.8	-	V_{CCQ}+0.3	V
Input Low (Logic 0) Voltage; DQ	V_{IL}	-0.3	-	0.2* V_{DDQ}	V
Clock Input Crossing Point Voltage; CK and $\overline{CK}$	V_{IX}	0.4*V_{DDQ}	-	0.6*V_{DDQ}	V

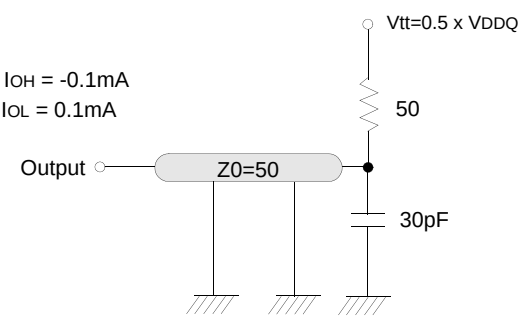
AC Operating Test Conditions

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, V_{DD} = 1.7V ~1.95V)

Parameter	Value	Unit
AC input levels (Vih/Vil)	0.8*VDDQ / 0.2*VDDQ	V
Input timing measurement reference level	0.5*VDDQ	V
Input signal minimum slew rate	1.0	V/ns
Output timing measurement reference level	0.5*VDDQ	V
Output load condition	See below figures	



DC Output Load Circuit



AC Output Load Circuit

AC Timing Parameters & Specification

AC CHARACTERISTICS			-5			
PARAMETER		**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output data access time from CK/$\overline{CK}$		^{t}AC	2	5	ns	3
CK high-level width		^{t}CH	0.45	0.55	^{t}CK	
CK low-level width		^{t}CL	0.45	0.55	^{t}CK	
Clock cycle time	CL = 3	^{t}CK (3)	5	-	ns	1
DQ and DM input hold time relative to DQS		^{t}DH	0.4		ns	5,6
DQ and DM input setup time relative to DQS		^{t}DS	0.4		ns	5,6
DQ and DM input pulse width (for each input)		^{t}DIPW	1.4		ns	
Access window of DQS from CK/$\overline{CK}$		^{t}DQSCK	2	5	ns	
DQS input high pulse width		^{t}DQSH	0.4	0.6	^{t}CK	
DQS input low pulse width		^{t}DQSL	0.4	0.6	^{t}CK	
DQS-DQ skew, DQS to last DQ valid, per group, per access		^{t}DQSQ		0.4	ns	1
Write command to first DQS latching transition		^{t}DQSS	0.7	1.2	^{t}CK	
Half clock period		^{t}HP	^{t}CH, ^{t}CL		ns	
Data-out high-impedance window from CK/$\overline{CK}$		^{t}HZ	0.4	0.6	^{t}CK	
Data-out low-impedance window from CK/$\overline{CK}$		^{t}LZ	1		ns	
Address and control input hold time		^{t}IH	0.9		ns	1
Address and control input setup time		^{t}IS	0.9		ns	1
LOAD MODE REGISTER command cycle time		^{t}MRD	2		^{t}CK	
DQ-DQS hold, DQS to first DQ to go non-valid, per access		^{t}QH	^{t}HP -^{t}QHS		ns	
Data hold skew factor		^{t}QHS		0.5	ns	
ACTIVE to PRECHARGE command		^{t}RAS	40	70K	ns	
ACTIVE to READ with Auto precharge command		^{t}RAP	15		ns	
ACTIVE to ACTIVE/AUTO REFRESH command period		^{t}RC	55		ns	
AUTO REFRESH command period		^{t}RFC	72		ns	
ACTIVE to READ or WRITE delay		^{t}RCD	15		ns	
PRECHARGE command period		^{t}RP	15		ns	

AC CHARACTERISTICS		-5			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
DQS read preamble	^{t}RPRE	0.9	1.1	^{t}CK	
DQS read postamble	^{t}RPST	0.4	0.6	^{t}CK	
ACTIVE bank A to ACTIVE bank B command	^{t}RRD	10		ns	
DQS write preamble	^{t}WPRE	0.25		^{t}CK	
DQS write preamble setup time	^{t}WPRES	0		ns	4
DQS write postamble	^{t}WPST	0.4	0.6	^{t}CK	
Write recovery time	^{t}WR	15		ns	
Internal WRITE to READ command delay	^{t}WTR	2		^{t}CK	
Average periodic refresh interval	^{t}REFI		7.8	us	
Power down exit time	^{t}PDEX	$1*^{t}$CK $+^{t}$IS		ns	

1. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	tIS	tIH
(V/ns)	(ps)	(ps)
1.0	0	0
0.8	+50	+50
0.6	+100	+100

This derating table is used to increase t_{IS}/t_{IH} in the case where the input slew rate is below 1.0V/ns.

2. Minimum 3CLK of tDAL(= tWR + tRP) is required because it need minimum 2CLK for tWR and minimum 1CLK for tRP.

3. tAC(min) value is measured at the high Vdd(1.95V) and cold temperature(-25 C).
tAC (max) value is measured at the low Vdd(1.7V) and hot temperature(85 C).
tAC is measured in the device with half driver strength and under the AC output load condition.

4. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.

5. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	tDS	tDH
(V/ns)	(ps)	(ps)
1.0	0	0
0.8	+75	+75
0.6	+150	+150

This derating table is used to increase t_{DS}/t_{DH} in the case where the I/O slew rate is below 1.0V/ns.

6. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

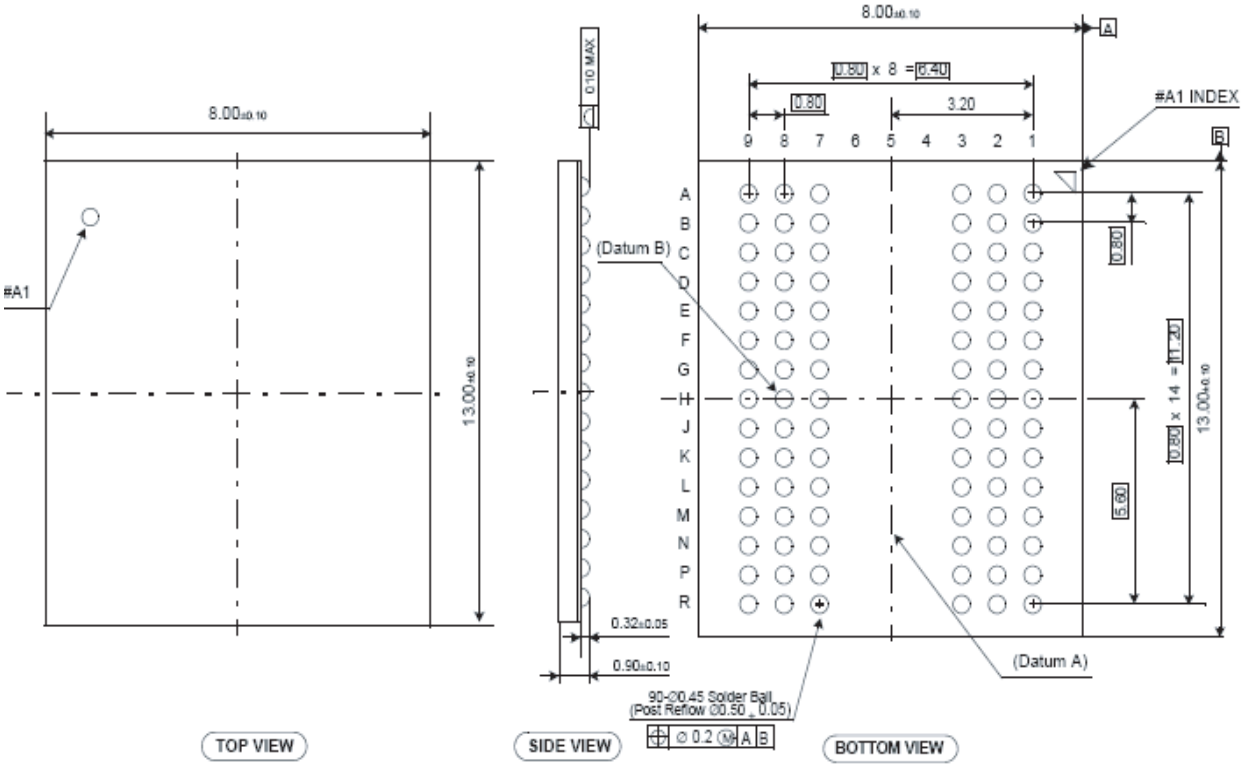
Delta Rise/Fall Rate	tDS	tDH
(ns/V)	(ps)	(ps)
0	0	0
0.25	+50	+50
0.5	+100	+100

This derating table is used to increase tDS/tDH in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calculated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 1.0V/ns and slew rate 2 =0.8V/ns, then the Delta Rise/Fall Rate =-0.25ns/V.

Package Diagram

90-BALL 0.8mm pitch BGA

Units:millimeters



PART NUMBERING SYSTEM

AS4C	64M32MD1	5	B	C/I	N
DRAM	64M32=64Mx32 MD1=MobileDDR1	5=200MHz	B = FBGA	C=Commercial (-25° C～85° C) I=Industrial (-40° C～85° C)	Indicates Pb and Halogen Free

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